TPS3852 Precision Voltage Supervisor with Programmable Window Watchdog Timer

1 Features

- VDD Input Voltage Range: 1.6 V to 6.5 V
- 0.8% Voltage Threshold Accuracy
- Low Supply Current: I_{DD} = 10 µA (typical)
- User-Programmable Watchdog Timeout
- Factory Programmed Precision Watchdog and Reset Timers:
  - ±15% Accurate WDT and RST Delays
- Open-Drain Outputs
- Manual Reset Input ($\overline{MR}$)
- Precision Undervoltage Monitoring
  - Supports Common Rails from 1.8 V to 5 V
  - 4% and 7% Thresholds Available
  - 0.5% Hysteresis
- Watchdog Disable Feature
- Available in a Small 3-mm × 3-mm, 8-Pin VSON Package

2 Applications

- Safety Critical Applications
- Telematics Control Units
- High-Reliability Industrial Systems
- Patient Monitoring
- Industrial Control Systems
- FPGAs and ASICs
- Microcontrollers and DSPs

3 Description

The TPS3852 is a precision voltage supervisor with an integrated window watchdog timer. The TPS3852 includes a precision undervoltage supervisor with an undervoltage threshold (V_{ITN}) that achieves 0.8% accuracy over the specified temperature range of –40°C to +125°C. In addition, the TPS3852 includes accurate hysteresis making the device ideal for use with tight tolerance systems. The supervisor $\overline{RESET}$ delay features a 15% accuracy, high-precision delay timer.

The TPS3852 includes a programmable window watchdog timer for a wide variety of applications. The dedicated watchdog output ($\overline{WDO}$) enables increased resolution to help determine the nature of fault conditions. The watchdog timeouts can be programmed either by an external capacitor, or by factory-programmed default delay settings. The watchdog can be disabled to avoid undesired watchdog timeouts during the development process.

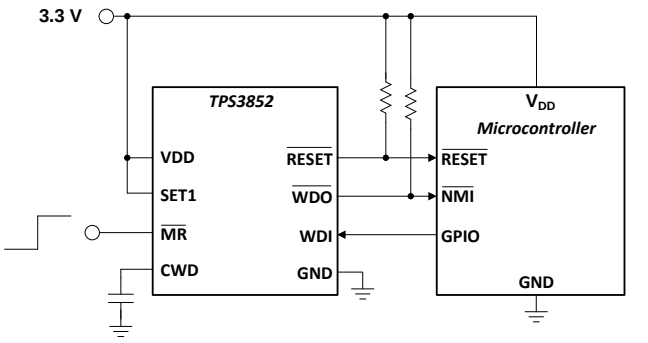
The TPS3852 is available in a small 3.00-mm × 3.00-mm, 8-pin VSON package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3852	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Undervoltage Threshold (V_{ITN}) Accuracy vs Temperature

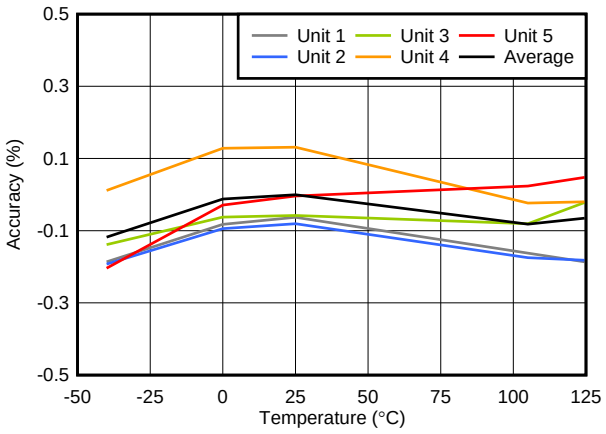


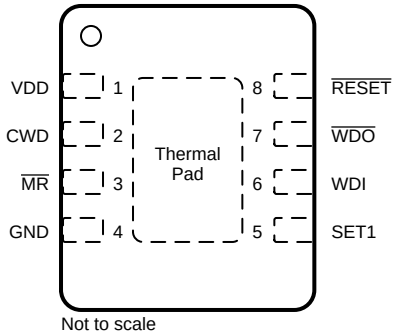
Table of Contents

4 Revision History

DATE	REVISION	NOTES
November 2016	*	Initial release.

5 Pin Configuration and Functions

DRB Package
VSON-8 (8-Pins)
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
CWD	2	—	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. Furthermore, this pin can also be connected by a 10-kΩ resistor to VDD, or leaving unconnected (NC) further enables the selection of the preset watchdog timeouts; see the *Timing Requirements* table. When using a capacitor, the TPS3852 determines the window watchdog upper boundary with Equation 1. See Table 3 and the *CWD Functionality* section for additional information.
GND	4	—	Ground pin
$\overline{MR}$	3	I	Manual reset pin. A logical low on this pin issues a $\overline{RESET}$. This pin is internally pulled up to V_{DD}. $\overline{RESET}$ remains low for a fixed reset delay (t_{RST}) time after $\overline{MR}$ is deasserted (high).
$\overline{RESET}$	8	O	Reset output. Connect $\overline{RESET}$ using a 1-kΩ to 100-kΩ resistor to the desired pullup voltage rail (V_{PU}). $\overline{RESET}$ goes low when V_{DD} goes below the undervoltage threshold (V_{ITN}). When V_{DD} is within the normal operating range, the $\overline{RESET}$ timeout-counter starts. At completion, $\overline{RESET}$ goes high. During startup, the state of $\overline{RESET}$ is undefined below the specified power-on-reset (POR) voltage (V_{POR}). Above POR, $\overline{RESET}$ goes low and remains low until the monitored voltage is within the correct operating range (above $V_{ITN}+V_{HYST}$) and the $\overline{RESET}$ timeout is complete.
SET1	5	I	Logic input. Grounding the SET1 pin disables the watchdog timer.
VDD	1	I	Supply voltage pin. For noisy systems, connecting a 0.1-μF bypass capacitor is recommended.
WDI	6	I	Watchdog input. A falling transition (edge) must occur at this pin between the lower ($t_{WDL(max)}$) and upper ($t_{WDU(min)}$) window boundaries in order for $\overline{WDO}$ to not assert. When the watchdog is not in use, the SET1 pin can be used to disable the watchdog. The input at WDI is ignored when $\overline{RESET}$ or $\overline{WDO}$ are low (asserted) and also when the watchdog is disabled. If the watchdog is disabled, then WDI cannot be left unconnected and must be driven to either VDD or GND.
$\overline{WDO}$	7	O	Watchdog output. Connect $\overline{WDO}$ with a 1-kΩ to 100-kΩ resistor to the desired pullup voltage rail (V_{PU}). $\overline{WDO}$ goes low (asserts) when a watchdog timeout occurs. $\overline{WDO}$ only asserts when $\overline{RESET}$ is high. When a watchdog timeout occurs, $\overline{WDO}$ goes low (asserts) for the set $\overline{RESET}$ timeout delay (t_{RST}). When $\overline{RESET}$ goes low, $\overline{WDO}$ is in a high-impedance state.
Thermal pad		—	Connect the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD	–0.3	7	V
Output voltage range	$\overline{\text{RESET}}$, $\overline{\text{WDO}}$	–0.3	7	V
Voltage ranges	SET1, WDI, $\overline{\text{MR}}$	–0.3	7	V
	CWD, CRST	–0.3	V_{DD} + 0.3(2)	V
Output pin current			±20	mA
Input current (all pins)			±20	mA
Continuous total power dissipation		See *Thermal Information*		
Temperature	Operating junction, T_J (3)	–40	150	°C
	Operating free-air temperature, T_A (3)	–40	150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{DD} + 0.3 V or 7.0 V, whichever is smaller.
(3) Assume that $T_J = T_A$ as a result of the low dissipated power in this device.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.6		6.5	V
V_{SET1}	SET1 pin voltage	0		6.5	V
$V_{\overline{MR}}$	MR pin voltage	0		6.5	V
C_{CWD}	Watchdog timing capacitor	0.1(1)		1000(1)	nF
CWD	Pull-up resistor to VDD	9	10	11	kΩ
R_{PU}	Pull-up resistor, $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$	1	10	100	kΩ
$I_{\overline{RESET}}$	$\overline{\text{RESET}}$ pin current			10	mA
$I_{\overline{WDO}}$	Watchdog output current			10	mA
T_J	Junction Temperature	–40		125	°C

(1) Using a C_{CWD} capacitor of 0.1 nF or 1000 nF gives a $t_{WDU(typ)}$ of 62.74 ms or 77.45 seconds, respectively.

6.4 Thermal Information

THERMAL METRIC(1)		TPS3852 DRB (VSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

At $V_{ITN} + V_{HYST} \le V_{DD} \le 6.5$ V over the operating temperature range of –40°C ≤ T_A, $T_J \le 125$°C, unless otherwise noted. The open-drain pull-up resistors are 10 kΩ for each output. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL CHARACTERISTICS						
V_{DD}(1)	Supply voltage		1.6		6.5	V
I_{DD}	Supply Current			10	19	µA
RESET FUNCTION						
V_{POR}(2)	Power-on reset voltage	$I_{\overline{RESET}}$ = 15 µA, $V_{OL(MAX)}$ = 0.25 V			0.8	V
V_{UVLO}(3)	Under Voltage Lock Out Voltage			1.35		V
V_{ITN}	Undervoltage threshold accuracy, entering $\overline{RESET}$	V_{DD} falling	V_{ITN} – 0.8%		V_{ITN} + 0.8%	
V_{HYST}	Hysteresis voltage	V_{DD} rising	0.2%	0.5%	0.8%	
$I_{\overline{MR}}$	$\overline{MR}$ pin internal pull-up current	$V_{\overline{MR}}$ = 0 V	500	620	700	nA
WINDOW WATCHDOG FUNCTION						
I_{CWD}	CWD pin charge current	CWD = 0.5 V	337	375	413	nA
V_{CWD}	CWD pin threshold voltage		1.192	1.21	1.228	V
V_{OL}	$\overline{RESET}$, $\overline{WDO}$ output low	VDD = 5 V, $I_{\overline{RESET}}$ = $I_{\overline{WDO}}$ = 3 mA			0.4	V
I_D	$\overline{RESET}$, $\overline{WDO}$ output leakage current, open-drain	VDD = V_{ITN} + V_{HYST}, $V_{\overline{RESET}}$ = $V_{\overline{WDO}}$ = 6.5 V			1	µA
V_{IL}	Low-level input voltage ($\overline{MR}$, SET1)				0.25	V
V_{IH}	High-level input voltage ($\overline{MR}$, SET1)		0.8			V
$V_{IL(WDI)}$	Low-level input voltage (WDI)				0.3 × V_{DD}	V
$V_{IH(WDI)}$	High-level input voltage (WDI)		0.8 × V_{DD}			V

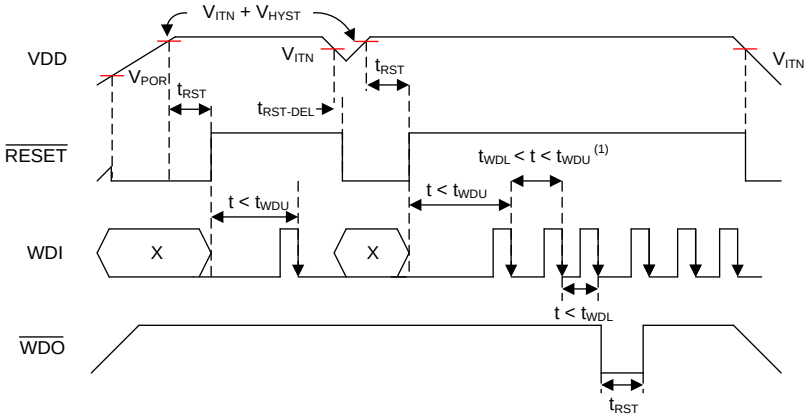
(1) During power on, V_{DD} must be a minimum 1.6 V for at least 300 µs before $\overline{RESET}$ correlates with V_{DD}.
(2) When V_{DD} falls below V_{POR}, $\overline{RESET}$ and $\overline{WDO}$ are undefined.
(3) When V_{DD} falls below UVLO, $\overline{RESET}$ is driven low.

6.6 Timing Requirements

At $V_{ITN} + V_{HYST} \le V_{DD} \le 6.5$ V over the operating temperature range of –40°C ≤ T_A, $T_J \le 125$°C, unless otherwise noted. The open-drain pull-up resistors are 10 kΩ for each output. Typical values are at T_J = 25°C.

			MIN	TYP	MAX	UNIT
t_{INIT}	CWD pin evaluation period			381		µs
	Minimum $\overline{MR}$, SET1 pin pulse duration			1		µs
	Startup delay			300		µs
RESET FUNCTION						
t_{RST}	Reset timeout period		170	200	230	ms
$t_{RST-DEL}$	V_{DD} to $\overline{RESET}$ delay	$V_{DD} = V_{ITN} + V_{HYST}$ + 2.5%		35		µs
		$V_{DD} = V_{ITN}$ - 2.5%		17		
t_{MR-DEL}	$\overline{MR}$ to $\overline{RESET}$ delay			200		ns
Watchdog Function						
t_{WDL}	Window watchdog lower boundary	CWD = NC, SET1 = 0 (1)		Watchdog disabled		
		CWD = NC, SET1 = 1 (1)	680	800	920	ms
		CWD = 10kΩ to VDD, SET1 = 0 (1)		Watchdog disabled		
		CWD = 10kΩ to VDD, SET1 = 1 (1)	1.5	1.85	2.2	ms
t_{WDU}	Window watchdog upper boundary	CWD = NC, SET1 = 0 (1)		Watchdog disabled		
		CWD = NC, SET1 = 1 (1)	1360	1600	1840	ms
		CWD = 10kΩ to VDD, SET1 = 0 (1)		Watchdog disabled		
		CWD = 10kΩ to VDD, SET1 = 1 (1)	9.3	11.0	12.7	ms
$t_{WD-setup}$	Setup time required for part to respond to changes on WDI after being enabled			150		µs
	Minimum WDI pulse width			50		ns
t_{WD-DEL}	WDI to $\overline{WDO}$ Delay			50		ns

(1) SET1 = 0 means $V_{SET1} < V_{IL}$, SET1 = 1 means $V_{SET1} > V_{IH}$



(1) See Figure 2 for WDI timing requirements.

Figure 1. Timing Diagram

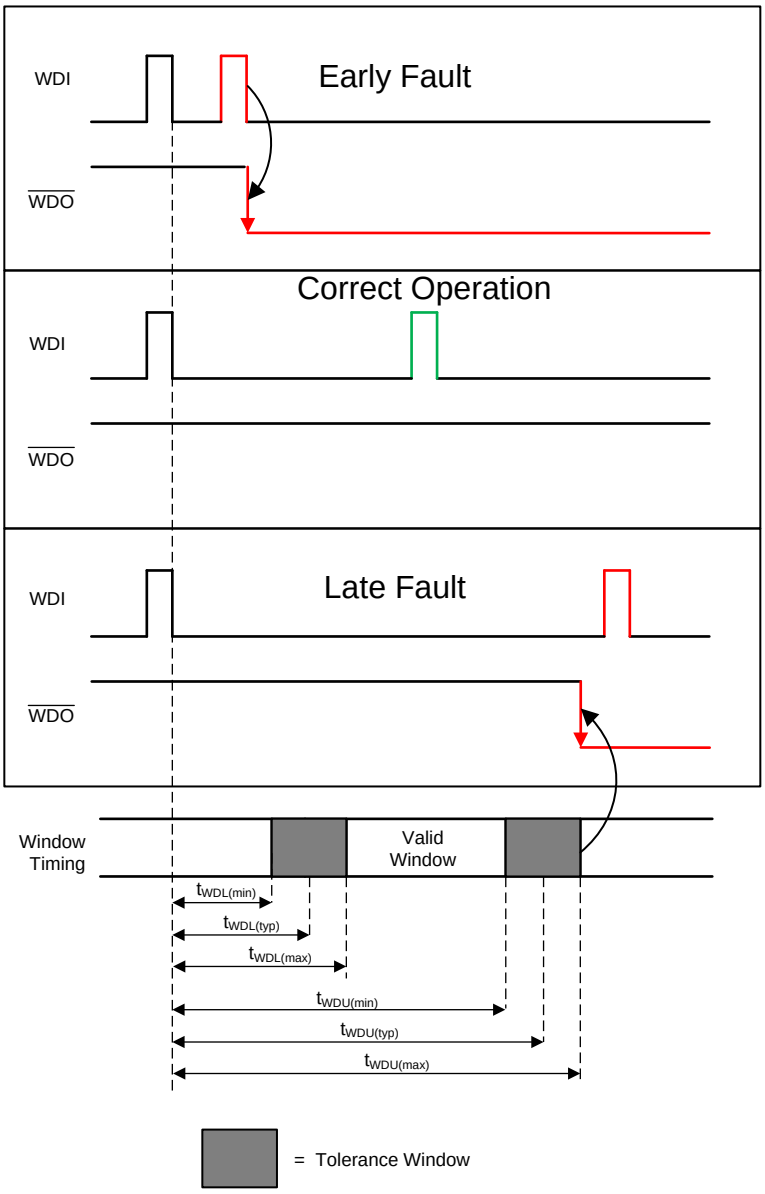


Figure 2. TPS3852 Window Watchdog Timing

6.7 Typical Characteristics

All Typical Characteristics curves are taken at 25°C with, 1.6 V ≤ VDD ≤ 6.5 V unless other wise noted.

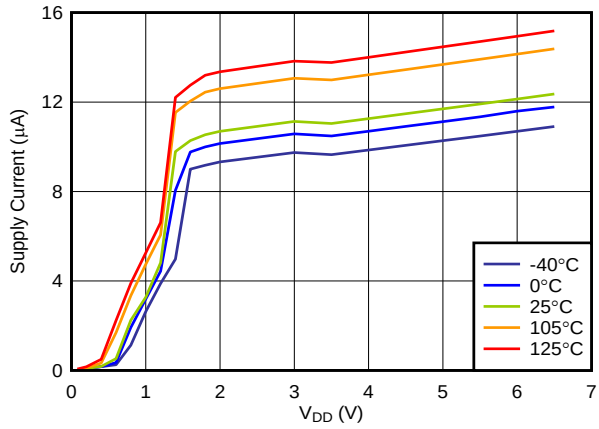
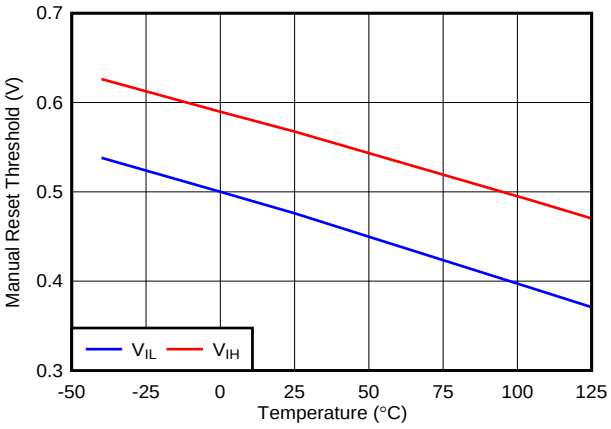


Figure 3. Supply Current vs V_{DD}



VDD = 1.6 V

Figure 4. $\overline{MR}$ Threshold vs Temperature

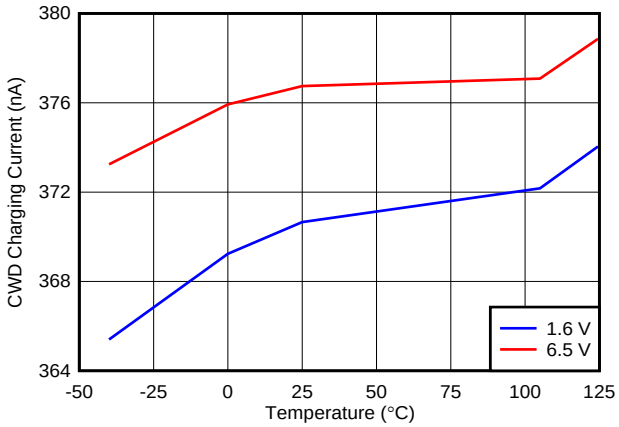
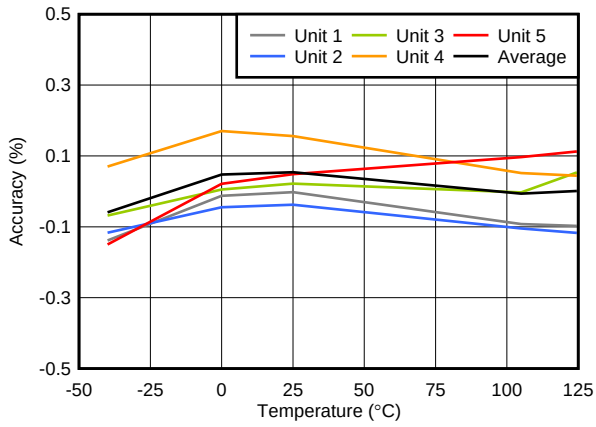
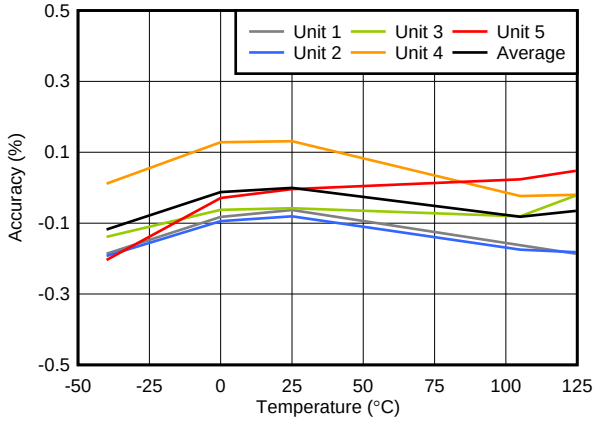


Figure 5. CWD Charging Current vs Temperature



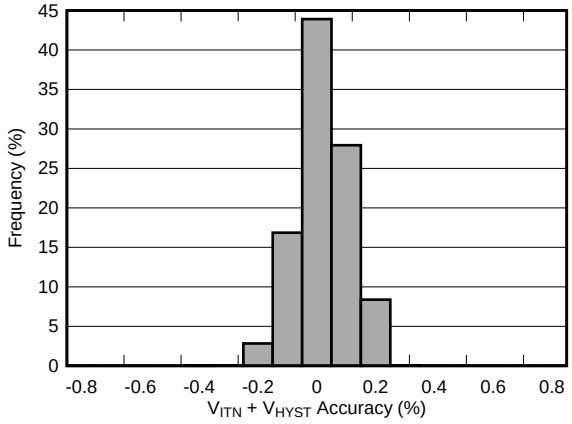
TPS3852G33

Figure 6. V_{ITN} + V_{HYST} Accuracy vs Temperature



TPS3852G33

Figure 7. V_{ITN} Accuracy vs Temperature

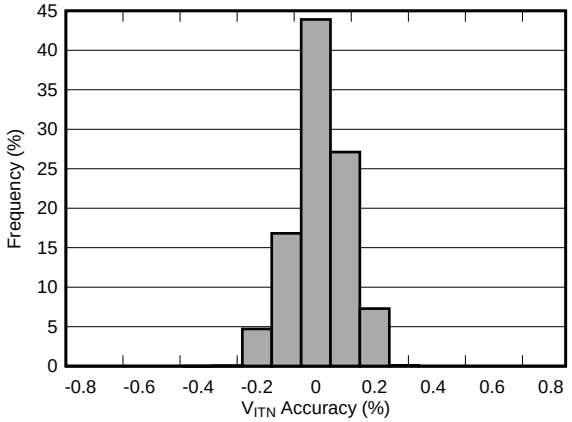


Includes G and H versions; with 3.3-V nominal monitored voltage; total units = 15,536

Figure 8. V_{ITN} + V_{HYST} Accuracy Histogram

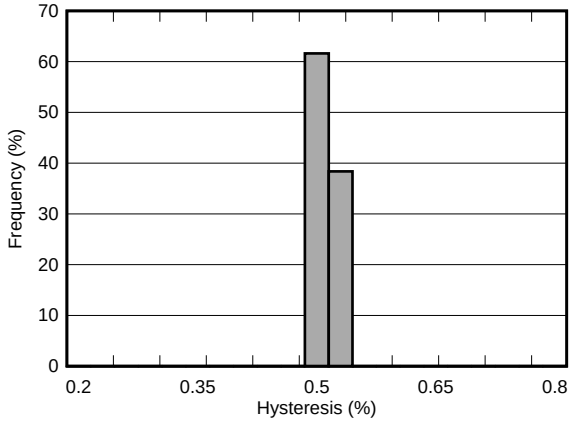
Typical Characteristics (continued)

All Typical Characteristics curves are taken at 25°C with, 1.6 V ≤ VDD ≤ 6.5 V unless other wise noted.



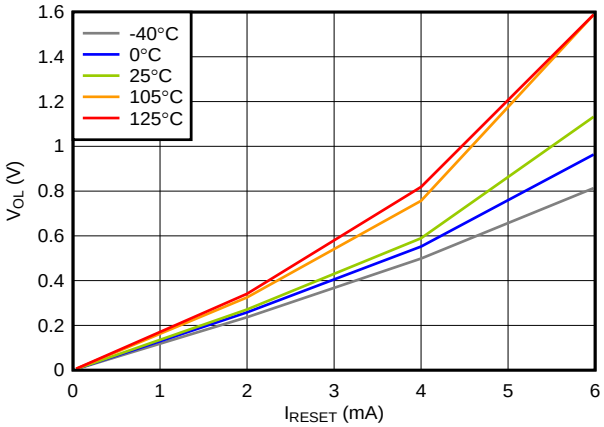
Includes G and H versions; with 3.3-V nominal monitored voltage; total units = 15,536

Figure 9. V_{ITN} Accuracy Histogram



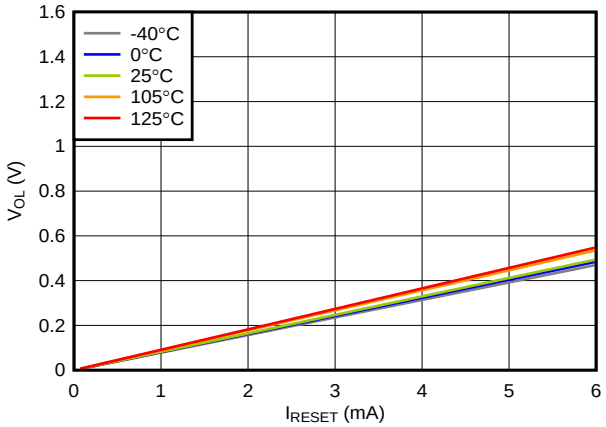
Includes G and H versions; with 3.3-V nominal monitored voltage; total units = 15,536

Figure 10. Hysteresis Histogram



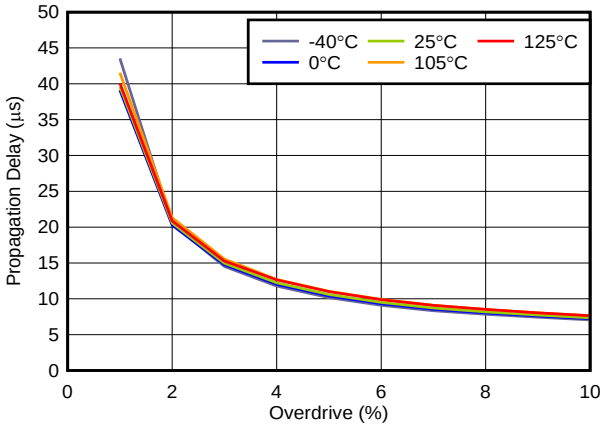
VDD = 1.6 V

Figure 11. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



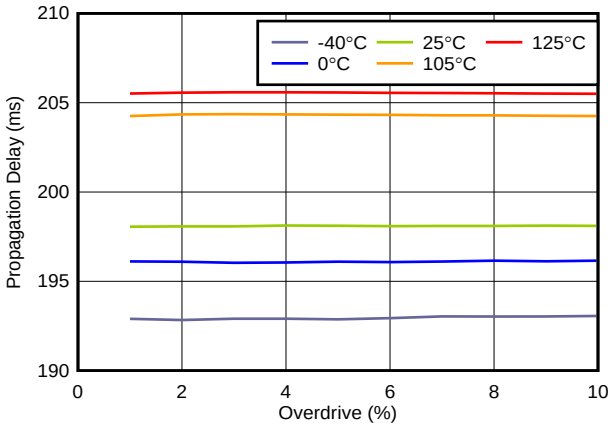
VDD = 6.5 V

Figure 12. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current



TPS3852G33 entering undervoltage

Figure 13. Propagation Delay vs Overdrive

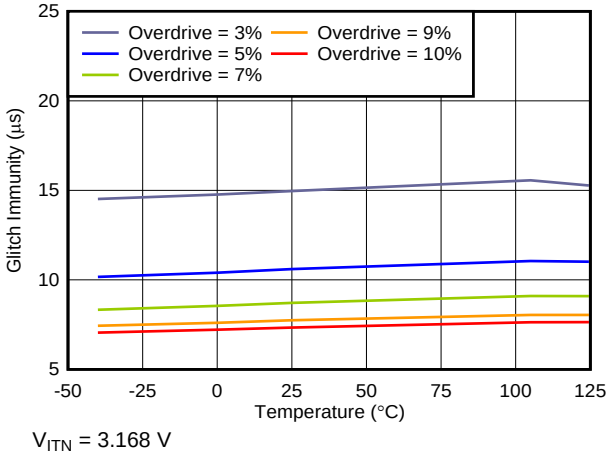


TPS3852G33 exiting undervoltage

Figure 14. Propagation Delay (t_{RST}) vs Overdrive

Typical Characteristics (continued)

All Typical Characteristics curves are taken at 25°C with, 1.6 V ≤ VDD ≤ 6.5 V unless other wise noted.



V_{ITN} = 3.168 V

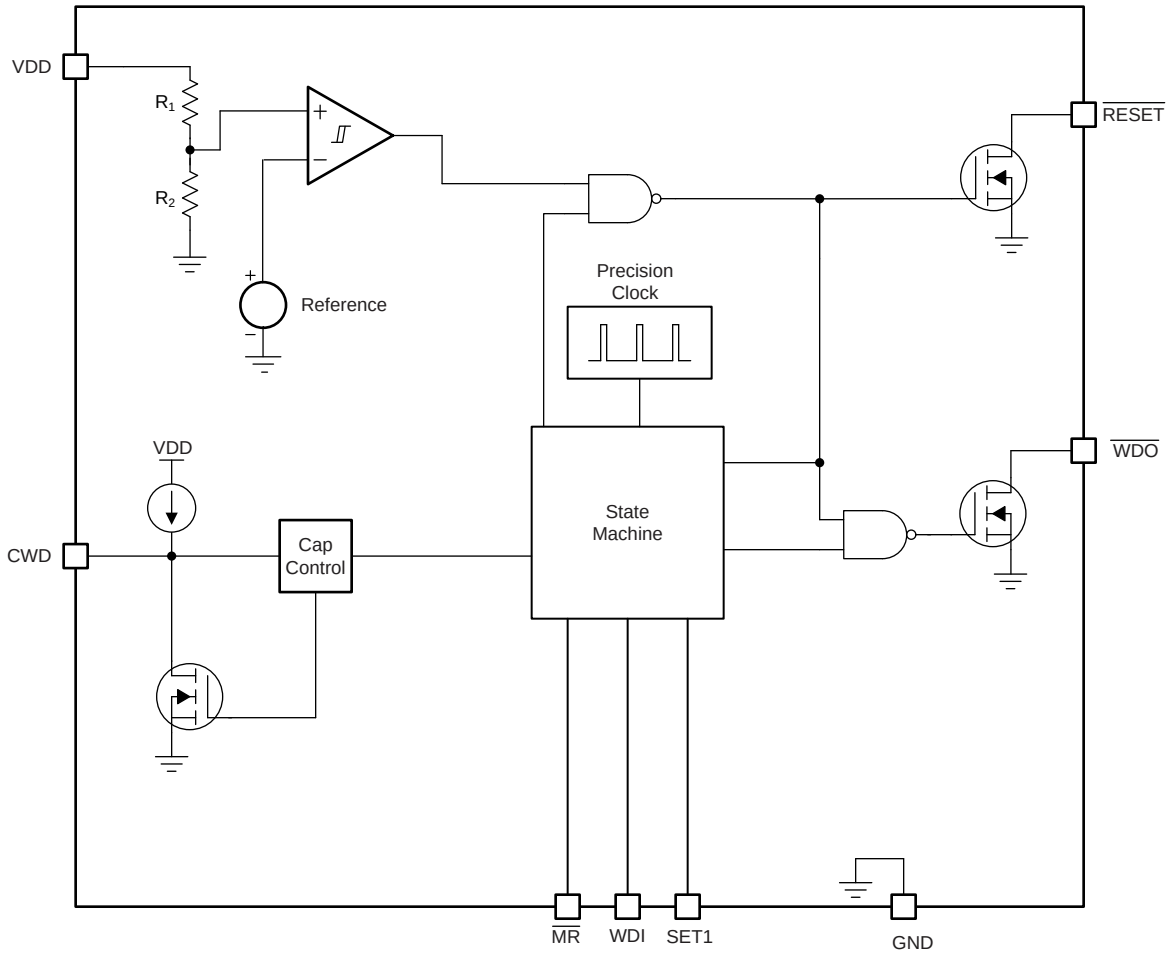
Figure 15. High to Low Glitch Immunity vs Temperature

7 Detailed Description

7.1 Overview

The TPS3852 is a high-accuracy voltage supervisor with an integrated window watchdog timer. This device includes a precision undervoltage supervisor with a threshold that achieves 0.8% accuracy over the specified temperature range of –40°C to +125°C. In addition, the TPS3852 includes accurate hysteresis on the threshold, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure a $\overline{\text{RESET}}$ before the minimum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached.

7.2 Functional Block Diagram



(1) Note: $R_1 + R_2 = 4.5M\Omega$

7.3 Feature Description

7.3.1 $\overline{\text{RESET}}$

Connect $\overline{\text{RESET}}$ to V_{PU} through a 1-kΩ to 100-kΩ pullup resistor. $\overline{\text{RESET}}$ remains high (deasserted) when V_{DD} is greater than the negative threshold voltage (V_{ITN}). If V_{DD} falls below the negative threshold (V_{ITN}), then $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to low impedance. When V_{DD} rises above V_{ITN} + V_{HYST}, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period (t_{RST}). When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. The pullup resistor must be connected to the desired voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by output logic low voltage (V_{OL}), leakage current (I_D), and the current through the $\overline{\text{RESET}}$ pin $I_{\overline{\text{RESET}}}$.

7.3.2 Manual Reset $\overline{\text{MR}}$

The manual reset ($\overline{\text{MR}}$) input allows a processor or other logic circuits to initiate a reset. A logic low on $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to assert. After $\overline{\text{MR}}$ returns to a logic high and V_{DD} is above V_{ITN} + V_{HYST}, $\overline{\text{RESET}}$ is deasserted after the reset delay time (t_{RST}). If $\overline{\text{MR}}$ is not controlled externally, then $\overline{\text{MR}}$ can either be connected to V_{DD} or left floating because the $\overline{\text{MR}}$ pin is internally pulled up. When $\overline{\text{MR}}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored.

7.3.3 UV Fault Detection

The TPS3852 features undervoltage detection for common rails between 1.8 V and 5 V. The voltage is monitored on the input rail of the device. If V_{DD} drops below V_{ITN}, then $\overline{\text{RESET}}$ is asserted (driven low). When V_{DD} is above V_{ITN} + V_{HYST}, $\overline{\text{RESET}}$ deasserts after t_{RST}, as shown in Figure 16. The internal comparator has built-in hysteresis that provides some noise immunity and ensures stable operation. Although not required in most cases, for noisy applications, good analog design practice is to place a 1-nF to 100-nF bypass capacitor close to the VDD pin to reduce sensitivity to transient voltages on the monitored signal.

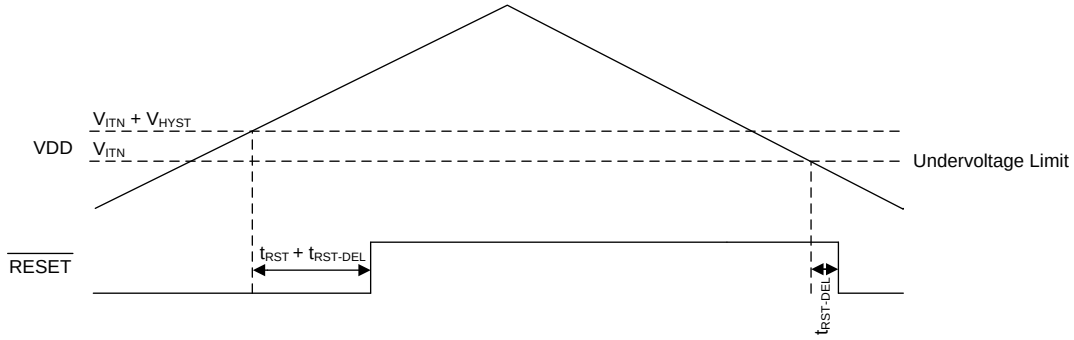


Figure 16. Undervoltage Detection

7.3.4 Watchdog Mode

This section provides information for the watchdog mode of operation.

7.3.4.1 SET1

The SET1 pin can enable and disable the watchdog timer. If SET1 is set to GND, the watchdog timer is disabled and WDI is ignored. When the watchdog is disabled $\overline{\text{WDO}}$ will be in a high impedance state. If the watchdog timer is disabled, drive the WDI pin to either GND or VDD to ensure that there is no increase in I_{DD}. When SET1 is logic high, the watchdog operates normally. The SET1 pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a setup time $t_{WD\text{-}setup}$ where the watchdog does not respond to changes on WDI, as shown in Figure 17.

Feature Description (continued)

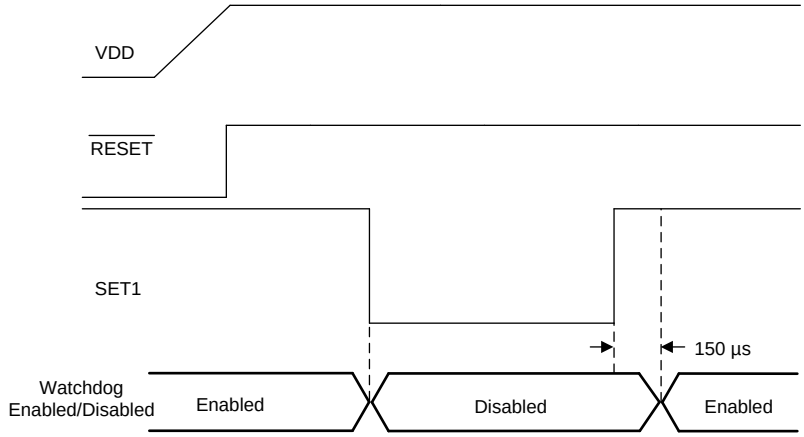


Figure 17. Enabling and Disabling the Watchdog

7.3.4.2 Window Watchdog Timer

This section provides information for the window watchdog mode of operation. A window watchdog is typically employed in safety critical applications where a traditional watchdog timer is inadequate. In a traditional watchdog there is a maximum time in which a pulse must be issued to prevent the reset from occurring. In a window watchdog the pulse must be issued between a maximum lower window time ($t_{WDL(max)}$) and the minimum upper window time ($t_{WDU(min)}$) set by the CWD pin.

7.3.4.3 Watchdog Input WDI

WDI is the watchdog timer input that controls the $\overline{WDO}$ output. The WDI input is triggered by the falling edge of the input signal. For the first pulse, the watchdog acts as a traditional watchdog timer; thus, the first pulse must be issued before $t_{WDU(min)}$. After the first pulse, to ensure proper functionality of the watchdog timer, always issue the WDI pulse within the window of $t_{WDL(max)}$ and $t_{WDU(min)}$. If the pulse is issued in this region, then $\overline{WDO}$ remains unasserted. Otherwise, the device asserts $\overline{WDO}$, putting the $\overline{WDO}$ pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. In order to ensure there is no increase in I_{DD}, drive the WDI pin to either VDD or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{DD}) because of the architecture of the digital logic gates. When $\overline{RESET}$ is asserted, the watchdog is disabled and all signals input to WDI are ignored. When $\overline{RESET}$ is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either VDD or GND.

7.3.4.4 CWD

The CWD pin provides the user the functionality of both high precision factory programmed window watchdog timing options and user programmable window watchdog timing. The CWD pin can be either pulled-up to V_{DD} through a resistor, have an external capacitor to ground, or be left floating. Every time that the part issues a reset event and the supply voltage is above V_{ITN} the part will try to determine, which of these three options is connected to the pin. There is an internal state machine that the device goes through to determine which option is connected to the CWD pin. The state machine can take up to 381 µs to determine if the CWD pin is left floating, pulled-up through a resistor, or connected to a capacitor.

If the CWD pin is being pulled up to V_{DD} using a pull-up resistor then a 10-kΩ resistor should be used.

Feature Description (continued)

7.3.4.5 Watchdog Output $\overline{WDO}$

The TPS3852 features a window watchdog with an independent watchdog output ($\overline{WDO}$). The independent watchdog output gives the flexibility to flag when there is a fault in the watchdog timing without performing an entire system reset. For legacy applications $\overline{WDO}$ can be tied to $\overline{RESET}$. While the $\overline{RESET}$ output is not asserted the $\overline{WDO}$ signal will maintain normal operation. However, when the $\overline{RESET}$ signal is asserted the $\overline{WDO}$ pin will go into a high impedance state. This is due to using the standard $\overline{RESET}$ timing options when a fault occurs on $\overline{WDO}$. Once $\overline{RESET}$ is unasserted the window watchdog timer will resume normal operation.

7.4 Device Functional Modes

Table 1 summarises the functional modes of TPS3852.

Table 1. Device Functional Modes

V_{DD}	WDI	$\overline{WDO}$	$\overline{RESET}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} \le V_{DD} < V_{DD(min)}$	Ignored	High	Low
$V_{DD(min)} \le V_{DD} \le V_{ITN} + V_{HYST}$ (1)	Ignored	High	Low
$V_{DD} > V_{ITN}$ (2)	$t_{WDL(max)} < t_{PULSE} < t_{WDU(min)}$ (3)	High	High
	$t_{PULSE} > t_{WDU(min)}$ (3)	Low	High
	$t_{PULSE} < t_{WDL(max)}$ (3)	Low	High

(1) Only valid before V_{DD} has gone above $V_{ITN} + V_{HYST}$
(2) Only valid after V_{DD} has gone above $V_{ITN} + V_{HYST}$
(3) Where t_{PULSE} is the time between falling edges on WDI

7.4.1 V_{DD} is Below V_{POR} ($V_{DD} < V_{POR}$)

When V_{DD} is less than V_{POR}, $\overline{RESET}$ is undefined and can be either high or low. The state of $\overline{RESET}$ largely depends on the load that the $\overline{RESET}$ pin is experiencing.

7.4.2 Above Power-On-Reset, But Less Than $V_{DD(min)}$ ($V_{POR} \le V_{DD} < V_{DD(min)}$)

When the voltage on V_{DD} is less than $V_{DD(min)}$, and greater than or equal to V_{POR}, the $\overline{RESET}$ signal is asserted (logic low). When $\overline{RESET}$ is asserted, the watchdog output $\overline{WDO}$ is in a high-impedance state regardless of the WDI signal that is input to the device.

7.4.3 Normal Operation ($V_{DD} \ge V_{DD(min)}$)

When V_{DD} is greater than or equal to $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by V_{DD}. When $\overline{RESET}$ is asserted, $\overline{WDO}$ goes to a high-impedance state. $\overline{WDO}$ is then pulled high through the pullup resistor.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 CWD Functionality

The TPS3852 features three options for setting the watchdog window: connecting a capacitor to the CWD pin, connecting a pullup resistor to VDD, and leaving the CWD pin unconnected. Figure 18 shows a schematic drawing of all three options. If this pin is connected to VDD through a 10-kΩ pullup resistor or left unconnected (high impedance), then the factory-programmed watchdog timeouts are enabled; see the *Timing Requirements* table. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

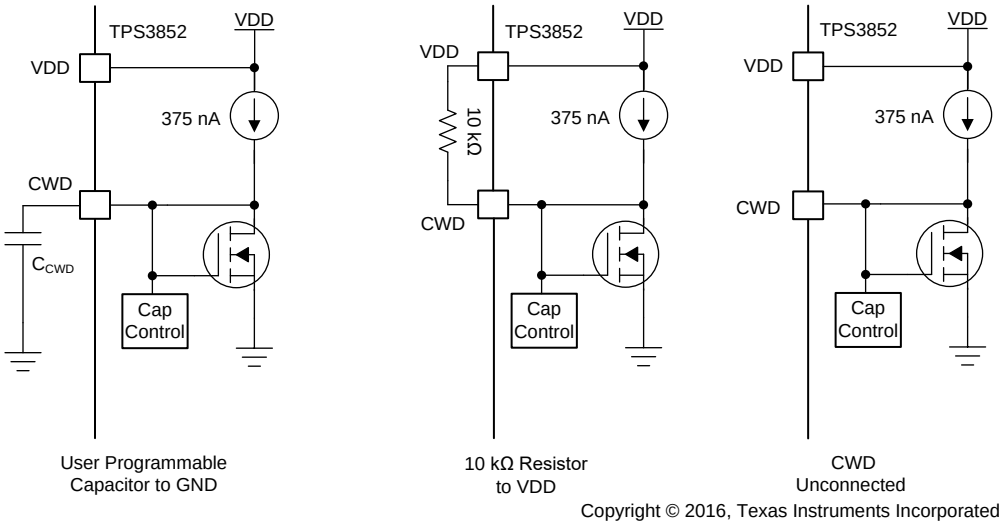


Figure 18. CWD Charging Circuit

8.1.1.1 Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in Table 2), the CWD pin must either be unconnected or pulled up to VDD through a 10-kΩ pullup resistor. Using these options enables high-precision, 15% accurate watchdog timing.

Table 2. Factory-Programmed Watchdog Timing

INPUT		WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
NC	0	Watchdog disabled			Watchdog disabled			
	1	680	800	920	1360	1600	1840	ms
10 kΩ to VDD	0	Watchdog disabled			Watchdog disabled			
	1	1.5	1.85	2.2	8.8	11.0	13.2	ms

8.1.1.2 Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375-nA current source charges C_{CWD} until V_{CWD} = 1.21 V. The TPS3852 determines the window watchdog upper boundary with the formula given in Equation 1, where C_{CWD} is in microfarads (µF) and t_{WDU} is in seconds.

$$t_{WDU(typ)}(s) = 77.4 \times C_{CWD}(\mu F) + 0.055(s) \quad (1)$$

The TPS3852 is limited to using C_{CWD} capacitors between 100 pF and 1 µF. Note that Equation 1 is for ideal capacitors, capacitor tolerances cause the actual device timing to vary. For the most accurate timing, use ceramic capacitors with COG dielectric material. As shown in Table 4, when using the minimum capacitance of 100 pF, the watchdog upper boundary is 62.74 ms; whereas with a 1-µF capacitance, the watchdog upper boundary is 77.455 seconds. If a C_{CWD} capacitor is used, Equation 1 can be used to set t_{WDU} the window watchdog upper boundary. Table 3 shows how t_{WDU} can be used to calculate t_{WDL}.

Table 3. Programmable CWD Timing

INPUT		WATCHDOG LOWER BOUNDARY (t_{WDL})			WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
CWD	SET1	MIN	TYP	MAX	MIN	TYP	MAX	
C_{CWD}	0	Watchdog disabled			Watchdog disabled			
	1	$t_{WDU(min)}$ x 0.5	t_{WDU} x 0.5	$t_{WDU(max)}$ x 0.5	0.85 x $t_{WDU(typ)}$	$t_{WDU(typ)}$ (1)	1.15 x $t_{WDU(typ)}$	s

(1) Calculated from Equation 1 using ideal capacitors.

Table 4. t_{WDU} Values for Common Ideal Capacitor Values

C_{CWD}	WATCHDOG UPPER BOUNDARY (t_{WDU})			UNIT
	MIN (1)	TYP	MAX (1)	
100 pF	53.32	62.74	72.15	ms
1 nF	112.5	132.4	152.2	ms
10 nF	704	829	953	ms
100 nF	6625	7795	8964	ms
1 µF	65836	77455	89073	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

8.1.2 Overdrive Voltage

Forcing a $\overline{\text{RESET}}$ is dependent on two conditions: the amplitude V_{DD} is beyond the trip point (ΔV_1 and ΔV_2), and the length of time that the voltage is beyond the trip point (t_1 and t_2). If the voltage is just under the trip point for a long period of time, $\overline{\text{RESET}}$ asserts and the output is pulled low. However, if V_{DD} is just under the trip point for a few nanoseconds, $\overline{\text{RESET}}$ does not assert and the output remains high. The length of time required for $\overline{\text{RESET}}$ to assert can be changed by increasing the amount V_{DD} goes under the trip point. If V_{DD} is under the trip point by 10%, the amount of time required for the comparator to respond is much faster and causes $\overline{\text{RESET}}$ to assert much quicker than when barely under the trip point voltage. Equation 2 shows how to calculate the percentage overdrive.

$$\text{Overdrive} = |(V_{DD} / V_{ITX} - 1) \times 100\% | \quad (2)$$

In Equation 2, V_{ITX} corresponds to the threshold trip point. If V_{DD} is exceeding the positive threshold, $V_{ITN} + V_{HYST}$ is used. V_{ITN} is used when V_{DD} is falling below the negative threshold. In Figure 19, t_1 and t_2 correspond to the amount of time that V_{DD} is over the threshold; the propagation delay versus overdrive for V_{ITN} and $V_{ITN} + V_{HYST}$ is illustrated in Figure 13 and Figure 14, respectively.

The TPS3852 is relatively immune to short positive and negative transients on VDD because of the overdrive voltage.

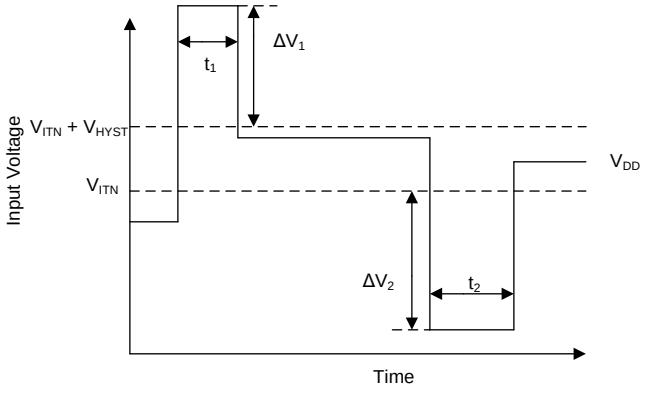


Figure 19. Overdrive Voltage

8.2 Typical Application

A typical application for the TPS3852 is shown in Figure 20. The TPS3852G33 is used to monitor the 3.3-V, V_{CORE} rail powering the microcontroller.

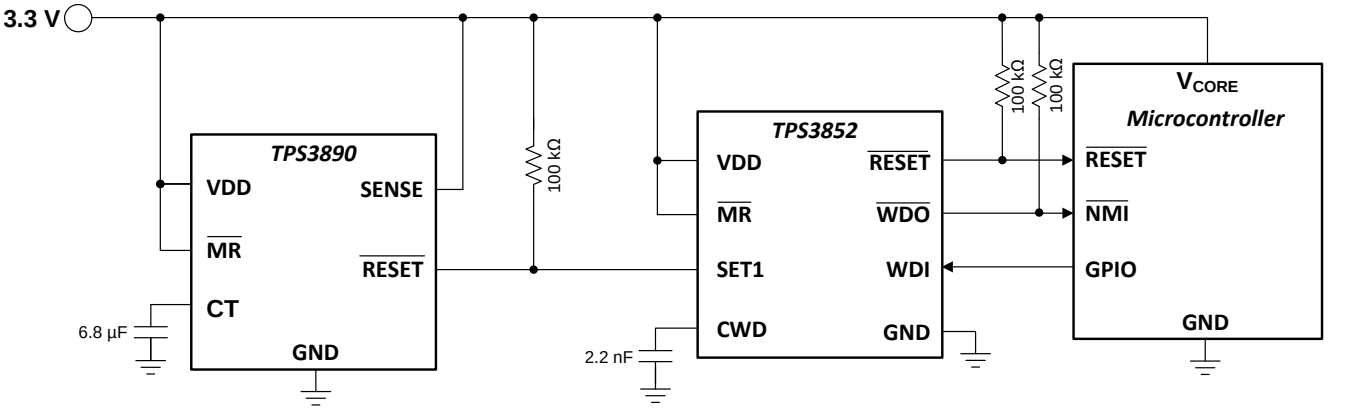


Figure 20. Monitoring Supply Voltage and Watchdog Supervision of a Microcontroller

8.2.1 Design Requirements

Parameter	Design Requirement	Design Result
Watchdog Disable For Initialization Period	Watchdog must remain disabled for 7 seconds until logic enables the watchdog timer	7.21 seconds (typ)
Output Logic Voltage	3.3V CMOS	3.3V CMOS
Monitored Rail	3.3 V with a 5% threshold	Worst Case V_{ITN} = 3.142 V (- 4.7% threshold)
Watchdog Window	250 ms, maximum	$t_{WDL(max)}$ = 135 ms, $t_{WDU(min)}$ = 181 ms
Maximum Device Current Consumption	50 uA	52 uA (worst case) when $\overline{\text{RESET}}$ or $\overline{\text{WDO}}$ is asserted(1)

(1) Only includes the TPS3852G33 current consumption.

8.2.2 Detailed Design Procedure

8.2.2.1 Monitoring the 3.3V Rail

This application calls for very tight monitoring of the rail with only 5% of variation allowed on the rail. To ensure this requirement is met, the TPS3852G33 was chosen for its -4% threshold. To calculate the worst-case for V_{ITN}, the accuracy must also be taken into account. The worst-case for V_{ITN} can be calculated by Equation 3:

$$V_{ITN(Worst\ Case)} = V_{ITN(typ)} \times 0.992 = 3.3 \times 0.96 \times 0.992 = 3.142\ V \quad (3)$$

8.2.2.2 Calculating $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ Pullup Resistor

The TPS3852 uses an open-drain configuration for the $\overline{\text{RESET}}$ circuit, as shown in Figure 21. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET attempts to pull the drain to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below the maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{RESET}}$ pin current ($I_{\overline{\text{RESET}}}$), and V_{OL}. The maximum V_{OL} is 0.4 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.4 V with $I_{\overline{\text{RESET}}}$ kept below 10 mA. For this example, with a V_{PU} of 3.3 V, a resistor must be chosen to keep $I_{\overline{\text{RESET}}}$ below 50 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 100 kΩ was selected, which sinks a maximum of 33 μA when $\overline{\text{RESET}}$ or $\overline{\text{WDO}}$ is asserted. As illustrated in Figure 11, when the $\overline{\text{RESET}}$ current is at 33 μA and the low-level output voltage is approximately zero.

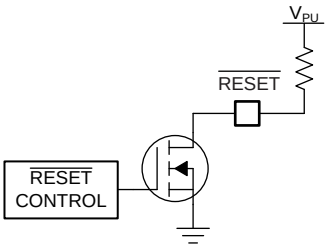


Figure 21. $\overline{\text{RESET}}$ Open-Drain Configuration

8.2.2.3 Setting the Window Watchdog

As illustrated in Figure 18, there are three options for setting the window watchdog. The design specifications in this application require the programmable timing option (external capacitor connected to CWD). When a capacitor is connected to the CWD pin, the window is governed by Equation 4. Equation 4 is only valid for ideal capacitors, any temperature or voltage derating must be accounted for separately.

$$C_{CWD}\left(\mu F\right) = \frac{t_{WDU} - 0.055}{77.4} = \frac{0.25 - 0.055}{77.4} = 0.0025\ \mu F \tag{4}$$

The nearest standard capacitor value to 2.5 nF is 2.2 nF. Selecting 2.2 nF for the C_{CWD} capacitor gives the following minimum and maximum timing parameters:

$$t_{WDU(MIN)} = 0.85 \times t_{WDU(TYP)} = 0.85 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right) = 191\ \text{ms} \tag{5}$$

$$t_{WDL(MAX)} = 0.5 \times t_{WDU(MAX)} = 0.5 \times \left[1.15 \times \left(77.4 \times 2.2 \times 10^{-3} + 0.055\right)\right] = 129\ \text{ms} \tag{6}$$

Capacitor tolerance also influence $t_{WDU(MIN)}$ and $t_{WDL(MAX)}$. Select a ceramic COG dielectric capacitor for high accuracy. For 2.2 nF, COG capacitors are readily available with a 5% tolerance, which results in a 5% decrease in $t_{WDU(MIN)}$ and a 5% increase in $t_{WDL(MAX)}$, giving 181 ms and 135 ms, respectively. A falling edge must be issued within this window.

8.2.2.4 Watchdog Disabled During Initialization Period

The watchdog is often needed to be disabled during startup to allow for an initialization period. When the initialization period is over, the watchdog timer is turned back on to allow the microcontroller to be monitored by the TPS3852. To achieve this setup SET1 must start at GND. In this design, SET1 is controlled by a TPS3890 supervisor. In this application, the TPS3890 was chosen to monitor V_{DD} as well, which means that $\overline{\text{RESET}}$ on the TPS3890 stays low until V_{DD} rises above V_{ITN}. When V_{DD} comes up, the delay time can be adjusted through the CT capacitor on the TPS3890. With this approach, the $\overline{\text{RESET}}$ delay can be adjusted from a minimum of 25 μs to a maximum of 30 seconds. For this design, a minimum delay of 7 seconds is needed until the watchdog timer is enabled. The CT capacitor calculation (see the TPS3890 data sheet) yields an ideal capacitance of 6.59 μF, giving a closest standard ceramic capacitor value of 6.8 μF. When connecting a 6.8-μF capacitor from CT to GND, the typical delay time is 7.21 seconds. Figure 22 illustrates the typical startup waveform for this circuit when the watchdog input is off. Figure 22 illustrates that when the watchdog is disabled, the $\overline{\text{WDO}}$ output remains high. See the TPS3890 data sheet for detailed information on the TPS3890.

8.2.3 Glitch Immunity

Figure 25 shows the high to low glitch immunity for the TPS3852G33 with a 7% overdrive with V_{DD} starting at 3.3 V. This curve shows that V_{DD} can go below the threshold for 5.2 µs without $\overline{\text{RESET}}$ asserting.

8.2.4 Application Curves

Unless otherwise stated, application curves were taken at T_A = 25°C.

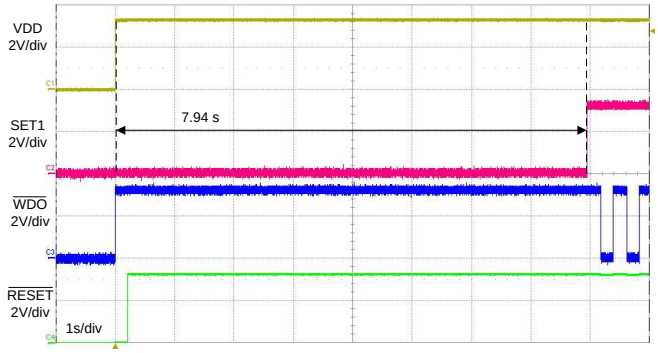


Figure 22. Startup Without a WDI Signal

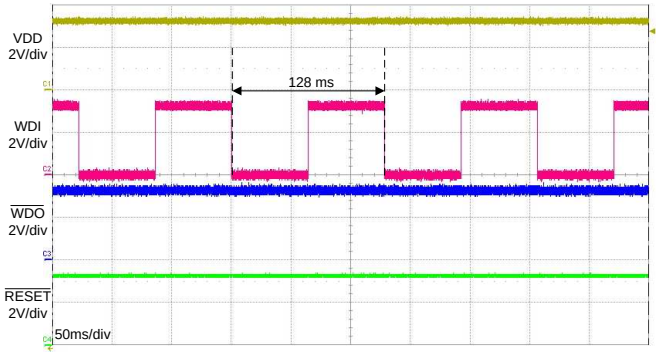


Figure 23. Typical WDI Signal

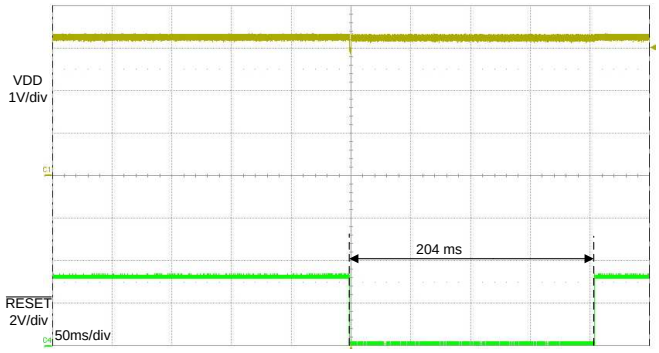


Figure 24. Typical $\overline{\text{RESET}}$ Delay

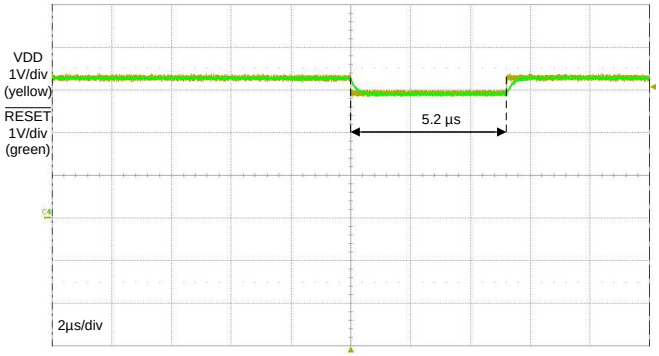


Figure 25. High to Low Glitch Immunity

9 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.6 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-µF capacitor between the VDD pin and the GND pin.

10 Layout

10.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CWD} capacitor or pull-up resistor is used place them as close as possible to the CWD pin. If the CWD pin is left unconnected make sure to minimize the amount of parasitic capacitance on the pin.
- The pull-up resistors on $\overline{\text{RESET}}$ and $\overline{\text{WDO}}$ should be placed as close to the pin as possible.

10.2 Layout Example

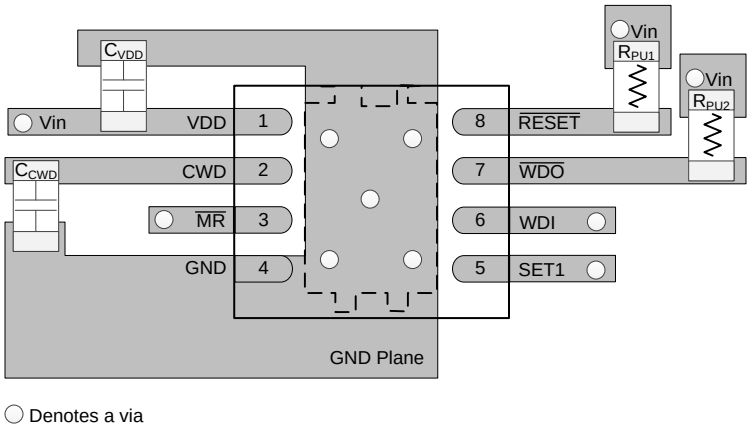


Figure 26. Typical Layout For TPS3852

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

The *TPS3851EVM-780 Evaluation Module* can be used to evaluate this part. If this evaluation module is being used then the part on the EVM must be changed to the TPS3852.

11.1.2 Device Nomenclature

Table 5. Device Nomenclature

DESCRIPTION	NOMENCLATURE	VALUE
TPS3852 (high-accuracy supervisor with window watchdog)	—	—
X (nominal threshold as a percent of the nominal monitored voltage)	G	V_{ITN} = –4%
	H	V_{ITN} = –7%
yy(y) (1) (nominal monitored voltage option)	33	3.3 V

(1) For example TPS3852G33 corresponds to a 3.3 V nominal monitored voltage with a -4% nominal threshold.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *TPS3890 Low Quiescent Current, 1% Accurate Supervisor with Programmable Delay* (SLVSD65)
- *TPS3851EVM-780 Evaluation Module* (SBVU033)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3852G33DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	852GA	Samples
TPS3852G33DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	852GA	Samples
TPS3852H33DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	852PA	Samples
TPS3852H33DRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	852PA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

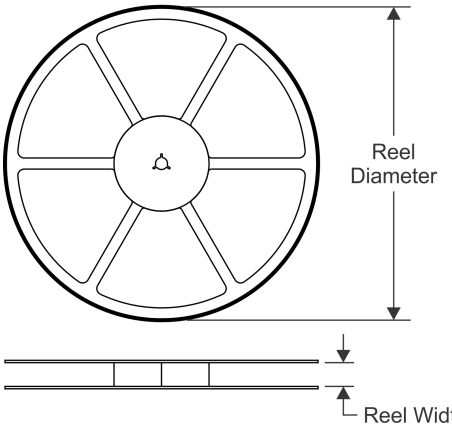
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

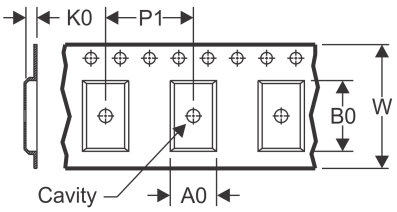
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

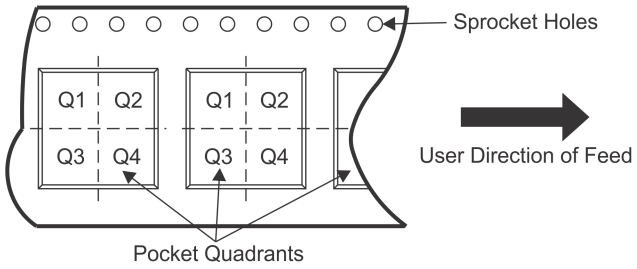


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

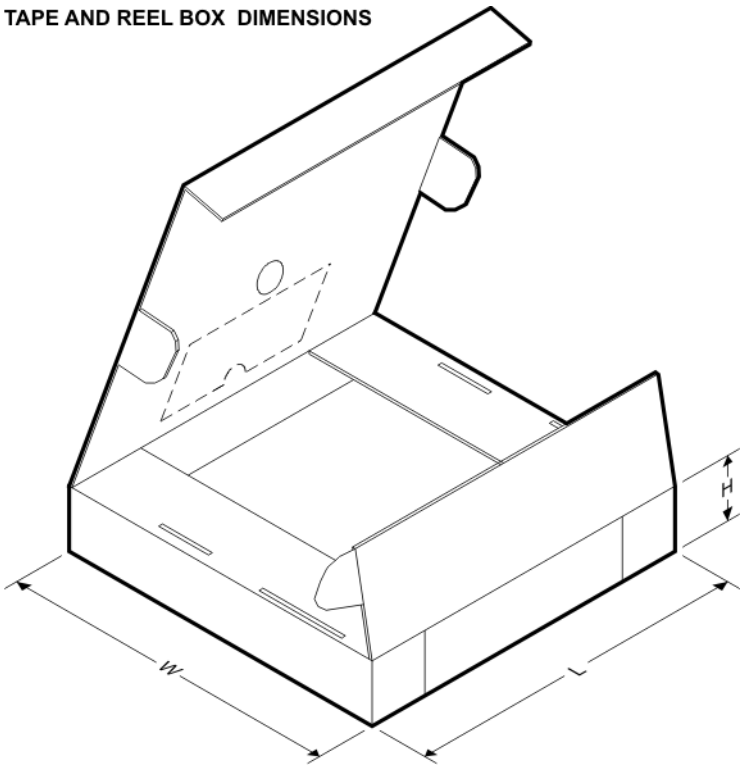
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3852G33DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3852G33DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3852H33DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS3852H33DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

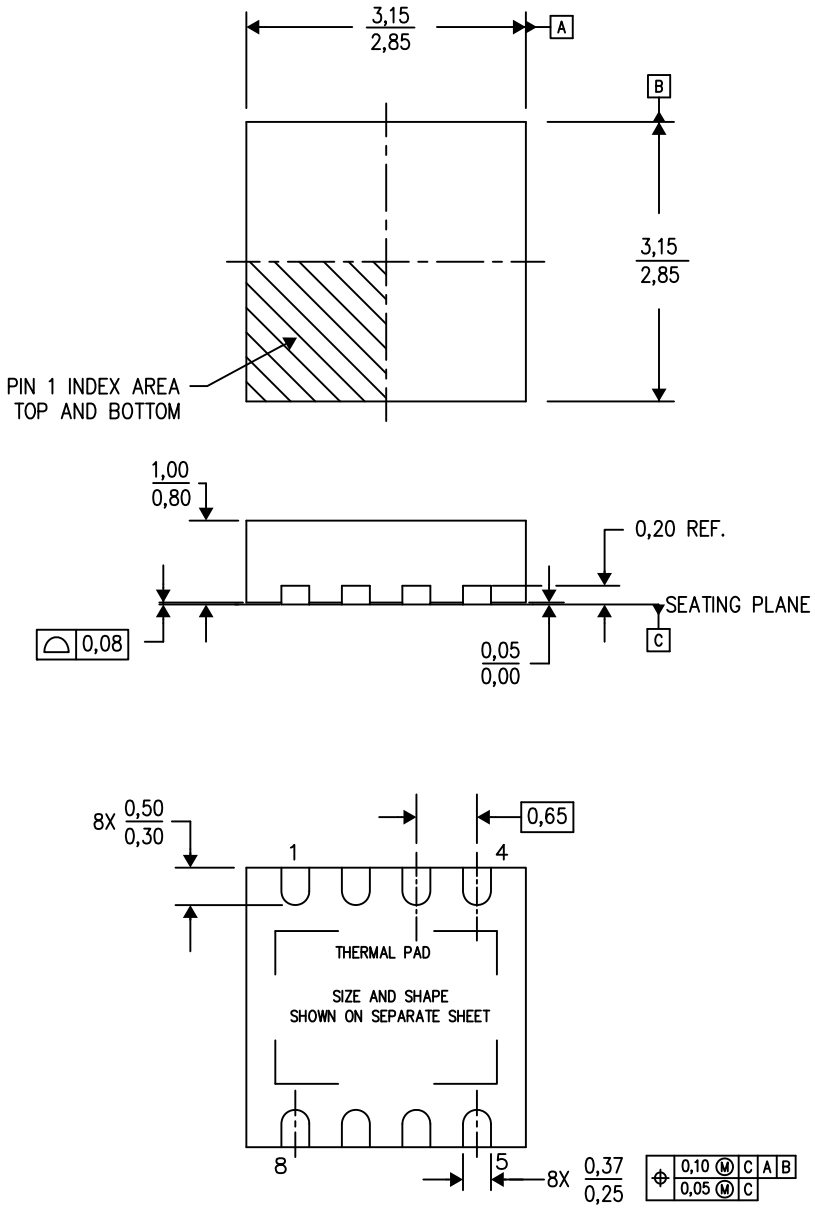
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3852G33DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS3852G33DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS3852H33DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS3852H33DRBT	SON	DRB	8	250	210.0	185.0	35.0

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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