# 1.2 - 8V, 3A PFET High Side Load Switch with Level Shift & Adjustable Slew Rate Control

**Check for Samples: TPS27081A**

## FEATURES

- **Low ON Resistance, High current PFET**
  - **$R_{DS(ON)}$ = 32mΩ (Typ) at $V_{GS}$ = –4.5V**
  - **$R_{DS(ON)}$ = 44mΩ (Typ) at $V_{GS}$ =–3.0V**
  - **$R_{DS(ON)}$ = 85mΩ (Typ) at $V_{GS}$ = –1.8V**
  - **$R_{DS(ON)}$ = 85mΩ (Typ) at $V_{GS}$ = –1.5V**
  - **$R_{DS(ON)}$ = 155mΩ (Typ) at $V_{GS}$ = –1.2V**
- **Adjustable Turn-ON and Turn-OFF slew rate control through discrete components R1, R2, and C1**
- **Supports a wide range of 1.2V up to 8V supply inputs**
- **Integrated NMOS for Inrush current Control**
- **NMOS Enable Supports a Wide Range of 1.2V up to 8V Control logic Interface**
- **Full Protection Against ESD (All Pins)**
  - **HBM 2kV, CDM 500V**
- **Ultra Low Leakage Current in Stand-by (Typ 100nA)**
- **–40°C to 85°C Temperature Rating**
- **Available in Tiny 6-pin Packages**
  - **2.9mm x 1.6mm Thin (0.9mm max) SOT-23 (DDC)**
  - **2mm x 2mm SON-6 (DRV) Preview Only**

## APPLICATIONS

- **High Side Load Switch**
- **Inrush-current control**
- **Power Sequencing and Control**
- **Stand-by Power Isolation**
- **Portable Power Switch**

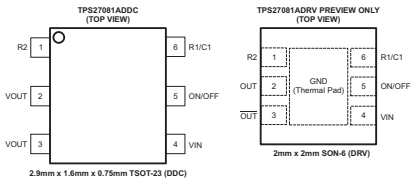


**Figure 1. TPS27081A Packages**

## DESCRIPTION

The TPS27081A IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package.

The TPS27081A is fully protected against ESD strikes on all pins. The TPS27081A features industry-standard ESD protection on all pins thus providing better ESD compatibility with other on-board components.

The TPS27081A level shifts ON/OFF logic signal to VIN levels and thus supports as low as 1.2V CPU or MCU logic to control higher voltage power supplies (VIN) without requiring an external level shifter.

Switching a large value output capacitor CL through a fast ON/OFF logic signal may result in an excessive inrush current. To control the load inrush current connect a resistor R2, as shown in Figure 2 To further limit the inrush current add an external capacitor C1. To configure the TPS27081A to achieve a specific slew rate refer to the Application section.

A single external component, R1, is required in applications that do not require inrush current control. In such applications connect the TPS27081A pin R2 to system ground.

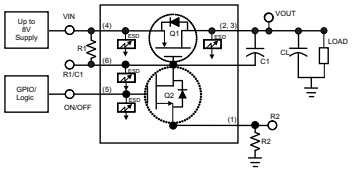


**Figure 2. Simplified Block & Application Diagram**

**Component Table (Typical Application)**

| COMPONENT | DESCRIPTION |
|---|---|
| R1 | Level Shift Pull-up Resistor |
| R2 | Optional(1) |
| C1 | Optional(1) |

(1) Required for load inrush current (slew rate) control

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| $T_A$ | PART NUMBER | PACKAGE | | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TPS27081ADDCR | 6-Pin TSOT | Reel of TBD | TBD |
| | TPS27081ADRVR | 6-Pin SON | Contact factory for availability(2) | Contact factory for availability(1) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Contact factory for details and availability for PREVIEW devices, minimum order quantity may apply.

## ABSOLUTE MAXIMUM RATINGS(1)(2)

Specified at $T_J$ = –40°C to 125°C unless otherwise noted.

| | | | VALUE | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{IN}$ | VIN/R1 Pin Maximum Voltage (VDS, VGS,VGD of Q1) | | –0.3 | 8 | V |
| $V_{EN}$ | Enable voltage (VGS of Q2) | | –0.3 | 8 | V |
| $I_{Q1-ON}$ | Max Continuous Drain Current of Q1 | | | 3 | A |
| | Max Pulsed Drain Current of Q1(3) | | | 9.5 | |
| $I_{F-peak}$ | Free-wheeling Diode Peak Forward Current | | | 140 | mA |
| $P_D$ | Max power dissipation at $T_A$ = 25°C, $T_J$ = 150°C(3) | 6 Pin - TSOT, $T_{JA}$ = 180°C/W | | 1190 | mW |
| All pins | ESD Rating – HBM | | | 2000 | V |
| | ESD Rating – MM | | | 200 | |
| | ESD Rating – CDM | | | 500 | |
| $T_A$ | Operating free-air ambient temperature range | | –40 | 85 | °C |
| $T_{J-max}$(4) | Operating virtual junction temperature | | | 150 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance
(3) Pulse Width <300us, Duty Cycle <2%
(4) Operating at the absolute $T_{J-max}$ of 150°C can affect reliability – for higher reliability it is recommended to ensure $T_J$ <125°C

## DISSIPATION RATINGS(1)(2)

| BOARD | PACKAGE | $\theta_{JC}$ | $\theta_{JA}$(3) | $T_A$ < 25°C | $T_A$ = 70°C | $T_A$ = 85°C | $T_A$ = 105°C | DERATING FACTOR ABOVE $T_A$ = 25ºC |
|---|---|---|---|---|---|---|---|---|
| High-K | 6-Pin TSOT (DDC) | TBD°C/W | 105°C/W | 1190 mW/ºC | 760 mW | 619 mW | 428 mW | 9.55 mW/°C |

(1) Maximum dissipation values for retaining a safe maximum device junction temperature of 125°C
(2) Refer to TI's design support web page at www.ti.com/thermal for improving device thermal performance.
(3) Operating at the absolute $T_{J-max}$ of 150°C can affect reliability

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DS}$ | Pins VIN1/R1 and VOUT/C1 voltage difference | -0.3 | | 7 | V |
| $V_{IL}$ | EN Pin Low-level input voltage | | | 0.4 | V |
| $V_{IH}$ | EN Pin High-level input voltage | 1.2 | | | V |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

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## ELECTRICAL CHARACTERISTICS

Specified over the recommended junction temperature range $T_J$ = –40°C to 125°C unless otherwise noted. Typical values are at $T_J$ = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{IN}$ | VIN breakdown voltage | $V_{EN}$ = 0 V, ID = 250 µA | 8 | | | V |
| $IF_{Leak}$ | Forward leakage current | VIN= 8 V, EN= 0 V | | 100 | | nA |
| **ON CHARACTERISTICS**(1) | | | | | | |
| $VTH_{Q1}$ | Q1 Threshold voltage (VGS) | ID(Q1) = 250 µA | | –0.7 | –0.85 | V |
| $VTH_{Q2}$ | Q2 Threshold voltage (VGS) | ID(Q2) = 250 µA | | 0.6 | 0.76 | V |
| $R_{DSQ1(ON)}$ | Q1 Channel ON resistance | VGS = -4.5 V, ID = 3.0 A | | 32 | 55 | mΩ |
| | | VGS = -3.0 V, ID = 2.5 A | | 44 | 77 | |
| | | VGS = -2.5 V, ID = 2.5 A | | 50 | 85 | |
| | | VGS = -1.8 V, ID = 2.0 A | | 82 | 147 | |
| | | VGS = -1.5 V, ID = 1.0 A | | 93 | 166 | |
| | | VGS = -1.2 V, ID = 0.5 A | | 155 | 260 | |
| $R_{DSQ2(ON)}$ | Q2 Channel ON resistance | VGS = 4.5 V, ID = 0.4 A | | 1.8 | 3 | Ω |
| | | VGS = 3.0 V, ID = 0.3 A | | 2.3 | 6.2 | |
| | | VGS = 2.5 V, ID = 0.2 A | | 2.6 | 6.1 | |
| | | VGS = 1.8 V, ID = -0.1 A | | 3.8 | 10 | |
| | | VGS = -1.5 V, ID = 0.05 A | | 4.4 | 8.5 | |
| | | VGS = 1.2 V, ID = 0.03 A | | 6.25 | 13.5 | |
| **Q1 DRAIN-SOURCE DIODE PARAMETERS**(1)(2) | | | | | | |
| $IF_{SD}$ | Source-drain diode peak forward current | $VF_{SD(Q1)}$= 0.8 V | 0.8 | 1.0 | | A |
| $V_{SD}$ | Source-drain diode forward voltage | VEN = 0 V, $IF_{SD(Q1)}$ = –0.6A | | | 1 | V |

(1) Pulse width <300 µs, Duty Cycle <2.0%
(2) Not rated for continuous current operation

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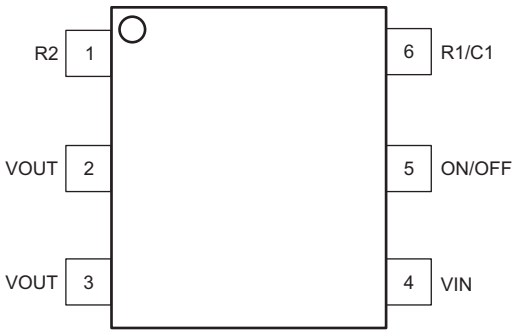
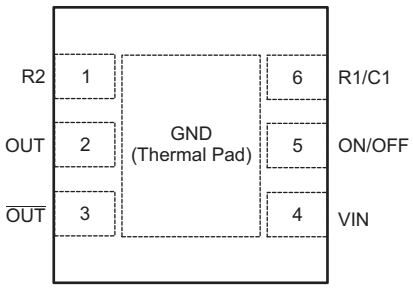
## DEVICE INFORMATION

TPS27081ADDC




2.9mm x 1.6mm TSOT-23 (DDC)
(TOP VIEW)

TPS27081ADRV PREVIEW ONLY




2mm x 2mm SON-6 (DRV)
(TOP VIEW)

### TPS27081A PIN DESCRIPTION

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NUMBER | |
| R2 | 1 | Source Terminal of NMOS (Q2) - Connect to system GND directly or through a slew control resistor |
| VOUT | 2, 3 | Drain Terminal of Power PFET (Q1) - Connect a slew control capacitor between pins VOUT/C1 and R1/C1 |
| VIN | 4 | Source Terminal of Power PFET (Q1) - connect a slew control/pull-up resistor between the pins VIN/R1 and R1/C1 |
| ON/OFF | 5 | Active high enable pin – when driven with a high impedance driver connect an external pull down resistor to GND |
| R1/C1 | 6 | Gate Terminal of Power PFET (Q1) |

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## APPLICATION INFORMATION

The TPS27081A IC is a high side load switch that integrates a Power PFET and a Control NMOS in a tiny package. The TPS27081A internal components are rated for up to 8V supply and support up to 3A of load current.The TPS27081A can be used in a variety applications. Figure 3 below shows a general application of TPS27081A to control the load inrush current.

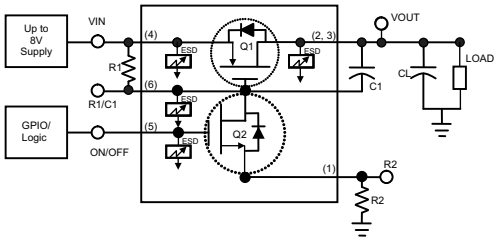


**Figure 3. Typical Application Diagram**

### Configuring Q1 ON Resistance

The $V_{GS-Q1}$ Gate-Source voltage across the PMOS transistor Q1 sets its ON resistance $RDS_{Q1(ON)}$. Directly connecting the pin R2 to ground maximizes the ON state $V_{GS-Q1}$ and thus minimizes the VIN to VOUT voltage dropout. When a resistor R2 is installed to control the Turn-ON slew rate then $V_{GS-Q1}$ is given by:

$$VGS_{Q1} = VIN \times \frac{R2}{R1 + R2} V \quad (1)$$

e.g. R1= 10 x R2, VIN = 5V sets $V_{GS-Q1}$ = 4.5V

**Note:** It is recommended to keep R1 > 20 x R2; while limiting maximum value of resistor R1 to approximately 2MΩ

### Configuring Turn-ON Slew Rate

Switching a large capacitive load CL instantaneously results in a load inrush current given by the following equation:

$$I_{inrush} = C_{load} \times \frac{dv}{dt} = C_{load} \times \frac{VOUT_{final} - VOUT_{initial}}{\text{Vout Slew Rate}} \quad (2)$$

An uncontrolled fast rising ON/OFF logic input may result in a high slew rate at the output resulting in a very high dv/dt thus leading to a higher inrush current. To control the inrush current connect a resistor R2 and a capacitor C1 as shown in the Figure 3. Use the following equation to configure the TPS27081A slew rate to a specific value. Refer to Table 1 for component values to configure TPS27081A to achieve standard slew rates.

$$t_{rise} = \frac{3.9 \times R2 \times C1}{VIN^{2/3}} sec \quad (3)$$

Where $t_{rise}$ is the time delta starting from the ON/OFF signal's rising edge to charge up the load capacitor CL from 10% to 90% of VIN voltage.

**Note:** The $t_{rise}$ equation is accurate to within +/-20% across full VIN range supported by TPS27081A. Ensure that R1 > 10xR2.

**Table 1. Component Values for VOUT Rise Time**

| Rise Time (sec) | VIN (V) | R2 (Ω) | C1 (µF) | CL (µF)(1) |
|---|---|---|---|---|
| 250n | 5.0 | 0 (short) | 0 (open) | 0 (open) |
| 100µ | 5.0 | 6.65k | 0.01 | 10.0µ |
| 200µ | 1.2 | 5.23k | 0.01 | 10.0µ |
| 470µ | 5.0 | 3.30k | 0.12 | 10.0µ |

(1) Component values for VOUT rise time

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**Table 1. Component Values for VOUT Rise Time (continued)**

| Rise Time (sec) | VIN (V) | R2 (Ω) | C1 (µF) | CL (µF)(1) |
|---|---|---|---|---|
| 1.00m | 5.0 | 61.9k | 0.01 | 10.0µ |
| 12.0m | 5.0 | 61.9k | 0.12 | 470µ |
| 21.0m | 1.5 | 61.9k | 0.12 | 470µ |
| 600m | 3.0 | 333k | 1.00 | 10.0µ |

## Low Voltage ON/OFF Interface

The $VGS_{Q2}$ is set by the ON/OFF logic level. To turn ON, the transistor Q2 requires a VGS > 1.0V (Typical). For reliable operation apply ON/OFF logic that has the following VIH and VIL limits:

$VIH_{ON}$ > 1.0V + $I_{Q2}$ × R2 V

$VIH_{OFF}$ 0.4 V

Minimizing $I_{Q2}$ x R2 drop helps achieve a direct interface with a low voltage ON/OFF logic. To minimize $I_{Q2}$ x R2 voltage drop select a high R1/R2 ratio. E.g. When VIN= 1.8V, selecting R1/R2 = 40 will require $V_{IH}$ > 1.0 + 45mV and thus allowing a 1.2V GPIO interface.

In applications where ON/OFF signal is not available connect ON/OFF pin to VIN. The TPS27081A will turn ON/OFF in sync with the input supply connected to VIN.

**Note:** Connect a pull down resistor between ON/OFF pin to GND when ON/OFF is driven by a high-impedance (tri-state) driver.

## On-Chip Power Dissipation

Use the below equation to calculate TPS27081A on-chip power dissipation $P_D$:

$PD = ID_{Q1}2 \times RDS_{Q1(ON)} + ID_{Q2}^2 \times RDS_{Q2(ON)}$

Where, $ID_{Q1}$ and $ID_{Q2}$ are the DC current flowing through the transistors Q1 and Q2 respectively. Refer to the ELECTRICAL CHARACTTERISTICS table and/or Figure x to estimate $RDS_{Q1(ON)}$ and $RDS_{Q1(ON)}$ for various values of $VGS_{Q1}$ and $VGS_{Q2}$ respectively.

**Note:** MOS switches can get extremely hot when operated in saturation region. As a general guideline, to avoid transistors Q1 and Q2 going into saturation region set VGS > VT +VDS. E.g. VGS > 1.5V and VDS < 200mV ensures switching region.

## Thermal Reliability

For higher reliability it is recommended to limit TPS27081A IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate maximum on-chip power dissipation to achieve the maximum die junction temperature target:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA} \quad (4)$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

$T_A$ is the operating ambient temperature.

$R_{\theta JA}$ is the package junction to ambient thermal resistance.

## Improving Package Thermal Performance

The package $\theta_{JA}$ value under standard conditions on a High-K board is listed in the DISSIPATION RATINGS. $\theta_{JA}$ value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce $\theta_{JA}$ and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

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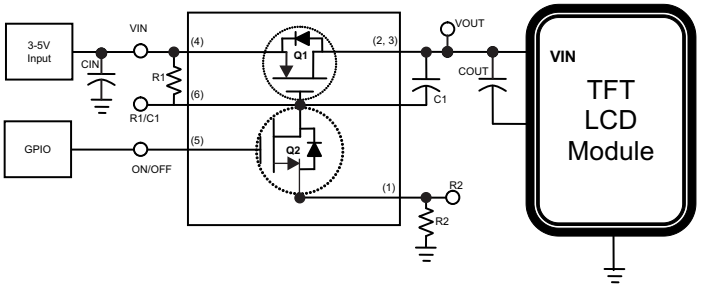
## APPLICATION EXAMPLES

### TFT LCD Module Inrush Current Control

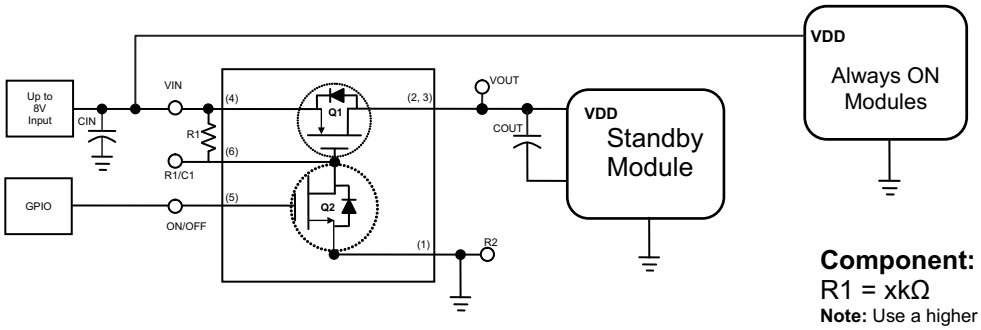



**VOUT rise time** = 470µs
VIN = 5.0V
**Components**:
R1 = xkΩ
R2 = 3.3kΩ
C1 = 120nF

**Figure 4. Inrush Current Control Using TPS27081A**

LCD panels require inrush current control to prevent permanent system damages during turn-ON and turn-OFF events.

### Standby Power Isolation




**Component:**
R1 = xkΩ
**Note:** Use a higher value of R1 to minimize IQ

**Figure 5. Standby Power Generation Using TPS27081A**

Many applications have some always ON modules to support various core functions. However, some modules are selectively powered ON or OFF to save power and multiplexing of various on board resources. Such modules that are selectively turned ON or OFF require standby power generation. In such applications TPS27081 requires only a single pull-up resistor. In this configuration the VOUT voltage rise time is approximately 250ns when VIN = 5V.

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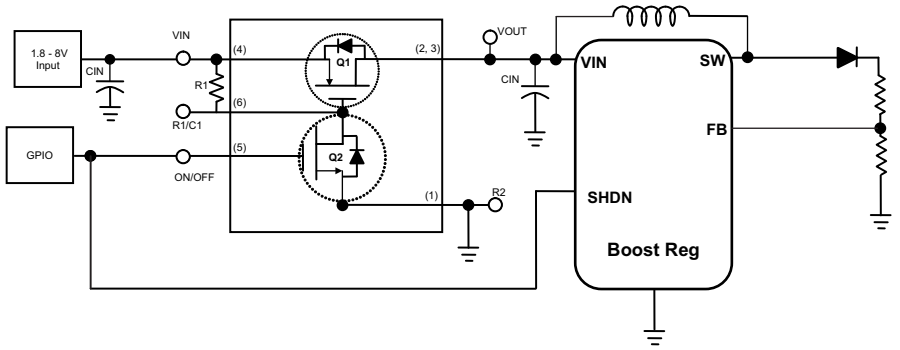
### Boost Regulator with True Shutdown




**Components:**

R1 = xkΩ (for, $IQ_{R1}$ = 3µA @ VIN = 3V)

**Note:** Higher value of resistor R1 minimizes IQ

**Figure 6. True Shutdown Using TPS27081A**

The most common boost regulator topology provides a current leakage path through inductor and diode into the feedback resistor even when the regulator is shut down. Adding a TPS27081A in the input side power path prevents this leakage current and thus providing a true shutdown.

### Single Module Multiple Power Supply Sequencing

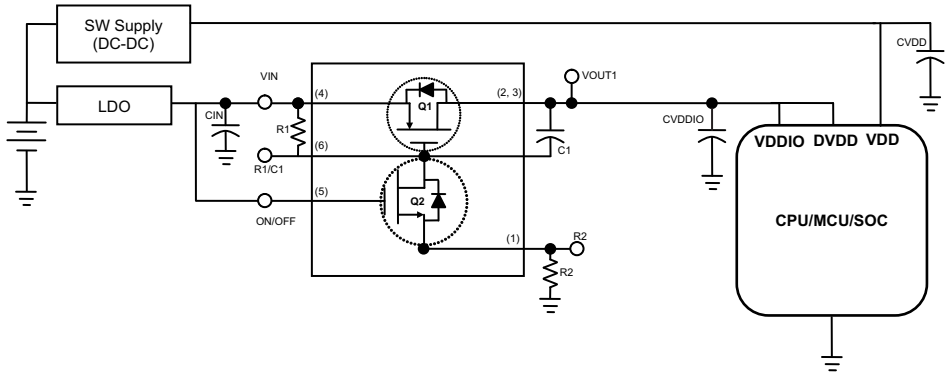



**Figure 7. Power Sequencing Using TPS27081A, Example 1**

Most modern SOCs and CPUs require multiple voltage inputs for its Analog, Digital cores and IO interfaces. These ICs require that these supplies be applied simultaneously or in a certain sequence. TPS27081A when configured, as shown in Figure 7, with the VOUT1 rise time adjusted appropriately through resistor R2 and capacitor C1, will delay the early arriving LDO output to match up with late arriving DC-DC output and thus achieving power sequencing.

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### Multiple Modules Interdependent Power Supply Sequencing

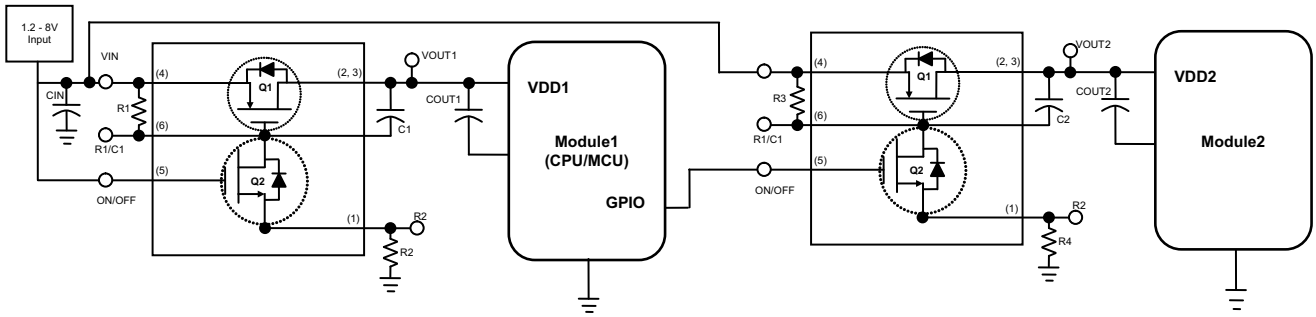


**Figure 8. Power Sequencing Using TPS27081A, Example 2**

For system integrity reasons a certain power sequencing may be required among various modules. As shown in Figure 8, Module 2 will power up only after Module 1 is powered up and the Module 1 GPIO output is enabled to turn ON Module 2. TPS27081A when used as shown in Figure 8 will not sequence the Module 2 power, but also it will help prevent inrush current into the power path of Module 1 and 2.

### Multiple Modules Interdependent Supply Sequencing without a GPIO Input

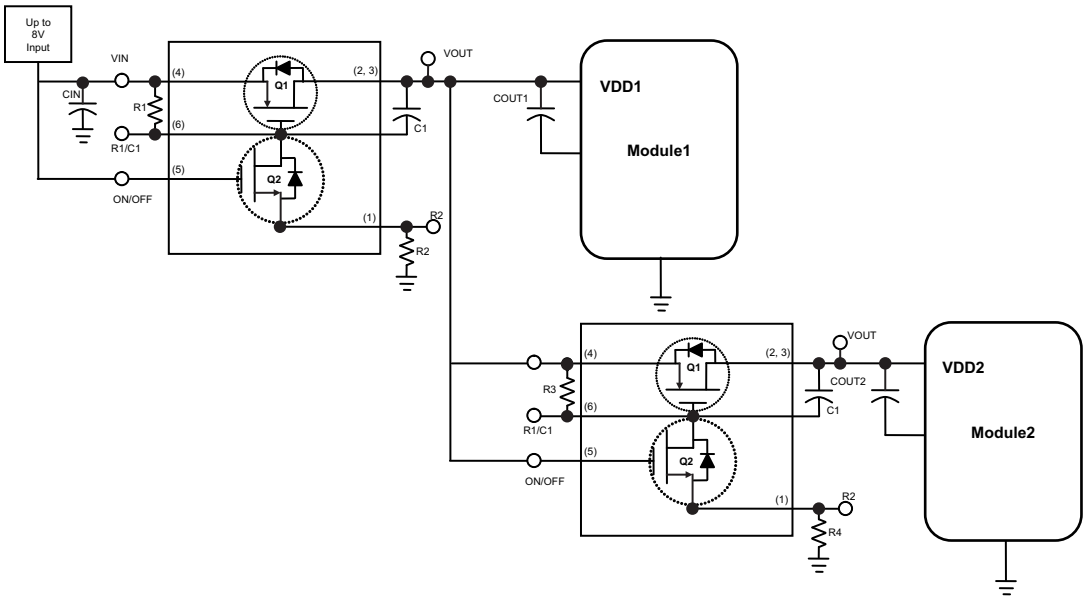


**Figure 9. Power Sequencing using TPS27081A, Example 3**

When a GPIO signal is not available connecting the ON/OFF pin of TPS27081 connected to Module 2 will power up Module 2 after Module 1, when resistor R4 and capacitor C2 are chosen appropriately. The two TPS27081A in this configuration will also control load inrush current.

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## TYPICAL CHARACTERISTICS

$T_A$ = +25°C

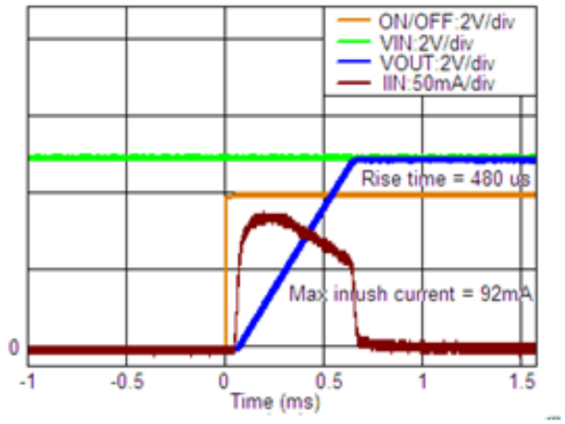



**Figure 10. VIN = 5V, R2 = 3.3kΩ, C1 = 120nF, CL = 10uF**

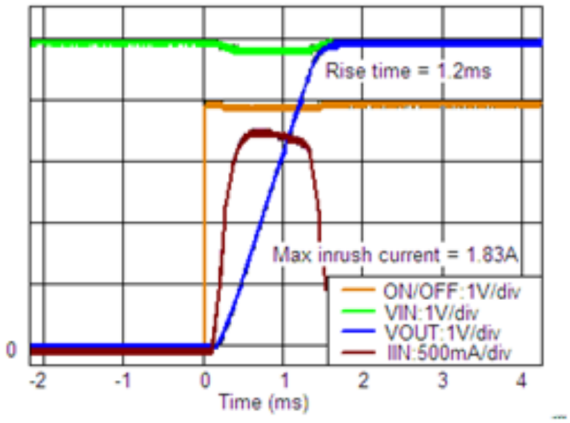



**Figure 11. VIN = 5V, R2 = 6.65kΩ, C1 = 120nF, CL = 470uF**

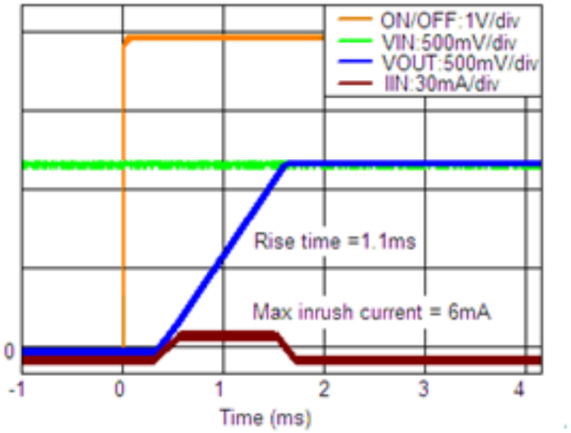



**Figure 12. VIN = 1.2V, R2 = 5.23kΩ, C1 = 120nF, CL = 10uF**

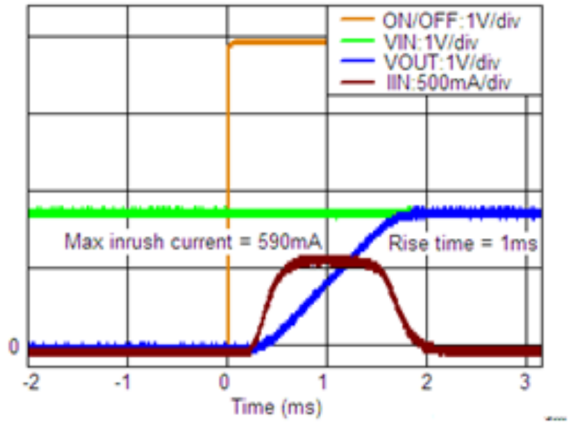



**Figure 13. VIN = 1.8V, R2 = 5.23kΩ, C1 = 120nF, CL = 470uF**

PRODUCT PREVIEW

## TYPICAL CHARACTERISTICS (continued)

$T_A$ = +25°C

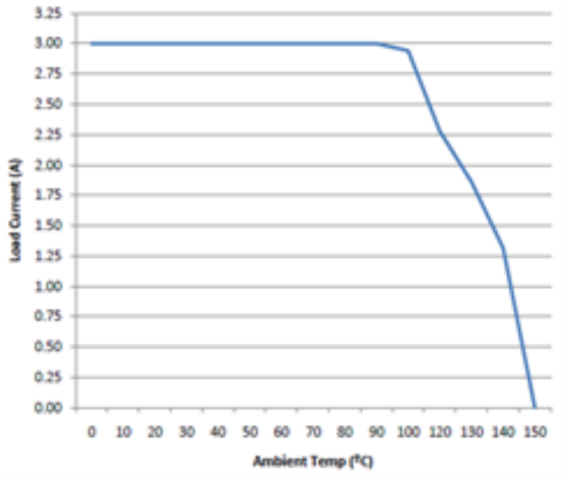



Figure 14. Q1 SOA @ VGS_Q1 = 4.5V

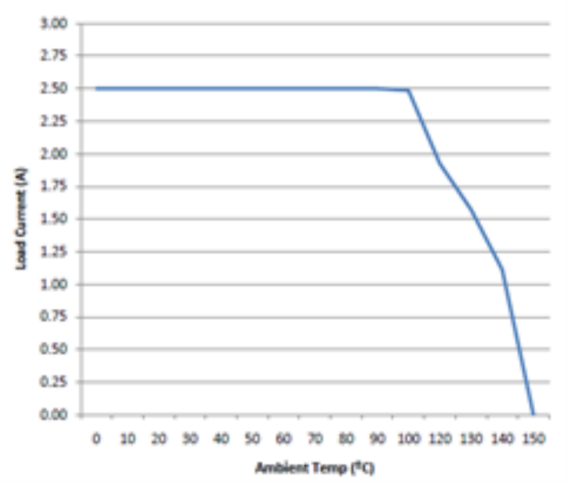



Figure 15. Q1 SOA @ VGS_Q1 = 3.0V

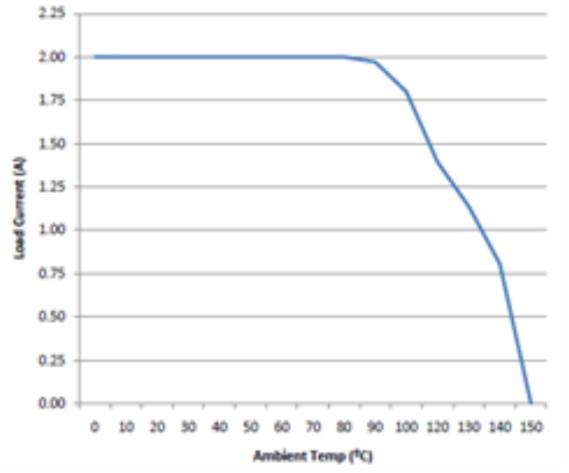



Figure 16. Q1 SOA @ VGS_Q1 = 1.8V

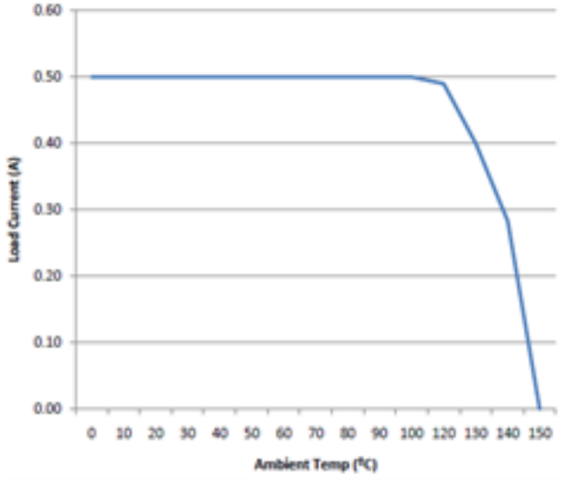



Figure 17. Q1 SOA @ VGS_Q1 = 1.2V

PRODUCT PREVIEW

## PACKAGING INFORMATION

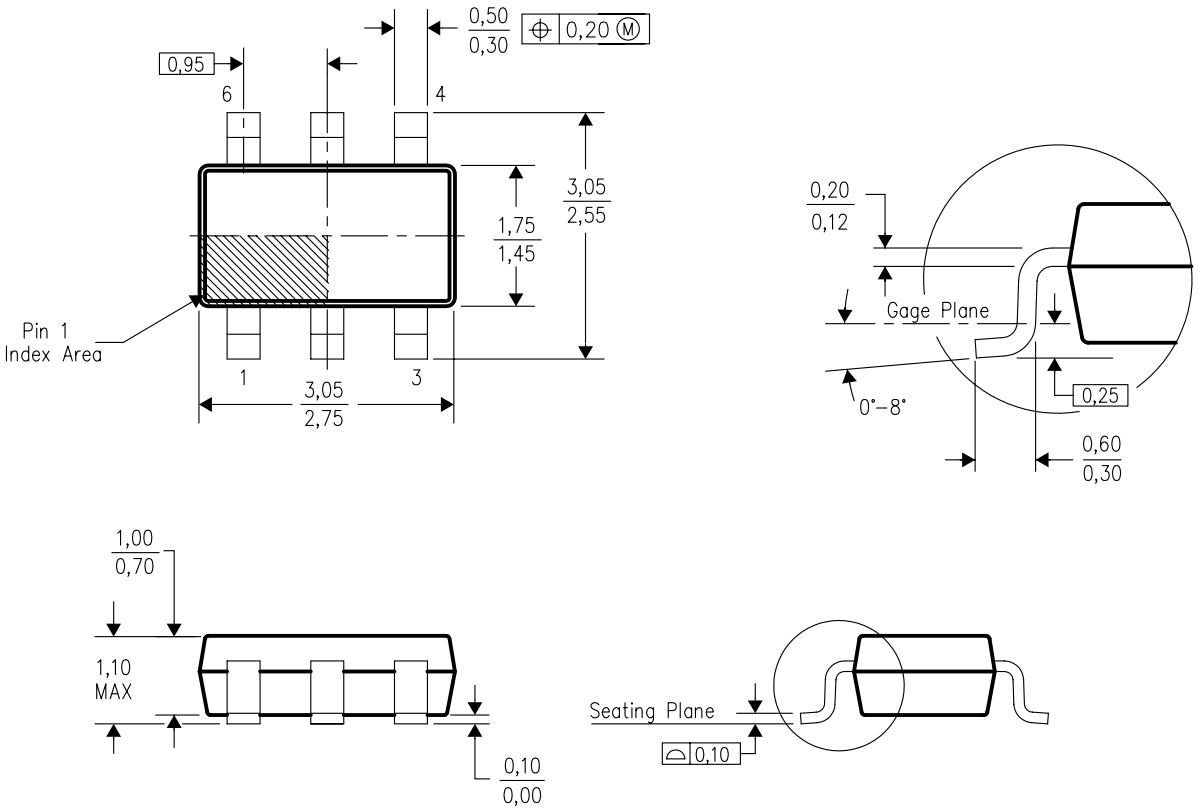
| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TPS27081ADDCR | PREVIEW | SOT | DDC | 6 | 3000 | TBD | Call TI | Call TI | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE




4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

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