TPS24772
TPS24771
TPS24770
SLVSCZ3 – MARCH 2015

TPS2477x 2.5 to 18-V High Performance Hot Swap

1 Features

- 2.5V to 18V Bus Operation (30V abs max)
- Programmable Protection Settings:
  - Current Limit: ±5% at 10mV
  - Fast Trip: ±10% at 20mV
- Programmable FET SOA Protection
- Programable Response Time for Fast Trip
- Dual Timer (Inrush/Fault)
- Analog Current Monitor (1% at 25mV)
- Programmable UV and OV
- Status Flags for Faults and Power Good
- 4mm × 4mm 24-pin QFN
- 70 = Latch, 71 = Retry, 72 = Fast Latch Off

2 Applications

- Enterprise Storage
- Enterprise Server
- Networking Cards
- 240 VA Applications

3 Description

The TPS2477x is a high performance analog Hot Swap Controller for 2.5 V to 18 V systems. The precise and highly programmable protection settings of the TPS2477x aid the design of high power high availability systems where isolating faults is critical.

Programmable current limit, fast shut down, and fault timer protect the load and supply during fault conditions such as a hot - short. The fast shutdown threshold and response time can be tuned to ensure a fast response to real faults, while avoiding nuisance trips. Programmable Safe Operating Area (SOA) protection and the inrush timer keep the MOSFET safe under all conditions. After asserting power good, TPS2477x acts as a circuit breaker and runs the fault timer during over current events, but doesn't current limit. It shuts down after the fault timer expires. Two independent timers (inrush/fault) allow the user to customize protection based on system requirements.

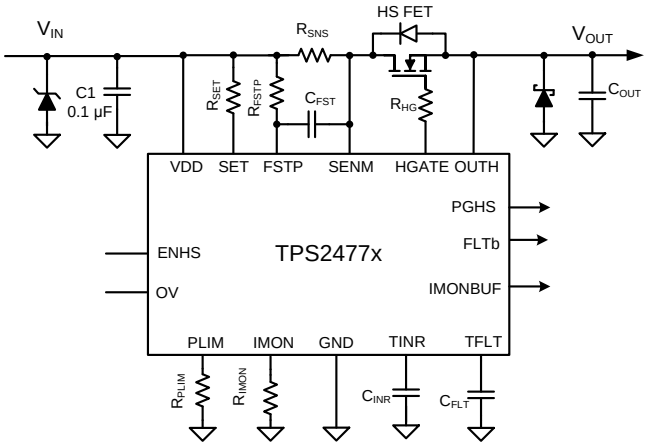
Finally, the flexibility of the TPS2477x aid Hot Swap design for the 240 VA requirement and a design example is shown in the datasheet.

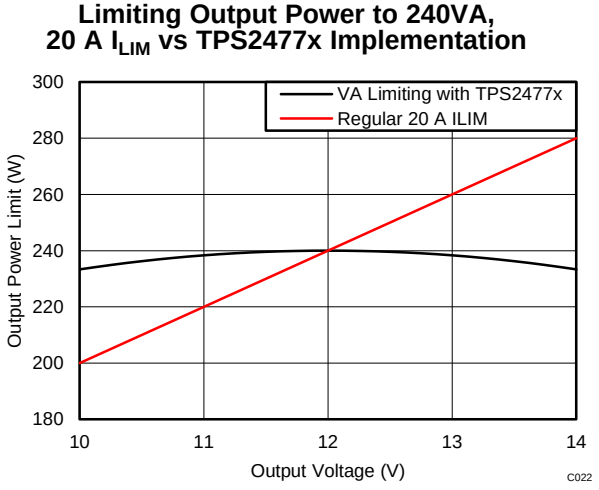
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS24770 TPS24771 TPS24772	RGE (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





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5 Revision History

DATE	REVISION	NOTES
March 2015	*	Initial release.

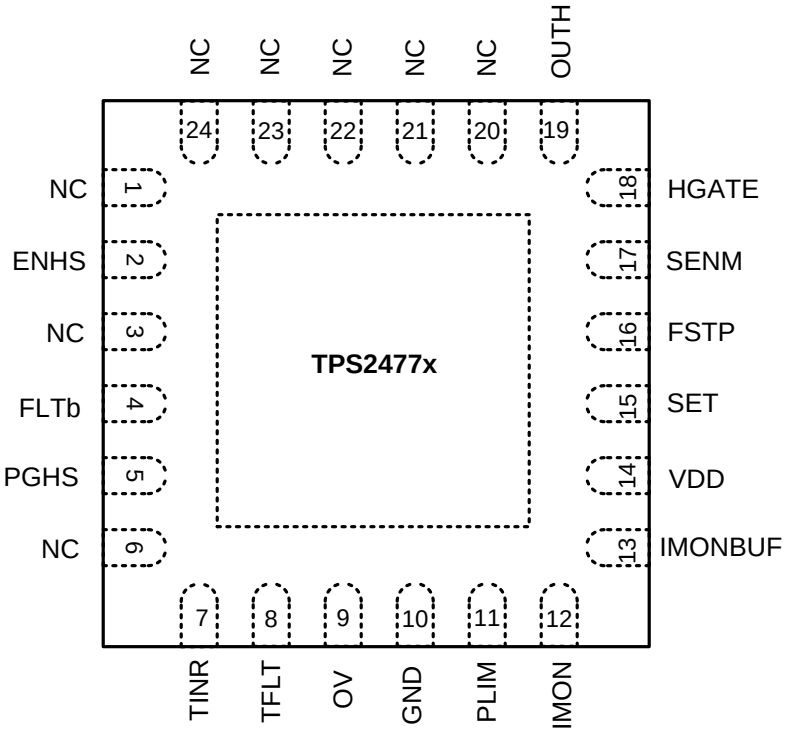
6 Device Comparison Table

PART NUMBER(1)	LATCH / RETRY OPTION
TPS24770	Latch
TPS24771	Auto – Retry
TPS24772	Fast Latch Off

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

7 Pin Configuration and Functions

QFN 24-Pin with Thermal Pad
RGE Package
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ENHS	2	I	Active-high enable input of Hot Swap. Logic input. Connects to resistor divider.
FLTb	4	O	Active-low, open-drain output indicating various faults.
FSTP	16	I	Fast trip programming set pin for Hot Swap. A resistor is connected from positive terminal of R_{SNS} to FSTP.
GND	10	–	Ground.
HGATE	18	O	Gate driver output for external Hot Swap MOSFET.
IMON	12	I/O	Analog monitor and current limit program point. Connect R_{IMON} to ground.
IMONBUF	13	O	Voltage output proportional to the load current (0V–3.0V).
NC	1,3, 6, 20–24	NC	No connect. Tie to ground or leave floating.

(1) I = Input; O = Output ; P = Power, NC = No Connect

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUTH	19	I	Output voltage sensor for monitoring Hot Swap MOSFET's power. Connects to the source terminal of the Hot Swap N channel MOSFET.
OV	9	I	Overvoltage comparator input. Connects to resistor divider. HGATE is pulled low when OV exceeds the threshold. Connect to ground when not used.
PGHS	5	O	Active-high, open-drain power-good indicator.
PLIM	11	I	Power limit programming pin. A resistor from this pin to GND sets the maximum power dissipation for the Hot Swap FET. Connect a 4.99 kΩ resistor to disable power limit.
SENM	17	I	Current-sensing input for the sense resistor. Directly connects to the negative terminal of the sense resistor.
SET	15	I	Current-limit programming set pin for Hot Swap. A resistor is connected from positive terminal of the sensing resistor.
TFLT	8	I/O	Fault timer, which runs when the device is in regular operation and there is an overcurrent condition.
TINR	7	I/O	Inrush timer, which runs during the inrush operation (start-up) if the part is in current limit or power limit.
VDD	14	P	Power Supply

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VDD,SET, FSTP,SENM, OUTH, ENHS, FLTb, PGHS, OV	–0.3	30	V
	HGATE to OUTH	–0.3	15	V
	SET to VDD	–0.3	0.3	V
	SENM, FSTP to VDD	–0.6	0.3	V
	TINR, TFLT, PLIM, IMON	–0.3	3.6	V
	IMONBUF	–0.3	7	V
Sink Current	FLTb, PGHS		5	mA
Source Current	IMON, IMONBUF		5	mA
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$(1) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage	VDD, SENM, SET, FSTP	2.5	18	V
	ENHS, FLTb, PGHS, OUTH	0	18	
Sink current	FLTb, PGHS	0	2	mA
Source current	IMON	0	1	mA
External resistance	PLIM	4.99	500	kΩ
	IMON	1	6	kΩ
	FSTP	10	4000	Ω
	SET	10	400	Ω
R_{IMON} / R_{SET}	w/o R_{STBL}	10	70	
	With appropriate R_{STBL} (1)	3	10	
	with C_{HGATE} > 47nF (2)	10	200	
External capacitor	TINR, TFLT	1		nF
	HGATE, (2)	0	1	µF
	IMON		30	pF
	IMONBUF		100	pF
Operating junction temperature, T_J		–40	125	°C

(1) Refer to R_{STBL} Requirment for R_{IMON} / R_{SET} < 10 as described in section Select R_{SNS} and $V_{SNS,CL}$ Setting.
(2) External capacitance tied to HGATE, should be in series with a resistor no less than 1kΩ.

8.4 Thermal Information

THERMAL METRIC (1)		RGE	UNIT
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	38.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	12.9	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	12.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

Unless otherwise noted these limits apply to the following: -40°C < T_J<125°C; 2.5V < V_{VDD}, V_{OUT} < 18V; V_{ENHS} = 2 V; V_{OV} = 0 V; V_{HGATE}, V_{PGHS}, V_{FLTB}, and $V_{IMONBUF}$ are floating; C_{INR} = 1nF; C_{FLT} = 1nF; R_{SET} = 44.2 Ω; R_{IMON} = 2.98k Ω; R_{FSTP} = 200 Ω; R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{UVR}	UVLO threshold, rising		2.2	2.32	2.45	V
V_{UVhyst}	UVLO hysteresis			0.10		V
I_{QON}	Supply current: I_{VDD} + I_{OUTH}	Device on, V_{ENHS} = 2V		2.95	4	mA
Hot Swap FET ENABLE (ENHS)						
V_{ENHS}	Threshold voltage, rising		1.3	1.35	1.4	V
$V_{ENHShyst}$	Hysteresis			50		mV
I_{ENHS}	Input Leakage Current	0 ≤ V_{ENHS} ≤ 30V	–1		1	µA
OVER VOLTAGE (OV)						
V_{OVR}	Threshold voltage, rising		1.3	1.35	1.4	mV
V_{OVhyst}	Hysteresis			50		mV
I_{OV}	Input leakage current	0 ≤ V_{OV} ≤ 30V	–1		1	µA

Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following: -40°C < T_J<125°C; 2.5V < V_{VDD}, V_{OUT} < 18V; V_{ENHS} = 2 V; V_{OV} = 0 V; V_{HGATE}, V_{PGHS}, V_{FLTB}, and $V_{IMONBUF}$ are floating; C_{INR} = 1nF; C_{FLT} = 1nF; R_{SET} = 44.2 Ω; R_{IMON} = 2.98k Ω; R_{FSTP} = 200 Ω; R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
POWER LIMIT PROGRAMING (PLIM)						
$V_{PLIM,BIAS}$	Bias voltage	Sourcing 10µA	0.65	0.675	0.7	V
$V_{IMON,PL}$	Regulated IMON voltage during power limit	R_{PLIM} = 52 kΩ; $V_{SENM-OUTH}$=12V	114.75	135	155.25	mV
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=12V	56.95	67	77.05	
		R_{PLIM} = 261 kΩ; $V_{SENM-OUTH}$=12V	18.9	27	35.1	
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=2V	341.7	402	462.3	
		R_{PLIM} = 105 kΩ; $V_{SENM-OUTH}$=18V	38.25	45	51.75	
SLOW TRIP THRESHOLD (SET)						
V_{OS_SET}	Input referred offset (V_{SNS} to V_{IMON} scaling)	R_{SET} = 44.2Ω; R_{IMON}=3kΩ to 1.2kΩ ($V_{SNS,CL}$=10mV to 25mV)	–150		150	µV
V_{GE_SET}	Gain error (V_{SNS} to V_{IMON} scaling)(1)		–0.4%		0.4%	
FAST TRIP THRESHOLD PROGRAMMING (FSTP)						
I_{FSTP}	FSTP input bias current	V_{FSTP}=12V	95	100	105	µA
$V_{FASTRIP}$	Fast trip threshold	R_{FSTP} = 200 Ω, V_{SNS} when V_{HGATE} ↓	18	20	22	mV
		R_{FSTP} = 1 kΩ, V_{SNS} when V_{HGATE} ↓	95	100	105	
		R_{FSTP} = 4 kΩ, V_{SNS} when V_{HGATE} ↓	380	400	420	
CURRENT SUMMING NODE (IMON)						
$V_{IMON,CL}$	Slow trip threshold at summing node	V_{IMON}↑, when I_{TFLT} starts sourcing	660	675	690	mV
$I_{IMON-LKG}$	IMON leakage current	V_{ENHS} =0V, V_{IMON} = 1.5V	–200		200	nA
CURRENT MONITOR (IMONBUF)						
$V_{OS\_IMONBUF}$	Buffer offset	V_{IMON} = 50mV to 675mV, Input referred	–3	0	3	mV
$GAIN_{IMONBUF}$	Buffer voltage gain	$\Delta V_{IMONBUF}$ / ΔV_{IMON}	2.97	2.99	3.01	V
$BW_{IMONBUF}$	Buffer closed loop bandwidth	$C_{IMONBUF}$ = 75pF		1		MHz
Hot Swap GATE DRIVER (HGATE)						
V_{HGATE}	HGATE output voltage	5 ≤ V_{VDD} ≤ 16V; measure $V_{HGATE-OUTH}$	12	13.6	15.5	V
		2.5V <V_{VDD} < 5V; 16V <V_{VDD} < 20V measure $V_{HGATE-OUTH}$	7	7.95	15	V
$V_{HGATEmax}$	Clamp voltage	Inject 10µA into HGATE, measure $V_{(HGATE\ -\ OUTH)}$	12	13.9	15.5	V
$I_{HGATEsrc}$	Sourcing current	$V_{HGAT-OUTH}$ = 2V-10V	44	55	66	µA
$I_{HGATEfastSink}$	Sinking current for fast trip	$V_{HGATE-OUTH}$ = 2V–15V; $V_{(FSTP\ -\ SENM)}$ = 20mV	0.45	1	1.6	A
$I_{HGATEsustSink}$	Sustained sinking current	Sustained, $V_{HGATE-OUTH}$ = 2V – 15V; V_{ENHS} = 0	30	44	60	mA
INRUSH TIMER (TINR)						
$I_{TINRsrc}$	Sourcing current	V_{TINR} = 0V, In power limit or current limit	8	10.25	12.5	µA
$I_{TINRsink}$	Sinking current	V_{TINR} = 2V, In regular operation	1.5	2	2.5	µA
V_{TINRup}	Upper threshold voltage	Raise V_{TINR} until HGATE starts sinking	1.3	1.35	1.4	V
V_{TINRlr}	Lower threshold voltage	Raise V_{TINR} to 2V. Reduce V_{TINR} until I_{TINR} is sourcing.	0.33	0.35	0.37	v
R_{TINR}	Bleed down resistance	V_{VDD} = 0V, V_{TINR} = 2V	70	104	130	kΩ
$I_{TINR-PD}$	Pulldown current	V_{TINR} = 2V, when V_{ENHS} = 0V	2	4.2	7	mA
$RETRY_{CYCLE}$	Cycle number	# of timer cycles before retry (TPS24771 only)	64	64	64	
$RETRY_{DUTY}$	Retry duty cycle	TFLT and TINR connected (TPS24771 only)		0.70%		
		TFLT and TINR not connected (TPS24771 only)		0.35%		
$V_{IMON,TINR}$	See Using Soft Start - I_{HGATE} and TINR Considerations	R_{PLIM} = 52kΩ, V_{SENM} = 12V, V_{OUTH} = 0 V. Raise IMON voltage and record IMON when TINR starts sourcing current.	47.75	90	132.25	mV
$V_{IMON,PL}$	See Using Soft Start - I_{HGATE} and TINR Considerations	R_{PLIM} = 52kΩ, $V_{SENM-OUTH}$ = 12V, Raise IMON voltage and record IMON when I_{HGATE} starts sinking current.	114.75	135	155.25	mV
$\Delta V_{IMON,TINR}$	See Using Soft Start - I_{HGATE} and TINR Considerations	$\Delta V_{IMON,TINR}$ = $V_{IMON,PL}$ - $V_{IMON,TINR}$	23	45	67	mV

(1) Specified by characterization.

Electrical Characteristics (continued)

Unless otherwise noted these limits apply to the following: -40°C < T_J<125°C; 2.5V < V_{VDD}, V_{OUT} < 18V; V_{ENHS} = 2 V; V_{OV} = 0 V; V_{HGATE}, V_{PGHS}, V_{FLTB}, and $V_{IMONBUF}$ are floating; C_{INR} = 1nF; C_{FLT} = 1nF; R_{SET} = 44.2 Ω; R_{IMON} = 2.98k Ω; R_{FSTP} = 200 Ω; R_{PLIM} = 52 kΩ.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
FAULT TIMER (TFLT)						
$I_{TFLTsrc}$	Sourcing current	V_{TFLT} = 0V, PGHS is high and in overcurrent	8	10.25	12.5	µA
$I_{TFLTsink}$	Sinking current	V_{TFLT} = 2V, Not in overcurrent	1.5	2	2.5	µA
V_{TFLTup}	Upper threshold voltage	Raise V_{TFLT} until HGATE starts sinking	1.3	1.35	1.4	V
R_{TFLT}	Bleed down resistance	V_{ENHS} = 0V, V_{TFLT} = 2V	70	104	130	kΩ
$I_{TFLT-PD}$	Pulldown current	V_{TFLT} = 2V, when V_{ENHS} = 0V	2	5.6	7	mA
HOT SWAP OUTPUT (OUTH)						
$I_{OUTH, BIAS}$	Input bias current	V_{OUTH} = 12V		30	70	µA
FAULT INDICATOR (FLTb)						
V_{OL_FLTb}	Output low voltage	Sinking 2 mA		0.11	0.25	V
I_{FLTb}	Input leakage current	V_{FLTb} = 0V, 30V	–1	0	1	µA
V_{HSFLT_IMON}	V_{IMON} threshold to detect Hot Swap FET short	V_{ENHS} = 0V, Measured V_{IMON} ↑ to GND when FLTb ↓	88	101	115	mV
V_{HSFL_hyst}	Hysteresis			25		mV
HOT SWAP POWER GOOD OUTPUT (PGHS)						
V_{PGHSth}	PGHS Threshold	Measure $V_{SENM-OUTH}$ ↓ when PGHS↑	170	270	375	mV
$V_{PGHShyst}$	PGHS hysteresis	$V_{SENM-OUTH}$ ↑		80		mV
V_{OL_PGHS}	PGHS Output low voltage	Sinking 2mA		0.11	0.25	V
I_{PGHS}	PHGS Input leakage current	V_{PGHS}=0V to 30V	–1	0	1	µA
THERMAL SHUTDOWN (OTSD)						
T_{OTSD}	Thermal shutdown threshold	Temperature rising		140		°C
$T_{OTSD,HYST}$	Hysteresis			10		°C

8.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
$DEGL_{UVLO}$	UVLO deglitch	Both rising and falling		14		µs
HOT SWAP FET ENABLE (ENHS)						
$DEGL_{ENHS}$	Deglitch time	Both rising and falling	2.2	3.8	5.5	µs
OVER VOLTAGE (OV)						
$DEGL_{OV}$	Deglitch time	Both rising and falling	2.2	3.9	5.7	µs
FAST TRIP (FSTP)						
$t_{FastOffDly}$	Fast turn-off delay	$V_{(FSTP\ –\ SENM)}$: –5mV to 5mV, C_{HGATE} = 0 pF		600		ns
		$V_{(FSTP\ –\ SENM)}$: -20mV to 20mV C_{HGATE} = 0 pF		300		
$t_{FastOffDur}$	Strong pull down current duration		53	63	73	µs
INRUSH TIMER (TINR)						
N_{RETRY}	Number of TINR cycles before retry	TPS24741 only		64		
$RETRY_{DUTY}$	Retry duty cycle	T_{INR} not connected to T_{FLT}		0.35%		
		T_{INR} connected to T_{FLT}		0.7%		
FAULT INDICATOR (FLTb)						
t_{FLT_degl}	Fault deglitch	Both rising and falling	2.2	3.9	5.3	ms
HOT SWAP POWER GOOD OUTPUT (PGHS)						
$t_{PGHSdegl}$	PGHS deglitch time	Rising	0.7	1	1.3	ms
		Falling	7	8	9	

8.7 Typical Characteristics

Unless otherwise noted these cureves apply to the following: -40°C < T_J<125°C; 2.5V < V_{VDD}, V_{OUT} < 18V; V_{ENHS} = 2 V; V_{OV} = 0 v; V_{HGATE}, V_{PGHS}, V_{FLTB}, and $V_{IMONBUF}$ are floating; C_{INR} = 1nF; C_{FLT} = 1nF; R_{SET} = 44.2 Ω; R_{IMON} = 2.98k Ω; R_{FSTP} = 200 Ω; R_{PLIM} = 52 kΩ.

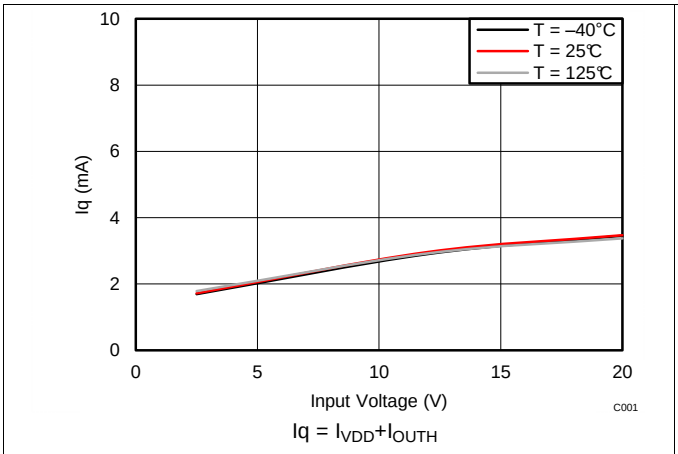


Figure 1.

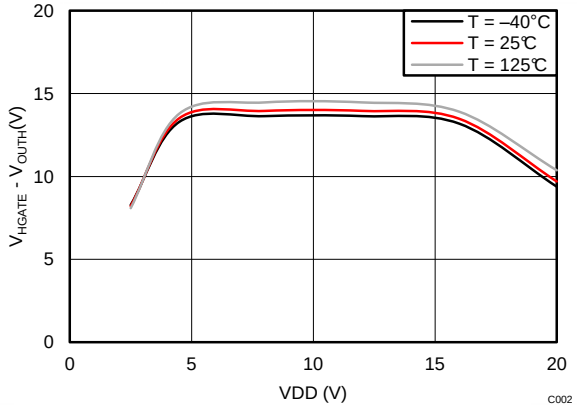


Figure 2.

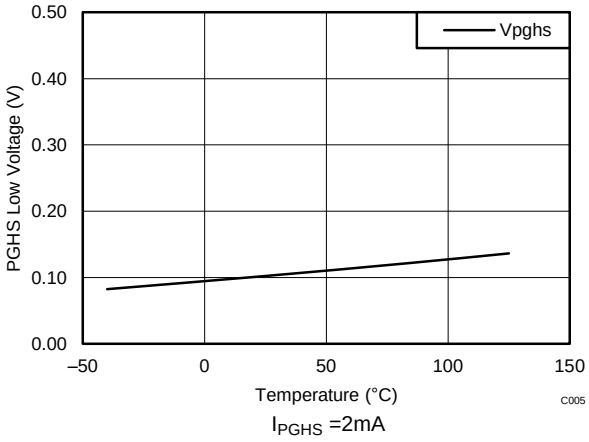


Figure 3.

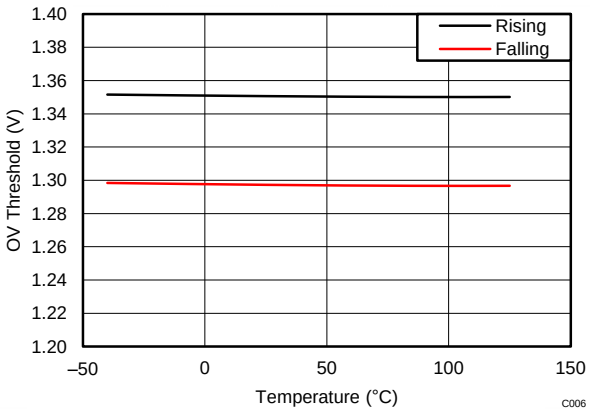


Figure 4.

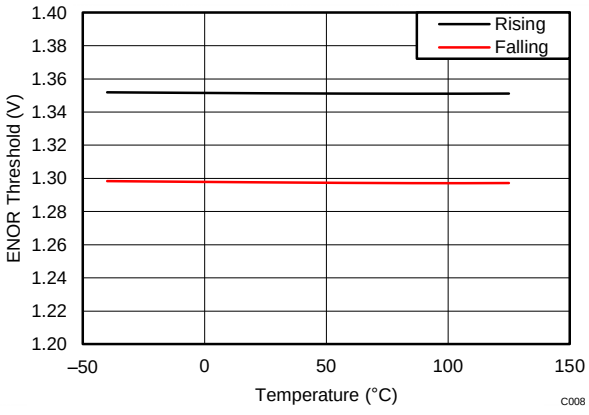


Figure 5.

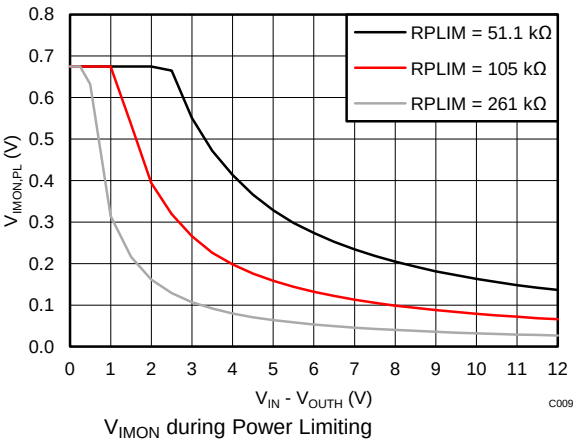
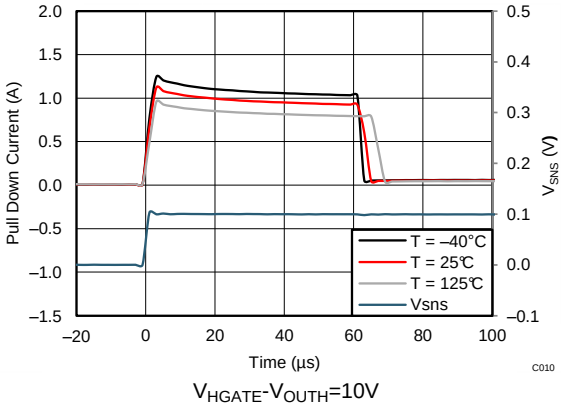


Figure 6.

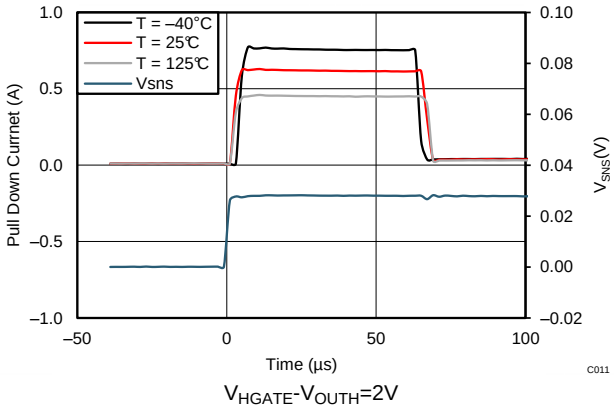
Typical Characteristics (continued)

Unless otherwise noted these cureves apply to the following: -40°C < T_J<125°C; 2.5V < V_{VDD}, V_{OUT} < 18V; V_{ENHS} = 2 V; V_{OV} = 0 v; V_{HGATE}, V_{PGHS}, V_{FLTB}, and $V_{IMONBUF}$ are floating; C_{INR} = 1nF; C_{FLT} = 1nF; R_{SET} = 44.2 Ω; R_{IMON} = 2.98k Ω; R_{FSTP} = 200 Ω; R_{PLIM} = 52 kΩ.



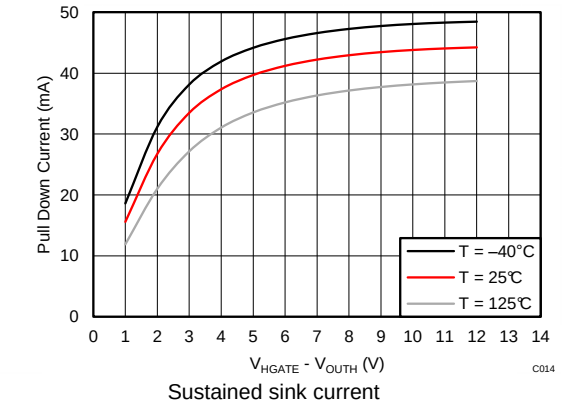
V_{HGATE}-V_{OUTH}=10V

Figure 7.



V_{HGATE}-V_{OUTH}=2V

Figure 8.



Sustained sink current

Figure 9.

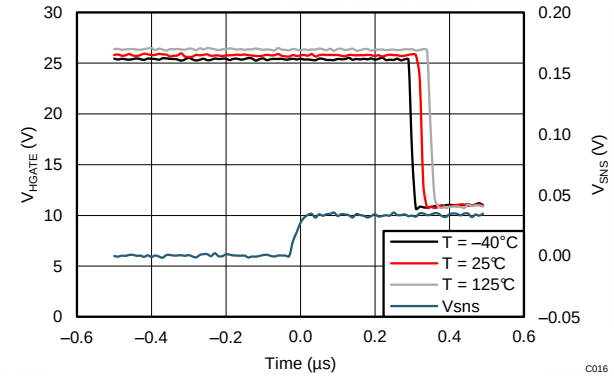
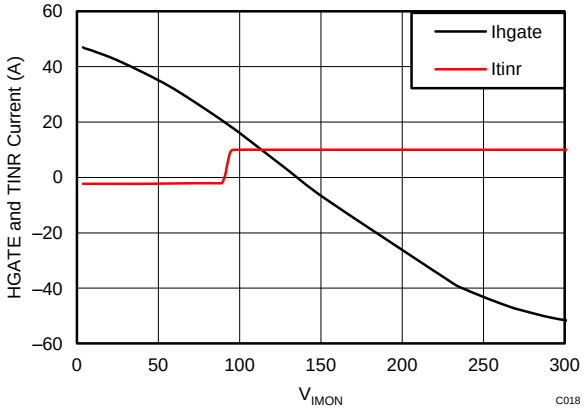


Figure 10.



$V_{HGATE-OUTH}$=4V
R_{PLIM} =52kΩ
T_J =25°C

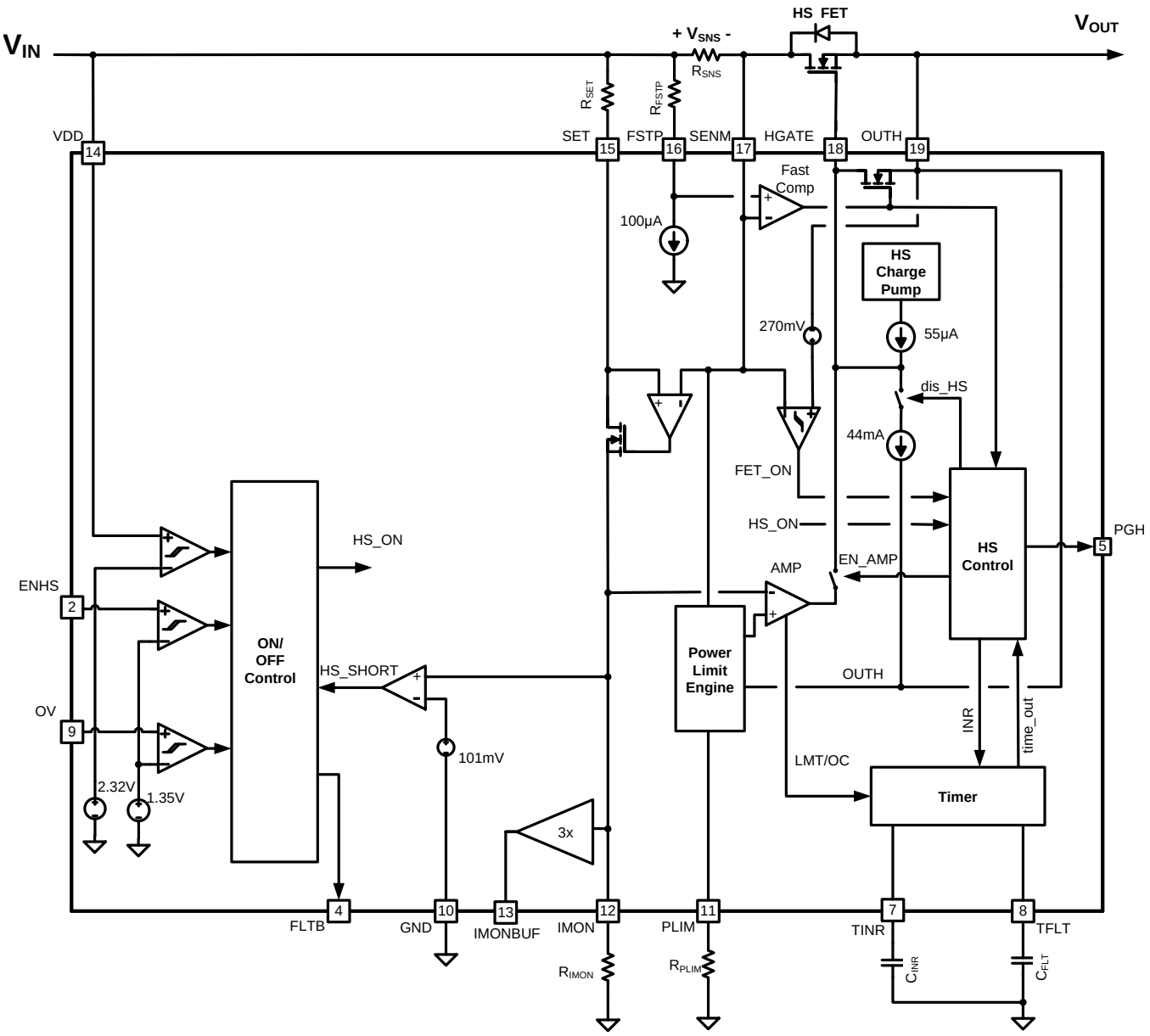
Figure 11.

9 Detailed Description

9.1 Overview

The TPS2477x Hot Swap features a programmable current limit, power limit, and fast trip threshold. It also has dual timers: one for inrush and one during over current faults. Finally it features an analog current monitor that can be used to provide current information to a microcontroller.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Enable and Over-voltage Protection

The part is enabled when the ENHS pin voltage exceeds 1.35V and is disabled when the pin voltage falls under 1.3V providing 50mV of hysteresis. A resistor divider can be connected to these pins to turn on the TPS2477x at a certain bus voltage. The part will turn off if the OV pin exceeds 1.35V.

9.3.2 Current Limit and Power Limit during Start-up

The current limit and power limit of the TPS2477x are programmable to protect the load, power supply, and the Hot Swap MOSFET. During start-up the active control loop will regulate the gate to ensure that the current through the MOSFET and the power dissipation of the MOSFET is below their respective pre-programmed thresholds. The maximum current allowed through the MOSFET (I_{LIM}) is determined with the equation below. $I_{LIM,CL}$ is the programmed current limit, P_{LIM} is the programmed power limit, and V_{DS} is the drain to source voltage across the Hot Swap MOSFET.

$$I_{LIM} = MIN\left(I_{LIM,CL}, \frac{P_{LIM}}{V_{DS}}\right) \quad (1)$$

This results in an IV curve shown in Figure 12. $I_{LIM,PL}$ denotes the maximum allowed MOSFET current (I_{DS}) when the part is in power limit. As V_{DS} increases, $I_{LIM,PL}$ decreases and $I_{LIM,PL,MIN}$ denotes the lowest $I_{LIM,PL}$, which occurs at the largest V_{DS} ($V_{DS,MAX}$). The TPS2477x enforce this by regulating the voltage across R_{SNS} (V_{SNS}). $V_{SNS,PL}$ denotes V_{SNS} when power limiting is active. Similarly to $I_{LIM,PL}$, $V_{SNS,PL}$ decreases as V_{DS} increases and $V_{SNS,PL,MIN}$ corresponds to the lowest $V_{SNS,PL}$, which occurs at $V_{DS,MAX}$. $V_{SNS,CL}$ is a current limiting sense voltage, which is programmable in the TPS2477x.

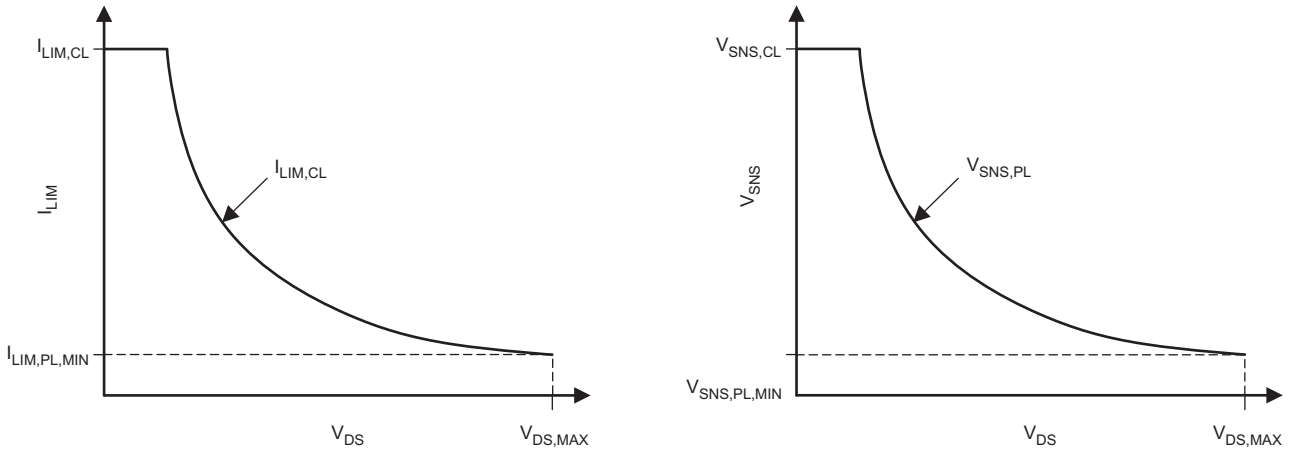


Figure 12. Current vs V_{DS} and V_{SNS} vs V_{DS} Programmed by Power Limit Engine.

The current and power limit can be programmed using the equations below.

$$V_{SNS,CL} = \frac{0.675 \times R_{SET}}{R_{IMON}} \quad (2)$$

$$I_{LIM,CL} = \frac{V_{SNS,CL}}{R_{SNS}} = \frac{0.675 \times R_{SET}}{R_{SNS}} \quad (3)$$

$$P_{LIM} = \frac{84375 \times R_{SET}}{R_{PLIM} \times R_{SNS} \times R_{IMON}} \quad (4)$$

Feature Description (continued)

Note, that the error is largest at $V_{SNS,PL,MIN}$ due to offset of the internal amplifier. Also the operation at $V_{DS,MAX}$ is most critical because it corresponds to the short circuit condition and has the biggest impact on start time. Thus it is critical to consider $V_{SNS,PL,MIN}$ during design. Equation 5 shows the relationship of $V_{SNS,PL,MIN}$ as a function of P_{LIM}, $I_{LIM,CL}$, $V_{SNS,CL}$, and $V_{DS,MAX}$. Note that $I_{LIM,CL}$ and $V_{DS,MAX}$ are usually determined by the system requirements. The designer will have control over P_{LIM} and $V_{SNS,CL}$. In general, there will be a desire to reduce the power limit to allow for smaller MOSFETs and to reduce the $V_{SNS,CL}$ to improve efficiency (lower R_{SNS}). However, this will also reduce $V_{SNS,PL,MIN}$ and the designer should ensure that it's above the minimum recommended value of 1.5mV.

$$V_{SNS,PL,MIN} = \frac{P_{LIM} \times V_{SNS,CL}}{V_{DS,MAX} \times I_{LIM,CL}} \quad (5)$$

9.3.3 Two Level Protection During Regular Operation

After the TPS2477x has gone through start-up it will no longer actively control the gate. Instead it will run the timer when the current is between the current limit and the fast trip threshold. Once the timer has expired the gate will be pulled down. If the current ever exceeds the fast trip threshold, the gate will be pulled down immediately.

9.3.4 Dual Timer (TFLT and TINR)

TPS2477x has two timer pins to allow the user to customize the protection. The TINR pin will source 10.25 µA when the device is in start-up mode and is actively regulating the gate to limit the MOSFET power or current. It will sink 2 µA otherwise. The TFLT pin will source 10.25 µA when the device is in regular operation and the FET current exceeds the current limit. It will sink 2 µA otherwise. If either of the timer pins exceeds 1.35, the TPS2477x will time out. The TPS24770 and TPS24772 will latch off. The TPS24771 will go through 64 cycles of TINR and attempt to start-up again.

Since the TINR usually runs when the MOSFET is being stressed, TINR should be sized to maintain the FET within its SOA. In general TFLT runs when the load is drawing more current than expected, which can stress the load and the power supply. Thus TFLT should be programmed to have the right protection settings for the power supply and the load. In some systems the load is allowed to draw current above the current limit for 250ms or 1s. In that case a large TFLT is required, but a short TINR may still be desired to minimize the worst case FET stress. In other applications a long TINR may be required to due to large downstream capacitances, but drawing excessive current from the power supply for more than 5ms is not desired. In that case a short TFLT and a long TINR should be used. Finally, many applications can use the same TINR and TFLT setting, in which case the pins can be tied together and a single capacitor can be used. The two different options are shown in Figure 13.

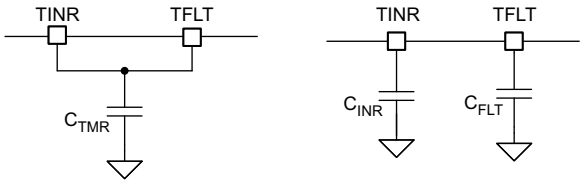


Figure 13. Timer Configurations

If two separate timer capacitors are used their values can be computed with the equations below:

$$C_{INR} = 7.59\ \mu F / s \times T_{INR} \quad (6)$$

$$C_{FLT} = 7.59\ \mu F / s \times T_{FLT} \quad (7)$$

If a single capacitor is used C_{TMR} can be computed with Equation 8.

Feature Description (continued)

$$C_{TMR} = 6.11\ \mu F / s \times T_{TMR} \quad (8)$$

9.3.5 3 Options for Response to a Fast Trip

The TPS24770, TPS24771, and TPS24772 have difference responses to a fast trip event to accommodate different design requirements. When the current exceeds the fast trip threshold, the gate is quickly pulled down to minimize damage that can be caused due to a short circuit. Figure 14 shows the response of the variout devices options to a hot short on the output. The TPS24770 (latch) will attempt to re-start once after the hot-short is observed and then stay off, the TPS24771 will continuously retry with a duty cycle of ~0.5% (0.7% if T_{FLT} and T_{INR} are connected, 0.35% if T_{FLT} and T_{INR} are not connected), and the TPS24772 (fast latch off) will shut off and never retry again. In general the TPS24772 will place the least amount of stress on the MOSFET, but is the least likely to recover from a nuissance trip.

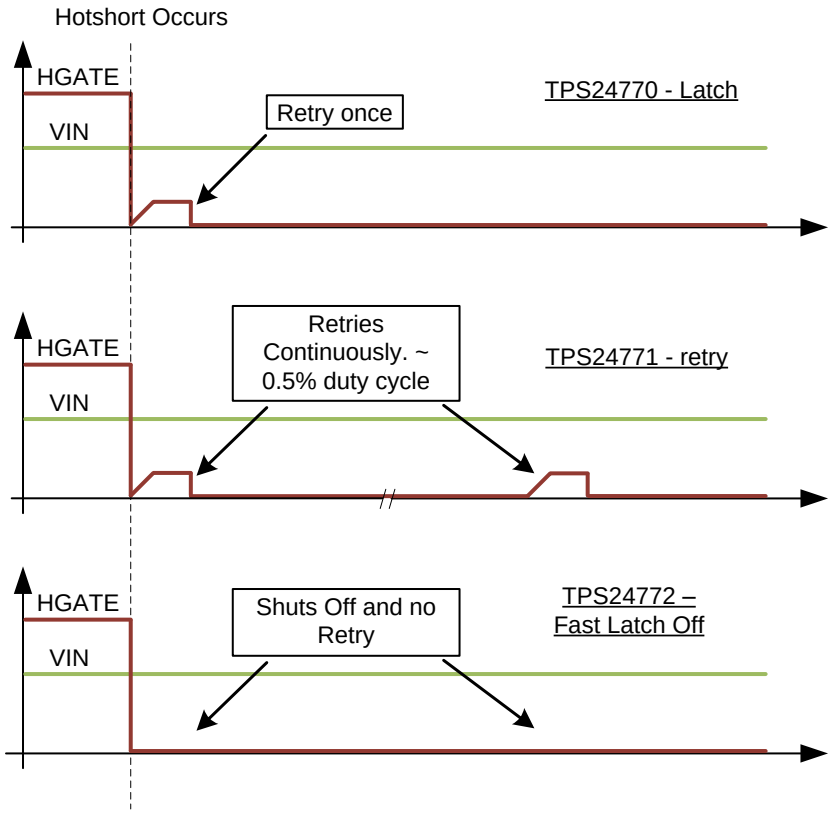


Figure 14. TPS24770/1/2 Response to a Short Circuit

9.3.6 Using Soft Start - I_{HGATE} and TINR Considerations

During start-up the TPS2477x regulates the HGATE to keep the FET power dissipation within P_{LIM}. This is accomplished by an amplifier that monitors the IMON voltage and an internal reference voltage. The TPS2477x will source current into HGATE if VIMON is lower than the reference voltage and will sink current into HGATE if VIMON is above the reference voltage. In steady state, the V_{IMON} will be regulated to the $V_{IMON,PL}$ point, where I_{HGATE} equals zero. Note that $V_{IMON,PL}$ is a determined by R_{PLIM} and $V_{SENM} – V_{OUTH}$.

The same amplifier feeds into the inrush timer circuitry to run the timer when the part is in power limit. The V_{IMON} threshold at which the timer starts to source current is denoted as V_{IMON}, T_{INR}. Note that $V_{IMON,TINR}$ is lower than $V_{IMON,PL}$ to account for tolerances and ensure that the timer is always active when the device is in power limit. The difference between the two thresholds is defined as $\Delta V_{IMON,\ TINR}$. Refer to Figure 11 for a typical I_{HGATE} and I_{TINR} vs V_{IMON} curve.

Feature Description (continued)

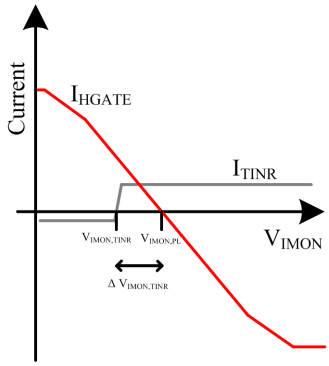


Figure 15. I_{TINR} and I_{HGATE} vs V_{IMON} (V_{DS} = 12V, R_{PLIM} = 52kΩ)

It is critical to consider $\Delta V_{IMON,\ TINR}$ and Figure 15 if a soft start circuit is used. Typically, the soft start is implemented by limiting the gate dv/dt with a capacitor, which in turn limits the inrush current to the output capacitor. Often times, the inrush current is kept below $I_{LIM,PL}$ to keep the timer from running. Note that the $I_{LIM,PL}$ is based on the $V_{IMON,PL}$ threshold and thus T_{INR} can be activated even if the inrush current is below $I_{LIM,PL}$. To prevent the timer from running unintentionally, the P_{LIM} should be chosen above $P_{LIM,MIN,SS}$, which can be computed as shown below. As an example consider the usage case where the maximum inrush current ($I_{INR,MAX}$) is 2A, the maximum input voltage ($V_{IN,MAX}$) is 13V and R_{SET}, R_{IMON}, and R_{SNS} are 100Ω, 2.7kΩ, and 1mΩ respectively. For that case the power limit should be set to at least 58.3 W + P_{LIM} tolerance to ensure that the inrush timer doesn't run.

$$P_{LIM,MIN,SS} = \left(I_{INR,MAX} + \Delta V_{IMON,TINR,MAX} \times \frac{R_{SET}}{R_{IMON} \times R_{SNS}} \right) \times V_{IN,MAX}$$
$$= \left(2A + 67mV \times \frac{100\Omega}{2.7k\Omega \times 1m\Omega} \right) \times 13V = 58.3W \quad (9)$$

9.3.7 Analog Current Monitor

The TPS2477x also features two analog current monitoring outputs: IMON and IMONBUF. Each has their own advantages and disadvantages. The IMON is more accurate, because it doesn't have the error added from the second stage. However it is a high impedance output and leakage current on that node would result in monitoring error. In addition it can only support 30pF of capacitance and its full scale range is 675mV (this is where current limit kicks in). The IMONBUF takes the IMON signal and buffers it 3x. This introduces more error, but the output is low impedance, has a larger full scale range, and can drive up to 100pF of capacitance.

Feature Description (continued)

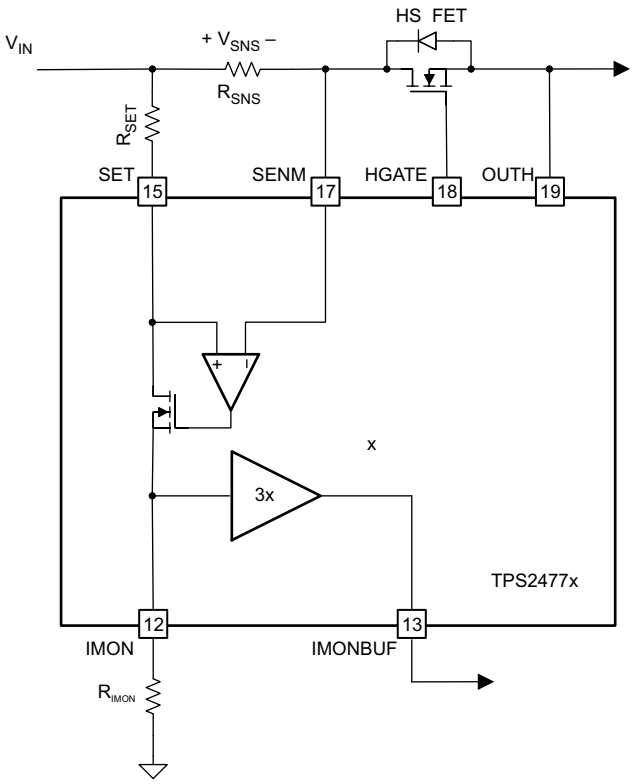


Figure 16. Current Monitoring Circuitry

9.3.8 Power Good Flag

The TPS2477x has a power good flag, which should be used to turn on downstream DC/DC converters. This reduces the stress on the Hot Swap MOSFET during start-up. The PGHS pin of the TPS2477x is asserted (with 1 ms deglitch) when both:

- Hot Swap is enabled and
- V_{DS} of Hot Swap MOSFET is below 240 mV.

PGHS is de-asserted (with 8 ms deglitch) when either:

- Hot Swap is disabled.
- VDS of Hot Swap MOSFET is above 310 mV
- In an overcurrent condition that causes the timer to time out and latch off.

9.3.9 Fault Reporting

TPS2477x will assert a fault by pulling down on the FLTb pin if any of the following occur:

- Hot Swap MOSFET Shorted Fault (ENHS = LO, but VIMON > 101 mV)
- Hot Swap timer times out.
- Over Temperature Shut Down (OTSD)

9.4 Device Functional Modes

9.4.1 Hot Swap Functional Modes

The state machine for the Hot Swap section is shown in Figure 17. After a POR / UVLO event the Hot Swap enters the Inrush up. Once operational the Hot Swap has the following functional modes:

- **Inrush Mode (INR):** In this state the Hot Swap controller is actively regulating the HGATE to meet the current limit and power limit settings. The inrush timer is running if the controller is in power or current limiting. If the inrush timer times out the gate will be pulled down. The TPS24770 and TPS24772 will go to latched mode and TPS24771 will go into retry mode.
- **Regular Operation Mode (REG):** In this mode everything is operating properly so both the timers are discharged and the HGATE is high. If there is an overcurrent condition (V_{SNS} > $V_{SNS,CL}$), the device will go into fault mode. If there is a fast trip condition (V_{SNS} > V_{FSTP}), the gate will be pulled down with a 1A / 63 µs pulse. The TPS24772 will go to the latched state and the TPS24770 and TPS24771 will go back to inrush for a retry.
- **Fault Mode (FLT):** In this mode the TPS2477x runs the fault timer. Once the timer expires the TPS24770 and TPS24772 will go to latch mode while TPS24771 will go to retry mode. If the overcurrent condition is removed the controller will go back to the regular operation mode.
- **Latched Mode (Latched):** In the latched mode the HGATE is low, the timer is being discharged, and the FLTb is asserted. If there is a rising edge on ENHS the part will discharge the timers and go to the inrush mode.
- **Retry Mode (Retry):** Here the part will charge and discharge the inrush timer 64 times before attempting another retry.

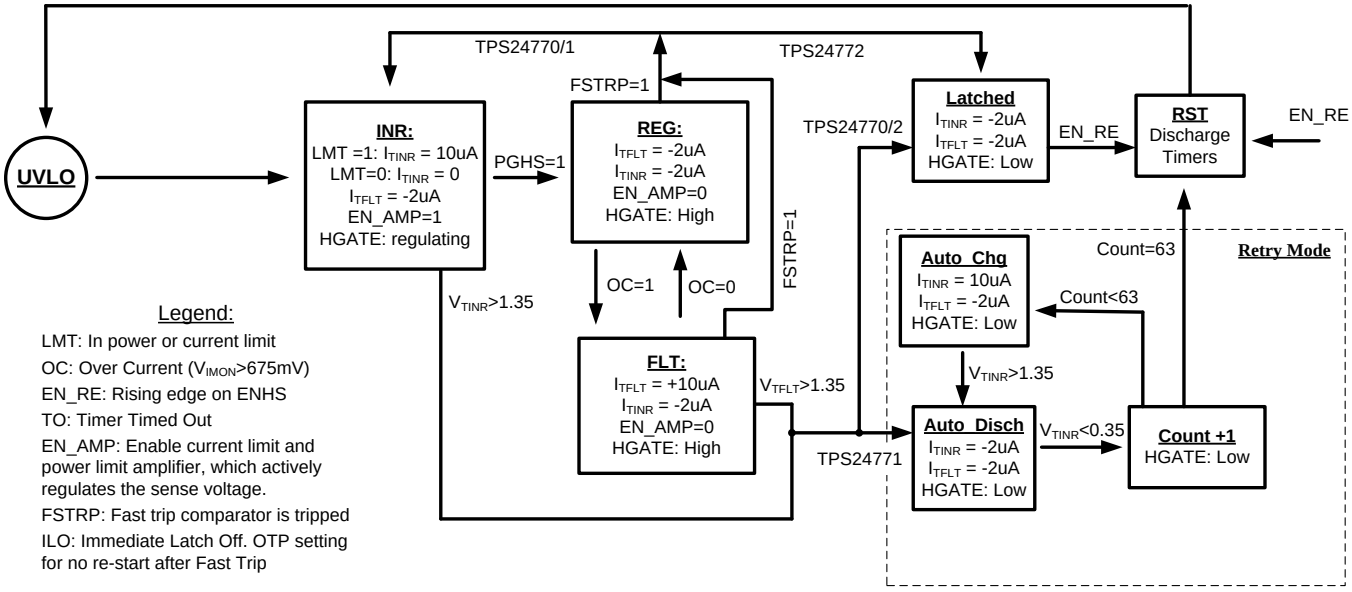


Figure 17. Hot Swap State Machine

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2477x is a highly configurable Hot Swap controller that can be fine-tuned for the application requirement. When designing a Hot Swap 3 key scenarios should be considered:

- Start-up.
- Output of a Hot Swap is shorted to ground when the Hot Swap is on. This is often referred to as a "Hot-Short".
- Powering up a board when the output and ground are shorted. This is usually called a "start into short".

All of these scenarios place a lot of stress on the Hot Swap MOSFET and special care must be taken when designing the Hot Swap circuit to keep the MOSFET within its Safe Operating Area (SOA). Note that the component selection can often be iteratively and it's recommended to use the publically available excel calculators to crunch the numbers. See the TPS24770 Design Calculator in the Tools & Software link on the Product folder.

10.2 Typical Application

Three application examples are provided. The first one is for a 100A Hot Swap with 5,500 µF of output capacitance that uses standard power limited based start-up. Then there are two examples of designing for the 240 VA design requirment. One uses the CSD16415Q5B, which is an older generation MOFSET with great SOA. The second one uses the CSD17573Q5B, which has lower SOA, but is more cost effective (price vs R_{DSON}).

10.2.1 12 V, 100 A, 5,500 µF Analog Hot Swap Design

The diagram below shows the application schematic for this design example.

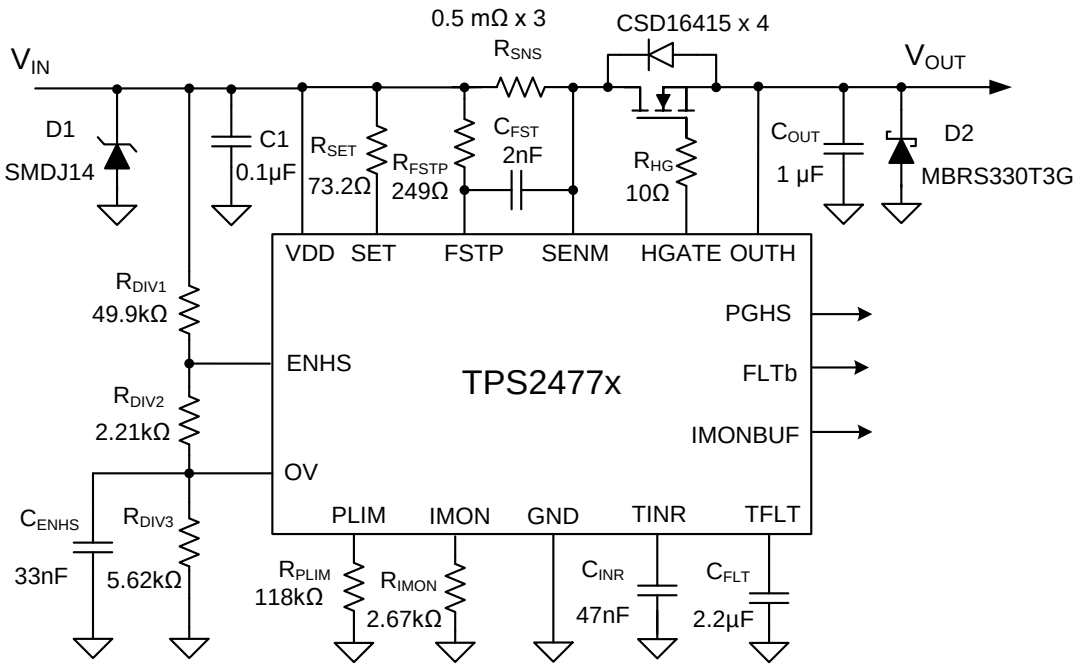


Figure 18. Application Schematic for 100 A Hot Swap

Typical Application (continued)

10.2.2 Design Requirements

Table 1 summarizes the design parameters that must be known before designing a Hot Swap circuit. When charging the output capacitor through the Hot Swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load current will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling will also reduce $R_{\theta CA}$. It's also important to know if there are any transient load requirements. Finally, whether current monitoring is needed and its accuracy requirement will drive the selection of R_{SNS}, R_{IMON}, and R_{SET}.

Table 1. Design Requirements for a 12V, 100A, 5500µF Hot Swap Design

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	11 V – 13 V
Maximum DC load current	100A
Maximum Output Capacitance of the Hot Swap	5500 µF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	50°C/W
Transient load requirement	130A for 250 ms
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Can a Hot Board be plugged in or Power Cycled?	No
IC used	TPS24772
Analog Current Monitor Used	No

10.2.3 Detailed Design Procedure

10.2.3.1 Select R_{SNS} and $V_{SNS,CL}$ Setting

TPS2477x has a programmable $V_{SNS,CL}$ with a recommended range of 10 mV to 67.5 mV. It can be used with a $V_{SNS,CL}$ up to 200 mV, but that requires a resistor between SET and SENM to ensure stability of an internal loop. This is shown in Figure 19. R_{STBL} can be computed using the equation below.

$$R_{STBL} = \frac{R_{IMON} \times R_{SET}}{10 \times R_{SET} - R_{IMON}} \tag{10}$$

For high power applications a lower $V_{SNS,CL}$ leads to better efficiency so 20 mV is targeted for this design. Targeting a current limit of 110A to allow margin for the load, the sense resistor can be calculated as follows:

$$R_{SNS,CLC} = \frac{V_{SNS,TGT}}{I_{LIM}} = \frac{20\ mV}{110\ A} = 0.18\ m\Omega \tag{11}$$

Since 0.18 mΩ resistors aren't available, the closest standard resistor should be chosen. To have better efficiency, three 0.5mΩ resistors are used in parallel. Next the $V_{SNS,CL}$ should be computed based on the actual R_{SNS} and then used to compute R_{SET} and R_{IMON}. R_{SET} is chosen to target 250 µA of current through SET and IMON pins during current limit.

$$V_{SNS,CL} = I_{LIM} \times R_{SNS} = 110\ A \times 0.1667\ m\Omega = 18.37\ mV \tag{12}$$

$$R_{SET,CLC} = \frac{V_{SNS,CL}}{250\ \mu A} = 73.3\ \Omega \tag{13}$$

Chose R_{SET} to equal 73.2 Ω, which is the closest available standard resistor. Next obtain the calculated R_{IMON} ($R_{IMON,CLC}$) as follows:

$$R_{IMON,CLC} = \frac{R_{SET} \times 675\ mV}{V_{SNS,CL}} = \frac{73.2\ \Omega \times 675\ mV}{18.37\ mV} = 2.69\ k\Omega \tag{14}$$

Choose 2.67kΩ resistor for R_{IMON}, which is the closest available standard resistor. Since accurate current monitoring is not needed a 2512 2 terminal sense resistor can be used.

Finally, compute the actual current limit ($I_{LIM,CL}$) and the analog current monitoring scaling factor $V_{IMON,GAIN}$ (V_{IMON} vs I_{LOAD})

$$I_{LIM,CL} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}} = \frac{0.675\ V \times 73.2\ \Omega}{2.67\ k\Omega \times 0.1667\ m\Omega} = 111\ A \quad (15)$$

$$V_{IMON,GAIN} = \frac{R_{IMON} \times R_{SNS}}{R_{SET}} = \frac{0.1667\ m\Omega \times 2.67\ k\Omega}{73.2\Omega} = 6.08\ mV / A \quad (16)$$

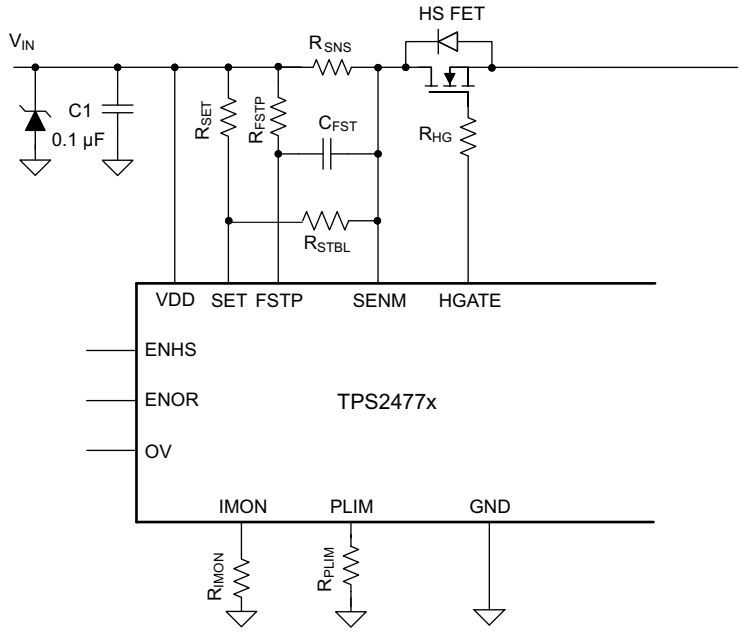


Figure 19. Adding R_{STBL} for $V_{SNS,CL}$ > 67.5mV

10.2.3.2 Selecting the Fast Trip Threshold and Filtering

The TPS2477x allows the user to program the fast trip threshold. When this threshold is exceeded the gate is quickly pulled down (<1µs). In addition C_{FSTP} can be added to include some filtering into the comparator. The selection of the fast trip threshold and filtering is influenced by the systems environment and requirements. In general, picking a larger threshold and larger filtering time will result in more immunity to nuisance trips, but also a slower response (possibly inadequate) to real fault conditions. It's best to fine tune these threshold after testing the real system. As a starting point it is recommended to set the fast trip threshold at least 1.25x larger than then current limit. For this design example a 150A fast trip threshold along with a 500ns filtering time constant were targeted to ensure that the transient requirement will be passed. The value for R_{FSTP} and C_{FSTP} can be computed as shown below:

$$R_{FSTP} = \frac{I_{FSTP} \times R_{SNS}}{100\ \mu A} = \frac{150\ A \times 0.1667\ m\Omega}{100\ \mu A} = 250\ \Omega \quad (17)$$

$$C_{FSTP} = \frac{t_{FSTP}}{R_{FSTP}} = \frac{500\ ns}{250\ \Omega} = 2\ nF \quad (18)$$

The next closest standard resistor and capacitor values should be chosen. In this case R_{FSTP} = 249Ω and C_{FSTP}=2nF

10.2.3.3 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q5B was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times \frac{R_{DSON}(T_J)}{n^2} \tag{19}$$

In the equation above n is the number of FETs used in parallel. For this example 4 FETS are used in parallel to prevent over- heating and improve efficiency. Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD16415Q5B datasheet, its R_{DSON} is about 1.3x greater at 100°C compared to room temperature . The equation below uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary. For this example an $R_{\theta CA}$ of 50°C/W was used since there are 4 FETs close together and it's expected that they will heat each other up. It's highly recommended to test the board at full load and double check the thermals with the calculations.

$$T_{C,MAX} = 55°C + 50°{}^{C}\!/_{W} \times (100A)^2 \times {}^{(1.3 \times 1\,m\Omega)}\!/_{4^2} = 95.6°C \tag{20}$$

10.2.3.4 Select Power Limit

In general, a lower power limit setting is preferred to reduce the stress on the MOSFET. However, at low power limit levels both the V_{SNS} and V_{IMON} become very low, which results in more error caused by offsets. It is recommended to keep V_{SNS} above 1.5mV and V_{IMON} above 27mV to ensure reasonable accuracy of the power limit engine. Based on these requirements the minimum power limit can be computed as shown below.

$$\begin{aligned} P_{LIM,MIN} &= \frac{V_{IN,MAX}}{R_{SNS}} \times MIN\left(V_{SNS,MIN}, \frac{V_{IMON,MIN} \times R_{SET}}{R_{IMON}}\right) \\ &= \frac{13\ V}{0.1667\ m\Omega} \times MIN\left(1.5\ mV, \frac{27\ mV \times 73.2\ \Omega}{2.67\ k\Omega}\right) = 117\ W \end{aligned} \tag{21}$$

In most applications the power limit can be set to $P_{LIM,MIN}$ using the equation below. Here R_{SNS} and R_{PWR} are in Ωs and P_{LIM} is in Watts.

$$R_{PLIM} = \frac{84375 \times R_{SET}}{R_{SNS} \times R_{IMON} \times P_{LIM}} = \frac{84375 \times 73.2\ \Omega}{0.1.667\ m\Omega \times 2.67\ k\Omega \times 117\ W} = 118.6\ k\Omega \tag{22}$$

The closest available resistor should be selected. In this case it is a 118 kΩ.

10.2.3.5 Set Fault Timer

The inrush timer runs when the Hot Swap is in power limit or current limit, which is the case during start-up. Thus the timer has to be sized large enough to prevent a time-out during start-up. If the part starts directly into current limit (I_{LIM} x V_{DS} < P_{LIM}) the maximum start time can be computed with the equation below:

$$t_{start,max} = \frac{C_{OUT} \times V_{IN,MAX}}{I_{LIM,CL}} \tag{23}$$

For most designs (including this example) $I_{LIM,CL}$ x V_{DS} > P_{LIM} so the Hot Swap will start in power limit and transition into current limit. In that case the maximum start time can be computed as follows:

$$t_{start,max} = \frac{C_{OUT}}{2} \times \left[\frac{V_{IN,MAX}^2}{P_{LIM}} + \frac{P_{LIM}}{I_{LIM,CL}^2} \right] = \frac{5500\ \mu F}{2} \times \left[\frac{(13\ V)^2}{117\ W} + \frac{117\ W}{(110\ A)^2} \right] = 4.0\ ms \tag{24}$$

Note that the above start-time is based on typical current limit and power limit values. To ensure that the timer never times out during start-up it is recommended to set the fault time (TINR) to be 1.5x $t_{start,max}$ or 6 ms. This will account for the variation in power limit, timer current, and timer capacitance.

Next the designer should decide if having equal TINR and TFLT is acceptable. Note that to pass the load transient the fault timer needs to be longer than 200 ms. If the inrush time is this long, it will place too much stress on the MOSFET during a start into short. For this reason, it's ideal to have two separate timers. To ensure proper start up and to pass the load transient a target inrush time ($T_{INR,TGT}$) of 6 ms and a target fault time ($T_{FLT,TGT}$) of 250ms is used. $C_{INR,CLC}$ and $C_{FLT,CLC}$ is computed as follows:

$$C_{INR,CLC} = 7.59\ \mu F/s \times T_{INR,TGT} = 7.59\ \mu F/s \times 6\ ms = 45.6\ nF \tag{25}$$

$$C_{FLT,CLC} = 7.59\ \mu F/s \times T_{FLT,TGT} = 7.59\ \mu F/s \times 250\ ms = 1898\ nF \tag{26}$$

The next largest available C_{INR} is chosen as 47 nF and the next largest available C_{FLT} is chosen as 2.2µF

Next, the actual T_{INR} and T_{FLT} can be computed as shown below: Once the C_{TMR} is chosen the actual programmed time out can be computed as follows.

$$T_{TMR} = \frac{C_{INR}}{7.59\ \mu F/s} = \frac{47\ nF}{7.59\ \mu F/s} = 6.2\ ms \tag{27}$$

$$T_{FLT} = \frac{C_{FLT}}{7.59\ \mu F/s} = \frac{2.2\ \mu F}{7.59\ \mu F/s} = 290\ ms \tag{28}$$

10.2.3.6 Check MOSFET SOA

Once the power limit and fault timer are chosen, it's critical to check that the FET will stay within its SOA during all test conditions. For this design example the TPS24772 is used, which does not retry during a hot-short. Thus the worst condition is a start-up into a short circuit. In this case the TPS24772 will start into a power limit and regulate at that point for 6.2 ms (T_{INR}). Based on the SOA of the CSD16415Q5B, it can handle 13 V, 15 A for 10 ms and it can handle 13 V, 100 A for 1 ms. The SOA for 6.2 ms can be extrapolated by approximating SOA vs time as a power function as shown below:

$$I_{SOA}(t) = a \times t^m$$

$$m = \frac{\ln\left(I_{SOA}(t_1)/I_{SOA}(t_2)\right)}{\ln(t_1/t_2)} = \frac{\ln\left(\frac{100\ A}{15\ A}\right)}{\ln\left(\frac{1\ ms}{10\ ms}\right)} = -0.82$$

$$a = \frac{I_{SOA}(t_1)}{t_1^m} = \frac{100\ A}{(1\ ms)^{-0.82}} = 100\ A \times (ms)^{0.82}$$

$$I_{SOA}(6.2\ ms) = 100\ A \times (ms)^{0.82} \times (6.2\ ms)^{-0.82} = 22.4\ A \tag{29}$$

Note that the SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ($T_{C,\ MAX,\ START}$). If a board has been off for a while and then it's turned on $T_{A,\ MAX}$ is a good estimate for $T_{C,MAX,\ START}$. However, if a board is on and then gets power cycled or a hot board is unplugged and plugged back in $T_{C,MAX}$ should be used for $T_{C,MAX,STAR}T$. This will depend on system requirements. For this design example it's assumed that the board can only be plugged in cold and $T_{A,MAX}$ is used to estimate $T_{C,MAX,START}$.

$$I_{SOA}\left(6.2\ ms, T_{C,MAX,START}\right) = I_{SOA}\left(6.2\ ms, 25°C\right) \times \frac{T_{J,ABSMAX} - T_{A,MAX}}{T_{J,ABSMAX} - 25°C} = 22.4\ A \times \frac{150°C - 55°C}{150°C - 25°C} = 17\ A \tag{30}$$

Based on this calculation the MOSFET can handle 17 A, 13 V for 6.2 ms at 55°C elevated case temperature, but is only required to handle 9A during a start into short. Thus there is good margin and this will be a robust design. In general, it is recommended that the MOSFET can handle 1.3x more than what is required during a hot-short. This provides margin to cover the variance of the power limit and fault time.

10.2.3.7 Choose Under Voltage and Over Voltage Settings

The TPS2477x has comparators with 1.35V threshold on the ENHS, ENOR, and OV pins. A resistor divider can be used to set Undervoltage and Overvoltage thresholds for the bus. For this design example 10V and 14V were chosen as the limits to allow some margin for the 11V to 13V input bus. Once these limits are known, R_{DIV2} and R_{DIV3} can be computed using the equations below. R_{DIV1} was set to 49.9 kΩ, which keeps the power consumption reasonable low without being too susceptible to leakage currents.

$$R_{DIV2,3} = R_{DIV2} + R_{DIV3} = \frac{R_{DIV1} \times 1.35\ V}{V_{UV} - 1.35\ V} = \frac{49.9\ k\Omega \times 1.35\ V}{10\ V - 1.35\ V} = 7.79\ k\Omega \tag{31}$$

$$R_{DIV3} = \frac{\left(R_{DIV1} + R_{DIV2,3}\right) \times 1.35\ V}{V_{OV}} = \frac{\left(49.9\ k\Omega + 7.79\ k\Omega\right) \times 1.35\ V}{14\ V} = 5.56\ k\Omega \tag{32}$$

$$R_{DIV2} = R_{DIV2,3} - R_{DIV1} = 7.79\ k\Omega - 5.56\ k\Omega = 2.23\ k\Omega \tag{33}$$

Choose closest available resistors standard 1% resistors: R_{DIV2} = 2.21 kΩ and R_{DIV3} = 5.62 kΩ. The actual Under Voltage and Over Voltage settings can be computed for the chosen resistors as follows:

$$V_{UV\_act} = 1.35V \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV2} + R_{DIV3}} = 1.35\ V \times \frac{2.21\ k\Omega + 5.62\ k\Omega + 49.9\ k\Omega}{2.21\ k\Omega + 5.62\ k\Omega} = 9.95\ V \tag{34}$$

$$V_{OV\_act} = 1.35\ V \times \frac{R_{DIV1} + R_{DIV2} + R_{DIV3}}{R_{DIV3}} = 1.35\ V \times \frac{2.21\ k\Omega + 5.62\ k\Omega + 49.9\ k\Omega}{5.62\ k\Omega} = 13.87\ V \tag{35}$$

10.2.3.8 Selecting C_1 and C_{OUT}

It is recommended to add ceramic bypass capacitors to help stabilize the voltages on the input and output. Since C_{IN} will be charged directly on hot-plug, its value should be kept small. 0.1µF is a good target. Since C_{OUT} doesn't get charged during hot-plug, a larger value such as 1 µF could be used.

10.2.3.9 Adding C_{ENHS}

When the ENHS pin is pulled below its threshold and raised back up the IC will reset. Note that during a hot short the input voltage can easily droop below the UV threshold and cycle the ENHS pin. For the TPS24770 and TPS24771 ICs this will not change the behavior. However, when using the TPS24772 the cycling of the ENHS will result in the IC attempting to restart, which is undesired (this is the main reason why someone would use the TPS24772). To avoid this behavior a capacitor should be added to the ENHS to provide filtering. 33 nF was chosen for this example.

10.2.3.10 Selecting D1 and D2

During hot plug and hot short events there could be significant transients on the input and output of the Hot Swap that could cause operation outside of the IC specifications. To ensure reliable operation a TVS on the input and a Schottkey diode on the output are recommended. In this example a SMDJ14A and MBRS330T3G are used.

10.2.3.11 Checking Stability

For most applications, the TPS2477x is stable without any additional components. However in some cases additional $C_{GS,EXT}$ is required as shown in the following figure to help stabilize the current and power limit loop. Typically this is for low current limits and low sense voltages. It is easy to check whether these extra components are needed using the equations below. Note that the transconductance (also referred to as gm and gfs) of the FET will vary based on the current and thus gm' is used in the equations as a normalizing parameter. The CSD16415Q5B has a gm of 168 siemens at 40A of I_{DS}, resulting in gm' of 26.56. For this example, $C_{GS,MIN}$ (per FET) was computed to be 0.25nF, while the C_{ISS} of the CSD16415Q5B is 3.15nF providing plenty of margin for the design. In general it is recommended to have a 2x margin from the typical C_{ISS} and $C_{GS,MIN}$ to account for any variation that the FET would have. If the C_{ISS} of the MOSFET isn't large enough an external RC should be added as shown in the figure below.

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times gm' \times \left(\frac{R_{IMON}}{R_{SET}}\right)^{1.5} \times \frac{\sqrt{R_{SNS}}}{\sqrt{n}} \tag{36}$$

$$g_m' = \frac{g_m(I_{DS})}{\sqrt{I_{DS}}} = \frac{168}{\sqrt{40}} = 26.56 \tag{37}$$

$$C_{GS,MIN} = 6.54 \times 10^{-12} \times 26.56 \times \left(\frac{2.67k}{73.2}\right)^{1.5} \times \frac{\sqrt{0.1667m}}{\sqrt{4}} = 0.25nF \tag{38}$$

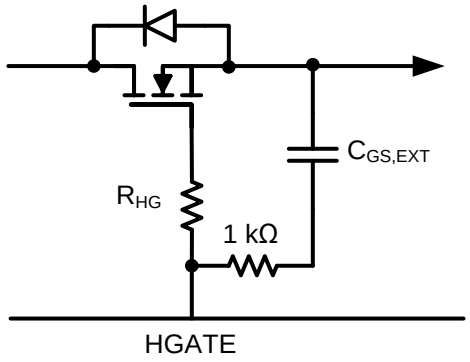


Figure 20. Adding $C_{GS,EXT}$ to Ensure Stability

10.2.3.12 Compute Tolerances

After finishing a design it is often desired to know the variations of each setting. Often times there are multiple error sources and there are two common ways to analyze the circuit. One is worst case, which adds all of the error sources and the other one is root sum square (RSS), which is less conservative. When error sources are independent, using the RSS method provides a more statistically accurate view of the tolerances. This method is used in this section. Note that the error calculations are quite long and tedious and it's recommended to use TI's excel tools, which support both worst case and RSS analysis. For this example the below tolerances are assumed. The following table lists the assumptions for the component tolerances. Note that the sense resistor itself is 1% accurate, but multiple two terminal 2512 resistors are used so additional error is introduced from solder resistance and layout limitations of paralleling resistors. For this example 3% is assumed as the total error of the sensing network.

Table 2. Component Tolerances

COMPONENTS	TOLERANCE
R_{IMON} and R_{SET}	1%
R_{SNS}(Including Layout + Soldering)	3%
R_{DIV1}, R_{DIV2}, R_{DIV3}, R_{PLIM}, R_{FST}	1%
C_{INR}, C_{FLT}	10%

First, the tolerance of the current monitoring and current limit is computed.

There are 5 error sourcing contributing to the current monitoring accuracy on the IMON pin: tolerance of R_{SET} (ER_{SET}), tolerance of R_{IMON} (ER_{IMON}), tolerance of R_{SNS} (E_{RSNS}), the IC gain error (ER_{GAIN}), and the IC offset error (ER_{OS}). All of these errors are in % with the exception of the offset error. To get a percent error due to the offset error ($ER_{OS\%}$) simply divide the offset by the sense voltage. For the TPS2477x, ER_{GAIN} is 0.4%, and ER_{OS} is 150 µV.

Based on these values the full scale ($I_{FS,ERR,IMON}$) current monitoring accuracy at the Imon pin can be computed with the following equations.

$$I_{FS,ERR,IMON} = \sqrt{(ER_{SET})^2 + (ER_{SNS})^2 + (ER_{IMON})^2 + (ER_{GAIN})^2 + \left(\frac{ER_{OS}}{R_{SNS} \times I_{LIM}}\right)^2}$$
$$= \sqrt{1\%^2 + 3\%^2 + 1\%^2 + 0.4\%^2 + (150\ \mu V / 18.34\ mV)^2} = 3.4\% \quad (39)$$

Note that the TPS2477x detects the current limit when the IMON pin exceeds 675 mV. Thus the current limit error $I_{LIM,ER}$ is a combination of the $I_{FS,ERR,IMON}$ and the current limit error at the I_{MON} pin ($I_{LIM,ERR,IMON}$). The 675 mV threshold varies up to 15 mV so $I_{LIM,ERR,IMON}$ is 2.3% and the current limit error can be computed as follows:

$$I_{LIM,ERR} = \sqrt{(I_{FS,ERR,IMON})^2 + (I_{LIM,ERR,IMON})^2} = \sqrt{3.4\%^2 + 2.3\%^2} = 4.1\% \quad (40)$$

Next the power limit error is computed. This error is made up of three sources: the error from external components (ER_{COMP}), the error when translating the sense voltage to IMON ($I_{PL,ERR,\ IMON}$), and the error of the power limit engine at IMON ($ER_{IMON,PL}$). Both ER_{SNS} and $ER_{IMON,\ PL}$ are a function of the operating point of the power limit engine. Note that this error is greatest at largest V_{DS}, since $V_{SNS,PL}$ is smallest (refer to Figure 12). For this example V_{DS} is largest when V_{IN} = 13 V (maximum V_{IN}) and V_{OUT} = 0 V and the error is computed at this operating point. The sense voltage (V_{SNS}) and the voltage at the IMON pin (V_{IMON}) should be computed for this operating point using the equations below:

$$V_{SNS} = \frac{P_{LIM} \times R_{SNS}}{V_{DS}} = \frac{117\ W \times 0.1667\ m\Omega}{13\ V} = 1.5\ mV \quad (41)$$

$$V_{IMON} = \frac{V_{SNS} \times R_{IMON}}{R_{SET}} = \frac{1.5\ mV \times 2670\ \Omega}{73.2\ \Omega} = 54.7\ mV \quad (42)$$

The $I_{PL,ERR,IMON}$ can be computed similarly to $I_{FS,ERR,IMON}$ using the equation below.

$$I_{PL,ERR,IMON} = \sqrt{(ER_{GAIN})^2 + \left(\frac{ER_{OS}}{V_{SNS}}\right)^2} = \sqrt{(0.4\%)^2 + \left(\frac{150\ \mu V}{1.5\ mV}\right)^2} = 10\% \quad (43)$$

The tolerance of the power limit engine is specified at three V_{IMON} points in the datasheet: 135 mV (±20.3 mV), 67.5 mV (±10.1 mV), and 27 mV (±8.1 mV). To get the % error at the real operating point, the absolute error should be extrapolated and divided by V_{IMON} as shown in the equation below. This is graphically depicted in Figure 23.

$$ERR_{IMON,PL} = \frac{8.1\ mV + (54.7\ mV - 27\ mV) \times \frac{10.1\ mV - 8.1\ mV}{67.5\ mV - 27\ mV}}{54.7\ mV} = 17.3\% \quad (44)$$

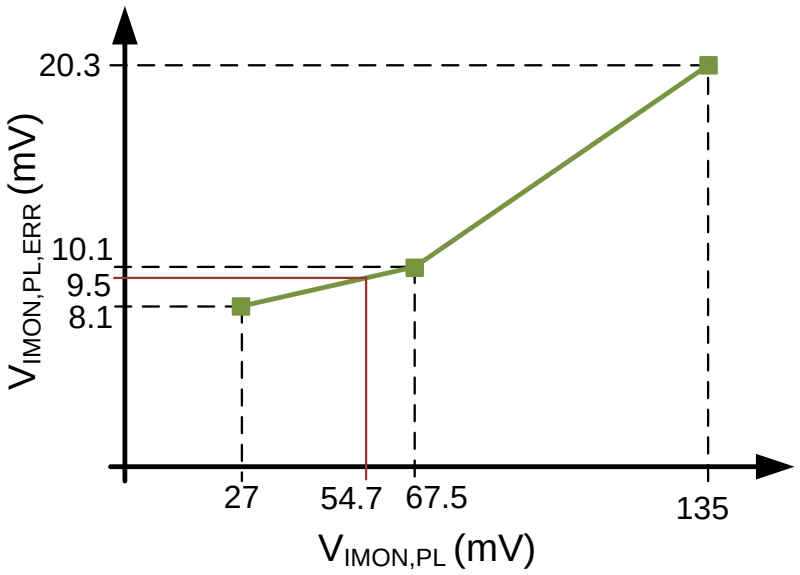


Figure 21. Extrapolating Power Limit Error

Once $ER_{IMON,PL}$ and $I_{PL,ERR,IMON}$ are known the total power limit error ($PL_{ERR,TOT}$) can be computed using the equation below. The component error (3.5%) comes from R_{SNS} (3%), R_{PLIM} (1%), R_{SET} (1%), and R_{IMON} (1%).

$$PL_{ERR,TOT} = \sqrt{\left(ERR_{IMON,PL}\right)^2 + \left(I_{PL,ERR,IMON}\right)^2 + \left(ERR_{COMP}\right)^2}$$
$$= \sqrt{(17.3\%)^2 + (10\%)^2 + (3.5\%)^2} = 20.3\% \quad (45)$$

After computing the fast trip voltage threshold to be 24.9 mV (100 µA × 249 Ω), the fast trip threshold error resulting from the IC ($FST_{ERR,\ IC}$) can be computed using a similar extrapolation method as used for power limit. The component error of R_{SNS} and R_{FST} should be added to obtain the total fast trip error ($FST_{ERR,TOT}$). Both equations are shown below.

$$FST_{ERR,IC} = \frac{2\ mV + (24.9\ mV - 20\ mV) \times \frac{5\ mV - 2\ mV}{100\ mV - 20\ mV}}{24.9\ mV} = 8.8\% \quad (46)$$

$$FST_{ERR,TOT} = \sqrt{(8.8\%)^2 + (1\%)^2 + (3\%)^2} = 9.4\% \quad (47)$$

The IC error of the UV / OV threshold is always 3.7% (0.05 V / 1.35 V). Assuming that all resistors have a 1% error the component error is 1.41% (2 resistors). When using the RSS method the total error is 4%. For the timer error, the IC contributes 22% and 10% comes from the component. When using the RSS method the total error becomes 24.2%.

The table below summarizes the final tolerances of the design:

Table 3. Design Tolerances

SETTINGS	ACCURACY
Current Limit	4.1%
Fast Trip	9.4%
Power Limit	20.3%
TFLT, TINR	24.2%
UV/OV	4.0%

10.2.4 Application Curves

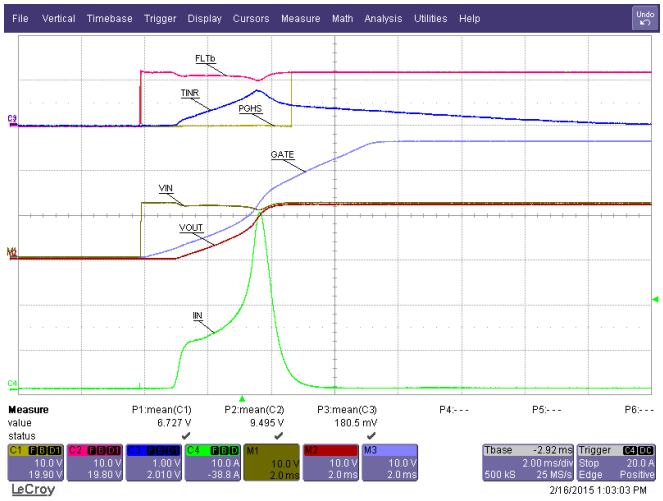


Figure 22. Start up (C_{OUT}=5500µF)

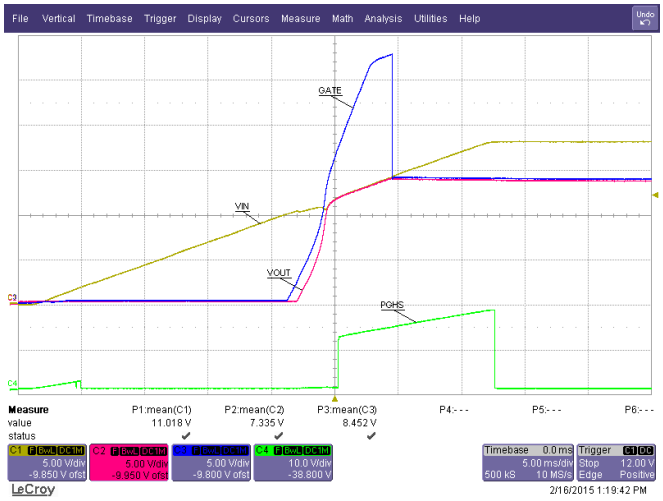


Figure 23. Undervoltage and Overvoltage

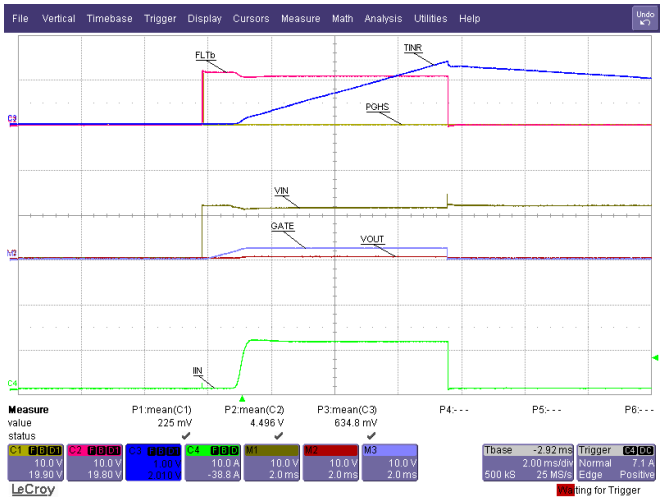


Figure 24. Start Up with Output Shorted to GND

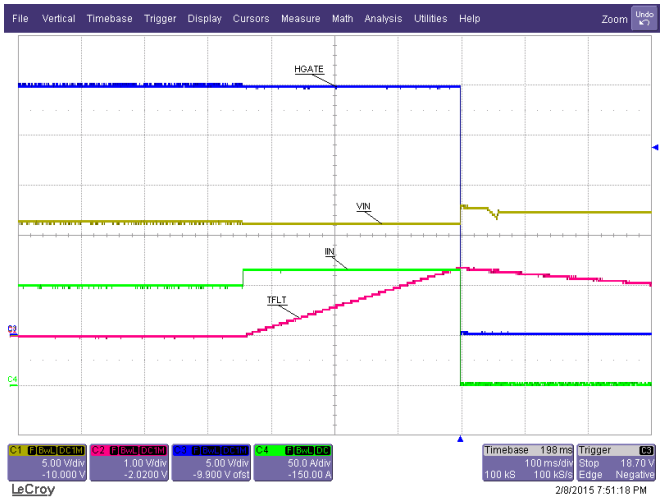


Figure 25. Load Step 100A to 120A

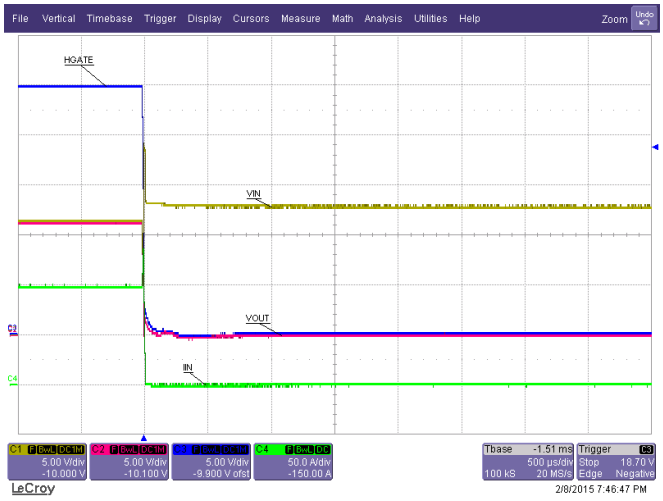


Figure 26. Hot Short on Output with Full Load (zoomed out)

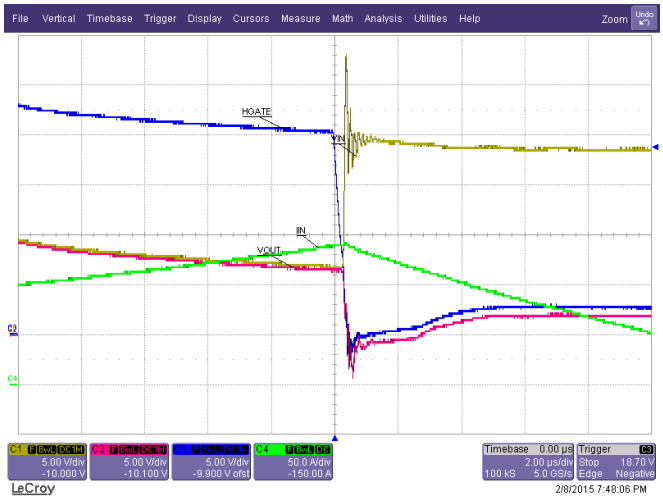


Figure 27. Hot Short on Output with Full Load (zoomed in)

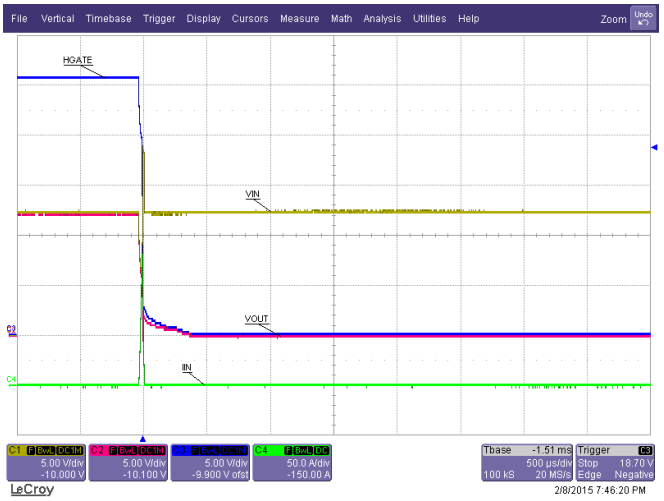


Figure 28. Hot Short on Output with No Load (zoomed out)

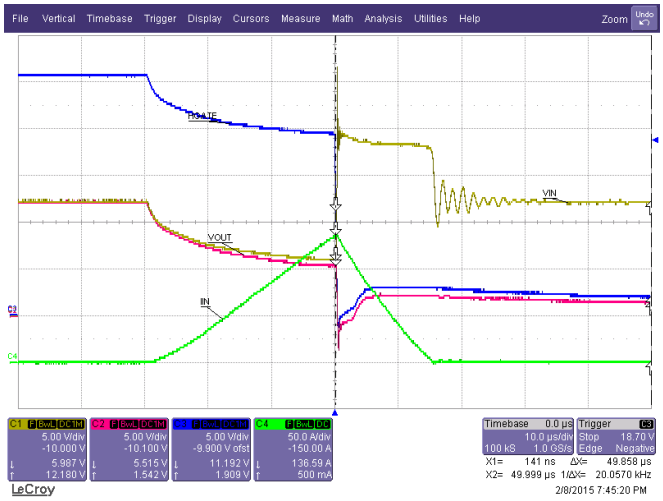


Figure 29. Hot Short on Output with No Load (zoomed in)

10.2.5 240 VA Application Using CSD16415Q5B

The diagram below shows the application schematic for this design example. See the TPS24770 Design Calculator to help with these calculations.

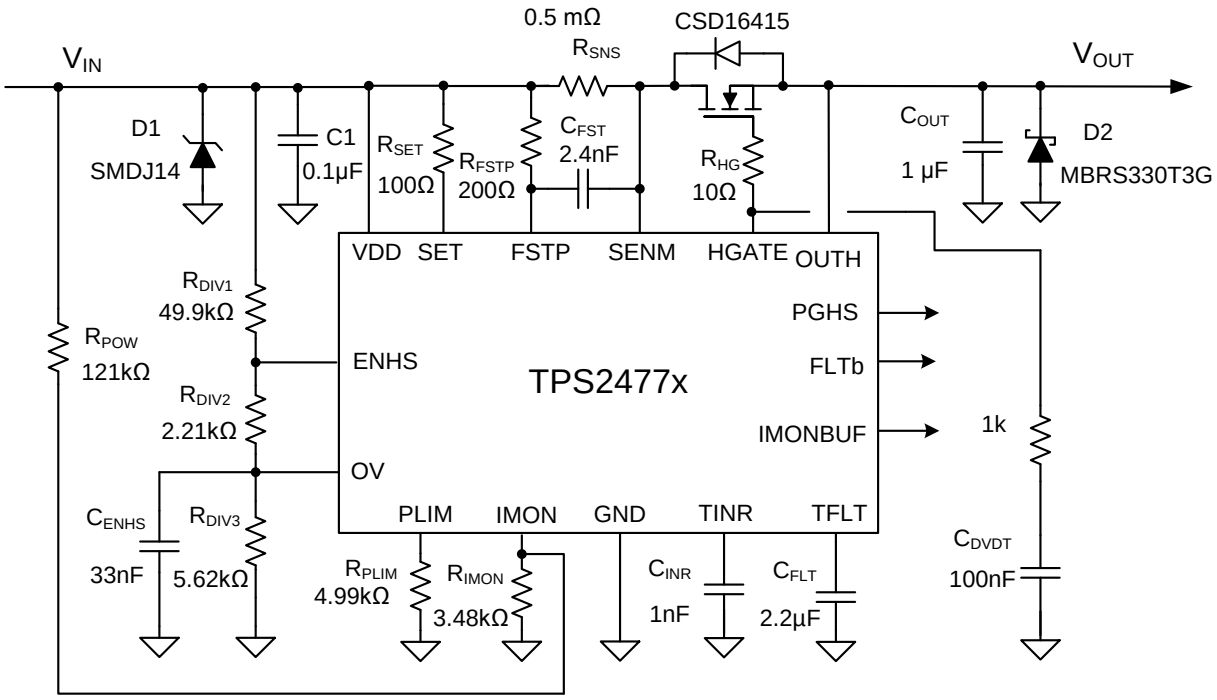


Figure 30. Application Schematic for 240VA Design with CSD16415Q5B

10.2.5.1 Design Requirements

The following table summarizes the requirements for this design. Note that the output power cannot exceed 240W for more than 250 ms.

Table 4. Design Requirements for a 240 VA Design using CSD16415Q5B

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10.8 V – 13.2V
Output Power Limit (VA limiting)	240 W
Maximum Output Capacitance of the Hot Swap	2500 uF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	35°C/W
Transient load requirement?	POUT is allowed to surpass 240W for <250 ms
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG asserted?	Yes
IC used	TPS24772
Analog Current Monitor Used	No
MOSFET	CSD16415Q5B
Can a Hot Board be plugged in or Power Cycled?	Yes

10.2.5.2 Theory of Operations

Before going into the details of the design it’s important to understand the impact that R_{POW} has on the circuit. Refer to Figure 31 for this discussion.

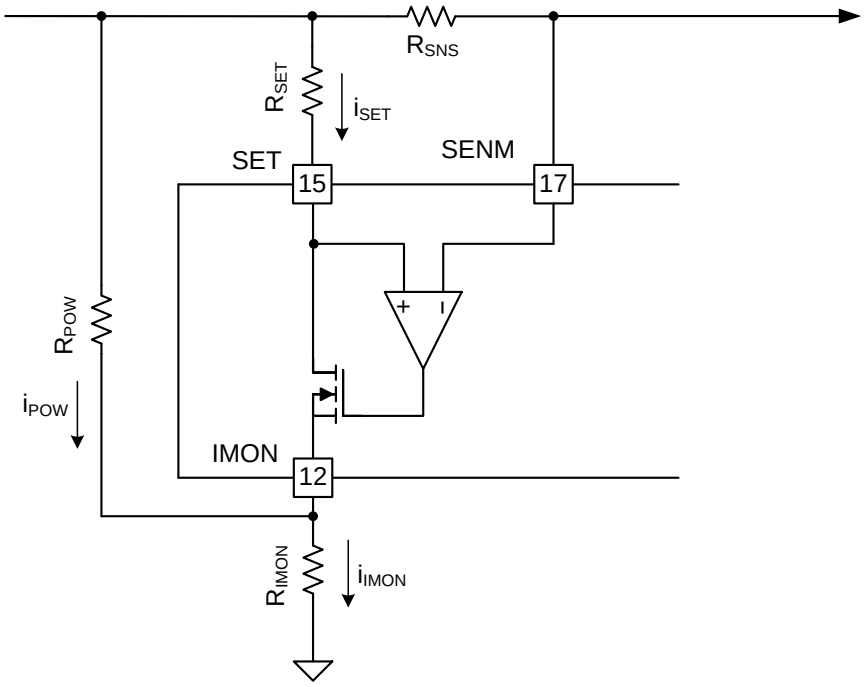


Figure 31. Impact of R_{POW} Resistor

Note that the TPS2477x detects overcurrent conditions when V_{IMON} reaches 675mV, which occurs when there is sufficient current (i_{IMON}) flowing through R_{IMON}. Also note that i_{IMON} is a sum of i_{SET} and i_{POW}. If $i_{IMON,CL}$, $i_{SET,CL}$, and $i_{POW,CL}$ correspond to these same current when V_{IMON} reaches 675mV and TPS2477x detects current limit, the following equations can be written.

$$i_{IMON,CL} = \frac{675\ mV}{R_{IMON}}; i_{IMON,CL} = i_{SET,CL} + i_{POW,CL} \quad (48)$$

$$i_{SET,CL} = \frac{675\ mV}{R_{IMON}} - \frac{V_{IN} - 675\ mV}{R_{POW}} \quad (49)$$

Also note that the amplifier ensures that SET and SENM are equal and thus I_{LIM} can be derived as follows:

$$i_{IMON,CL} = \frac{675\ mV}{R_{IMON}}; i_{IMON,CL} = i_{SET,CL} + i_{POW,CL} \quad (50)$$

$$I_{LIM} = i_{SET,CL} \times \frac{R_{SET}}{R_{SNS}} = \frac{R_{SET}}{R_{SNS}} \times \left(\frac{675mV}{R_{IMON}} + \frac{675mV}{R_{POW}} \right) - \frac{V_{IN} \times R_{SET}}{R_{SNS} \times R_{POW}} \quad (51)$$

Examining the equation above, it can be seen that I_{LIM} reduces as V_{IN} becomes larger. Note that the ultimate goal is to limit output power. However, when the FET is on, V_{IN} is very close to V_{OUT} and they can be assumed to be equal.

The figure below compares the ideal I_{LIM} vs V_{OUT} (I_{LIM} =240 W / V_{OUT}) profile to that of the R_{POW} implementation shown here. The error is large when the output voltage is far from 12V, but the performance is quite good near 12V. The next figure shows the effective output power limit for output voltages from 10 V to 14 V. It can be seen that the results are quite good and much better than using a simple 20A current limit, without the R_{POW} resistor to compensate for V_{IN} variation.

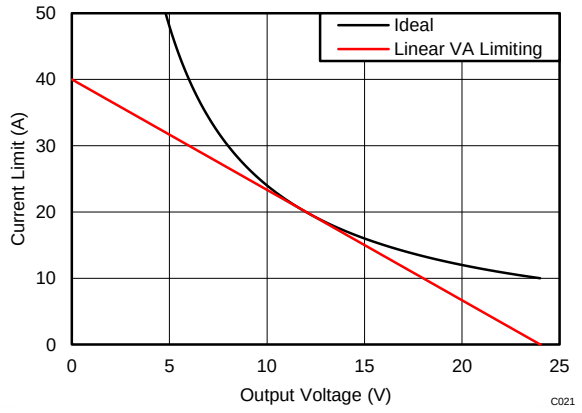


Figure 32. Current Limit (with R_{POW}) vs Output Voltage

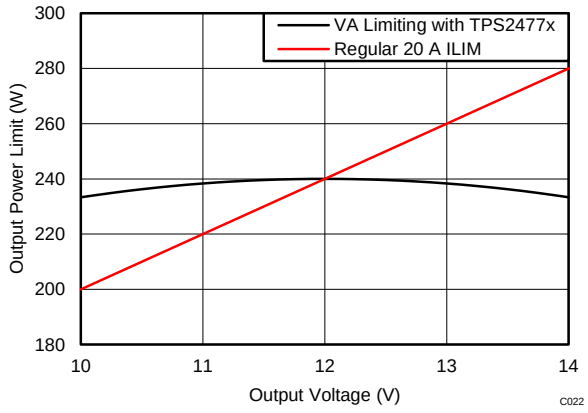


Figure 33. Output Power Limiting using R_{POW} vs Standard ILIM

10.2.5.3 Design Procedure

10.2.5.3.1 Select $V_{SNS,CL}$, R_{SNS}, and R_{SET} Setting

For this example, $V_{SNS,CL}$ of 10 mV was selected to optimize efficiency. Then R_{SNS} can be computed to 0.5mΩ. There is some flexibility in picking the R_{SET} value. In this case targeting 100 µA for $I_{SET,CL}$, R_{SET} is computed to be 100 Ω as shown in the following equation.

$$R_{SET} = \frac{V_{SNS,CL}}{i_{SET,CL}} = \frac{10\ mV}{100\ \mu A} = 100\ \Omega \quad (52)$$

10.2.5.3.1.1 Select R_{POW} and R_{IMON}

R_{POW} controls the slope of the I_{LIM} vs V_{IN} curve and thus the ideal slope should be found first before selecting R_{POW}. This can be done by taking the derivative of the ideal current limit ($I_{LIM,\ IDEAL}$) vs V_{IN} curve and evaluating it at 12V. This is found to be –1.667 A/V as shown in the equations below. Next the derivative of equation 51 is taken to isolate the terms that influence the slope of I_{LIM} vs V_{IN} curve. Since R_{SET} and R_{SNS} have already been selected, R_{POW} remains the only parameter that can be varied. Thus, R_{POW} is computed using the last equation below.

$$\frac{dI_{LIM,IDEAL}}{dV_{IN}}(V_{IN} = 12\ V) = \frac{-240\ W}{(12\ V)^2} = -1.667\ A/V \quad (53)$$

$$\frac{dI_{LIM}}{dV_{IN}} = \frac{-R_{SET}}{R_{SNS} \times R_{POW}} \quad (54)$$

$$R_{POW,CLC} = \frac{\frac{-R_{SET}}{R_{SNS}}}{\frac{dI_{LIM,IDEAL}}{dV_{IN}}(V_{IN} = 12\ V)} = \frac{\frac{-100\ \Omega}{0.5m\ \Omega}}{-1.667\ \frac{A}{V}} = 120\ k\Omega \quad (55)$$

The closest available standard resistor is chosen for R_{POW}, which is 121kΩ.

Next R_{IMON} should be chosen to ensure that the output power limit is 240 W at 12 V, which is the typical operating point. R_{IMON} is computed to be 3.49kΩ and the closest available standard resistor of 3.48 kΩ is chosen.

$$i_{IMON,CL} = i_{SET,CL} + i_{POW,CL} = 100\ \mu A + \frac{12\ V - 0.675\ V}{121\ k\Omega} = 193.6\ \mu A \quad (56)$$

$$R_{IMON} = \frac{V_{IMON,CL}}{i_{IMON,CL}} = \frac{675\ mV}{193.6\ \mu A} = 3.49\ k\Omega \quad (57)$$

10.2.5.3.1.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD16415Q5B was selected for its low R_{DSON} and superior SOA. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times \frac{R_{DSON}(T_J)}{n^2} \quad (58)$$

In the equation above n is the number of FETs used in parallel. Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD16415Q5B datasheet, its R_{DSON} is about 1.2 x greater at 75°C compared to room temperature. . The equation below uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

$$T_{C,MAX} = 55°C + 35° \frac{C}{W} \times (20A)^2 \times (1.2 \times 1\ m\Omega) = 72°C \quad (59)$$

10.2.5.3.1.3 Keeping MOSFET within SOA During Normal Start-up

Next, the designer must ensure that the MOSFET will stay within SOA during start-up and a start-up into short. Note that the TPS24772 (fast latch off) is used for this design so the MOSFET stress during a hot short is minimal.

Since R_{POW} biases the I_{MON} pin, it interferes with FET power limiting and it's recommended to disable FET power limiting it by selecting a 4.99kΩ resistor for R_{POW}.

The inrush current can be limited by adding a capacitor from HGATE to GND (C_{DVDT}) as shown in the application diagram. This capacitor limits the slew rate of HGATE at start-up, which will in turn limit the slew rate of V_{OUT}. Assuming that the load is off until PGHS is asserted, all of the inrush current would be going into C_{OUT} and be inversely proportional to the slew rate of V_{OUT}. Refer to the application plots for a start-up waveform. In addition, a 1kΩ resistor is placed in series with C_{DVDT} to ensure that C_{DVDT} doesn't slow down the short circuit response of the Hot Swap.

For this example, a 100 nF capacitor was used for C_{DVDT}. This results in an inrush current (I_{INR}) of 1.375A, total inrush time (t_{INR}) of 24.5, and peak FET power dissipation ($P_{FET,PEAK}$) of 18.7W as shown in equations below. This assumes maximum input voltage of 13.2 V

$$I_{INR} = \frac{I_{HGATE} \times C_{OUT}}{C_{DVDT}} = \frac{55\ \mu A \times 2500\ \mu F}{100\ nF} = 1.375\ A \tag{60}$$

$$t_{INR} = \frac{V_{IN,MAX} \times C_{DVDT}}{I_{HGATE}} = \frac{13.2\ V \times 100\ nF}{55\ \mu A} = 24.5\ ms \tag{61}$$

$$P_{INR,MAX} = V_{IN,MAX} \times I_{INR} = 13.2\ V \times 1.375\ A = 18.2\ W \tag{62}$$

Next, it's importation to check that the MOSFET can handle this stress level. Note that the power dissipation of the MOSFET will start at $P_{INR,MAX}$ and will reduce to zero as the V_{DS} drop across the MOSFET reduces. The effective stress on the MOSFET can be approximated to be $P_{INR,MAX}$ for t_{INR}/2, which is the equivalent amount of energy. For this example, the FET stress is 18.7W for 12.3 ms. Looking at the SOA curve of the CSD16415Q5B, at V_{DS} of 13.2 V it can handle ~15A for 10ms or ~4A for 100ms. Using the same method as the previous design example, it can be computed that the MOSFET can handle 13.4A for 12.3 ms when V_{DS}=13.2 V.

The SOA of a MOSFET is specified at a case temperature of 25°C, while the real case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ($T_{C,\ MAX,\ START}$). If a board has been off for a while and then it's turned on, $T_{A,\ MAX}$ is a good estimate for $T_{C,MAX,\ START}$. However, if a board is on and then gets power cycled or gets unplugged and plugged back in, $T_{C,MAX}$ should be used for $T_{C,MAX,START}$. This will depend on system requirements. For this design example, it is assumed that a hot board can be power cycled or hot plugged and thus $T_{C,MAX}$ is used to estimate $T_{C,MAX,START}$.

$$I_{SOA}\left(12.3\ ms, T_{C,MAX,START}\right) = I_{SOA}\left(12.3\ ms,\ 25°C\right) \times \frac{T_{J,ABSMAX} - T_{C,MAX,START}}{T_{J,ABSMAX} - 25°C}$$
$$= 13.4\ A \times \frac{150°C - 72°C}{150°C - 25°C} = 8.4\ A \tag{63}$$

Based on this calculation the MOSFET can handle 8.4 A, 13.2 V for 12.3 ms at 72°C elevated case temperature, but is only required to handle 1.375 A. Thus there is good margin and this will be a robust design. In general a 1.3x margin is recommended to cover for variations.

Next, the start into short case is considered. Since the MOSFET power limit is disabled, the current through the MOSFET will reach 20A before the part starts to regulate and runs the inrush timer. In order to minimize FET stress, a short inrush timer is chosen (1nF of C_{INR}). Unfortunately, when a very short timer is used and there is a dv/dt capacitor, the FET stress cannot be simply estimated by T_{INR}. In the following figure, it is clear that the FET has both voltage and significant current across it for longer than just T_{INR}. This occurs because TINR is only activated when IIN reaches the current limit threshold, which doesn't happen immediately due to the slow dv/dt on the gate and the limited transconductance of the FET.

The current is not a square pulse, which makes it hard to compare the FET stress to the SOA curves. Thus the stress shown in the following figure needs to be converted to an equivalent square pulse. For this example, the equivalent pulse was assumed to be 20 A for 1ms. The MOSFET can handle 100A, 13.2 V for 1ms, which can be derated to 62 A when accounting for elevated case temperature. This provides plenty of margin and ensures a robust design.

$$I_{SOA}\left(1\ ms, T_{C,MAX,START}\right) = I_{SOA}\left(1\ ms,\ 72°C\right) \times \frac{T_{J,ABSMAX} - T_{C,MAX,START}}{T_{J,ABSMAX} - 25°C}$$
$$= 100\ A \times \frac{150°C - 72°C}{150°C - 25°C} = 62\ A \quad (64)$$

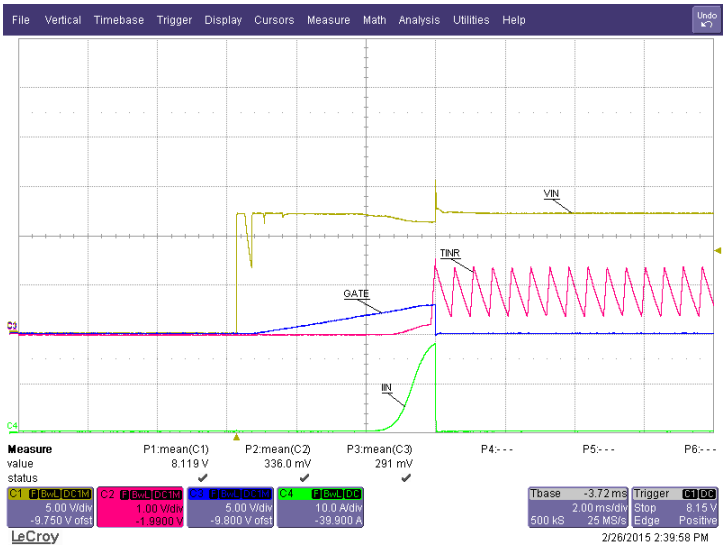


Figure 34. Start-up Into Short

10.2.5.3.1.4 Choose Fault Timer

To pass the load transient, a target fault time ($T_{FLT,TGT}$) of 250ms is used. $C_{FLT,CLC}$ is computed as follows:

$$C_{FLT,CLC} = 7.59\ \mu F/s \times T_{FLT,TGT} = 7.59\ \mu F/s \times 250\ ms = 1898\ nF \quad (65)$$

The next largest available C_{FLT} is chosen as 2.2µF, which results in a TFLT of 290ms as shown below.

$$T_{FLT} = \frac{C_{FLT}}{7.59\ \mu F/s} = \frac{2.2\ \mu F}{7.59\ \mu F/s} = 290\ ms \quad (66)$$

10.2.5.3.1.5 Choose Under Voltage and Over Voltage Settings

For this design example 10V and 14V were chosen as the limits to allow some margin for the 10.8V to 13.2V input bus. These are identical to the previous design example. See Choose Under Voltage and Over Voltage Settings section for programming these thresholds.

10.2.5.3.1.6 Selecting C_{IN} and C_{OUT}

It is recommended to add ceramic bypass capacitors to help stabilize the voltages on the input and output. Since C_{IN} will be charged directly on hot-plug, it's value should be kept small. 0.1µF is a good target. Since C_{OUT} doesn't get charged during hot-plug, a larger value such as 1 µF could be used.

10.2.5.3.1.7 Selecting D1 and D2

During hot plug and hot short events there could be significant transients on the input and output of the Hot Swap that could cause operation outside of the IC specifications. To ensure reliable operation a TVS on the input and a Schottkey diode on the output are recommended. In this example a SMDJ14A and MBRS330T3G are used.

10.2.5.3.1.8 Adding C_{ENHS}

When the ENHS pulled below its threshold and raised back up the IC will reset. Note that during a hot short the input voltage can easily droop below the UV threshold and cycle the ENHS pin. For the TPS24770 and TPS24771 ICs this will not change the behavior. However, when using the TPS24772 the cycling of the ENHS will result in the IC attempting to restart, which is undesired (this is the main reason why someone would use the TPS24772). To avoid this behavior a capacitor should be added to the ENHS to provide filtering. 33 nF was chosen for this example.

10.2.5.3.1.9 Stability Considerations

Since there is a 100nF C_{DVDT} attached to HGATE, this significantly increases the effective capacitance of HGATE and guarantees stability for this application.

10.2.5.4 Application Curves

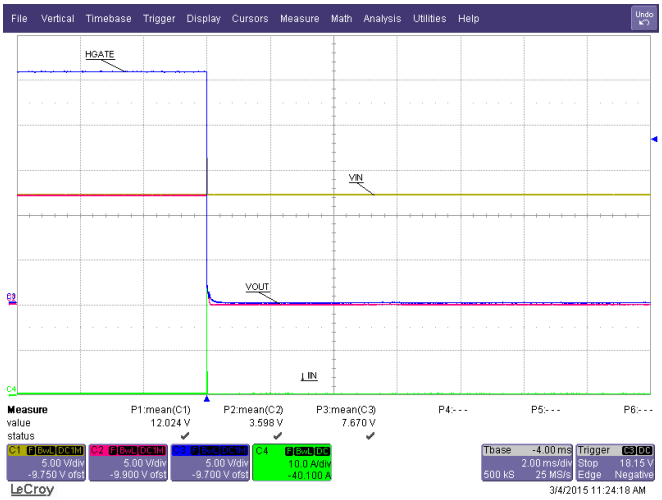


Figure 35. No Load then Hot Short (Zoomed Out)

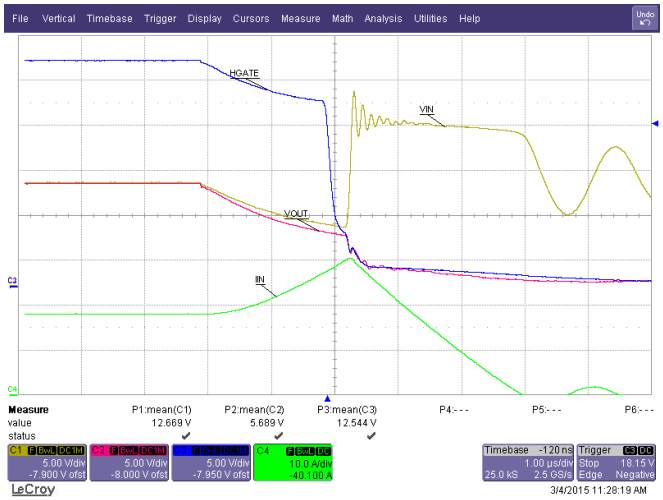


Figure 36. Full Load then Hot Short (Zoomed In)

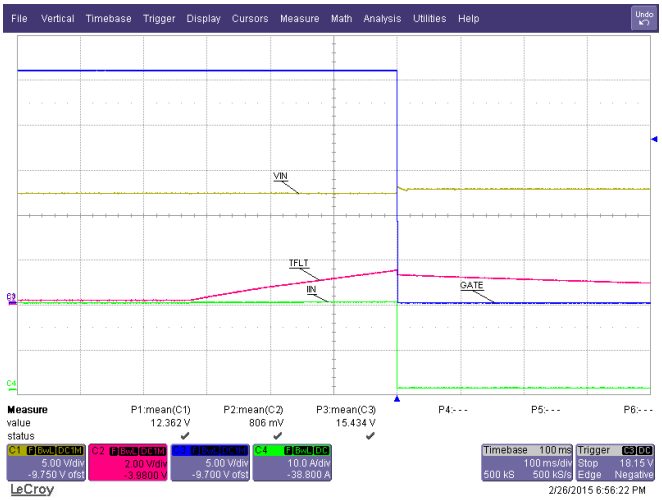


Figure 37. Overcurrent

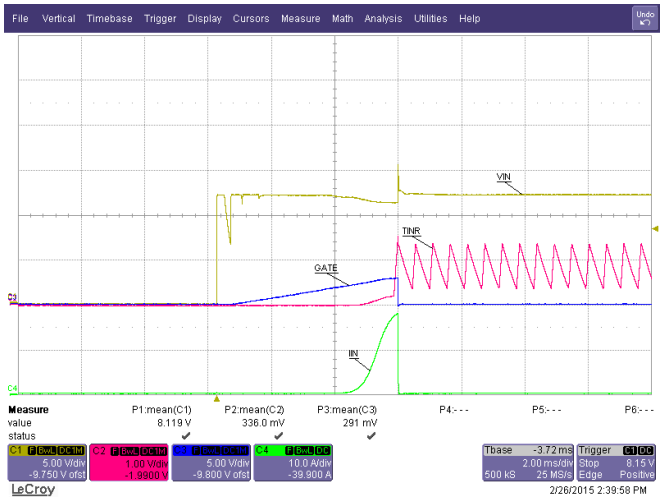


Figure 38. Start Up into Short

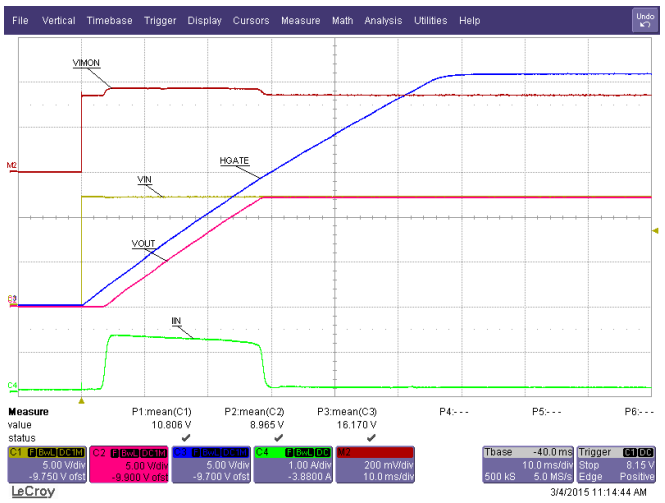


Figure 39. Start up (C_{OUT} = 2500 µF)

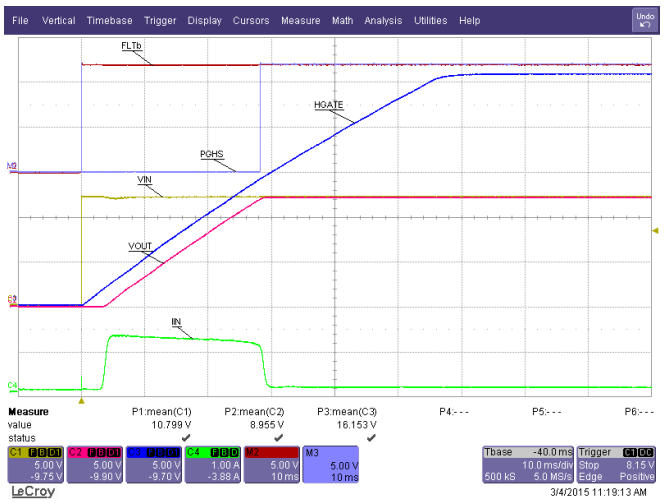


Figure 40. Start up showing PGHS and FLTb (C_{OUT} = 2500 µF)

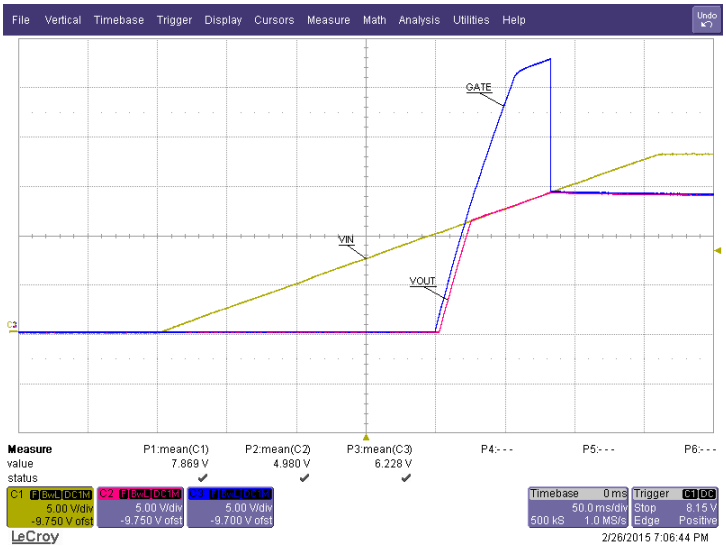


Figure 41. Under Voltage and Over Voltage with V_{IN} Rising

10.2.6 240 VA Application Using CSD17573Q5B

This design example has identical requirements to the previous one, but the CSD17573Q5B is used instead of the CSD16415Q5B. The CSD17573Q5B is cheaper and offers better R_{DSON}, but its SOA is not as good. Thus it was necessary to add Q_2 and R_{SET2} to reduce the stress during a start up into a short circuit. Given that Q_2 is a small signal PFET that is cheap, the overall BOM cost of this solution should be cheaper than the previous one. See the TPS24770 Design Calculator to help with these calculations.

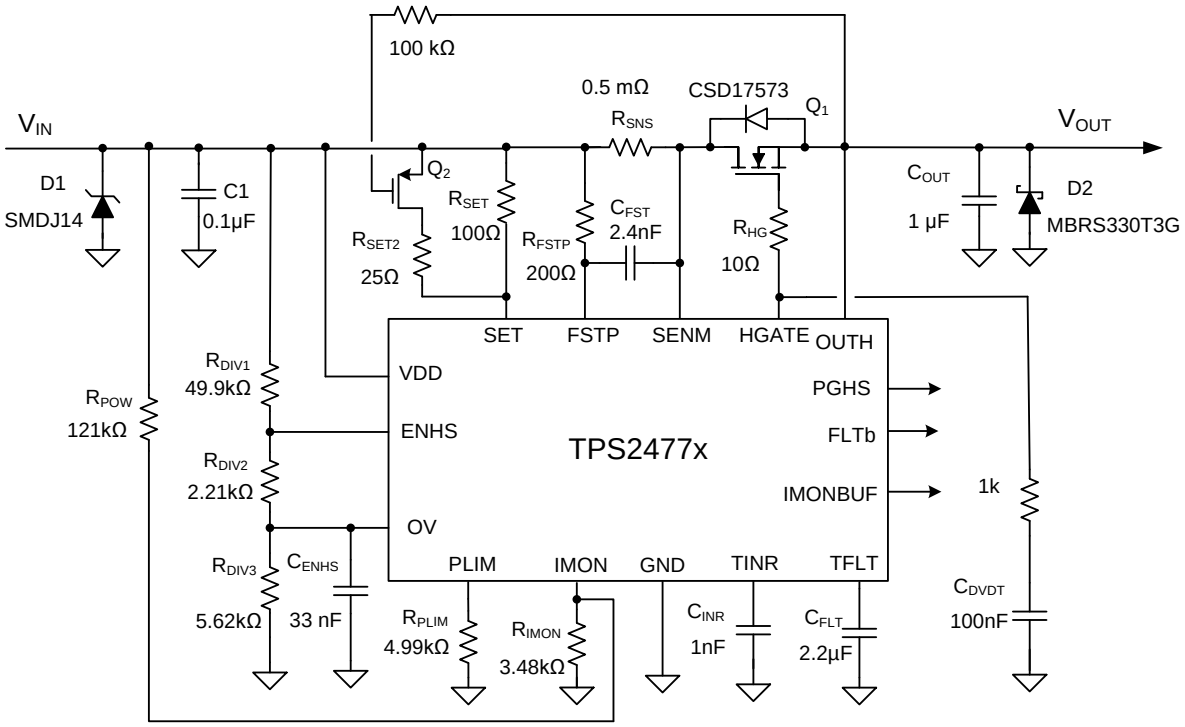


Figure 42. 240 VA Design Using CSD17573Q5B

10.2.6.1 Design Requirements

The following table summarizes the requirements for this design.

Table 5. Design Requirements for the 240 VA Design Using CSD17573Q5B

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	10.8 V – 13.2 V
Output Power Limit (VA limiting)	240 W
Maximum Output Capacitance of the Hot Swap	2500 µF
Maximum Ambient Temperature	55°C
MOSFET $R_{\theta CA}$ (function of layout)	35°C/W
Transient load requirement?	POUT is allowed to surpass 240W for <250 ms
Pass “Hot-Short” on Output?	Yes
Pass a “Start into short”?	Yes
Is the load off until PG is asserted?	Yes
IC used	TPS24772
Analog Current Monitor Used	No
MOSFET	CSD17573Q5B
Can a Hot Board be plugged in or Power Cycled?	Yes

10.2.6.1.1 Choosing C_1, C_{OUT}, C_{FLT}, C_{ENHS}, D_1, D_2, R_{SET}, R_{POW}, R_{IMON}, R_{SNS}, C_{DVDT}, R_{PLIM}, and UV/OV Thresholds

These components and settings are chosen in the same fashion as the previous design example. See 240 VA Application Using CSD16415Q5B.

10.2.6.1.2 Selecting the Hot Swap FET(s)

It is critical to select the correct MOSFET for a Hot Swap design. The device must meet the following requirements:

- The V_{DS} rating should be sufficient to handle the maximum system voltage along with any ringing caused by transients. For most 12V systems a 25 V or 30V FET is a good choice.
- The SOA of the FET should be sufficient to handle all usage cases: start-up, hot-short, start into short.
- R_{DSON} should be sufficiently low to maintain the junction and case temperature below the maximum rating of the FET. In fact, it is recommended to keep the steady state FET temperature below 125°C to allow margin to handle transients.
- Maximum continuous current rating should be above the maximum load current and the pulsed drain current must be greater than the current threshold of the circuit breaker. Most MOSFETs that pass the first three requirements will also pass these two.
- A V_{GS} rating of +16 V is required, because the TPS2477x can pull up the gate as high as 15.5 V above source.

For this design the CSD17573Q5B was selected for its low R_{DSON} and great cost point. After selecting the MOSFET, the maximum steady state case temperature can be computed as follows:

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times I^2_{LOAD,MAX} \times \frac{R_{DSON}(T_J)}{n^2} \quad (67)$$

In the equation above n is the number of FETs used in parallel. Note that the R_{DSON} is a strong function of junction temperature, which for most MOSFETS will be very close to the case temperature. A few iterations of the above equations may be necessary to converge on the final R_{DSON} and $T_{C,MAX}$ value. According to the CSD17573Q5B datasheet, its R_{DSON} is about 1.2 x greater at 65°C compared to room temperature. The equation below uses this R_{DSON} value to compute the $T_{C,MAX}$. Note that the computed $T_{C,MAX}$ is close to the junction temperature assumed for R_{DSON}. Thus no further iterations are necessary.

$$T_{C,MAX} = 55°C + 35° \frac{C}{W} \times (20\ A)^2 \times (1.2 \times 0.84\ m\Omega) = 69°C \quad (68)$$

10.2.6.1.3 Keeping the MOSFET within SOA

As in the previous example, it is important to ensure that the MOSFET stays within its SOA during both regular start-up and start-up into short.

First consider the regular start-up. The same C_{DVDT} is used as the last example so the FET is required to handle 18.2W (or 1.38A and 13.2V) for 12.3 ms. Based on the SOA curve of the CSD17573Q55B, at V_{DS} of 13.2 V it can handle 4.5 A for 10 ms or 2 A for 100 ms. Using the same method as the previous design example, it can be inferred that the MOSFET can handle 4.2 A for 12.3 ms when V_{DS}=13.2 V.

The SOA of a MOSFET is specified at a case temperature of 25°C, while the case temperature can be hotter during a start into a short. It is important to understand the hottest temperature that a MOSFET can be during a start-up ($T_{C,\ MAX,\ START}$). If a board has been off for a while and then it's turned on $T_{A,\ MAX}$ is a good estimate for $T_{C,MAX,\ START}$. However, if a board is on and then gets power cycled $T_{C,MAX}$ should be used for $T_{C,MAX,START}$. This will depend on system requirements. For this design example, it's assumed that a hot board can be power cycled or hot plugged and $T_{C,MAX}$ is used to estimate $T_{C,MAX,START}$.

$$I_{SOA}\left(12.3\ ms, T_{C,MAX,START}\right) = I_{SOA}\left(12.3\ ms, 25°C\right) \times \frac{T_{J,ABSMAX} - T_{C,MAX,START}}{T_{J,ABSMAX} - 25°C}$$

$$= 4.2\ A \times \frac{150°C - 69°C}{150°C - 25°C} = 2.7\ A \tag{69}$$

Based on this calculation the MOSFET can handle 2.7 A, 13.2 V for 12.3 ms at 69°C elevated case temperature, but is only required to handle 1.38 A. Thus there is sufficient margin to make this a robust design. Again a 1.3x margin is recommended to cover for variations.

Next, consider the start into short condition. Similar to the previous design the MOSFET would need to handle 20A and 13.2 V for ~1ms. Checking the SOA curve of the CSD17573Q5B, it can only handle 10A and 13.2 V for 1ms, so it's SOA is clearly not sufficient.

This is where Q_2 and R_{SET2} come in. They serve to reduce the current limit during starting up ($I_{LIM,START}$) while the V_{DS} of the Hot Swap MOSFET is above V_T of Q_2 (1V to 2V). The ratio of I_{LIM} to $I_{LIM,START}$, denoted as I_{RATIO}, is a function of R_{SET} and R_{SET2} as shown below. For this example a ratio of 0.2 ($I_{LIM,START}$=4A) was targeted to reduce MOSFET stress, keep the current limit above I_{INR}, and ensure sufficient signal on V_{SNS} to keep the error reasonable. Once $_{IRATIO}$ is chosen, R_{SET2} is computed to be 25 Ω as shown below.

$$I_{RATIO} = \frac{I_{LIM,START}}{I_{LIM}} = \frac{R_{SET}\ //\ R_{SET2}}{R_{SET}} \tag{70}$$

$$R_{SET2} = R_{SET} \times \frac{I_{RATIO}}{1 - I_{RATIO}} = 100\ \Omega \times \frac{0.2}{1 - 0.2} = 25\ \Omega \tag{71}$$

The start-up into short (with R_{SET2} and Q_2) is shown in Figure 43 below. The equivalent power pulse is now 4A for ~0.5ms. The MOSFET can handle 10A, 13.2 V for 1ms, which can be derated to 6.5 A when accounting for elevated case temperature. Since the MOSFET is only required to handle 4A for 0.5ms there is plenty of margin in the design.

$$I_{SOA}\left(1\ ms, T_{C,MAX,START}\right) = I_{SOA}\left(1\ ms, 25°C\right) \times \frac{T_{J,ABSMAX} - T_{C,MAX,START}}{T_{J,ABSMAX} - 25°C}$$

$$= 10\ A \times \frac{150°C - 69°C}{150°C - 25°C} = 6.5\ A \tag{72}$$

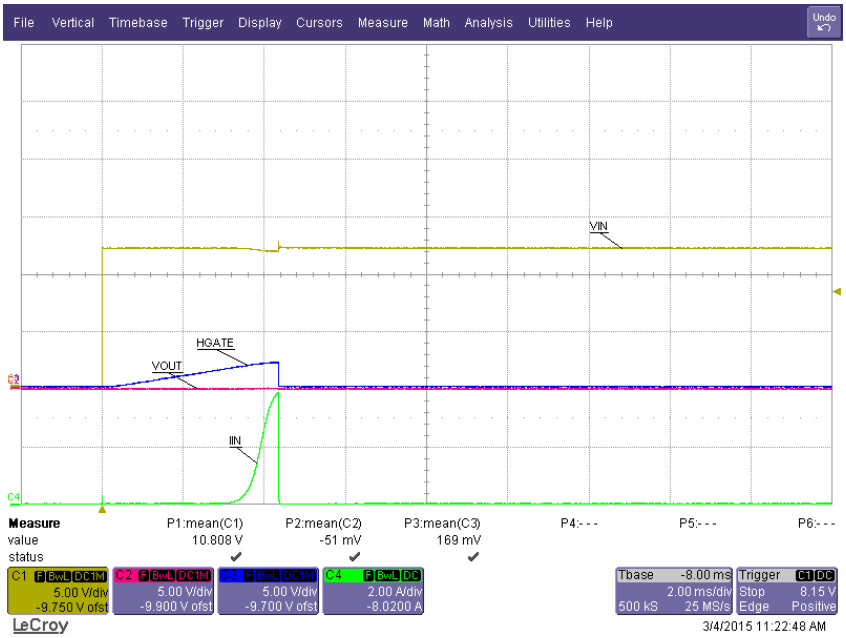


Figure 43. Start-up Into Short (with R_{SET} and Q_2)

10.2.6.2 Q2 Selection

There is a lot of flexibility when selecting Q_2. Any PMOS with a ±20V V_{GS} rating and 20V of V_{DS} rating is sufficient. For this example IRLML5203PbF was used. Note that the 100k series resistor along with the C_{ISS} of Q2 (~500pF) for a filter with a 50 µs time constant. This protects Q_2 in case there is high frequency ringing on V_{IN} that causes $V_{IN} - V_{OUT}$ to exceed 20V. This will usually happened during hot-plug or hot-short.

10.2.6.3 Application Curves

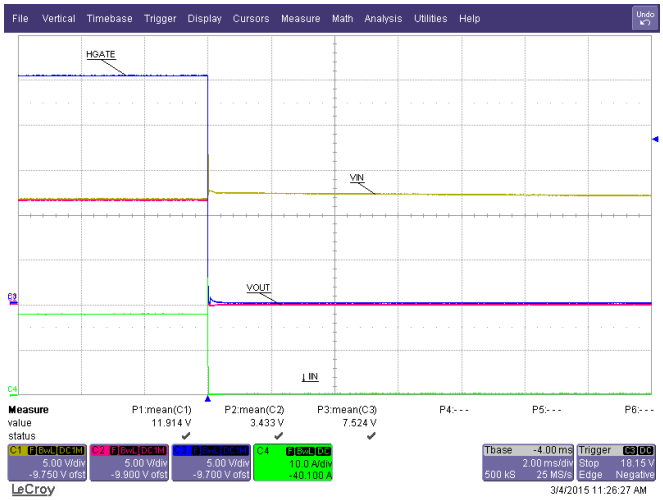


Figure 44. Full Load then Hot Short (Zoomed Out)

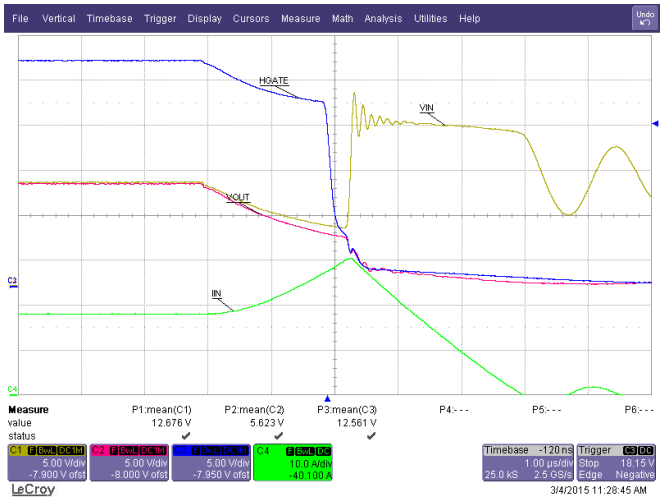


Figure 45. Full Load then Hot Short (Zoomed In)

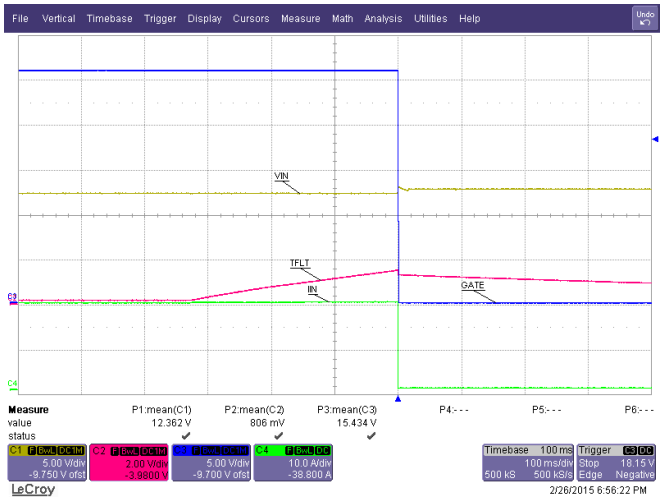


Figure 46. Over Current

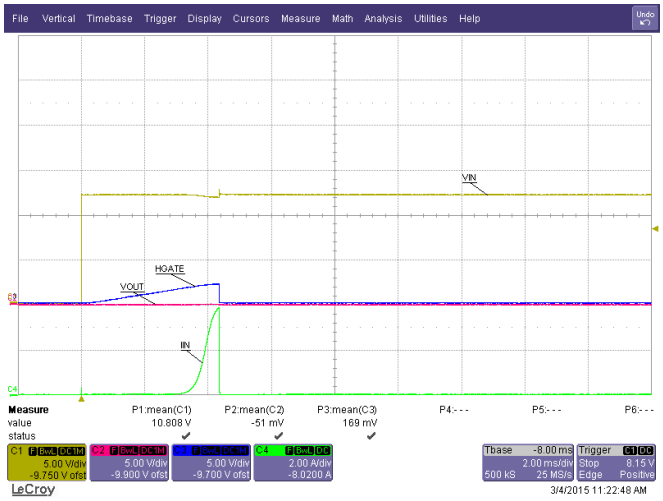


Figure 47. Start Up Into Short

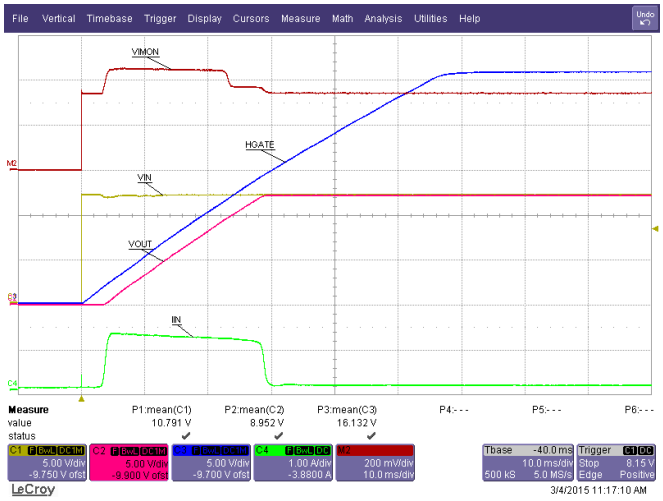


Figure 48. Start up (C_{OUT} = 2500 µF)

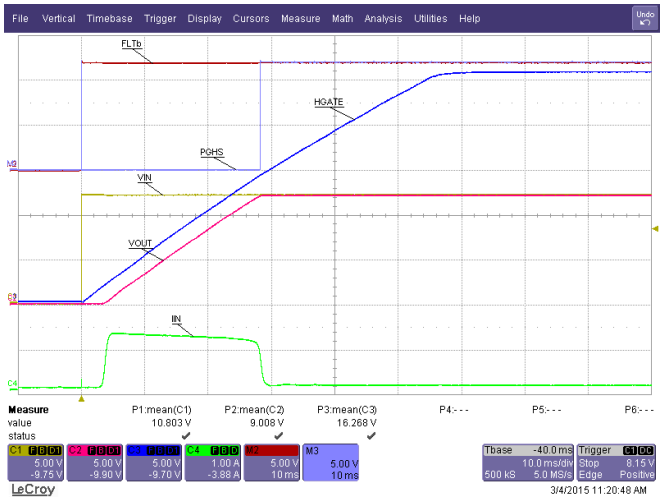


Figure 49. Start up showing PGHS and FLTb (C_{OUT} = 2500 µF)

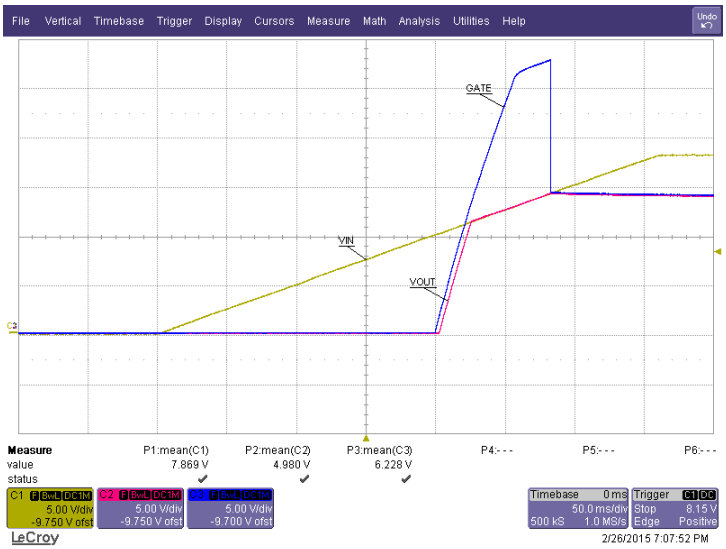


Figure 50.

11 Power Supply Recommendations

In general, operation is best when the input supply isn't noisy and doesn't have significant transients. For noisier environments filtering on input, output, and fast trip should be adjusted to avoid nuisance trips.

12 Layout

12.1 Layout Guidelines

When doing the layout of the TPS2477x the following are considered best practice.

- Ensure proper Kelvin Sense of R_{SNS}.
- Keep the filtering capacitor C_{FSTP} as close to the IC as possible.
- Place a Shottky diode and a ceramic bypass capacitor close to the source of the Hot Swap MOSFET
- Do not connect VDD to the Kelvin Sense trace for SET and FSTP
- Note that special care must be taken when placing the bypass capacitor for the VDD pin. During Hot Shorts, there is a very large dv/dt on input voltage during the MOSFET turn off. If the bypass capacitor is placed right next to the pin and the trace from R_{SNS} to the pin is long, an LC filter is formed. As a result a large differential voltage can develop between VDD and SENM if there is a large transient on Vin. This could result in a violation of the abs max rating from VDD to SENM. To avoid this, place the bypass capacitor close to RSNS instead of the VDD pin.

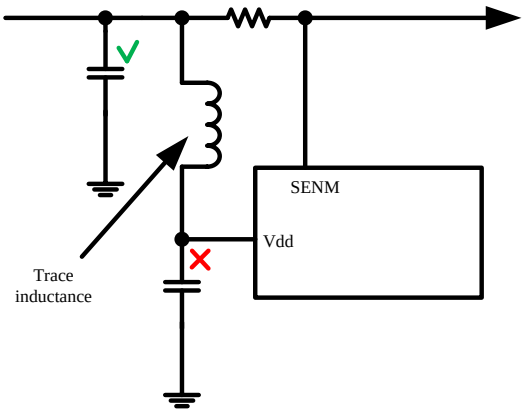


Figure 51. Layout Don't

- When using parallel resistors the layout becomes even more critical. Due to PCB parasitics, the current through each R_{SNS} may be different, which results in different sense voltages across the two resistors. It's important to average these in order to get a proper current measurement. This can be accomplished by forming a resistor divider with the traces. As long as Dis1 = Dis2, the final V_{SNS} will be an average of the drop across the two resistors.

Layout Guidelines (continued)

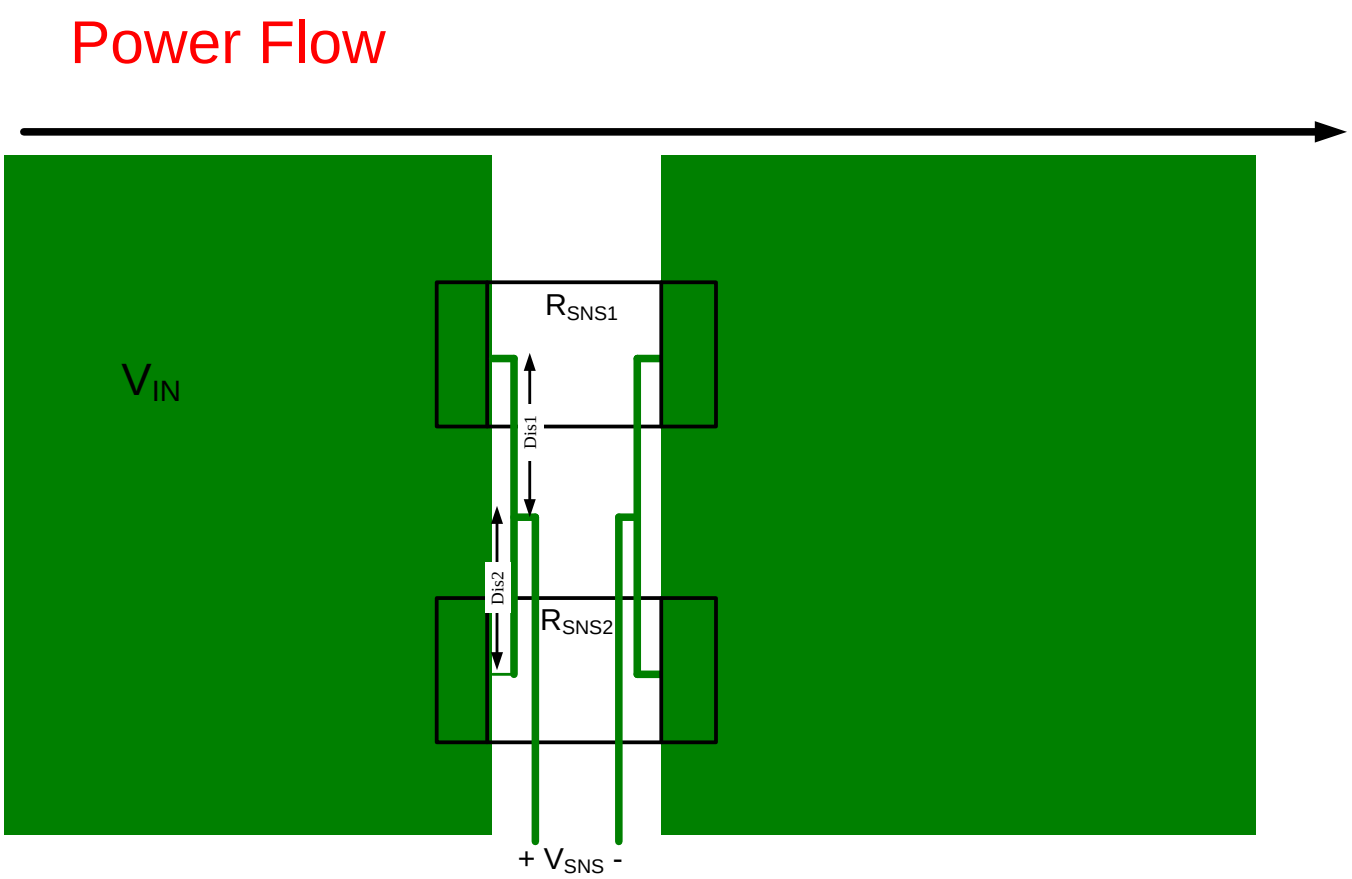
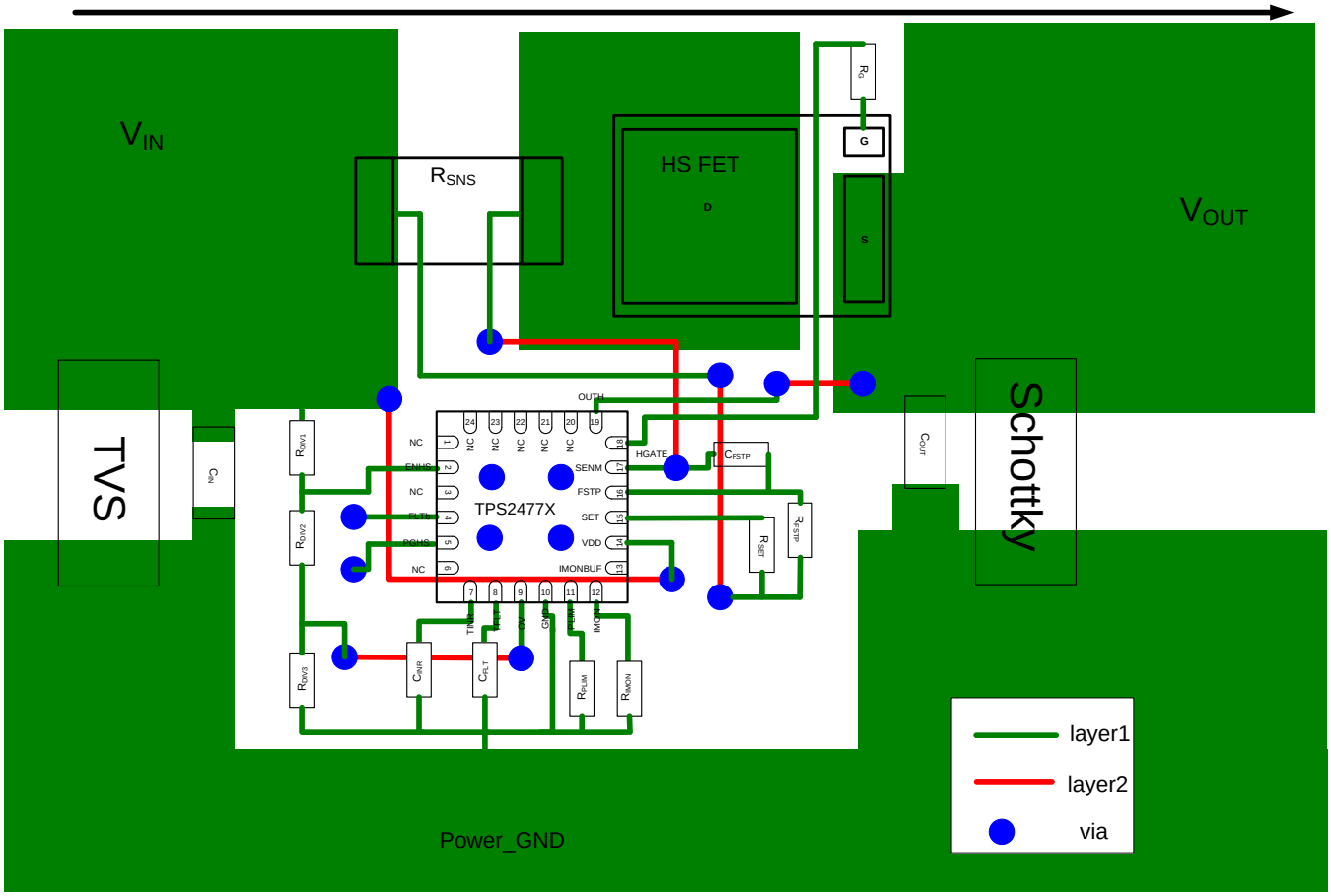


Figure 52. Sense Layout with 2 R_{SNS}

12.2 Layout Example



13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS24770	Click here	Click here	Click here	Click here	Click here
TPS24771	Click here	Click here	Click here	Click here	Click here
TPS24772	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS24770RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24770	Samples
TPS24770RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24770	Samples
TPS24771RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24771	Samples
TPS24771RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24771	Samples
TPS24772RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24772	Samples
TPS24772RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 24772	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

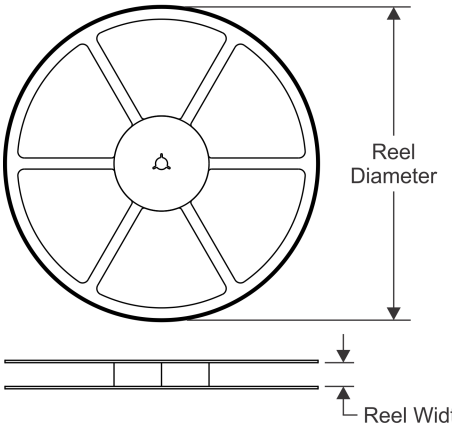
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

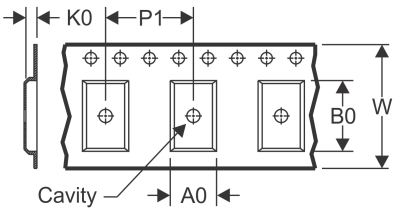
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

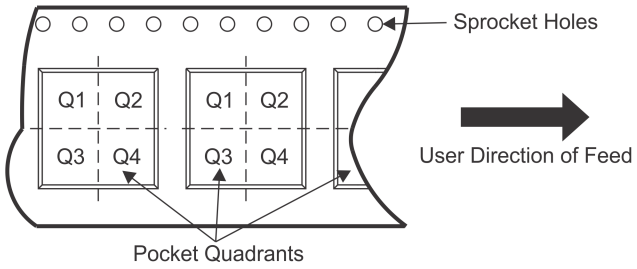


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

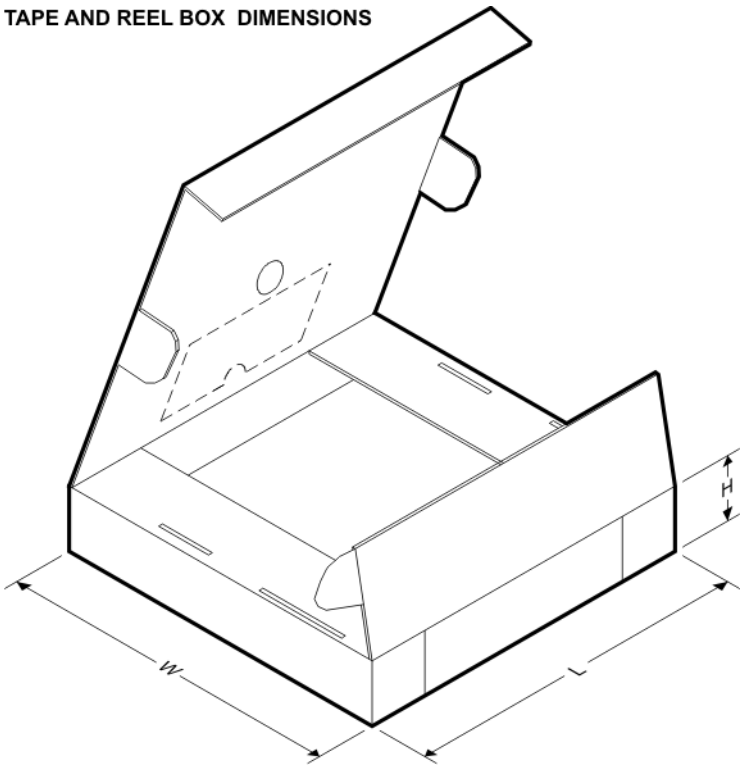
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24770RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24770RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24771RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24771RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24772RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS24772RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

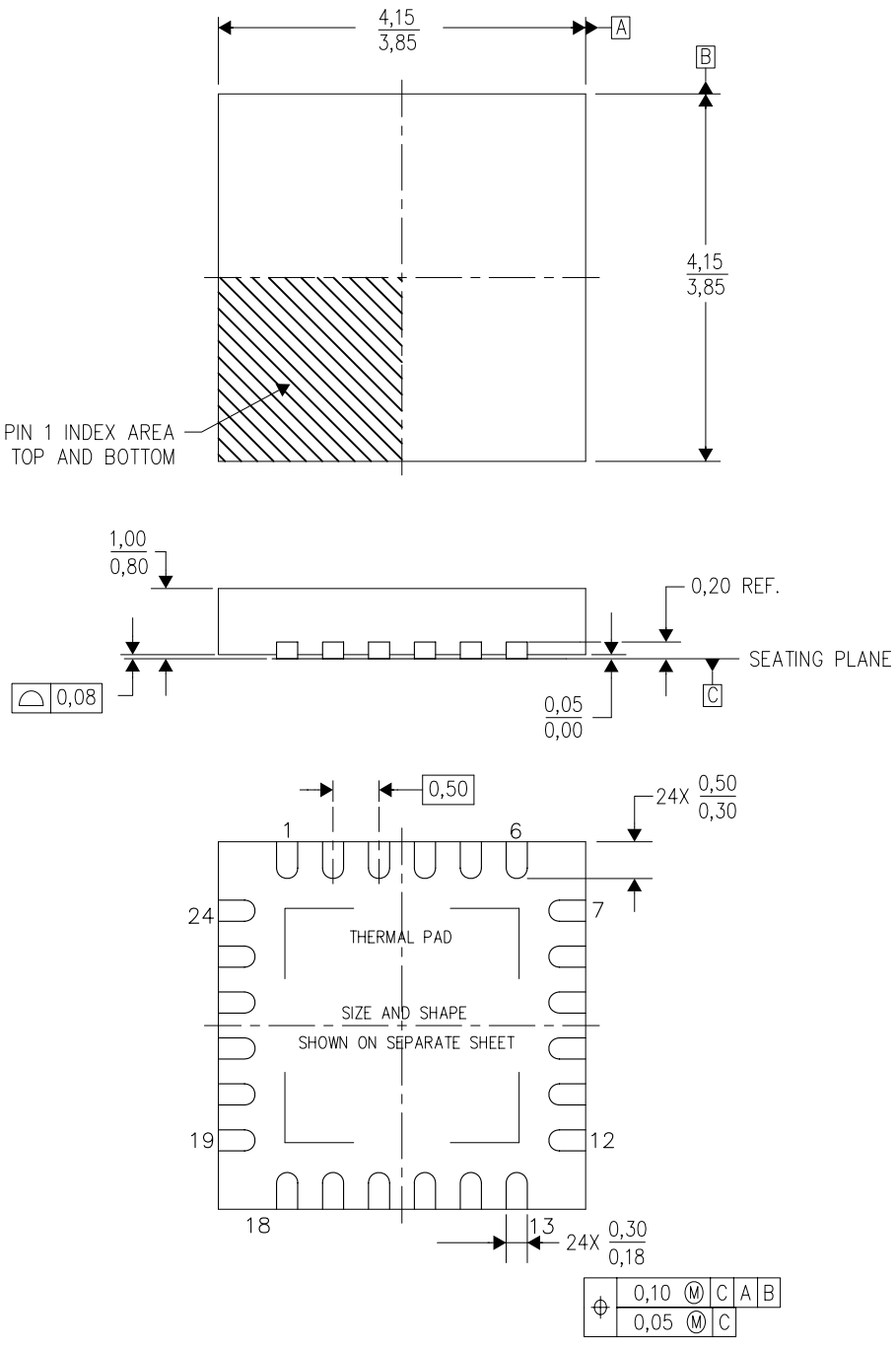
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24770RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24770RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24771RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24771RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS24772RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS24772RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

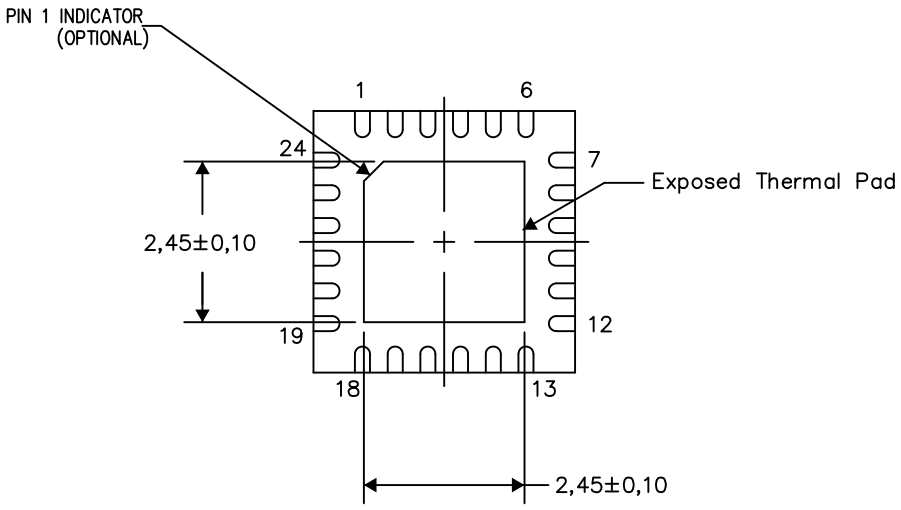
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



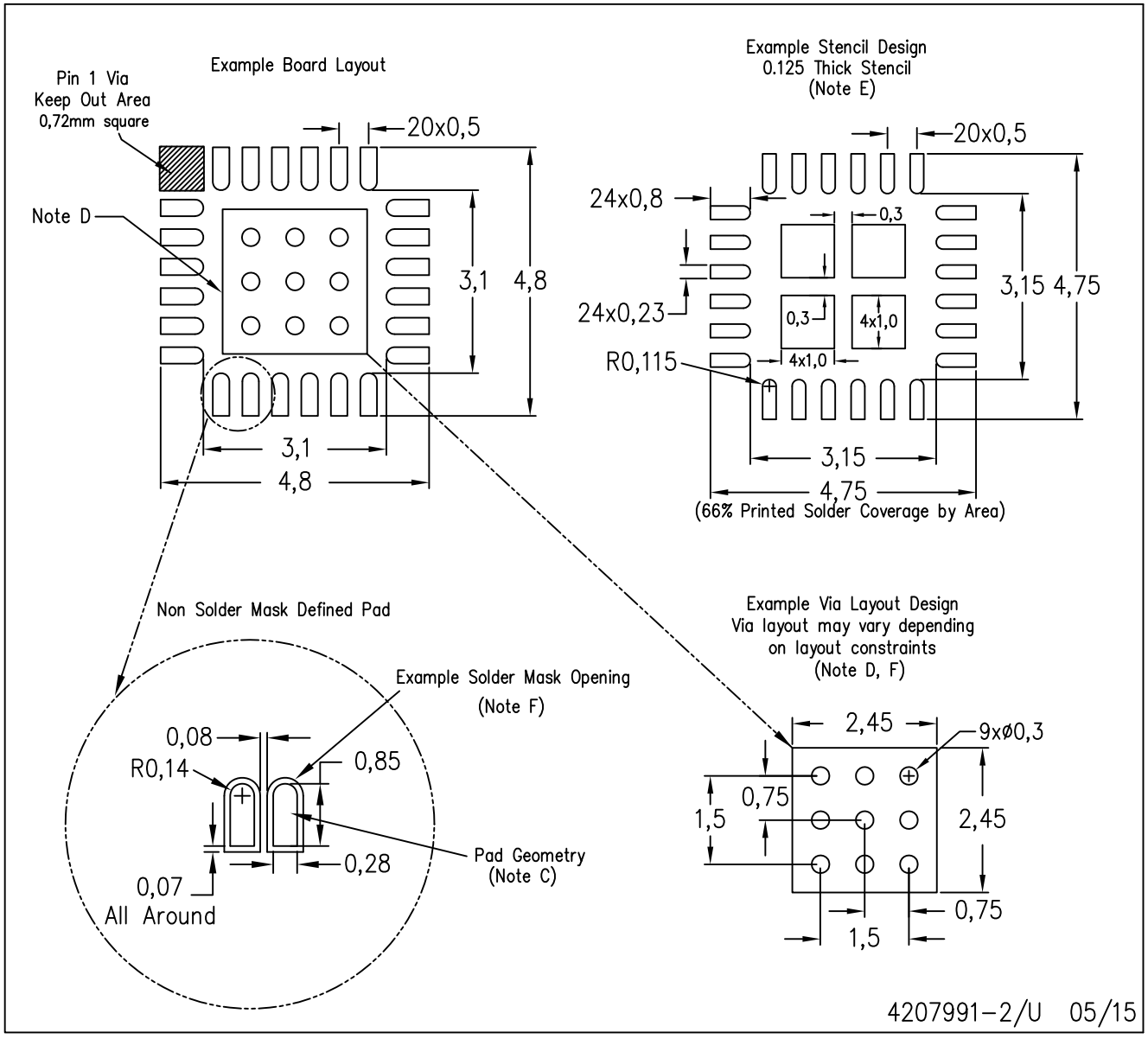
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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