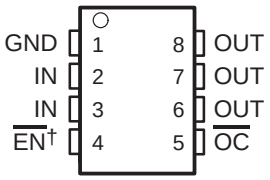
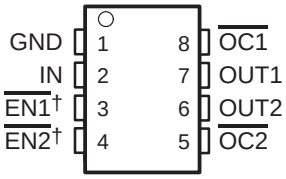
- **80-mΩ High-Side MOSFET Switch**
- **500 mA Continuous Current Per Channel**
- **Independent Thermal and Short-Circuit Protection With Overcurrent Logic Output**
- **Operating Range . . . 2.7 V to 5.5 V**
- **CMOS- and TTL-Compatible Enable Inputs**
- **2.5-ms Typical Rise Time**
- **Undervoltage Lockout**
- **10 μA Maximum Standby Supply Current for Single and Dual (20 μA for Triple and Quad)**
- **Bidirectional Switch**
- **Ambient Temperature Range, 0°C to 85°C**
- **ESD Protection**
- **UL Listed – File No. E169910**

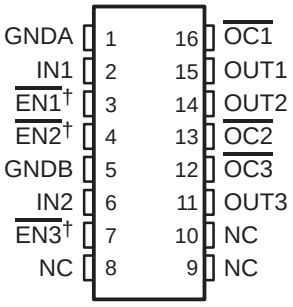
TPS2041A, TPS2051A
D PACKAGE
(TOP VIEW)



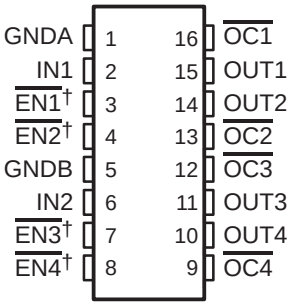
TPS2042A, TPS2052A
D PACKAGE
(TOP VIEW)



TPS2043A, TPS2053A
D PACKAGE
(TOP VIEW)



TPS2044A, TPS2054A
D PACKAGE
(TOP VIEW)



† All enable inputs are active high for the TPS205xA series.
NC – No connect

description

The TPS2041A through TPS2044A and TPS2051A through TPS2054A power-distribution switches are intended for applications where heavy capacitive loads and short circuits are likely to be encountered. These devices incorporate 80-mΩ N-channel MOSFET high-side power switches for power-distribution systems that require multiple power switches in a single package. Each switch is controlled by an independent logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

When the output load exceeds the current-limit threshold or a short is present, these devices limit the output current to a safe level by switching into a constant-current mode, pulling the overcurrent ($\overline{OCx}$) logic output low. When continuous heavy overloads and short circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures the switch remains off until valid input voltage is present. These power-distribution switches are designed to current limit at 0.9 A.

GENERAL SWITCH CATALOG

33 mΩ, single			**80 mΩ, dual**			**80 mΩ, dual**	**80 mΩ, triple**	**80 mΩ, quad**	**80 mΩ, quad**
	TPS201xA	0.2 A – 2 A		TPS2042	500 mA				
	TPS202x	**0.2 A – 2 A**		TPS2052	500 mA				
	TPS203x	0.2 A – 2 A		TPS2046	250 mA				
				TPS2056	250 mA				
80 mΩ, single	TPS2014	600 mA	**260 mΩ**	TPS2100/1		TPS2080 500 mA	TPS2043 500 mA	TPS2044 500 mA	TPS2085 500 mA
	TPS2015	1 A	IN1	IN1	500 mA	TPS2081 500 mA	TPS2053 500 mA	TPS2054 500 mA	TPS2086 500 mA
	TPS2041	500 mA	IN2 OUT	IN2	10 mA	TPS2082 500 mA	TPS2047 250 mA	TPS2048 250 mA	TPS2087 500 mA
	TPS2051	500 mA		TPS2102/3/4/5		TPS2090 250 mA	TPS2057 250 mA	TPS2058 250 mA	TPS2095 250 mA
	TPS2045	250 mA	**1.3 Ω**	IN1	500 mA	TPS2091 250 mA			TPS2096 250 mA
	TPS2055	250 mA		IN2	100 mA	TPS2092 250 mA			TPS2097 250 mA

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

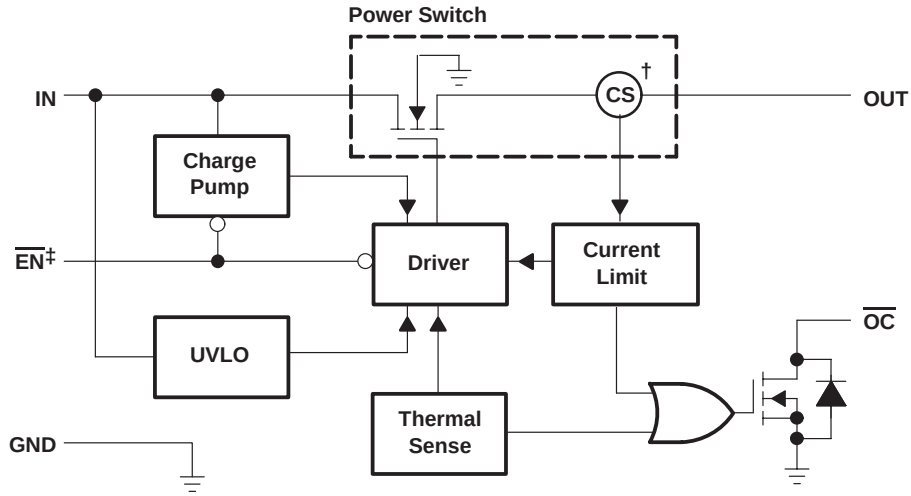
AVAILABLE OPTIONS

T_A	ENABLE	RECOMMENDED MAXIMUM CONTINUOUS LOAD CURRENT (A)	TYPICAL SHORT-CIRCUIT CURRENT LIMIT AT 25°C (A)	NUMBER OF SWITCHES	PACKAGED DEVICES
					SOIC (D)†
0°C to 85°C	Active low	0.5	0.9	Single	TPS2041AD
	Active high				TPS2051AD
	Active low			Dual	TPS2042AD
	Active high				TPS2052AD
	Active low			Triple	TPS2043AD
	Active high				TPS2053AD
	Active low			Quad	TPS2044AD
	Active high				TPS2054AD

† The D package is available taped and reeled. Add an R suffix to device type (e.g., TPS2041ADR)

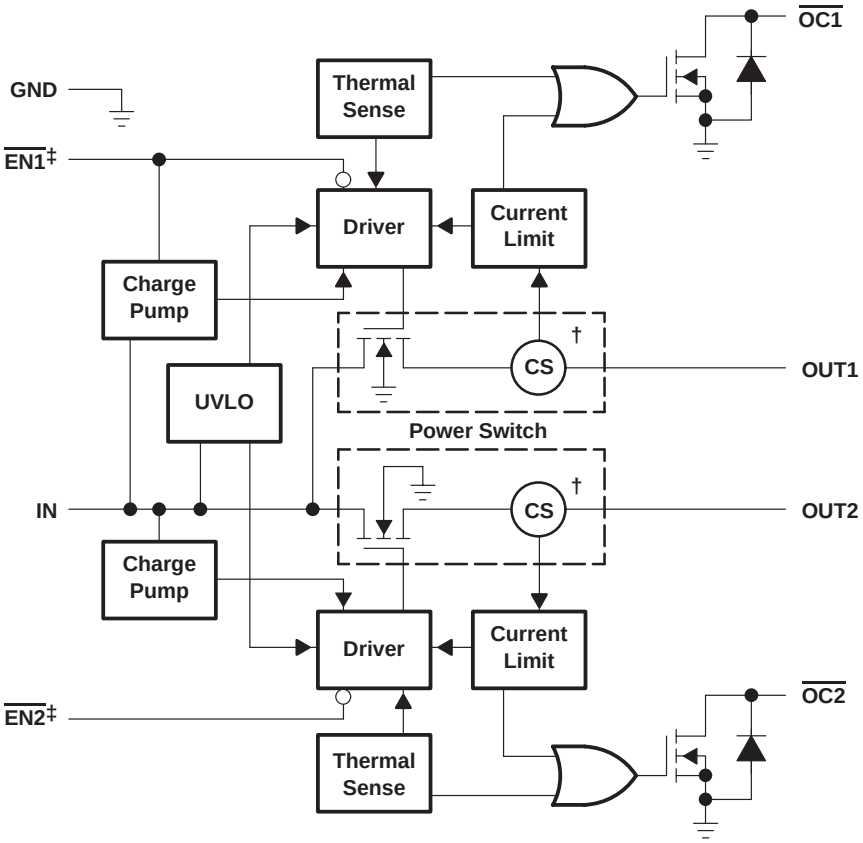
functional block diagrams

TPS2041A



† Current sense
‡ Active high for TPS205xA series

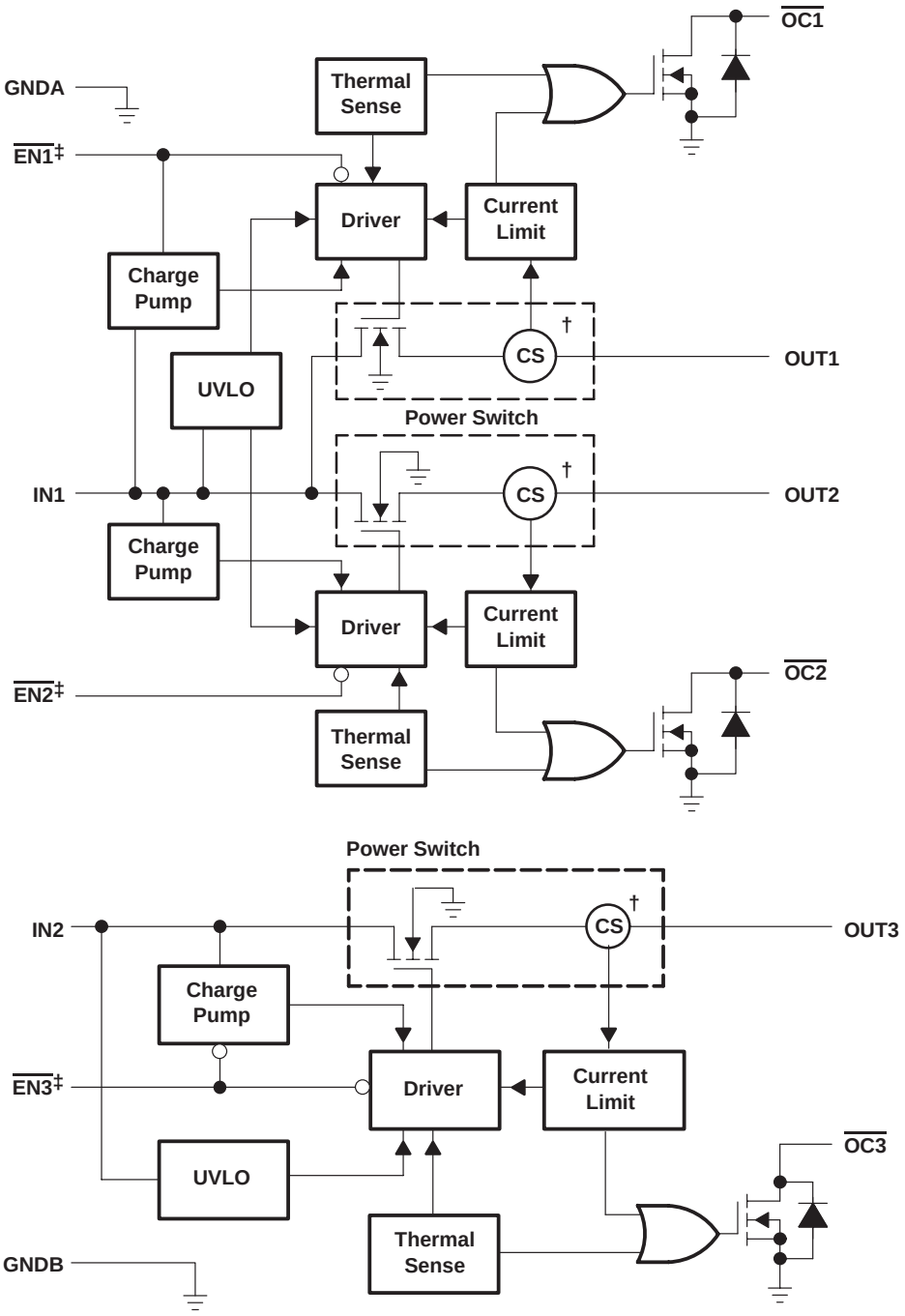
TPS2042A



† Current sense
‡ Active high for TPS205xA series

functional block diagrams

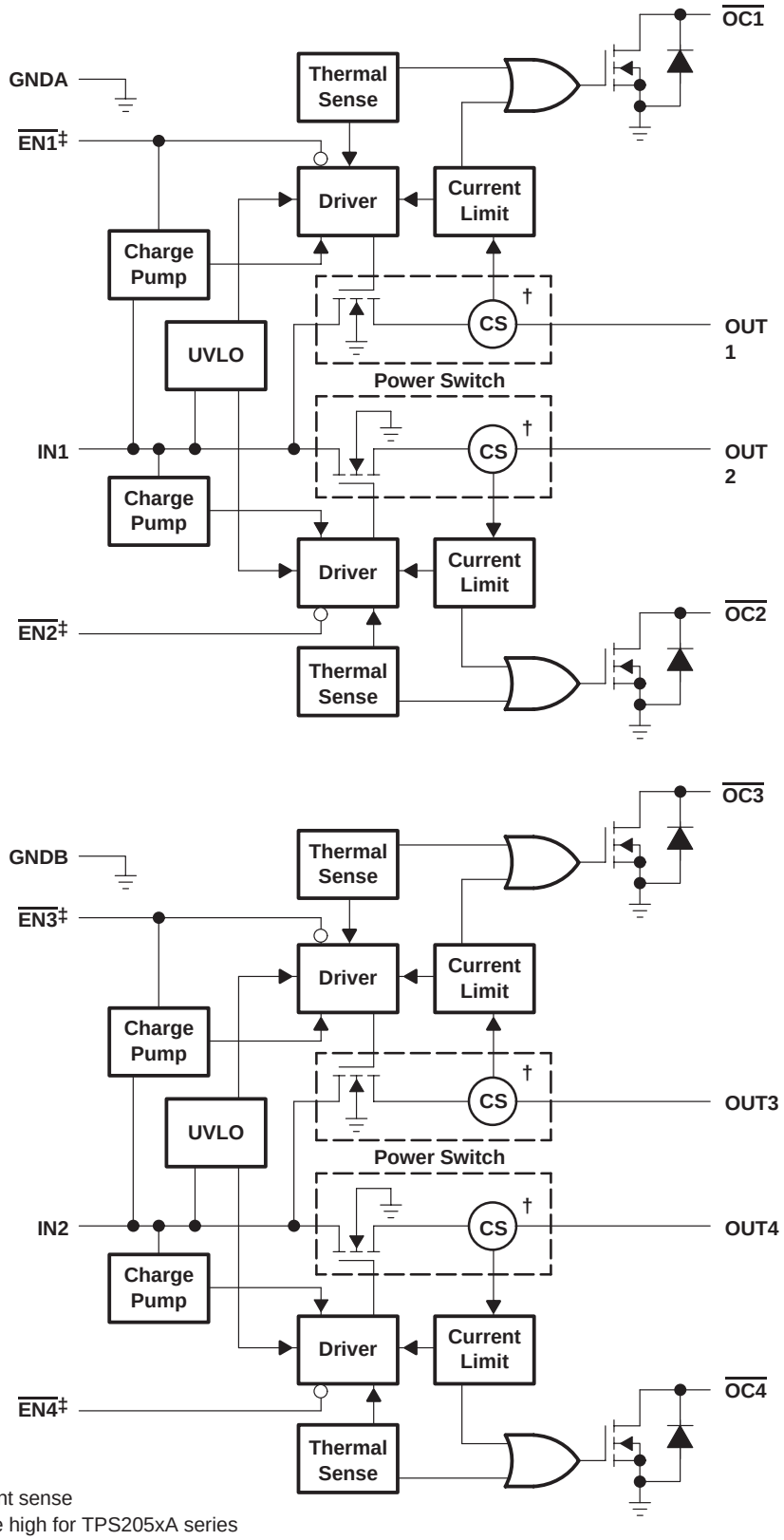
TPS2043A



† Current sense
‡ Active high for TPS205xA series

functional block diagrams

TPS2044A



† Current sense
‡ Active high for TPS205xA series

Terminal Functions

TPS2041A and TPS2051A

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2041A	TPS2051A		
$\overline{EN}$	4	–	I	Enable input. Logic low turns on power switch.
EN	–	4	I	Enable input. Logic high turns on power switch.
GND	1	1	I	Ground
IN	2, 3	2, 3	I	Input voltage
$\overline{OC}$	5	5	O	Overcurrent. Logic output active low
OUT	6, 7, 8	6, 7, 8	O	Power-switch output

TPS2042A and TPS2052A

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2042A	TPS2052A		
$\overline{EN1}$	3	–	I	Enable input. Logic low turns on power switch, IN-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN-OUT2.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN-OUT2.
GND	1	1	I	Ground
IN	2	2	I	Input voltage
$\overline{OC1}$	8	8	O	Overcurrent. Logic output active low, for power switch, IN-OUT1
$\overline{OC2}$	5	5	O	Overcurrent. Logic output active low, for power switch, IN-OUT2
OUT1	7	7	O	Power-switch output
OUT2	6	6	O	Power-switch output

Terminal Functions (Continued)

TPS2043A and TPS2053A

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2043A	TPS2053A		
$\overline{EN1}$	3	–	I	Enable input, logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input, logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input, logic low turns on power switch, IN2-OUT3.
EN1	–	3	I	Enable input, logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input, logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input, logic high turns on power switch, IN2-OUT3.
GNDA	1	1		Ground for IN1 switch and circuitry.
GNDB	5	5		Ground for IN2 switch and circuitry.
IN1	2	2	I	Input voltage
IN2	6	6	I	Input voltage
$\overline{NC}$	8, 9, 10	8, 9, 10		No connection
$\overline{OC1}$	16	16	O	Overcurrent, logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent, logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent, logic output active low, IN2-OUT3
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3

TPS2044A and TPS2054A

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	TPS2044A	TPS2054A		
$\overline{EN1}$	3	–	I	Enable input. logic low turns on power switch, IN1-OUT1.
$\overline{EN2}$	4	–	I	Enable input. Logic low turns on power switch, IN1-OUT2.
$\overline{EN3}$	7	–	I	Enable input. Logic low turns on power switch, IN2-OUT3.
$\overline{EN4}$	8	–	I	Enable input. Logic low turns on power switch, IN2-OUT4.
EN1	–	3	I	Enable input. Logic high turns on power switch, IN1-OUT1.
EN2	–	4	I	Enable input. Logic high turns on power switch, IN1-OUT2.
EN3	–	7	I	Enable input. Logic high turns on power switch, IN2-OUT3.
EN4	–	8	I	Enable input. Logic high turns on power switch, IN2-OUT4.
GNDA	1	1		Ground for IN1 switch and circuitry.
GNDB	5	5		Ground for IN2 switch and circuitry.
IN1	2	2	I	Input voltage
IN2	6	6	I	Input voltage
$\overline{OC1}$	16	16	O	Overcurrent. Logic output active low, IN1-OUT1
$\overline{OC2}$	13	13	O	Overcurrent. Logic output active low, IN1-OUT2
$\overline{OC3}$	12	12	O	Overcurrent. Logic output active low, IN2-OUT3
$\overline{OC4}$	9	9	O	Overcurrent. Logic output active low, IN2-OUT4
OUT1	15	15	O	Power-switch output, IN1-OUT1
OUT2	14	14	O	Power-switch output, IN1-OUT2
OUT3	11	11	O	Power-switch output, IN2-OUT3
OUT4	10	10	O	Power-switch output, IN2-OUT4

detailed description

power switch

The power switch is an N-channel MOSFET with a maximum on-state resistance of 135 mΩ ($V_{I(IN)}$ = 5 V). Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum of 500 mA per switch.

charge pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires very little supply current.

driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage. The rise and fall times are typically in the 2-ms to 4-ms range.

enable ($\overline{\text{ENx}}$, ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 10 μA on the single and dual devices (20 μA on the triple and quad devices) when a logic high is present on $\overline{\text{ENx}}$ (TPS204xA†) or a logic low is present on ENx (TPS205xA†). A logic zero input on $\overline{\text{ENx}}$ or a logic high on ENx restores bias to the drive and control circuits and turns the power on. The enable input is compatible with both TTL and CMOS logic levels.

overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed.

current sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

thermal sense

The TPS204xA and TPS205xA implement a dual-threshold thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks to determine which power switch is in an overcurrent condition and turns off that switch, thus isolating the fault without interrupting operation of the adjacent power switch. Hysteresis is built into the thermal sense, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The ($\overline{\text{OCx}}$) open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

undervoltage lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

† Product series designations TPS204x and TPS205x refer to devices presented in this data sheet and not necessarily to other TI devices numbered in this sequence.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input voltage range, $V_{I(IN)}$ (see Note 1) . . . . . –0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ (see Note 1) . . . . . –0.3 V to $V_{I(IN)}$ + 0.3 V
Input voltage range, $V_{I(\overline{ENx})}$ or $V_{I(ENx)}$ . . . . . –0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$ . . . . . internally limited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . 0°C to 125°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Electrostatic discharge (ESD) protection: Human body model MIL-STD-883C . . . . . 2 kV
Machine model . . . . . 0.2 kV

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D–8	725 mW	5.9 mW/°C	464 mW	377 mW
D–16	1123 mW	9 mW/°C	719 mW	584 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(\overline{EN})}$ or $V_{I(EN)}$	0	5.5	V
Continuous output current, $I_{O(OUT)}$ (per switch)	0	500	mA
Operating virtual junction temperature, T_J	0	125	°C

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = $V_{I(IN)}$ (unless otherwise noted)

power switch

PARAMETER		TEST CONDITIONS†	TPS204xA			TPS205xA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation	$V_{I(IN)}$ = 5 V, I_O = 0.5 A, T_J = 25°C,		80	100		80	100	mΩ
		$V_{I(IN)}$ = 5 V, I_O = 0.5 A, T_J = 85°C,		90	120		90	120	
		$V_{I(IN)}$ = 5 V, I_O = 0.5 A, T_J = 125°C,		100	135		100	135	
	Static drain-source on-state resistance, 3.3-V operation	$V_{I(IN)}$ = 3.3 V, I_O = 0.5 A, T_J = 25°C,		90	125		90	125	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.5 A, T_J = 85°C,		110	145		110	145	
		$V_{I(IN)}$ = 3.3 V, I_O = 0.5 A, T_J = 125°C,		120	160		120	160	
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF, T_J = 25°C, R_L=10 Ω		2.5			2.5		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF, T_J = 25°C, R_L=10 Ω		3			3		
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V, C_L = 1 µF, T_J = 25°C, R_L=10 Ω		4.4			4.4		ms
		$V_{I(IN)}$ = 2.7 V, C_L = 1 µF, T_J = 25°C, R_L=10 Ω		2.5			2.5		

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

enable input $\overline{ENx}$ or ENx

PARAMETER			TEST CONDITIONS	TPS204xA			TPS205xA			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V	2			2			V
V_{IL}	Low-level input voltage		4.5 V ≤ $V_{I(IN)}$ ≤ 5.5 V			0.8			0.8	V
			2.7 V≤ $V_{I(IN)}$ ≤ 4.5 V			0.4			0.4	
I_I	Input current	TPS204xA	$V_{I(\overline{ENx})}$ = 0 V or $V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–0.5		0.5				µA
		TPS205xA	$V_{I(ENx)}$ = $V_{I(IN)}$ or $V_{I(ENx)}$ = 0 V				–0.5		0.5	
t_{on}	Turnon time		C_L = 100 µF, R_L=10 Ω			20			20	ms
t_{off}	Turnoff time		C_L = 100 µF, R_L=10 Ω			40			40	

current limit

PARAMETER		TEST CONDITIONS†	TPS204xA			TPS205xA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, Device enabled into short circuit	0.7	1	1.3	0.7	1	1.3	A

† Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = $V_{I(IN)}$ (unless otherwise noted) (continued)

supply current (TPS2041A, TPS2051A)

PARAMETER	TEST CONDITIONS			TPS2041A			TPS2051A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$V_{I(\overline{EN})}$ = $V_{I(IN)}$	T_J = 25°C		0.025	1				µA
			–40°C ≤ T_J ≤ 125°C			10				
		$V_{I(EN)}$ = 0 V	T_J = 25°C					0.025	1	
			–40°C ≤ T_J ≤ 125°C						10	
Supply current, high-level output	No Load on OUT	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		85	110				µA
			–40°C ≤ T_J ≤ 125°C		100					
		$V_{I(EN)}$ = $V_{I(IN)}$	T_J = 25°C					85	110	
			–40°C ≤ T_J ≤ 125°C					100		
Leakage current	OUT connected to ground	$V_{I(\overline{EN})}$ = $V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C		100					µA
		$V_{I(EN)}$= 0 V	–40°C ≤ T_J ≤ 125°C					100		
Reverse leakage current	IN = High impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		0.3					µA
		$V_{I(EN)}$ = $V_{I(IN)}$						0.3		

supply current (TPS2042A, TPS2052A)

PARAMETER	TEST CONDITIONS			TPS2042A			TPS2052A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUT	$V_{I(\overline{ENx})}$ = $V_{I(IN)}$	T_J = 25°C		0.025	1				µA
			–40°C ≤ T_J ≤ 125°C			10				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C					0.025	1	
			–40°C ≤ T_J ≤ 125°C						10	
Supply current, high-level output	No Load on OUT	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C		85	110				µA
			–40°C ≤ T_J ≤ 125°C		100					
		$V_{I(ENx)}$ = $V_{I(IN)}$	T_J = 25°C					85	110	
			–40°C ≤ T_J ≤ 125°C					100		
Leakage current	OUT connected to ground	$V_{I(\overline{ENx})}$ = $V_{I(IN)}$	–40°C ≤ T_J ≤ 125°C		100					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C					100		
Reverse leakage current	IN = high impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		0.3					µA
		$V_{I(EN)}$ = $V_{I(IN)}$						0.3		

electrical characteristics over recommended operating junction temperature range, $V_{I(IN)}$= 5.5 V, I_O = rated current, $V_{I(\overline{EN})}$ = 0 V, $V_{I(EN)}$ = $V_{I(IN)}$ (unless otherwise noted) (continued)

supply current (TPS2043A, TPS2053A)

PARAMETER	TEST CONDITIONS			TPS2043A			TPS2053A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = $V_{I(INx)}$	T_J = 25°C		0.05	2				µA
			–40°C ≤ T_J ≤ 125°C			20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C					0.05	2	
			–40°C ≤ T_J ≤ 125°C						20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C		160	200				µA
			–40°C ≤ T_J ≤ 125°C		200					
		$V_{I(ENx)}$ = $V_{I(INx)}$	T_J = 25°C					160	200	
			–40°C ≤ T_J ≤ 125°C					200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})}$ = $V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C		200					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C					200		
Reverse leakage current	IN = high impedance	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C		0.3					µA
		$V_{I(ENx)}$ = $V_{I(IN)}$						0.3		

supply current (TPS2044A, TPS2054A)

PARA-METER	TEST CONDITIONS			TPS2044A			TPS2054A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply current, low-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = $V_{I(INx)}$	T_J = 25°C		0.05	2				µA
			–40°C ≤ T_J ≤ 125°C			20				
		$V_{I(ENx)}$ = 0 V	T_J = 25°C					0.05	2	
			–40°C ≤ T_J ≤ 125°C						20	
Supply current, high-level output	No Load on OUTx	$V_{I(\overline{ENx})}$ = 0 V	T_J = 25°C		170	220				µA
			–40°C ≤ T_J ≤ 125°C		200					
		$V_{I(ENx)}$ = $V_{I(INx)}$	T_J = 25°C					170	220	
			–40°C ≤ T_J ≤ 125°C					200		
Leakage current	OUTx connected to ground	$V_{I(\overline{ENx})}$ = $V_{I(INx)}$	–40°C ≤ T_J ≤ 125°C		200					µA
		$V_{I(ENx)}$ = 0 V	–40°C ≤ T_J ≤ 125°C					200		
Reverse leakage current	IN = high impedance	$V_{I(\overline{EN})}$ = 0 V	T_J = 25°C		0.3					µA
		$V_{I(EN)}$ = $V_{I(IN)}$						0.3		

undervoltage lockout

PARAMETER	TEST CONDITIONS	TPS204xA			TPS205xA			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Low-level input voltage		2		2.5	2		2.5	V
Hysteresis	T_J = 25°C		100			100		mV

overcurrent $\overline{OC}$

PARAMETER	TEST CONDITIONS	TPS204xA			TPS205xA			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Sink current†	V_O = 5 V			10			10	mA
Output low voltage	I_O = 5 V, $V_{OL(\overline{OC})}$			0.5			0.5	V
Off-state current†	V_O = 5 V, V_O = 3.3 V			1			1	µA

† Specified by design, not production tested.

PARAMETER MEASUREMENT INFORMATION

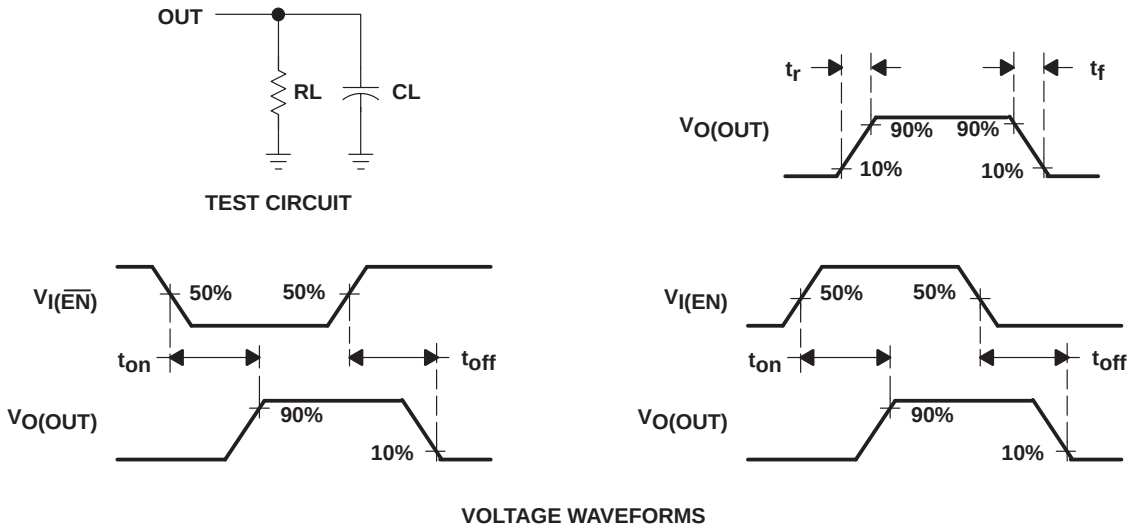


Figure 1. Test Circuit and Voltage Waveforms

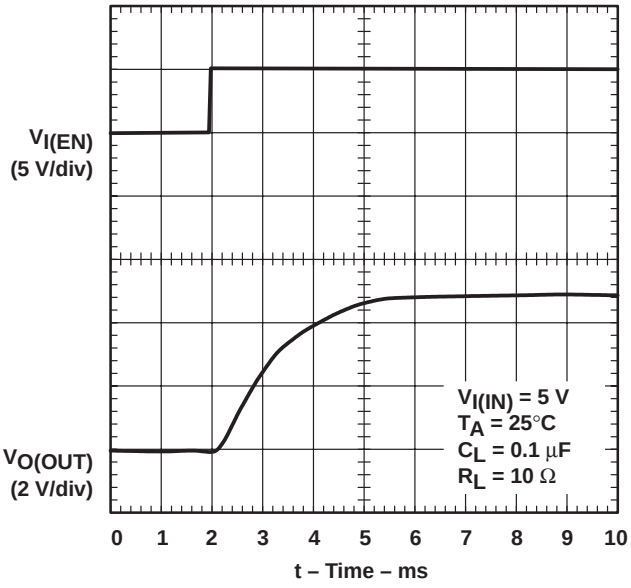


Figure 2. Turnon Delay and Rise Time with 0.1-μF Load

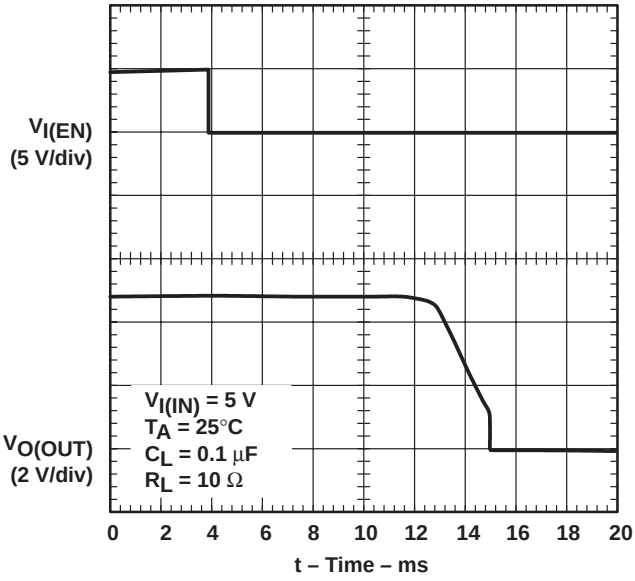


Figure 3. Turnoff Delay and Fall Time with 0.1-μF Load

PARAMETER MEASUREMENT INFORMATION

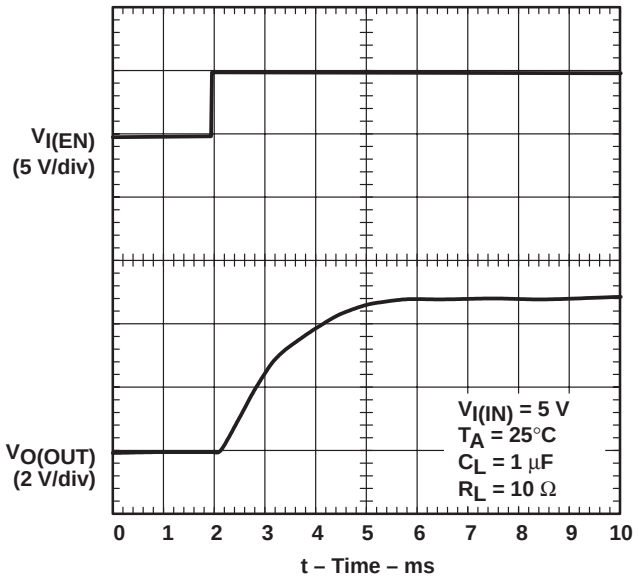


Figure 4. Turnon Delay and Rise Time with 1-μF Load

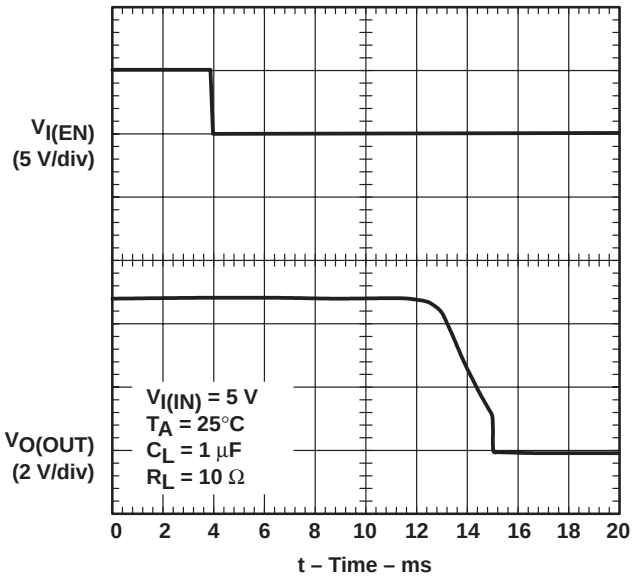


Figure 5. Turnoff Delay and Fall Time with 1-μF Load

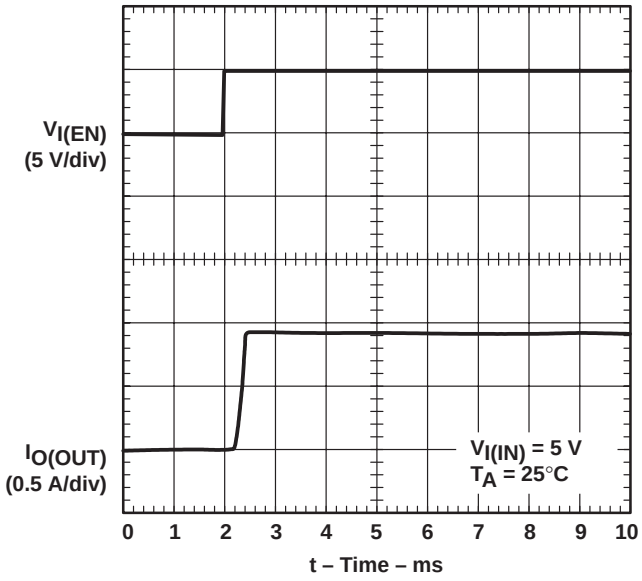


Figure 6. TPS2051A, Short-Circuit Current, Device Enabled into Short

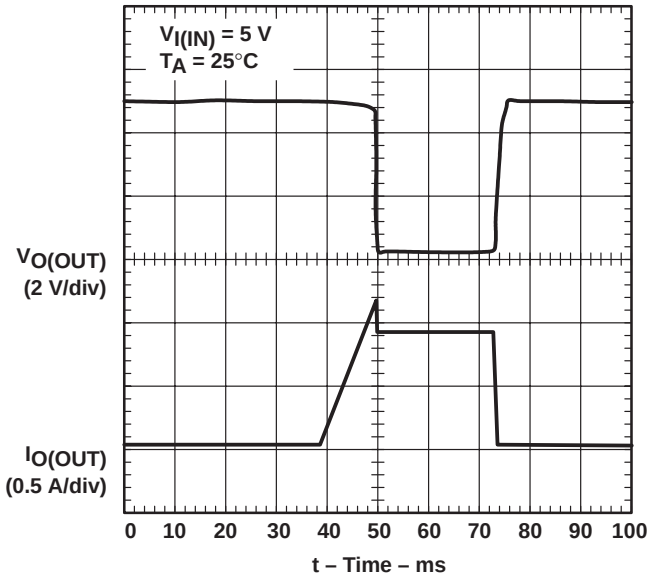


Figure 7. TPS2051A, Threshold Trip Current with Ramped Load on Enabled Device

PARAMETER MEASUREMENT INFORMATION

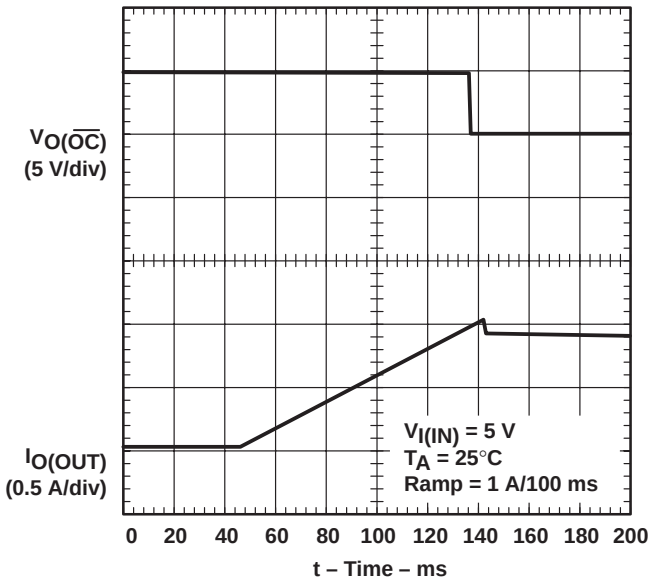


Figure 8. OC Response With Ramped Load on Enabled Device

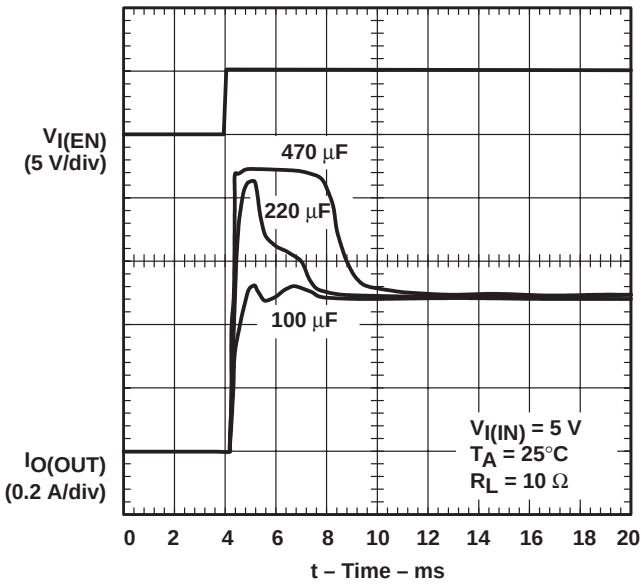


Figure 9. Inrush Current with 100-μF, 220-μF and 470-μF Load Capacitance

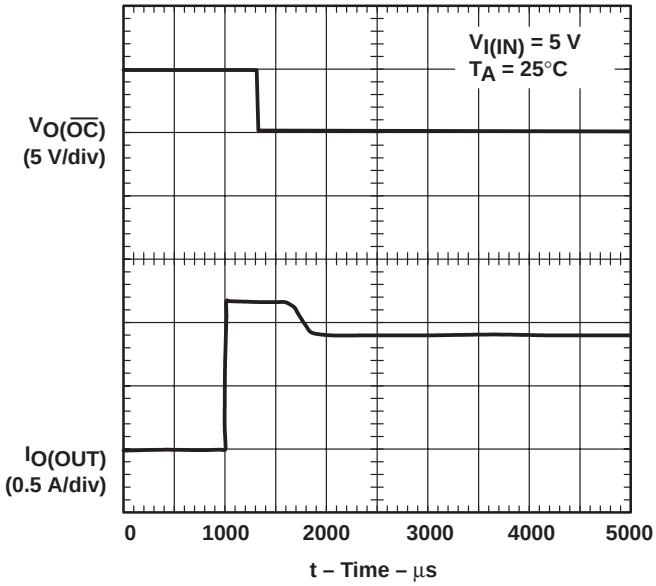


Figure 10. 4-Ω Load Connected to Enabled Device

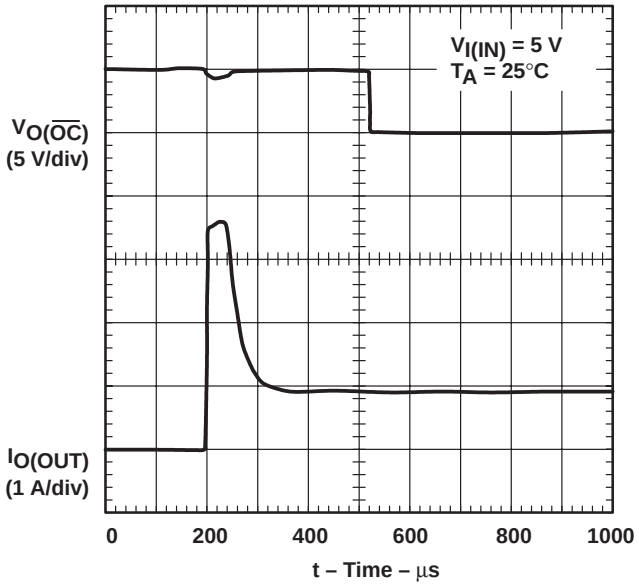


Figure 11. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURNON DELAY TIME vs INPUT VOLTAGE

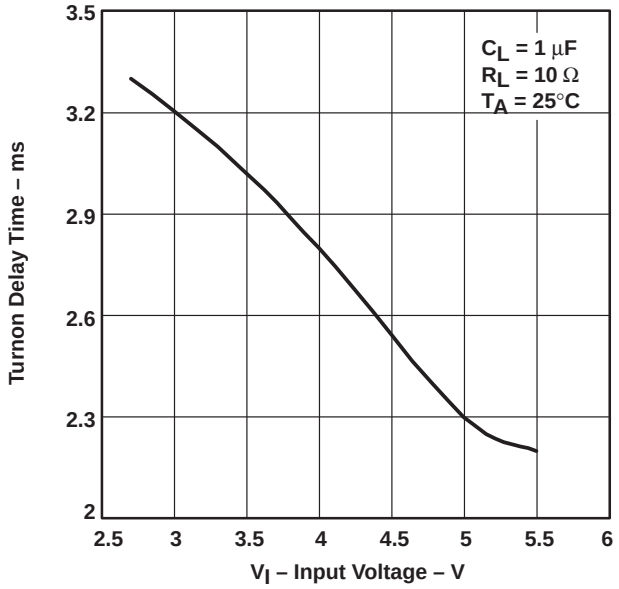


Figure 12

TURNOFF DELAY TIME vs INPUT VOLTAGE

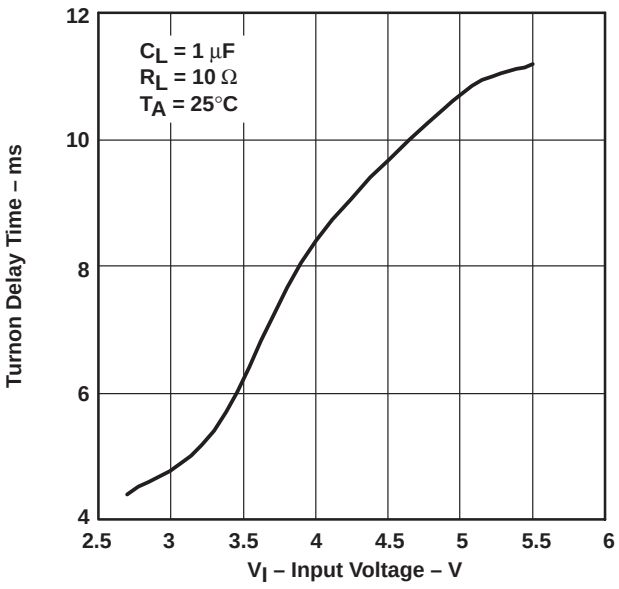


Figure 13

RISE TIME vs INPUT VOLTAGE

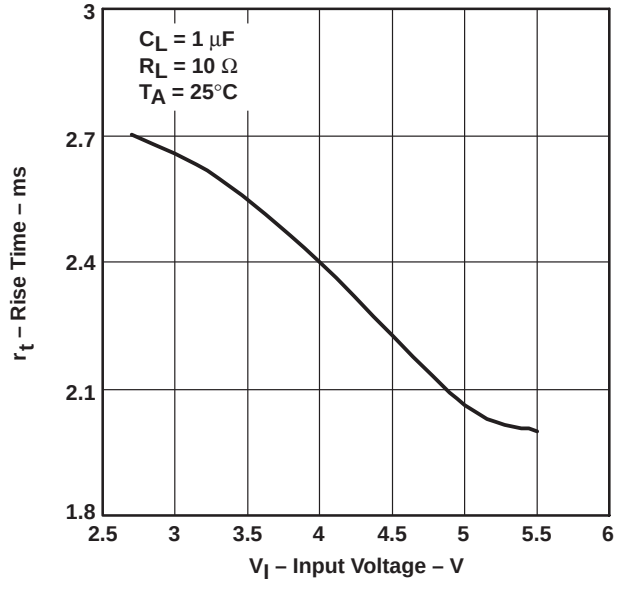


Figure 14

FALL TIME vs INPUT VOLTAGE

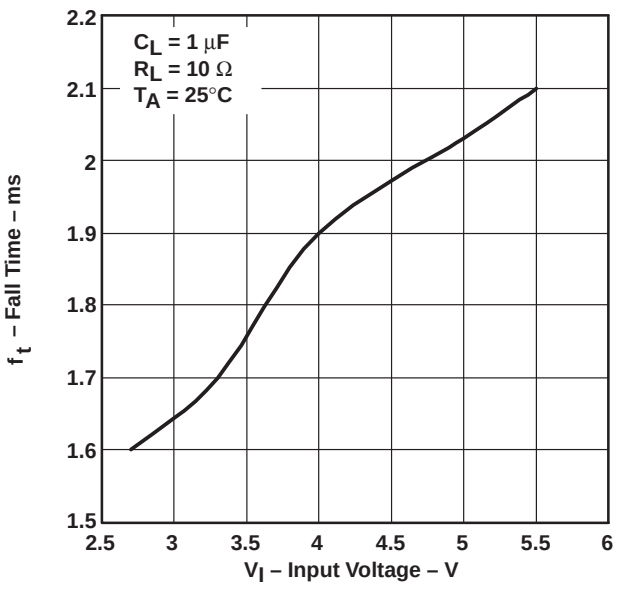


Figure 15

TYPICAL CHARACTERISTICS

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

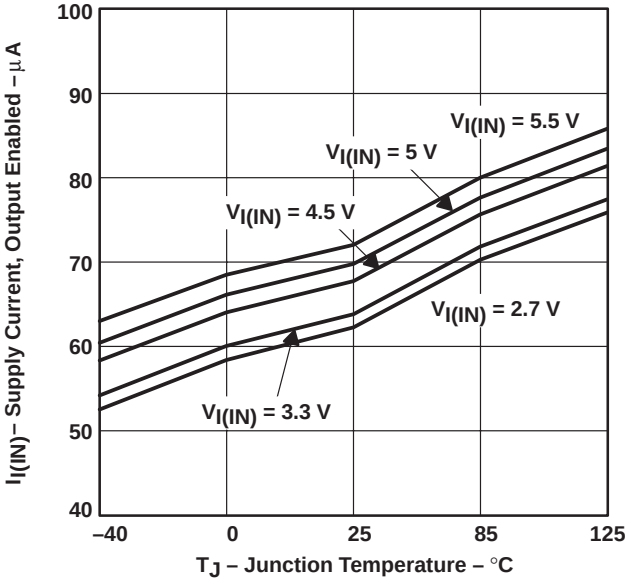


Figure 16

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

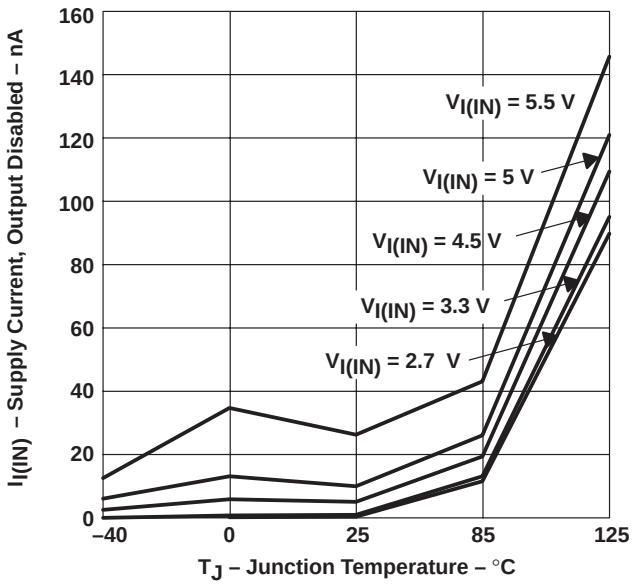


Figure 17

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

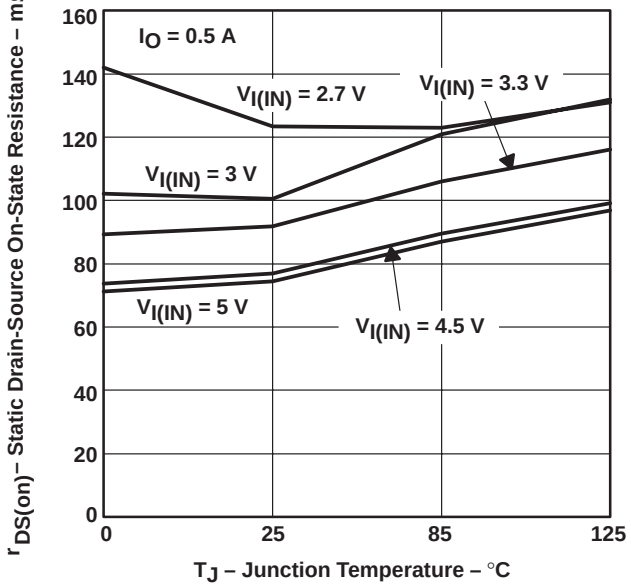


Figure 18

INPUT-TO-OUTPUT VOLTAGE vs LOAD CURRENT

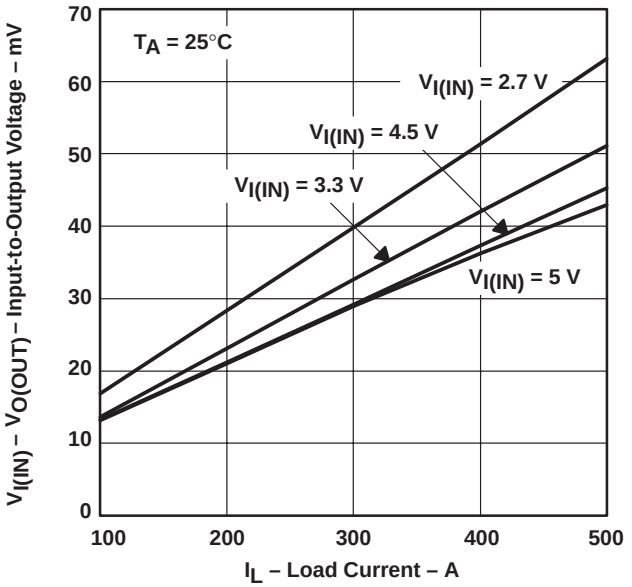


Figure 19

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

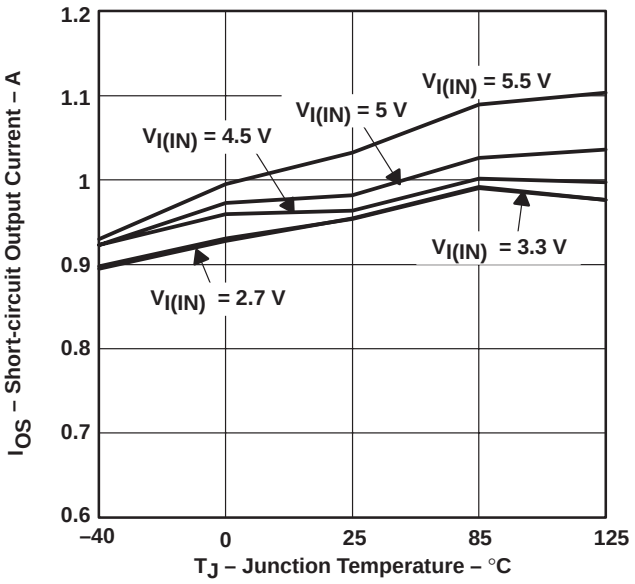


Figure 20

THRESHOLD TRIP CURRENT vs INPUT VOLTAGE

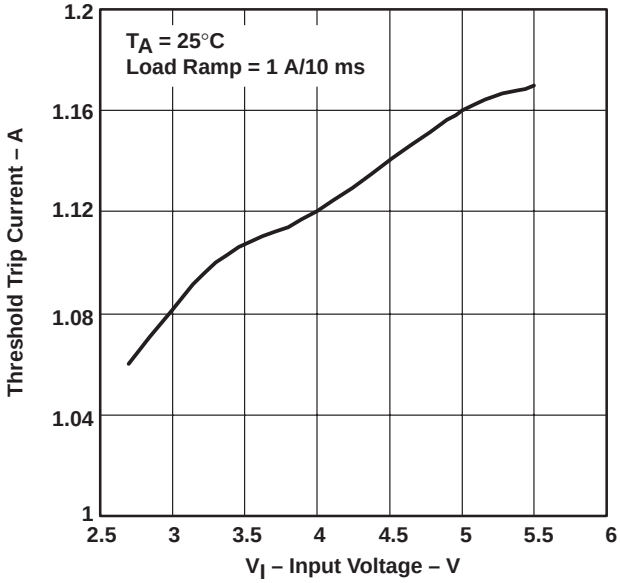


Figure 21

UNDERVOLTAGE LOCKOUT vs JUNCTION TEMPERATURE

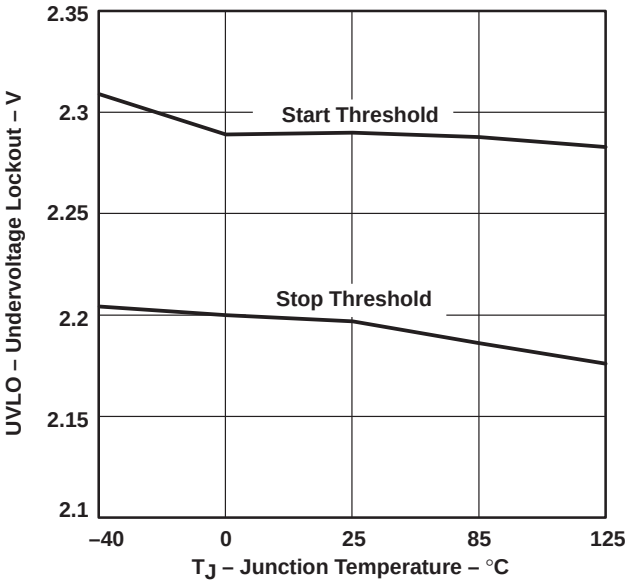


Figure 22

CURRENT-LIMIT RESPONSE vs PEAK CURRENT

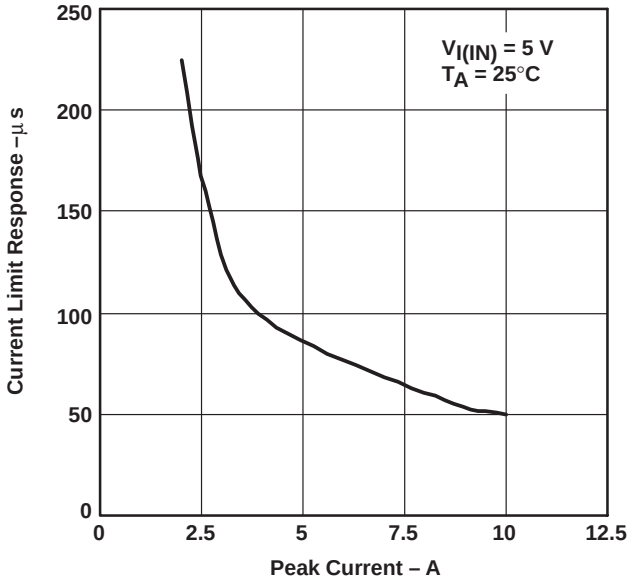


Figure 23

APPLICATION INFORMATION

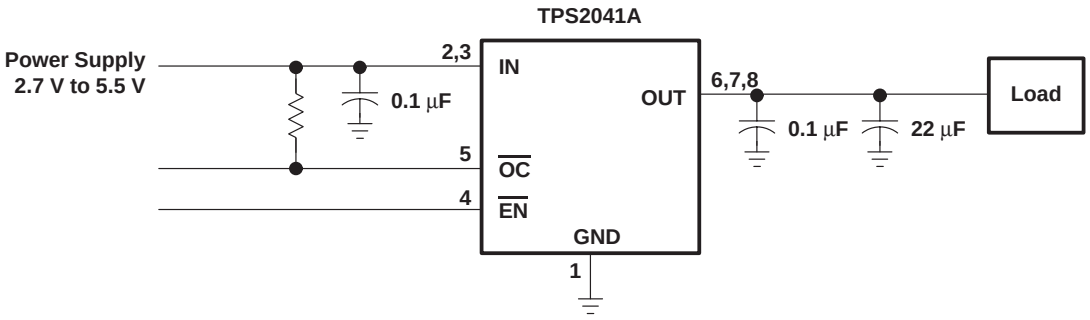


Figure 24. Typical Application (Example, TPS2041A)

power-supply considerations

A 0.01-μF to 0.1-μF ceramic bypass capacitor between INx and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-μF to 0.1-μF ceramic capacitor improves the immunity of the device to short-circuit transients.

overcurrent

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 6). The TPS204xA and TPS205xA sense the short and immediately switch into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, very high currents may flow for a short time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshhold) the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 7). The TPS204xA and TPS205xA are capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ response

The $\overline{\text{OC}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output will remain asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause momentary false overcurrent reporting from the inrush current flowing through the device, charging the downstream capacitor. The TPS204xA and TPS205xA family of devices are designed to reduce false overcurrent reporting. An internal overcurrent transient filter eliminates the need for external components to remove unwanted pulses. Using low-ESR electrolytic capacitors on the output lowers the inrush current flow through the device during hot-plug events by providing a low-impedance energy source, also reducing erroneous overcurrent reporting.

APPLICATION INFORMATION

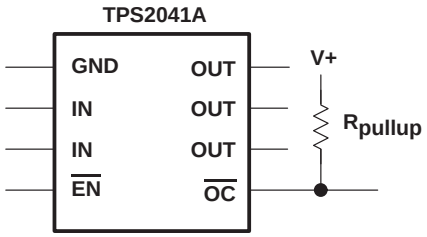


Figure 25. Typical Circuit for $\overline{OC}$ Pin (Example, TPS2041A)

power dissipation and junction temperature

The low on-resistance on the n-channel MOSFET allows small surface-mount packages, such as SOIC, to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 18. Using this value, the power dissipation per switch can be calcultaed by:

$$P_D = r_{DS(on)} \times I^2$$

Depending on which device is being used, multiply this number by the number of switches being used. This step will render the total power dissipation from the N-channel MOSFETs.

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

T_A = Ambient Temperature °C
$R_{\theta JA}$ = Thermal resistance SOIC = 172°C/W (for 8 pin), 111°C/W (for 16 pin)
P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

thermal protection

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The faults force the TPS204xA and TPS205xA into constant-current mode, which causes the voltage across the high-side switch to increase; under short-circuit conditions, the voltage across the switch is equal to the input voltage. The increased dissipation causes the junction temperature to rise to high levels. The protection circuit senses the junction temperature of the switch and shuts it off. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 20 degrees, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed.

The TPS204xA and TPS205xA implement a dual thermal trip to allow fully independent operation of the power distribution switches. In an overcurrent or short-circuit condition the junction temperature will rise. Once the die temperature rises to approximately 140°C, the internal thermal sense circuitry checks which power switch is in an overcurrent condition and turns that power switch off, thus isolating the fault without interrupting operation of the adjacent power switch. Should the die temperature exceed the first thermal trip point of 140°C and reach 160°C, both switches turn off. The $\overline{OC}$ open-drain output is asserted (active low) when overtemperature or overcurrent occurs.

APPLICATION INFORMATION

undervoltage lockout (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch will be quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO will also keep the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. Upon reinsertion, the power switch will be turned on, with a controlled rise time to reduce EMI and voltage overshoots.

universal serial bus (USB) applications

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

Self-powered and bus-powered hubs distribute data and power to downstream functions. The TPS204xA and TPS205xA can provide power-distribution solutions for many of these classes of devices.

host/self-powered and bus-powered hubs

Hosts and self-powered hubs have a local power supply that powers the embedded functions and the downstream ports (see Figures 26 and 27). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

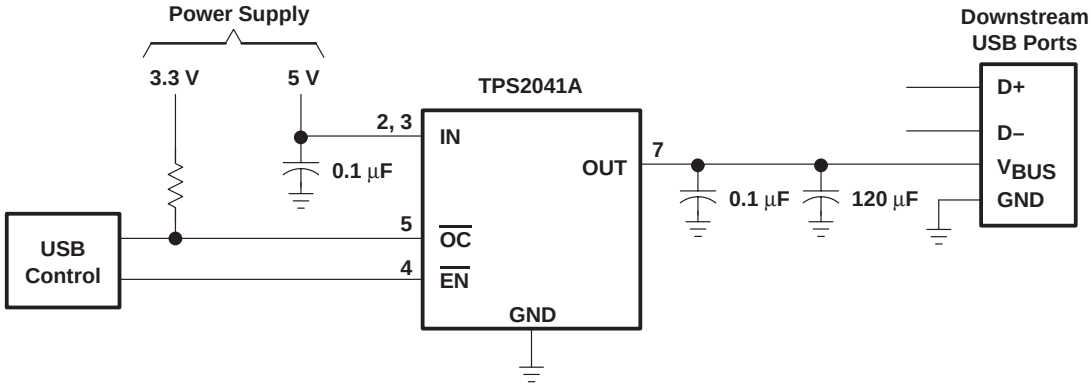


Figure 26. Typical One-Port Solution

APPLICATION INFORMATION

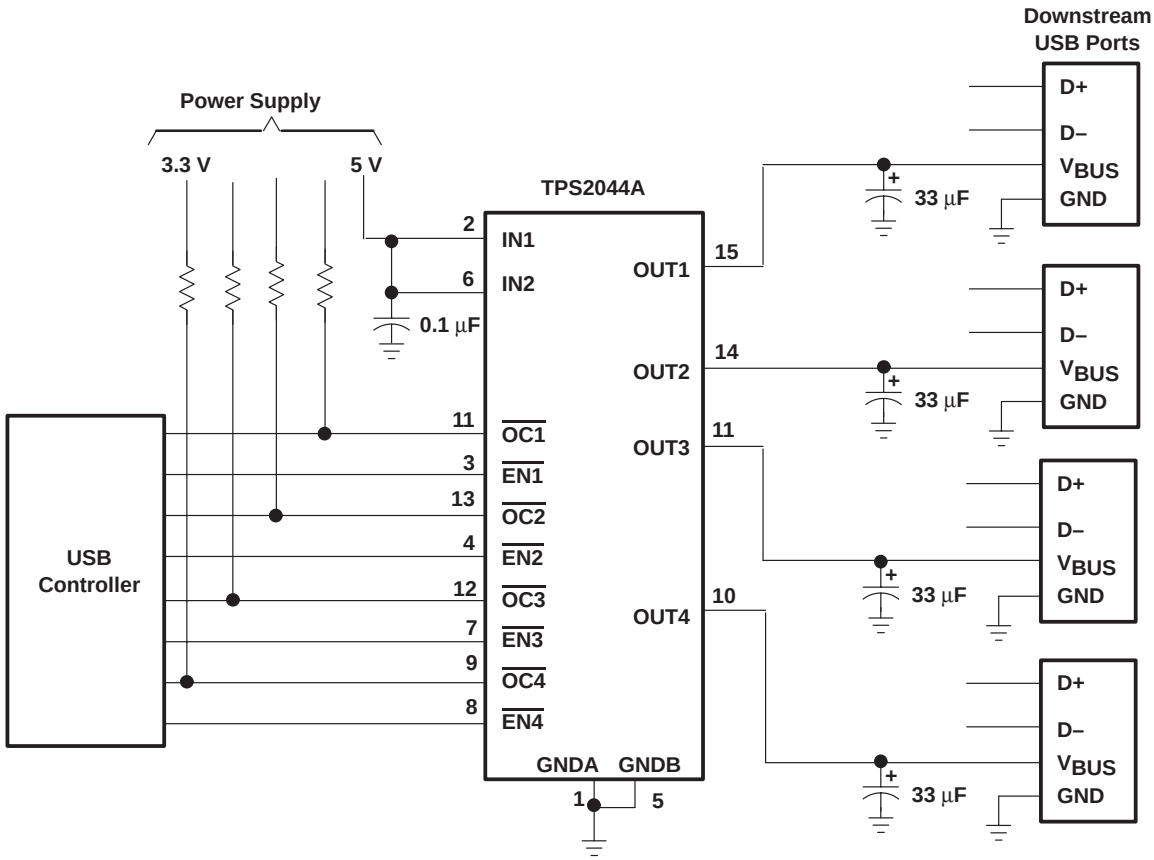


Figure 27. Typical Four-Port USB Host/Self-Powered Hub

Bus-powered hubs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on powerup, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

APPLICATION INFORMATION

low-power bus-powered functions and high-power bus-powered functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 μF at power up, the device must implement inrush current limiting (see Figure 28).

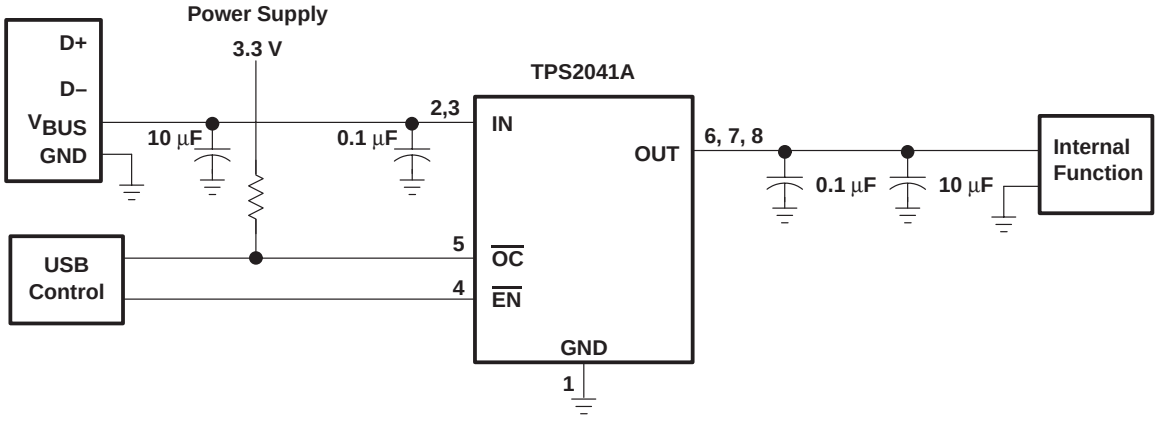


Figure 28. High-Power Bus-Powered Function (Example, TPS2041A)

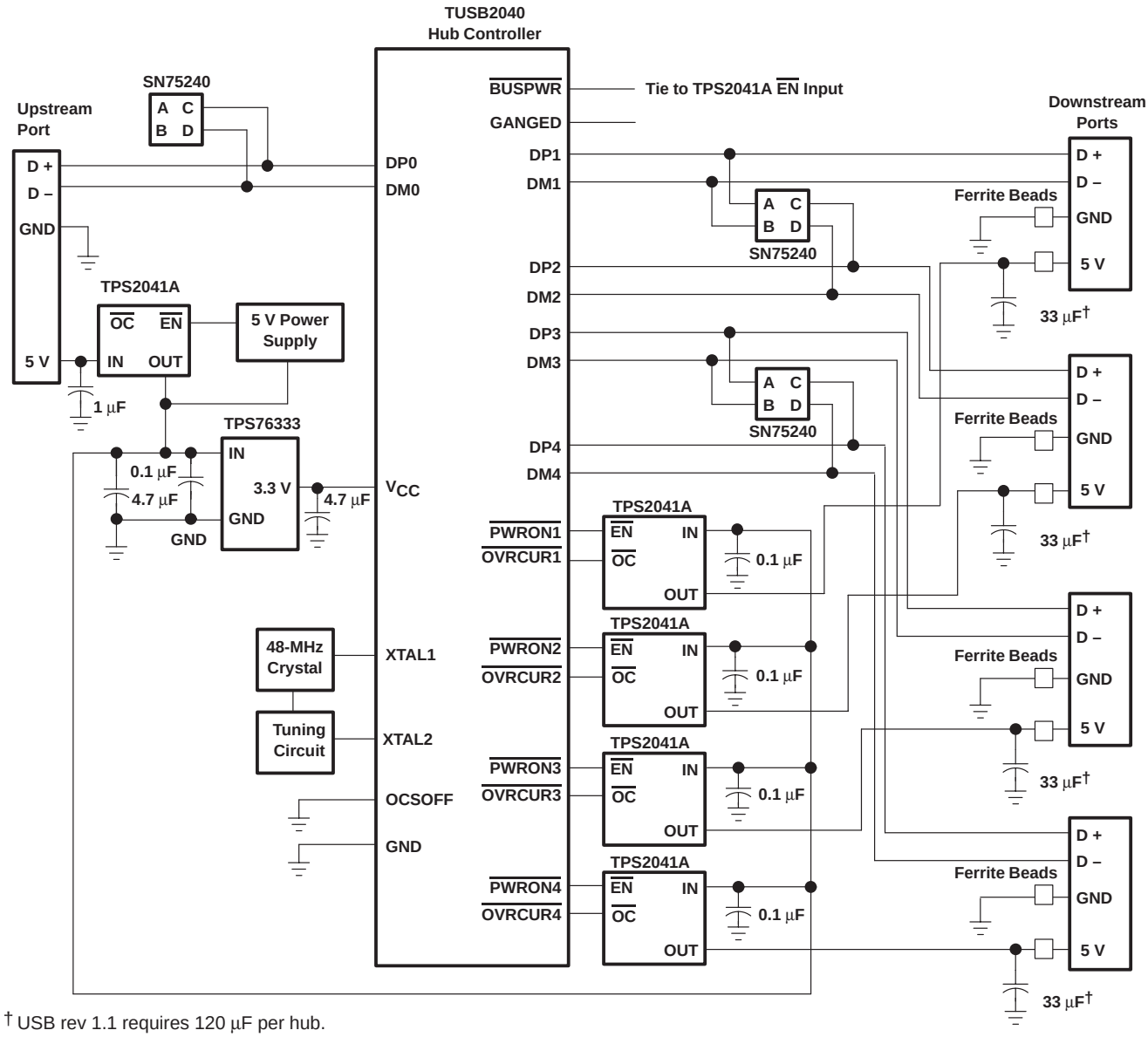
USB power-distribution requirements

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/self-powered hubs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- Bus-powered hubs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 μF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS204xA and TPS205xA allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-power hubs, as well as the input ports for bus-power functions (see Figures 29 through 32).

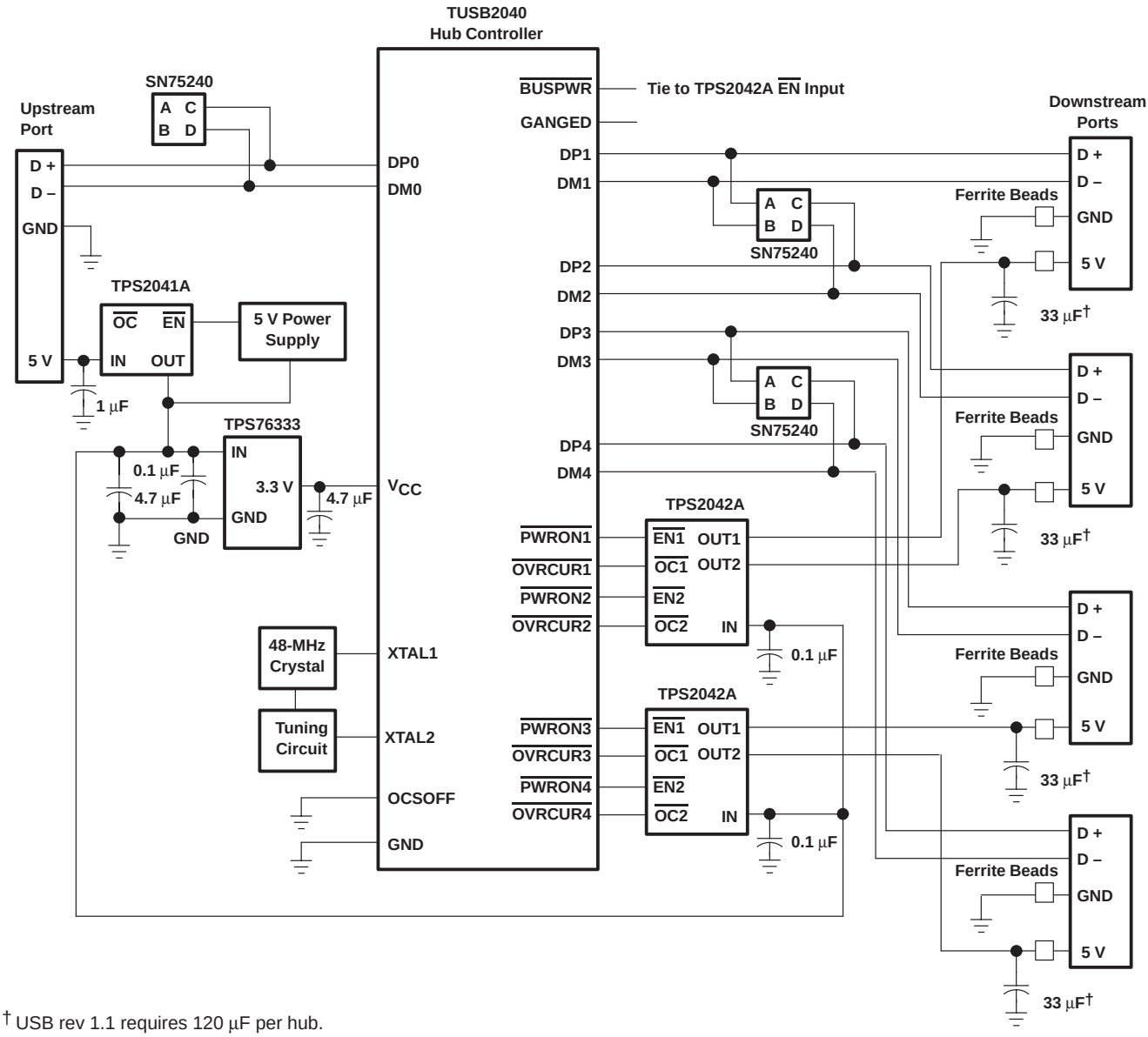
APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 29. Hybrid Self/Bus-Powered Hub Implementation, TPS2041A

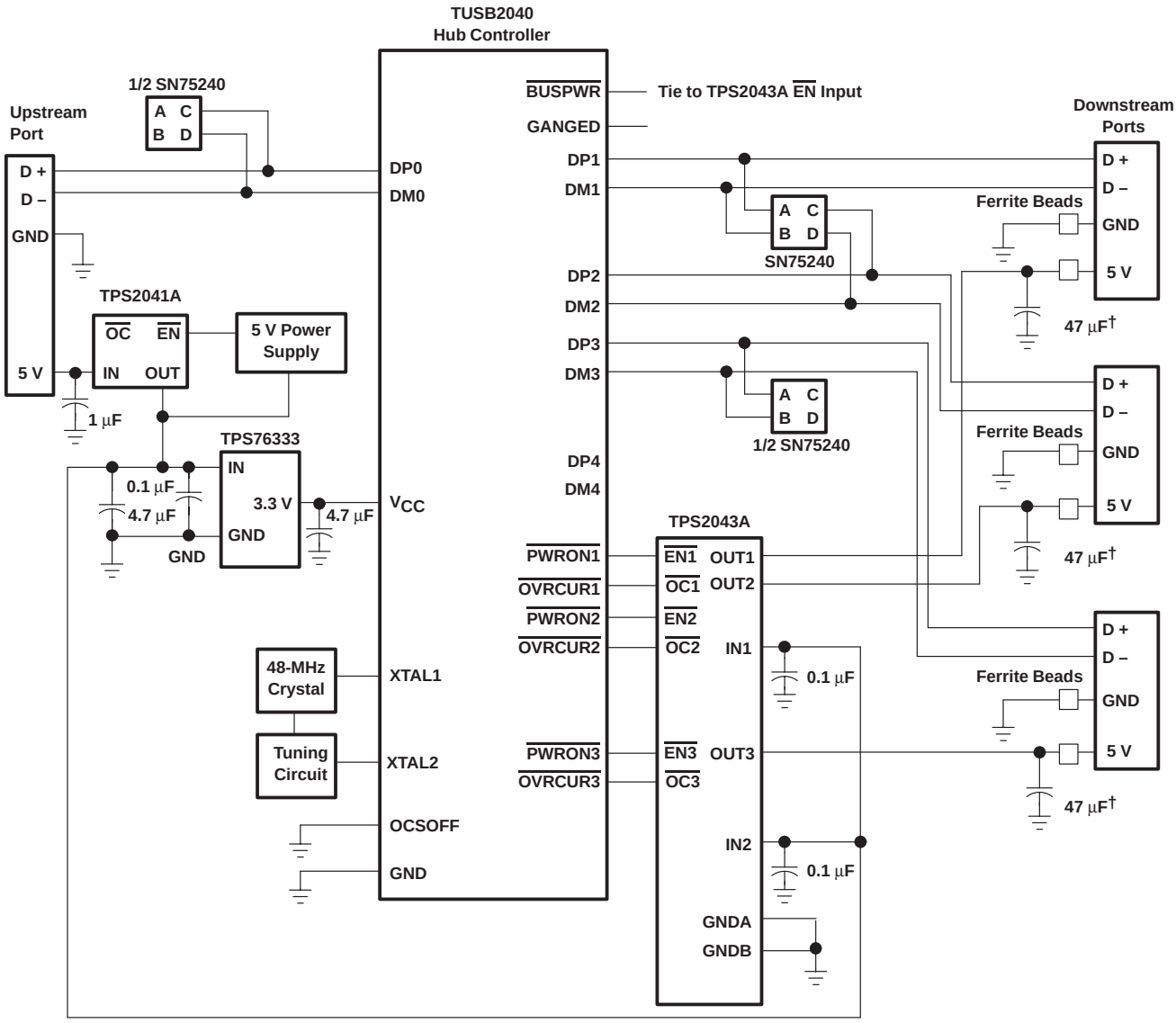
APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 30. Hybrid Self/Bus-Powered Hub Implementation, TPS2042A

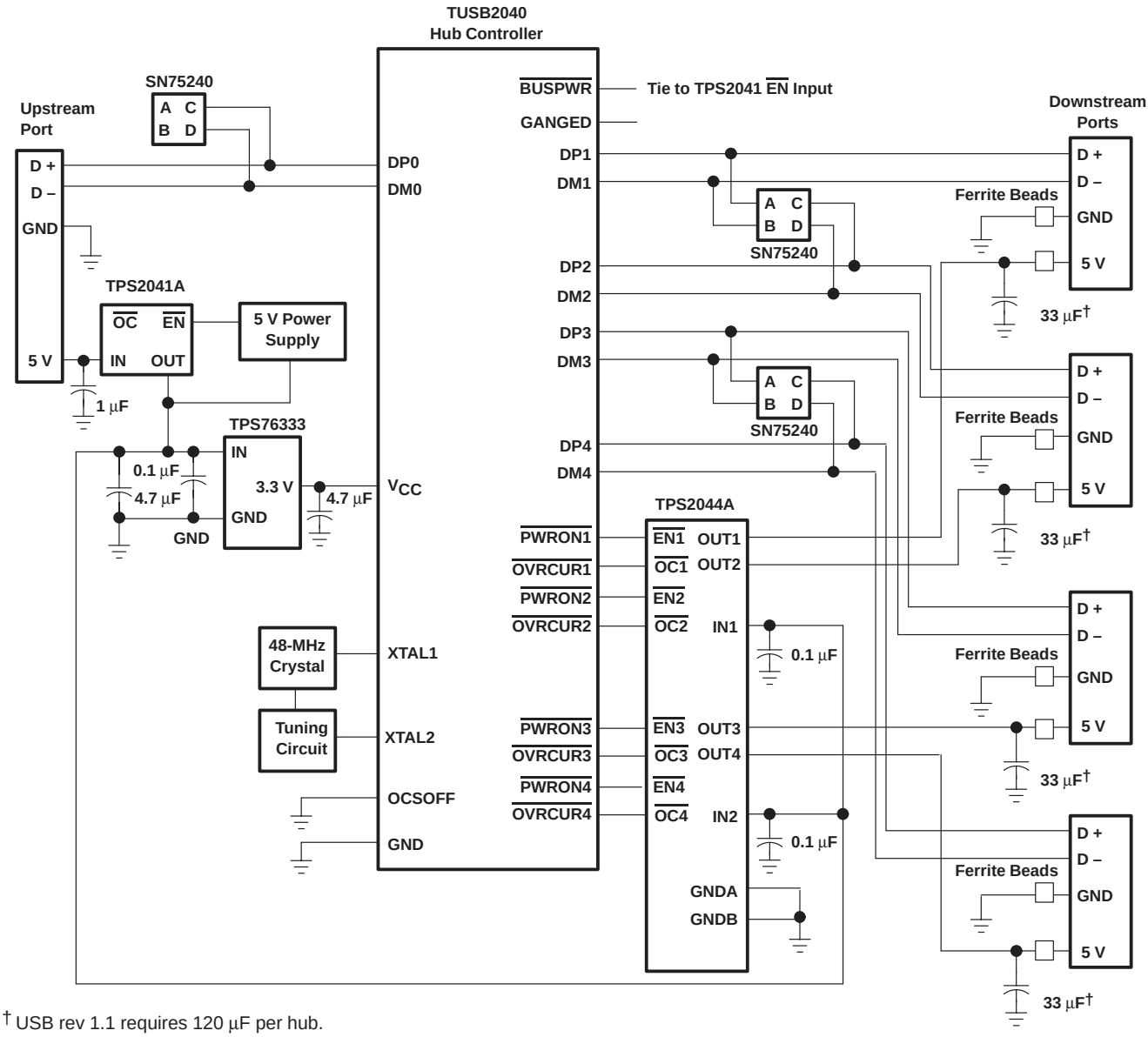
APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 31. Hybrid Self/Bus-Powered Hub Implementation, TPS2043A

APPLICATION INFORMATION



† USB rev 1.1 requires 120 µF per hub.

Figure 32. Hybrid Self/Bus-Powered Hub Implementation, TPS2044A

APPLICATION INFORMATION

generic hot-plug applications (see Figure 33)

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS204xA and TPS205xA, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS204xA and TPS205xA also ensures the switch will be off after the card has been removed, and the switch will be off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

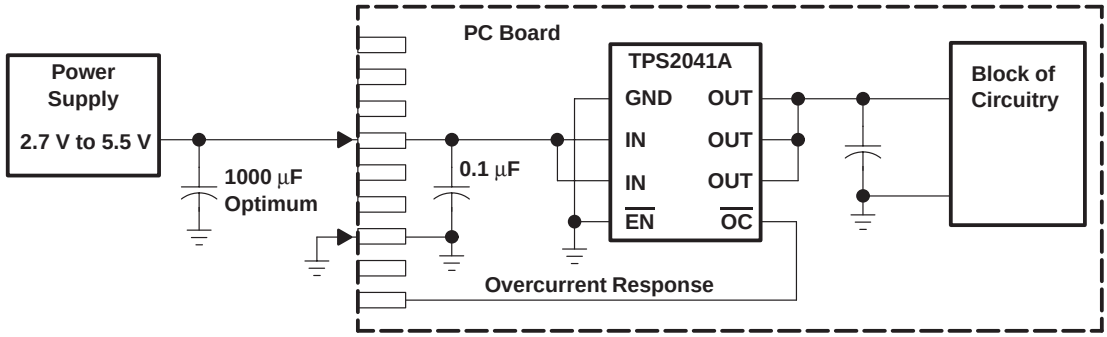


Figure 33. Typical Hot-Plug Implementation (Example, TPS2041A)

By placing the TPS204xA and TPS205xA between the V_{CC} input and the rest of the circuitry, the input power will reach these devices first after insertion. The typical rise time of the switch is approximately 2.5 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2041AD	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2041A	
TPS2041ADG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2041A	
TPS2041ADR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2041A	
TPS2041ADRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2041A	
TPS2042AD	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2042A	
TPS2042ADG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2042A	
TPS2042ADR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2042A	
TPS2042ADRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2042A	
TPS2043AD	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2043A	
TPS2043ADG4	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2043A	
TPS2044AD	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2044A	
TPS2044ADG4	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2044A	
TPS2044ADR	NRND	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2044A	
TPS2044ADRG4	NRND	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2044A	
TPS2051AD	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2051A	
TPS2051ADG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2051A	
TPS2051ADR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2051A	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2052AD	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2052A	
TPS2052ADG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2052A	
TPS2052ADR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2052A	
TPS2054AD	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2054A	
TPS2054ADG4	NRND	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	2054A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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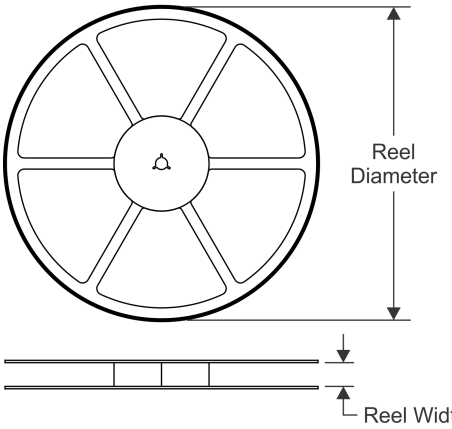
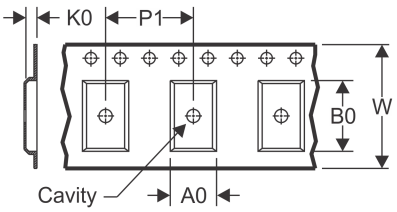
TAPE AND REEL INFORMATION

REEL DIMENSIONS

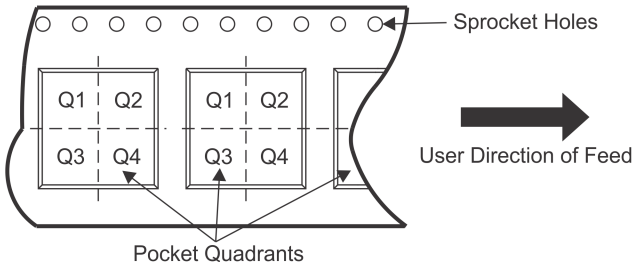


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

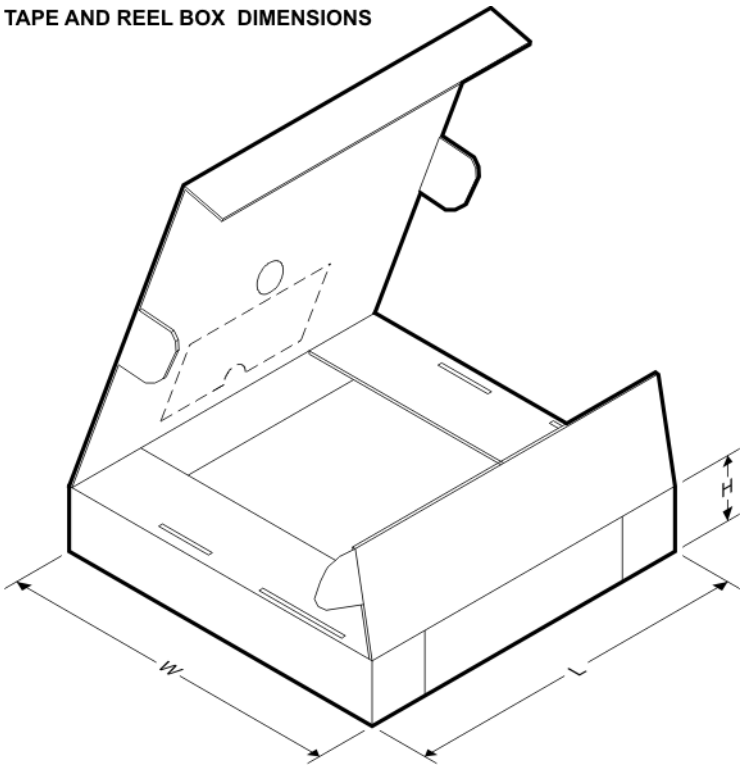
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2041ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2042ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2044ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TPS2051ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2052ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2041ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2042ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2044ADR	SOIC	D	16	2500	333.2	345.9	28.6
TPS2051ADR	SOIC	D	8	2500	340.5	338.1	20.6
TPS2052ADR	SOIC	D	8	2500	340.5	338.1	20.6

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