TPS1HB50-Q1 40-V, 50-mΩ Single-Channel Smart High-Side Switch

1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C4B
  - Withstands 40-V load dump
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Single-channel smart high-side switch with 50-mΩ R_{ON} (T_J = 25°C)
- Improve system level reliability through adjustable current limiting
  - Current limit set-point from 2 A to 18 A
- Robust integrated output protection:
  - Integrated thermal protection
  - Protection against short to ground and battery
  - Protection against reverse battery events including automatic switch on of FET with reverse voltage
  - Automatic shut off on loss of battery and ground
  - Integrated output clamp to demagnetize inductive loads
  - Configurable fault handling
- Analog sense output can be configured to accurately measure:
  - Load current
  - Device temperature
- Provides fault indication through SNS pin
  - Detection of open load and short-to-battery

2 Applications

- Automotive display module
- ADAS modules
- Seat comfort module
- Transmission control unit
- HVAC control module
- Body control modules
- Incandescent and LED lighting

3 Description

The TPS1HB50-Q1 device is a smart high-side switch intended for use in 12-V automotive systems. The device integrates robust protection and diagnostic features to ensure output port protection even during harmful events like short circuits in automotive systems. The device protects against faults through a reliable current limit, which, depending on device variant, is adjustable from 2 A to 18 A . The high current limit range allows for usage in loads that require large transient currents, while the low current limit range provides improved protection for loads that do not require high peak current. The device is capable of reliably driving a wide range of load profiles.

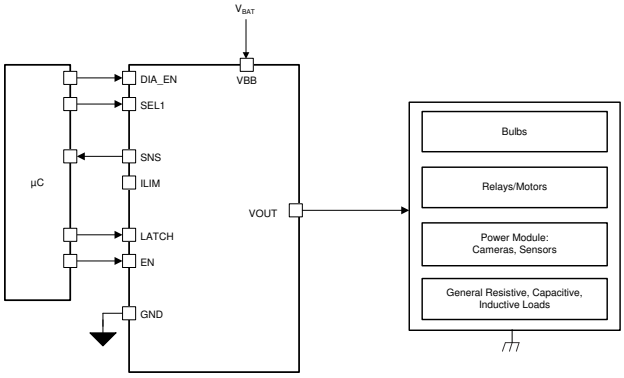
The TPS1HB50-Q1 also provides a high accuracy analog current sense that allows for improved load diagnostics. By reporting load current and device temperature to a system MCU, the device enables predictive maintenance and load diagnostics that improves the system lifetime.

The TPS1HB50-Q1 is available in a HTSSOP package which allows for reduced PCB footprint.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
TPS1HB50-Q1	HTSSOP (16)	5.0 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

Changes from Revision * (June 2019) to Revision A (October 2020)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Changed status from Advance Information to Production Data	1

5 Device Comparison Table

Table 5-1. Device Options

Device Version	Part Number	Current Limit	Current Limit Range	Overcurrent Behavior
A	TPS1HB50**A**-Q1	Resistor Programmable	2 A to 10 A	Disable switch immediately
B	TPS1HB50**B**-Q1	Resistor Programmable	3.6 A to 18 A	Disable switch immediately

6 Pin Configuration and Functions

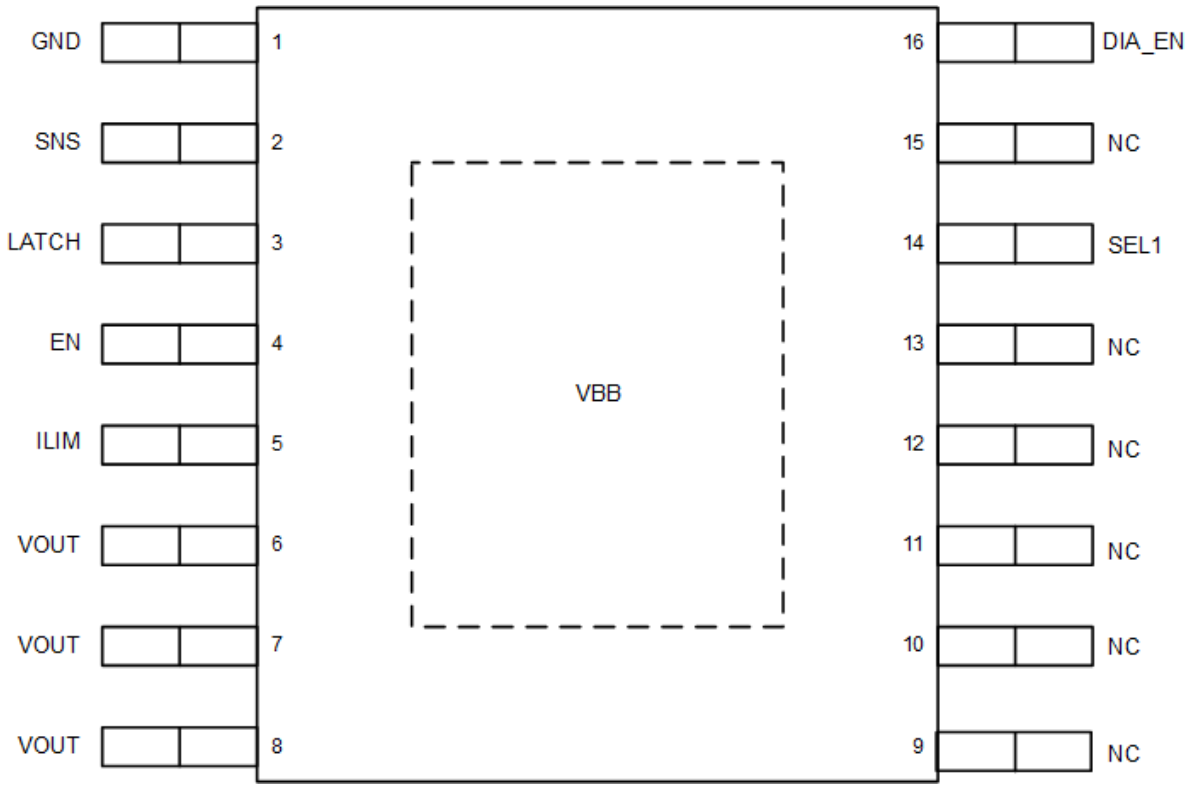


Figure 6-1. PWP Package 16-Pin HTSSOP Top View

Table 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	GND	—	Device ground
2	SNS	O	Sense output
3	LATCH	I	Sets fault handling behavior (latched or auto-retry)
4	EN	I	Control input, active high
5	ILIM	O	Connect resistor to set current-limit threshold
6 - 8	VOUT	O	Channel output
9 - 13, 15	NC	I	No Connect, leave floating
14	SEL1	I	Diagnostics select.
16	DIA_EN	I	Diagnostic enable, active high
Exposed pad	VBB	I	Power supply input

6.1 Recommended Connections for Unused Pins

The TPS1HC100-Q1 is designed to provide an enhanced set of diagnostic and protection features. However, if the system design only allows for a limited number of I/O connections, some pins may be considered as optional.

Table 6-2. Connections for Optional Pins

PIN NAME	CONNECTION IF NOT USED	IMPACT IF NOT USED
SNS	Ground through 1-kΩ resistor	Analog sense is not available.
LATCH	Float or ground through R_{PROT} resistor	With LATCH unused, the device will auto-retry after a fault. If latched behavior is desired, but the system describes limited I/O, it is possible to use one microcontroller output to control the latch function of several high-side channels.
ILIM	Float	If the ILIM pin is left floating, the device will be set to the default internal current-limit threshold. This is considered a fault state for the device.
$\overline{\text{FAULT}}$	Float	If the $\overline{\text{FAULT}}$ pin is unused, the system cannot read faults from the output.
DIA_EN	Float or ground through R_{PROT} resistor	With DIA_EN unused, the analog sense, open-load, and short-to-battery diagnostics are not available.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum continuous supply voltage, V_{BB}			36	V
Load dump voltage, V_{LD}	ISO16750-2:2010(E)		40	V
Reverse battery voltage, V_{Rev}, t ≤ 3 minutes		–18		V
Enable pin voltage, V_{EN}		–1	7	V
LATCH pin voltage, V_{LATCH}		–1	7	V
Diagnostic Enable pin voltage, V_{DIA_EN}		–1	7	V
Sense pin voltage, V_{SNS}		–1	18	V
Select pin voltage, V_{SEL1}		–1	7	V
Reverse ground current, I_{GND}	V_{BB} < 0 V		–50	mA
Energy dissipation during turnoff, E_{TOFF}	Single pulse, L_{OUT} = 5 mH, $T_{J,start}$ = 125°C		17(2)	mJ
Energy dissipation during turnoff, E_{TOFF}	Repetitive pulse, L_{OUT} = 5 mH, $T_{J,start}$ = 125°C		7(2)	mJ
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) For further details, see the section regarding switch-off of an inductive load.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	All pins except VBB and VOUT	±2000	V
			VBB and VOUT	±4000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±750	

(1) AEC-Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specifications.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{BB}	Nominal supply voltage (1)	6	18	V
V_{BB}	Extended lower supply voltage	3	6	V
V_{BB}	Extended higher supply voltage(2)	18	28	V
V_{EN}	Enable voltage	–1	5.5	V
V_{LATCH}	LATCH voltage	–1	5.5	V
V_{DIA_EN}	Diagnostic Enable voltage	–1	5.5	V
V_{SEL1}	Select voltage	–1	5.5	V
V_{SNS}	Sense voltage	–1	7	V
T_A	Operating free-air temperature	–40	125	°C

(1) All operating voltage conditions are measured with respect to device GND.

(2) Device parameters still valid, short circuit protection valid to value specificed by V_{SC} parameter.

7.4 Thermal Information

THERMAL METRIC (1) (2)		TPS1HB50-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

7.5 Electrical Characteristics

V_{BB} = 6 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
$V_{DSCLAMP}$	V_{DS} clamp voltage			40		46	V
$V_{BBCLAMP}$	V_{BB} clamp voltage			58		76	V
V_{UVLOF}	V_{BB} undervoltage lockout falling	Measured with respect to the GND pin of the device		2.0		3	V
V_{UVLOR}	V_{BB} undervoltage lockout rising	Measured with respect to the GND pin of the device		2.2		3	V
I_{SB}	Standby current (total device leakage including MOSFET channel)	V_{BB} = 13.5 V, T_J = 25°C V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V				0.1	µA
		V_{BB} = 13.5 V, T_J = 85°C, V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V				0.5	µA
IL_{NOM}	Continuous load current	T_{AMB} = 70°C			4		A
$I_{OUT(standby)}$	Output leakage current	V_{BB} = 13.5 V, T_J = 25°C V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V			0.01	0.5	µA
		V_{BB} = 13.5 V, T_J = 125°C V_{EN} = V_{DIA_EN} = 0 V, V_{OUT} = 0 V				1.5	µA
I_{DIA}	Current consumption in diagnostic mode	V_{BB} = 13.5 V, I_{SNS} = 0 mA V_{EN} = 0 V, V_{DIA_EN} = 5 V, V_{OUT} = 0V			3	6	mA
I_Q	Quiescent current	V_{BB} = 13.5 V V_{EN} = V_{DIA_EN} = 5 V, I_{OUT} = 0 A			3	6	mA
t_{STBY}	Standby mode delay time	V_{EN} = V_{DIA_EN} = 0 V to standby		12	17	22	ms
RON CHARACTERISTICS							
R_{ON}	On-resistance (Includes MOSFET and package)	T_J = 25°C, 6 V ≤ V_{BB} ≤ 28 V			50		mΩ
		T_J = 150°C, 6 V ≤ V_{BB} ≤ 28 V				100	mΩ
		T_J = 25°C, 3 V ≤ V_{BB} ≤ 6 V				75	mΩ
$R_{ON(REV)}$	On-resistance during reverse polarity	T_J = 25°C, –18 V ≤ V_{BB} ≤ –8 V			50		mΩ
		T_J = 105°C, –18 V ≤ V_{BB} ≤ –8 V				115	mΩ
CURRENT SENSE CHARACTERISTICS							
K_{SNS}	Current sense ratio I_{OUT} / I_{SNS}	I_{OUT} = 1 A			1500		
I_{SNSI}	Current sense current and accuracy	V_{EN} = V_{DIA_EN} = 5 V, V_{SEL1} = 0 V	I_{OUT} = 3 A		2.000		mA
				–4		4	%
			I_{OUT} = 1 A		0.667		mA

7.5 Electrical Characteristics (continued)

V_{BB} = 6 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
				–4		4	%
			I_{OUT} = 300 mA		0.2		mA
				–4		4	%
			I_{OUT} = 100 mA		0.067		mA
				–6		6	%
			I_{OUT} = 50 mA		0.034		mA
				–10		10	%
			I_{OUT} = 20 mA		0.014		mA
				–20		20	%
TJ SENSE CHARACTERISTICS							
I_{SNST}	Temperature sense current	V_{DIA_EN} = 5 V, V_{SEL1} = 5 V	T_J = –40°C	0.00	0.12	0.38	mA
			T_J = 25°C	0.72	0.85	0.98	mA
			T_J = 85°C	1.25	1.52	1.79	mA
			T_J = 125°C	1.61	1.96	2.31	mA
			T_J = 150°C	1.80	2.25	2.70	mA
dI_{SNST}/dT	Coefficient				0.0112		mA/°C
SNS CHARACTERISTICS							
I_{SNSFH}	I_{SNS} fault high-level	V_{DIA_EN} = 5 V, V_{SEL1} = 0 V		4	4.5	5.3	mA
$I_{SNSleak}$	I_{SNS} leakage	V_{DIA_EN} = 0 V				1	µA
CURRENT LIMIT CHARACTERISTICS							
V_{SC}	Short Circuit Maximum Supply Voltage	Version A				18	V
		Version B				18	V
I_{CL}	Current limit threshold	Device Version A, T_J = –40°C to 150°C	R_{ILIM} = GND, open, or out of range		14		A
			R_{ILIM} = 5 kΩ	8.32	10	12.62	A
			R_{ILIM} = 25 kΩ	1.325	2	3.2	A
		Device Version B, T_J = –40°C to 150°C	R_{ILIM} = GND, open, or out of range		26		A
			R_{ILIM} = 5 kΩ	14.97	18	22.72	A
			R_{ILIM} = 25 kΩ	2.7	3.6	4.5	A
K_{CL}	Current Limit Ratio	Version A			50		A * kΩ
		Version B			90		A * kΩ
FAULT CHARACTERISTICS							
V_{OL}	Open-load (OL) detection voltage	V_{EN} = 0 V, V_{DIA_EN} = 5 V, V_{SEL1} = 0 V		2	3	4	V
t_{OL1}	OL and STB indication-time from EN falling	V_{EN} = 5 V to 0 V, V_{DIA_EN} = 5 V, V_{SEL1} = 0 V I_{OUT} = 0 mA, V_{OUT} = 4 V		300	500	700	µs
t_{OL2}	OL and STB indication-time from DIA_EN rising	V_{EN} = 0 V, V_{DIA_EN} = 0 V to 5 V, V_{SEL1} = 0 V I_{OUT} = 0 mA, V_{OUT} = 4 V		2	20	50	µs
t_{OL3}	OL and STB indication-time from VOUT rising	V_{EN} = 0 V, V_{DIA_EN} = 5 V, V_{SEL1} = 0 V I_{OUT} = 0 mA, V_{OUT} = 0 V to 4 V		2	20	50	µs
T_{ABS}	Thermal shutdown			150			°C
T_{REL}	Relative thermal shutdown				60		°C
T_{HYS}	Thermal shutdown hysteresis			20	25	30	°C

7.5 Electrical Characteristics (continued)

V_{BB} = 6 V to 18 V, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{FAULT}	Fault shutdown indication-time	V_{DIA_EN} = 5 V Time between switch shutdown and I_{SNS} settling at I_{SNSFH}			50	µs
t_{RETRY}	Retry time	Time from fault shutdown until switch re-enable (thermal shutdown or current limit).	1	2	3	ms
EN PIN CHARACTERISTICS						
$V_{IL, EN}$	Input voltage low-level	No GND network diode			0.8	V
$V_{IH, EN}$	Input voltage high-level	No GND network diode	2.0			V
$V_{IHYS, EN}$	Input voltage hysteresis			350		mV
R_{EN}	Internal pulldown resistor		0.5	1	2	MΩ
$I_{IL, EN}$	Input current low-level	V_{EN} = 0.8 V		0.8		µA
$I_{IH, EN}$	Input current high-level	V_{EN} = 5 V		5.0		µA
DIA_EN PIN CHARACTERISTICS						
V_{IL, DIA_EN}	Input voltage low-level	No GND network diode			0.8	V
V_{IH, DIA_EN}	Input voltage high-level	No GND network diode	2.0			V
V_{IHYS, DIA_EN}	Input voltage hysteresis			350		mV
R_{DIA_EN}	Internal pulldown resistor		0.5	1	2	MΩ
I_{IL, DIA_EN}	Input current low-level	V_{DIA_EN} = 0.8 V		0.8		µA
I_{IH, DIA_EN}	Input current high-level	V_{DIA_EN} = 5 V		5.0		µA
SEL1 PIN CHARACTERISTICS						
$V_{IL, SEL1}$	Input voltage low-level	No GND network diode			0.8	V
$V_{IH, SEL1}$	Input voltage high-level	No GND network diode	2.0			V
$V_{IHYS, SEL1}$	Input voltage hysteresis			350		mV
R_{SEL1}	Internal pulldown resistor		0.5	1	2	MΩ
$I_{IL, SEL1}$	Input current low-level	V_{SEL1} = 0.8 V		0.8		µA
$I_{IH, SEL1}$	Input current high-level	V_{SEL1} = 5 V		5.0		µA
LATCH PIN CHARACTERISTICS						
$V_{IL, LATCH}$	Input voltage low-level	No GND network diode			0.8	V
$V_{IH, LATCH}$	Input voltage high-level	No GND network diode	2.0			V
$V_{IHYS, LATCH}$	Input voltage hysteresis			350		mV
R_{LATCH}	Internal pulldown resistor		0.5	1	2	MΩ
$I_{IL, LATCH}$	Input current low-level	V_{LATCH} = 0.8 V		0.8		µA
$I_{IH, LATCH}$	Input current high-level	V_{LATCH} = 5 V		5.0		µA

7.6 SNS Timing Characteristics

V_{BB} = 6 V to 18 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNS TIMING - CURRENT SENSE						
$t_{SNSION1}$	Settling time from rising edge of DIA_EN	V_{EN} = 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			40	µs
$t_{SNSION2}$	Settling time from rising edge of EN and DIA_EN	V_{EN} = V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			200	µs
$t_{SNSION3}$	Settling time from rising edge of EN	V_{EN} = 0 V to 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			165	µs

V_{BB} = 6 V to 18 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SNSIOFF1}$	Settling time from falling edge of DIA_EN	V_{EN} = 5 V, V_{DIA_EN} = 5 V to 0 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			20	µs
$t_{SETTLEH}$	Settling time from rising edge of load step	V_{EN} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 1 A to 5 A			20	µs
$t_{SETTLEL}$	Settling time from falling edge of load step	V_{EN} = 5 V, V_{DIA_EN} = 5 V R_{SNS} = 1 kΩ, I_{OUT} = 5 A to 1 A			20	µs
SNS TIMING - TEMPERATURE SENSE						
$t_{SNSTON1}$	Settling time from rising edge of DIA_EN	V_{EN} = 5 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ			40	µs
$t_{SNSTON2}$	Settling time from rising edge of DIA_EN	V_{EN} = 0 V, V_{DIA_EN} = 0 V to 5 V R_{SNS} = 1 kΩ			70	µs
$t_{SNSTOFF}$	Settling time from falling edge of DIA_EN	V_{EN} = X, V_{DIA_EN} = 5 V to 0 V R_{SNS} = 1 kΩ			20	µs
SNS TIMING - MULTIPLEXER						
t_{MUX}	Settling time from temperature sense to current sense	V_{EN} = 5 V, V_{DIA_EN} = 5 V V_{SEL1} = 5 V to 0 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			60	µs
	Settling time from current sense to temperature sense	V_{EN} = 5 V, V_{DIA_EN} = 5 V V_{SEL1} = 0 V to 5 V R_{SNS} = 1 kΩ, R_L ≤ 6 Ω			60	µs

7.7 Switching Characteristics

V_{BB} = 13.5 V, T_J = -40°C to +150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DR}	Turnon delay time (from Active)	V_{BB} = 13.5 V, R_L ≤ 6 Ω 50% EN rising to 10% V_{OUT} rising	20	60	100	µs
t_{DF}	Turnoff delay time	V_{BB} = 13.5 V, R_L ≤ 6 Ω 50% EN falling to 90% V_{OUT} Falling	20	60	100	µs
SR_R	VOUT rising slew rate	V_{BB} = 13.5 V, 20% to 80% of V_{OUT} rising, R_L ≤ 6 Ω	0.1	0.4	0.7	V/µs
SR_F	VOUT falling slew rate	V_{BB} = 13.5 V, 80% to 20% of V_{OUT} falling, R_L ≤ 6 Ω	0.1	0.4	0.7	V/µs
t_{ON}	Turnon time (active)	V_{BB} = 13.5 V, R_L ≤ 6 Ω, 50% EN rising to 80% V_{OUT} rising	39	94	235	µs
t_{OFF}	Turnoff time	V_{BB} = 13.5 V, R_L ≤ 6 Ω, 50% EN falling to 20% V_{OUT} falling	39	94	235	µs
Δ_{PWM}	PWM accuracy - average load current	200-µs enable pulse, V_S = 13.5 V, R_L = 6 Ω	–25	0	25	%
t_{ON} - t_{OFF}	Turnon and turnoff matching	200-µs enable pulse, R_L ≤ 6 Ω	–85	0	85	µs
E_{ON}	Switching energy losses during turnon	V_{BB} = 13.5 V, R_L ≤ 6 Ω		0.7		mJ
E_{OFF}	Switching energy losses during turnoff	V_{BB} = 13.5 V, R_L ≤ 6 Ω		0.7		mJ

7.8 Typical Characteristics

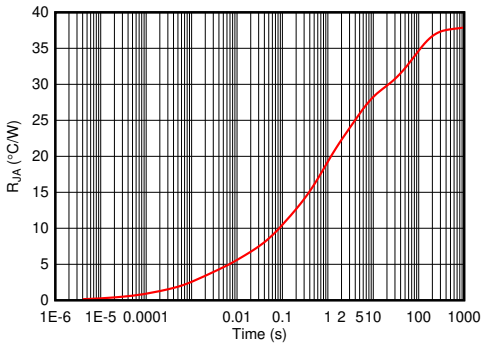
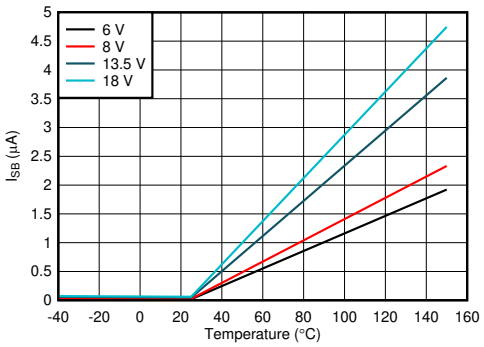
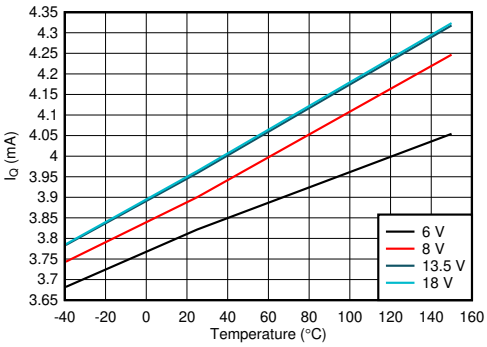


Figure 7-1. Transient Thermal Impedance



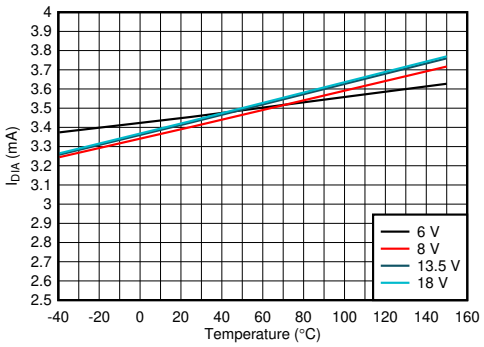
V_{OUT} = 0 V V_{EN} = 0 V V_{DIAG_EN} = 0 V

Figure 7-2. Standby Current (I_{SB}) vs Temperature



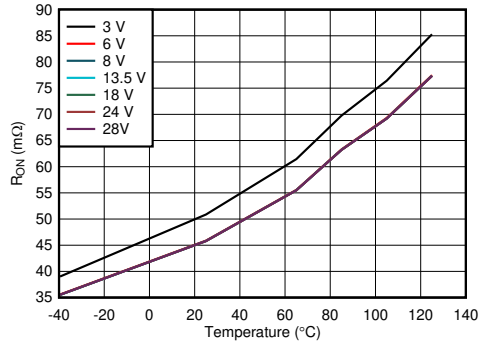
I_{OUT} = 0 A V_{EN} = 5 V V_{DIAG_EN} = 5 V
R_{SNS} = 1 kΩ V_{SEL1} = 0 V

Figure 7-3. Quiescent Current (I_Q) vs Temperature



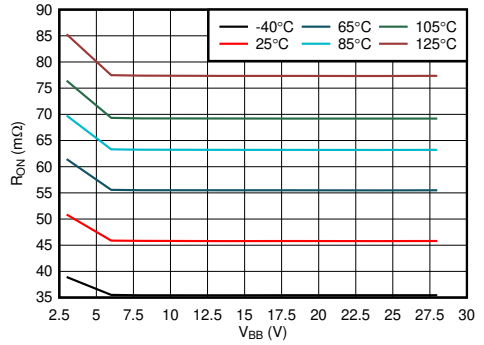
I_{OUT} = 0 A V_{EN} = 0 V V_{DIAG_EN} = 5 V
R_{SNS} = 1 kΩ V_{SEL1} = 0 V

Figure 7-4. Diag enable Current (I_{DIA}) vs Temperature



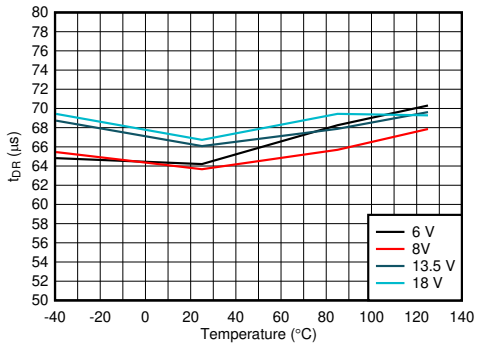
I_{OUT} = 200 mA V_{EN} = 5 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ

Figure 7-5. On Resistance (R_{ON}) vs Temperature



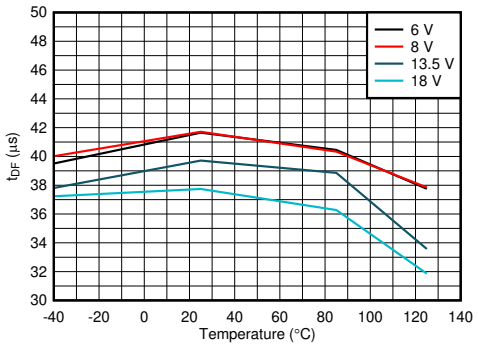
I_{OUT} = 200 mA V_{EN} = 5 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ

Figure 7-6. On Resistance (R_{ON}) vs V_{BB}



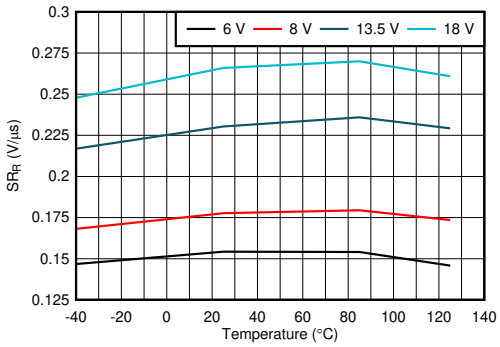
R_{OUT} = 6 Ω V_{EN} = 0 V to 5 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

Figure 7-7. Turn-on Delay Time (t_{DR}) vs Temperature



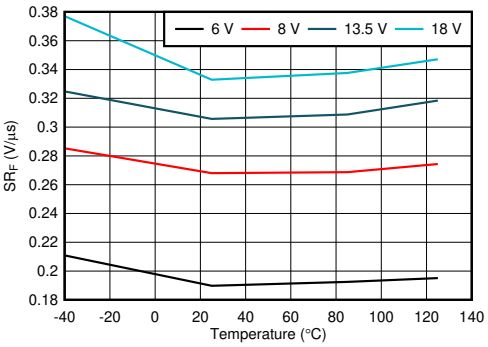
R_{OUT} = 6 Ω V_{EN} = 5 V to 0 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

Figure 7-8. Turn-off Delay Time (t_{DF}) vs Temperature



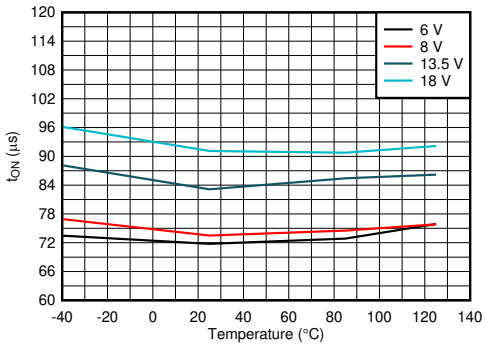
R_{OUT} = 6 Ω V_{EN} = 0 V to 5 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

Figure 7-9. V_{OUT} Slew Rate Rising (SR_R) vs Temperature



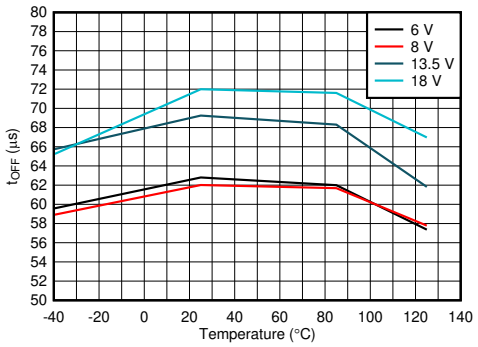
R_{OUT} = 6 Ω V_{EN} = 5 V to 0 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

Figure 7-10. V_{OUT} Slew Rate Falling (SR_F) vs Temperature



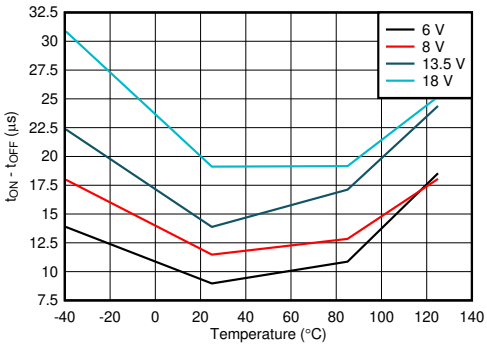
R_{OUT} = 6 Ω V_{EN} = 0 V to 5 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

Figure 7-11. Turn-on Time (t_{ON}) vs Temperature



R_{OUT} = 6 Ω V_{EN} = 5 V to 0 V V_{DIAG_EN} = 0 V
R_{SNS} = 1 kΩ V_{BB} = 13.5 V

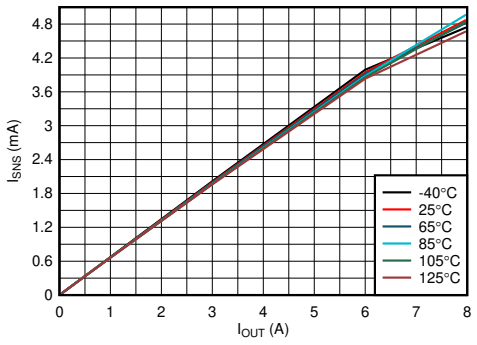
Figure 7-12. Turn-off Time (t_{OFF}) vs Temperature



R_{OUT} = 6 Ω V_{EN} = 0 V to 5 V and 5 V to 0 V V_{DIAG_EN} = 0 V

R_{SNS} = 1 kΩ V_{BB} = 13.5 V

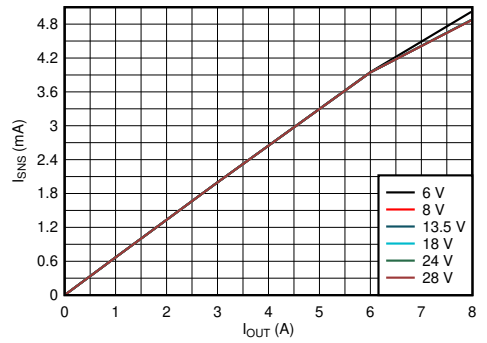
Figure 7-13. Turn-on and Turn-off Matching (t_{ON} - t_{OFF}) vs Temperature



V_{SEL} = 0 V V_{EN} = 5 V V_{DIAG_EN} = 5 V

R_{SNS} = 1 kΩ V_{BB} = 13.5 V

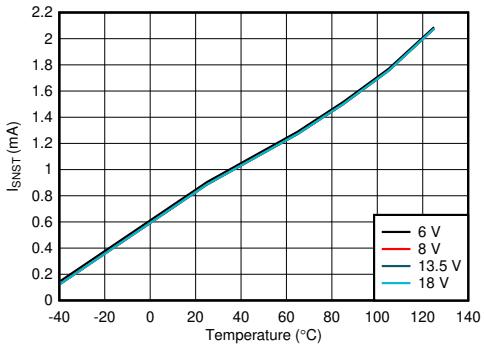
Figure 7-14. Current Sense Output Current (I_{SNSI}) vs Load Current (I_{OUT}) Across Temperature



V_{SEL} = 0 V V_{EN} = 5 V V_{DIAG_EN} = 5 V

R_{SNS} = 1 kΩ T_A = 25°C

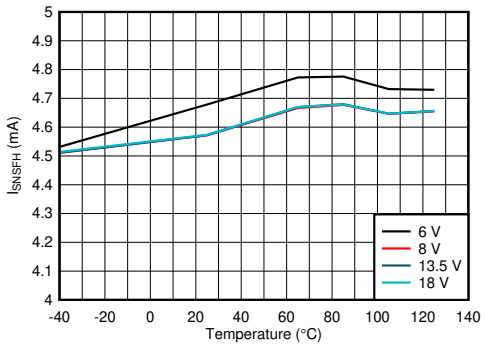
Figure 7-15. Current Sense Output Current (I_{SNSI}) vs Load Current (I_{OUT}) Across V_{BB}



V_{SEL} = 5 V V_{EN} = 0 V V_{DIAG_EN} = 5 V

R_{SNS} = 1 kΩ

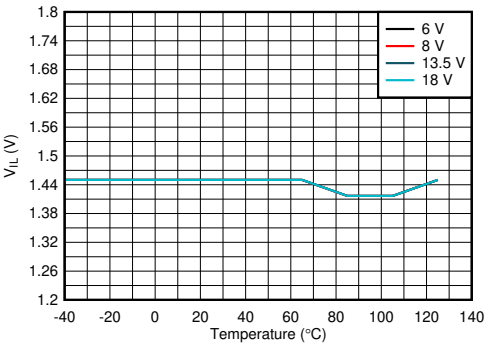
Figure 7-16. Temperature Sense Output Current (I_{SNST}) vs Temperature



V_{SEL} = 0 V V_{EN} = 0 V V_{DIAG_EN} = 5 V

R_{SNS} = 1 kΩ V_{OUT} Floating

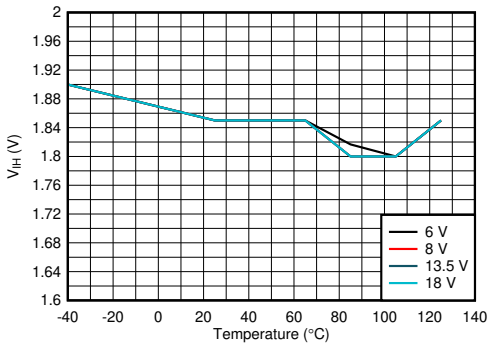
Figure 7-17. Fault High Output Current (I_{SNSFH}) vs Temperature



V_{EN} = 3.3 V to 0 V V_{OUT} = 0 V V_{DIAG_EN} = 0 V

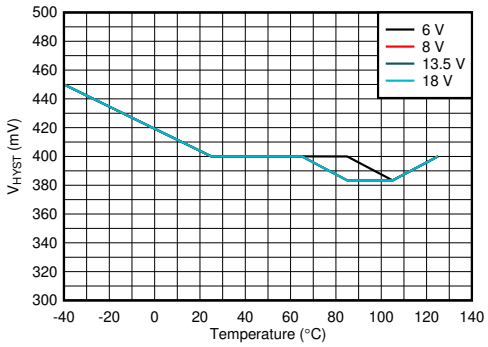
R_{OUT} = 1 kΩ V_{BB} = 13.5 V

Figure 7-18. V_{IL} vs Temperature



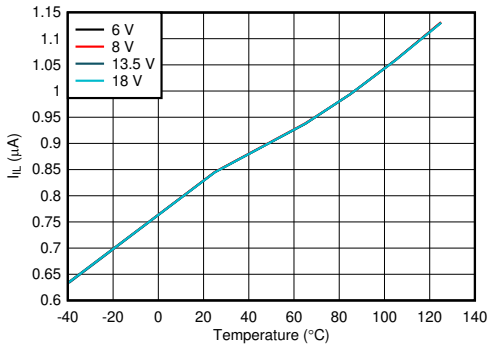
V_{EN} = 0 V to 3.3 V V_{OUT} = 13.5 V V_{DIAG_EN} = 0 V
R_{OUT} = 1 kΩ V_{BB} = 13.5 V

Figure 7-19. V_{IH} vs Temperature



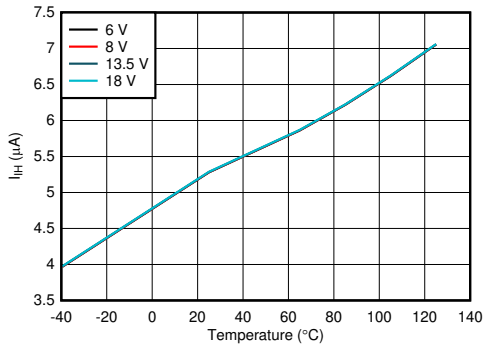
V_{EN} = 0 V to 3.3 V and 3.3 V to 0 V V_{OUT} = 0 V V_{DIAG_EN} = 0 V
R_{OUT} = 1 kΩ V_{BB} = 13.5 V

Figure 7-20. V_{HYST} vs Temperature



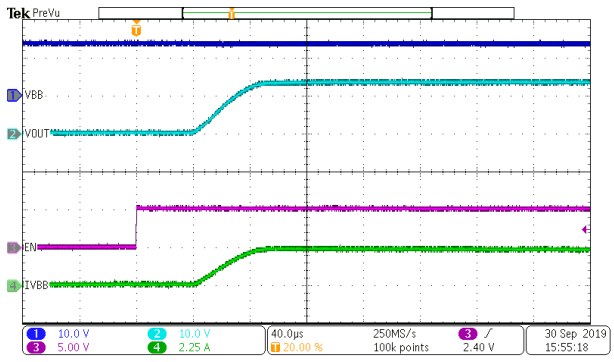
V_{EN} = 0.8 V V_{OUT} = 0 V V_{DIAG_EN} = 0 V
R_{OUT} = 1 kΩ V_{BB} = 13.5 V

Figure 7-21. I_{IL} vs Temperature



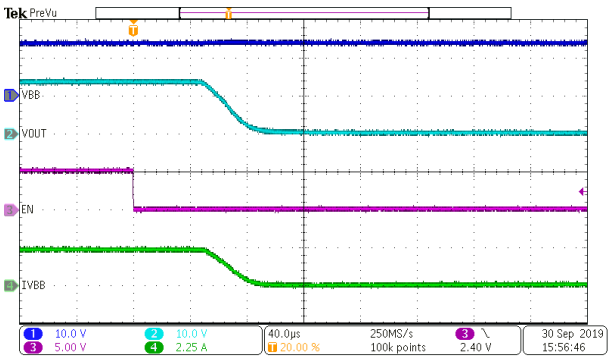
V_{EN} = 5 V V_{OUT} = 13.5V V V_{DIAG_EN} = 0 V
R_{OUT} = 1 kΩ V_{BB} = 13.5 V

Figure 7-22. I_{IH} vs Temperature



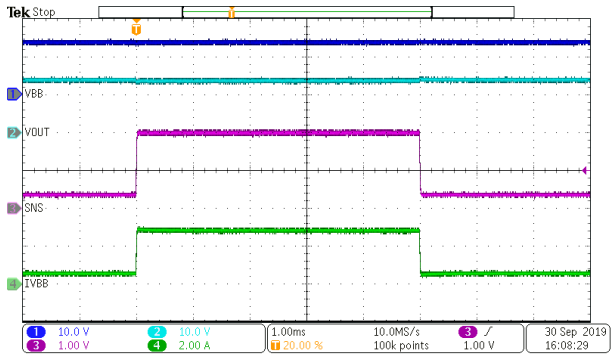
R_{OUT} = 6 Ω R_{SNS} = 1 kΩ V_{DIA_EN} = 5 V
V_{SEL} = 0 V

Figure 7-23. Turn-on Time (t_{ON})



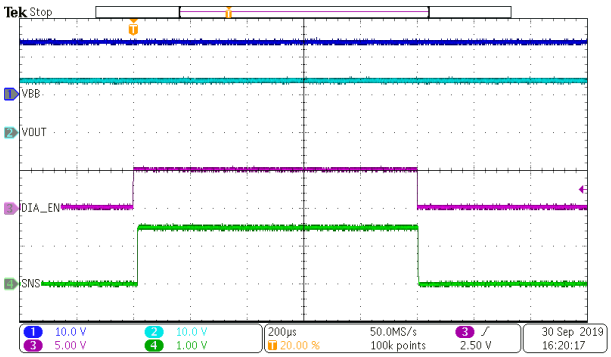
R_{OUT} = 6 Ω R_{SNS} = 1 kΩ V_{DIA_EN} = 5 V
V_{SEL} = 0 V

Figure 7-24. Turn-off Time (t_{OFF})



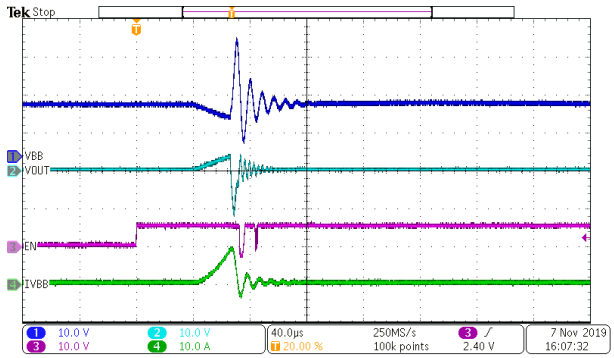
R_{OUT} =13 Ω to 6 Ω R_{SNS} = 1 kΩ V_{SEL} = 0 V
I_{OUT} = 1 A to 3 A V_{BB} = 13.5 V

Figure 7-25. I_{SNS} Settling time ($t_{SNSION1}$) on Load Step



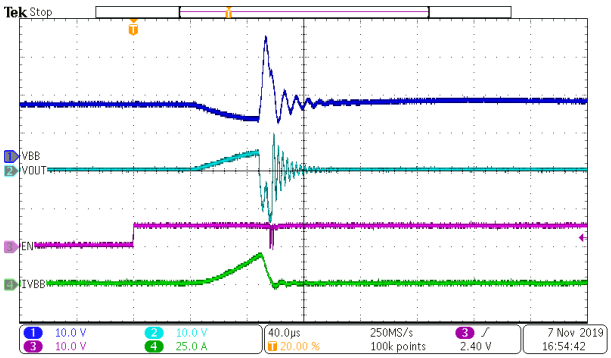
V_{BB} = 13.5 V T_A = 25°C I_{OUT} = 3 A
V_{EN} = 0 V to 5 V

Figure 7-26. SNS Output Current Measurement Enable on DIAG_EN PWM



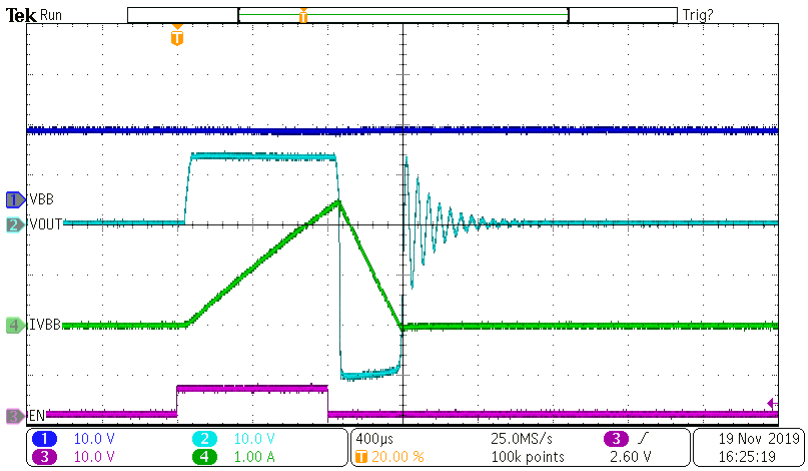
L_{OUT} = 5 µH to GND R_{LIM} = 5 kΩ V_{SEL} = 0 V
V_{EN} = 0 V to 5 V V_{DIAG_EN} = 5 V T_A = 25°C

Figure 7-27. Device Version A Short Circuit Event



L_{OUT} = 5 µH to GND R_{LIM} = 5 kΩ V_{SEL} = 0 V
V_{EN} = 0 V to 5 V V_{DIAG_EN} = 5 V T_A = 25°C

Figure 7-28. Device Version B Short Circuit Event



V_{BB} = 13.5 V T_A = 25°C L_{OUT} = 5 mH

Figure 7-29. 5 mH Inductive Load Demagnetization

8 Parameter Measurement Information

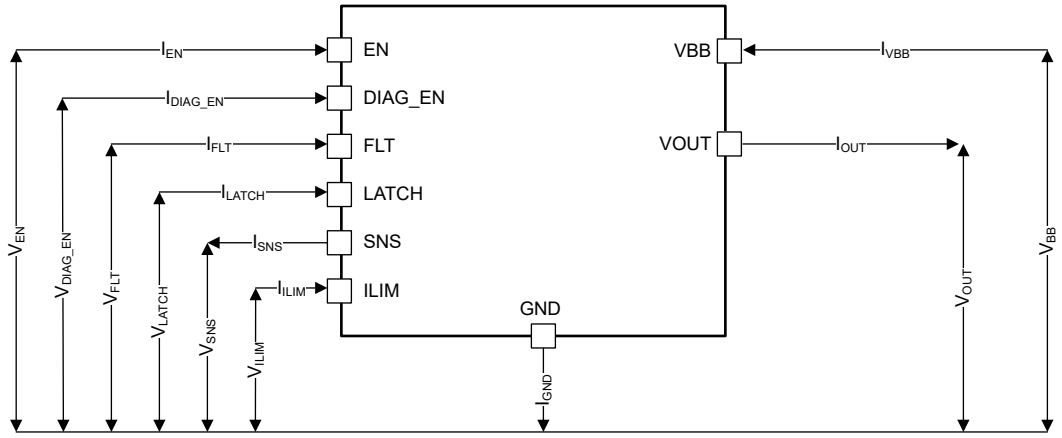
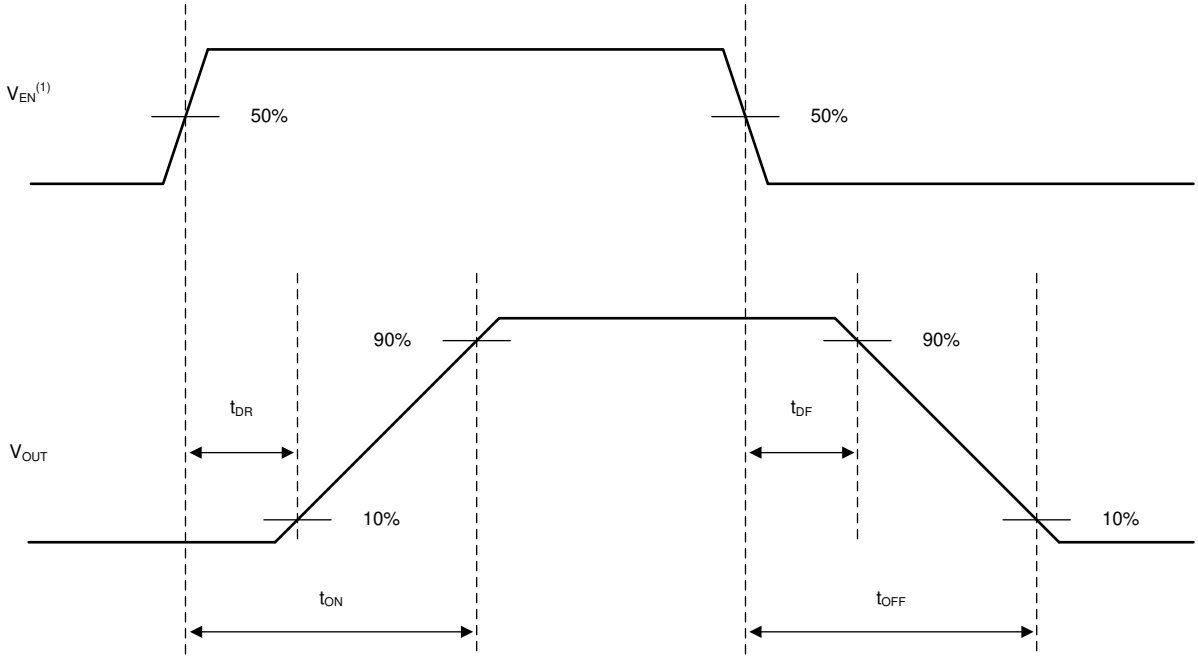
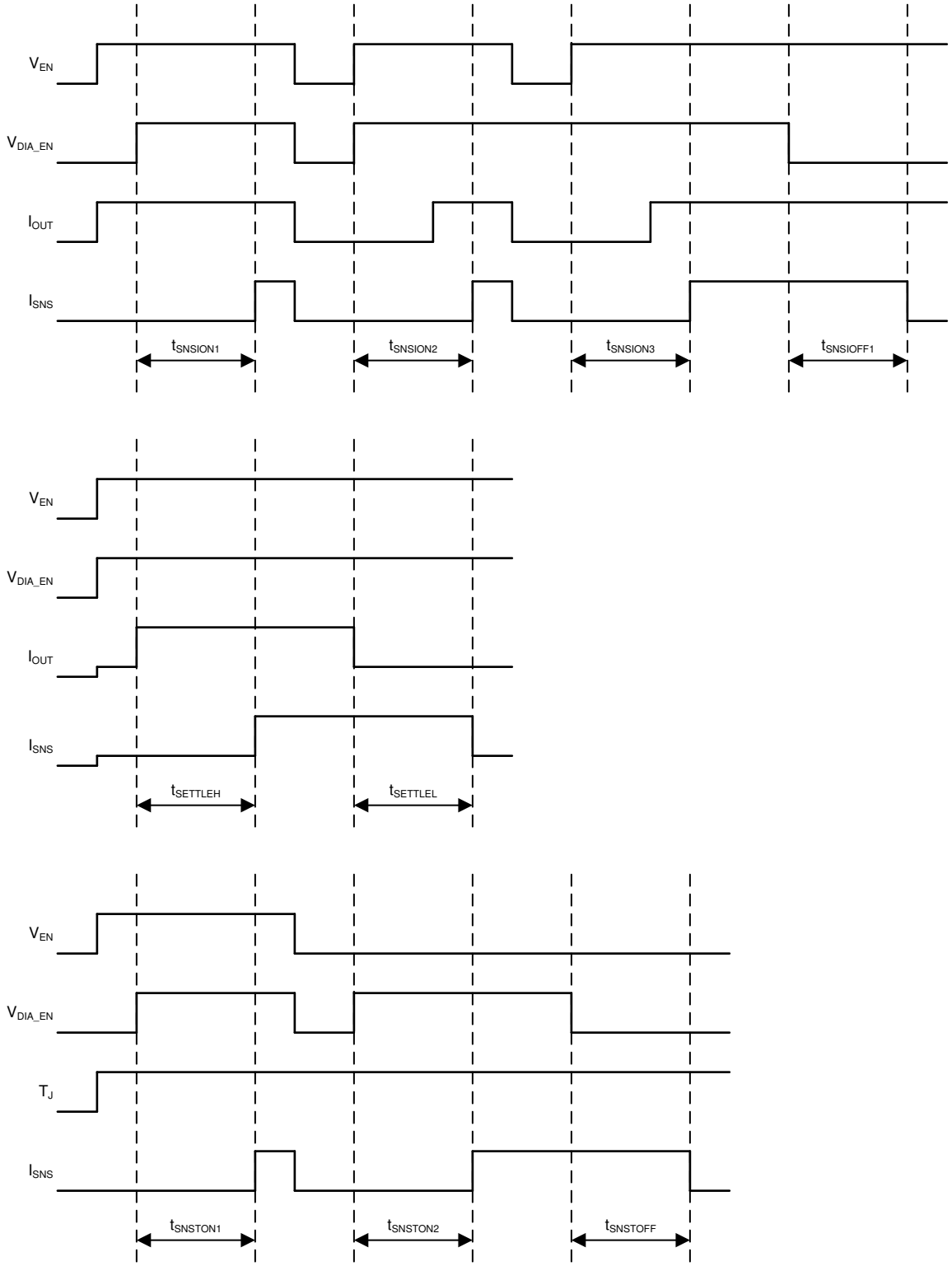


Figure 8-1. Parameter Definitions



Rise and fall time of V_{EN} is 100 ns.

Figure 8-2. Switching Characteristics Definitions



Rise and fall times of control signals are 100 ns. Control signals include: EN, DIA_EN.

Figure 8-3. SNS Timing Characteristics Definitions

9 Detailed Description

9.1 Overview

The TPS1HB50-Q1 device is a single-channel smart high-side switch intended for use with 12-V automotive batteries. Many protection and diagnostic features are integrated in the device.

Diagnostics features include the analog SNS output that is capable of providing a signal that is proportional to load current or device temperature. The high-accuracy load current sense allows for diagnostics of complex loads.

This device includes protection through thermal shutdown, current limiting, transient withstand, and reverse battery operation. For more details on the protection features, refer to the *Feature Description* and *Application Information* sections of the document.

The TPS1HB50-Q1 is one device in a family of TI high side switches. For each device, the part number indicates elements of the device behavior. Figure 9-1 gives an example of the device nomenclature.

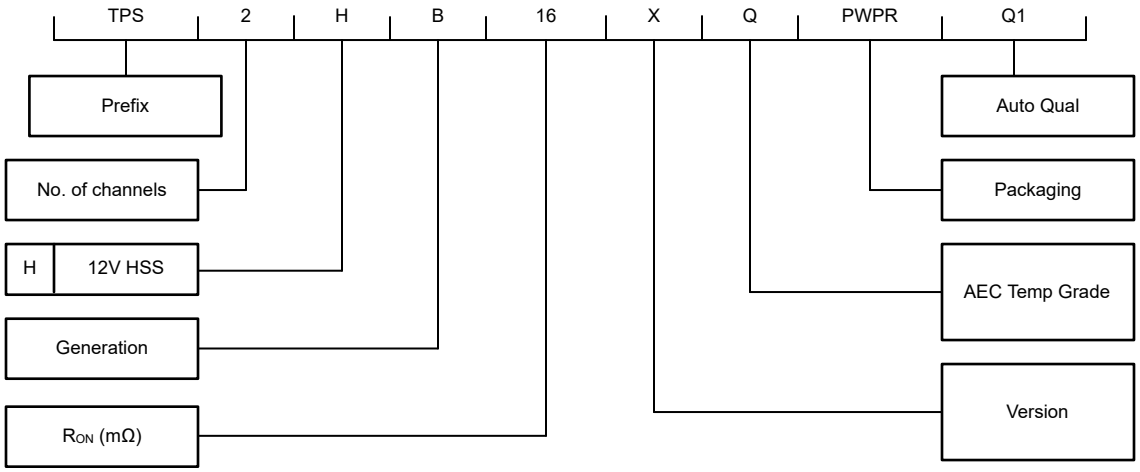
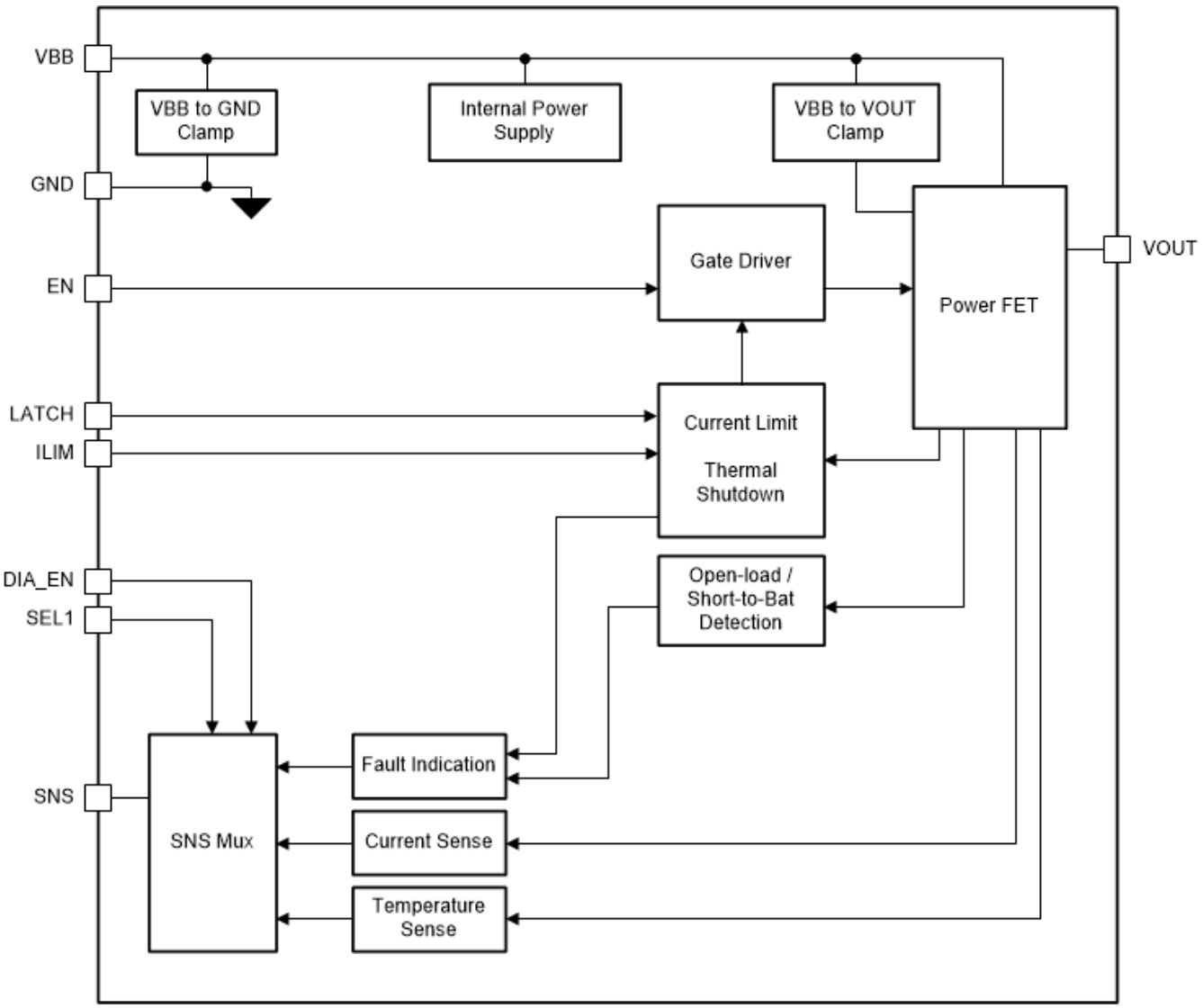


Figure 9-1. Naming Convention

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Protection Mechanisms

The TPS1HB50-Q1 is designed to operate in the automotive environment. The protection mechanisms allow the device to be robust against many system-level events such as load dump, reverse battery, short-to-ground, and more.

There are two protection features which, if triggered, will cause the switch to automatically disable:

- Thermal Shutdown
- Current Limit

When any of these protections are triggered, the device will enter the FAULT state. In the FAULT state, the fault indication will be available on the SNS pin (see the *Diagnostic Mechanisms* section of the data sheet for more details).

The switch is no longer held off and the fault indication is reset when all of the below conditions are met:

- LATCH pin is low
- t_{RETRY} has expired

- All faults are cleared (thermal shutdown, current limit)

9.3.1.1 Thermal Shutdown

The TPS1HB50-Q1 includes a temperature sensor on the power FET and also within the controller portion of the device. There are two cases that the device will consider to be a thermal shutdown fault:

- $T_{J,FET} > T_{ABS}$
- $(T_{J,FET} – T_{J,controller}) > T_{REL}$

After the fault is detected, the switch will turn off. If $T_{J,FET}$ passes T_{ABS}, the fault is cleared when the switch temperature decreases by the hysteresis value, T_{HYS}. If instead the T_{REL} threshold is exceeded, the fault is cleared after T_{RETRY} passes.

9.3.1.2 Current Limit

When I_{OUT} reaches the current limit threshold, I_{CL}, the channel will switch off immediately. The I_{CL} value will vary with slew rate and a fast current increase that occurs during a powered-on short circuit can temporarily go above the specified I_{CL} value. When the switch is in the FAULT state it will output an output current I_{SNSFH} on the SNS pin .

During a short circuit event, the device will hit the I_{CL} value that is listed in the Electrical Characteristics table (for the given device version and R_{ILIM}) and then turn the output off to protect the device. The device will register a short circuit event when the output current exceeds I_{CL}, however the measured maximum current may exceed the I_{CL} value due to the TPS1HB50-Q1 deglitch filter and turn-off time. This deglitch time is defined at 3 µs so therefore use the test setup described in *AEC-Q100-012 Short Circuit Reliability* and take 3 µs before the peak value as the I_{CL}. The device is guaranteed to protect itself during a short circuit event over the nominal supple voltage range (as defined in the Electrical Characteristics table) at 125°C.

9.3.1.2.1 Current Limit Foldback

Version B of the TPS1HB50-Q1 implements a current limit foldback feature that is designed to protect the device in the case of a long-term fault condition. If the device undergoes fault shutdown events (either of thermal shutdown or current limit) seven consecutive times, the current limit will be reduced to half of the original value. The device will revert back to the original current limit threshold if either of the following occurs:

- The device goes to standby mode.
- The switch turns on and turns off without any fault occurring.

Version A does not implement the current limit foldback due to the lower current limit causing less harm during repetitive long-term faults.

9.3.1.2.2 Programmable Current Limit

All versions of the TPS1HB50-Q1 include an adjustable current limit. Some applications (for example, incandescent bulbs) will require a high current limit while other applications can benefit from a lower current limit threshold. In general, wherever possible a lower current limit is recommended due to allowing system advantages through:

- Reduced size and cost in current carrying components such as PCB traces and module connectors
- Less disturbance at the power supply (V_{BB} pin) during a short circuit event
- Improved protection of the downstream load

To set the current limit threshold, connect a resistor from I_{LIM} to V_{BB}. The current limit threshold is determined by Equation 1 (R_{ILIM} in kΩ):

$$I_{CL} = K_{CL} / R_{ILIM} \quad (1)$$

The R_{ILIM} range is between 5 kΩ and 25 kΩ . An R_{ILIM} resistor is required, however in the fault case where the pin is floating, grounded, or outside of this range the current limit will default to an internal level that is defined in

the *Specifications* section of this document. If R_{ILIM} is out of this range, the device cannot guarantee complete short-circuit protection.

Note

Capacitance on the I_{LIM} pin can cause I_{LIM} to go out of range during short circuit events. For accurate current limiting, place R_{ILIM} near to the device with short traces to ensure < 5-pF capacitance to GND on the I_{LIM} pin.

9.3.1.2.3 Undervoltage Lockout (UVLO)

The device monitors the supply voltage V_{BB} to prevent unpredicted behaviors in the event that the supply voltage is too low. When the supply voltage falls down to V_{UVLOF}, the output stage is shut down automatically. When the supply rises up to V_{UVLOR}, the device turns back on.

During an initial ramp of V_{BB} from 0 V at a ramp rate slower than 1 V/ms, V_{EN} pin will have to be held low until V_{BB} is above UVLO threshold (with respect to board ground) and the supply voltage to the device has reliably reached above the UVLO condition. For best operation, ensure that V_{BB} has risen above UVLO before setting the V_{EN} pin to high.

9.3.1.2.4 V_{BB} During Short-to-Ground

When V_{OUT} is shorted to ground, the module power supply (V_{BB}) can have a transient decrease. This is caused by the sudden increase in current flowing through the wiring harness cables. To achieve ideal system behavior, it is recommended that the module maintain V_{BB} > 3 V (above the maximum V_{UVLOF}) during V_{OUT} short-to-ground. This is typically accomplished by placing bulk capacitance on the power supply node.

9.3.1.3 Voltage Transients

The TPS1HB50-Q1 device contains two types of voltage clamps which protect the FET against system-level voltage transients. The two different clamps are shown in Figure 9-2.

The clamp from V_{BB} to GND is primarily used to protect the controller from positive transients on the supply line (for example, ISO7637-2). The clamp from V_{BB} to V_{OUT} is primarily used to limit the voltage across the FET when switching off an inductive load. If the voltage potential from V_{BB} to GND exceeds the V_{BB} clamp level, the clamp will allow current to flow through the device from V_{BB} to GND (path 2). If the voltage potential from V_{BB} to V_{OUT} exceeds the clamping voltage, the power FET will allow current to flow from V_{BB} to V_{OUT} (path 3). Additional capacitance from V_{BB} to GND can increase the reliability of the system during ISO 7637 pulse 2-A testing.

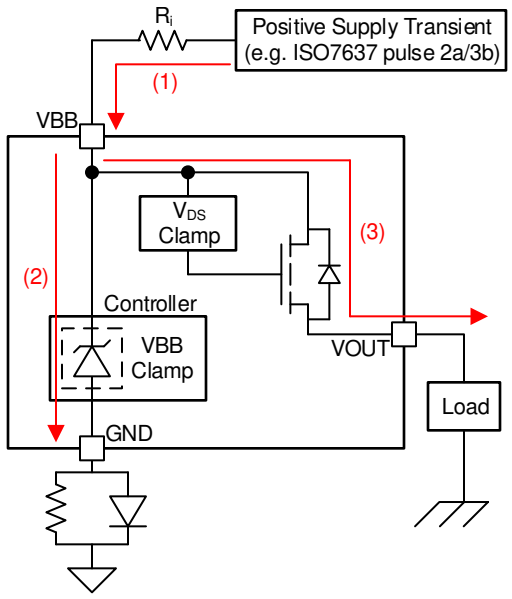


Figure 9-2. Current Path During Supply Voltage Transient

9.3.1.3.1 Load Dump

The TPS1HB50-Q1 device is tested according to ISO 16750-2:2010(E) suppressed load dump pulse. The device supports up to 40-V load dump transient and will maintain normal operation during the load dump pulse. If the switch is enabled, it will stay enabled and if the switch is disabled, it will stay disabled.

9.3.1.3.2 Driving Inductive Loads

When switching off an inductive load, the inductor may impose a negative voltage on the output of the switch. The TPS1HB50-Q1 includes a voltage clamp to limit voltage across the FET. The maximum acceptable load inductance is a function of the device robustness.

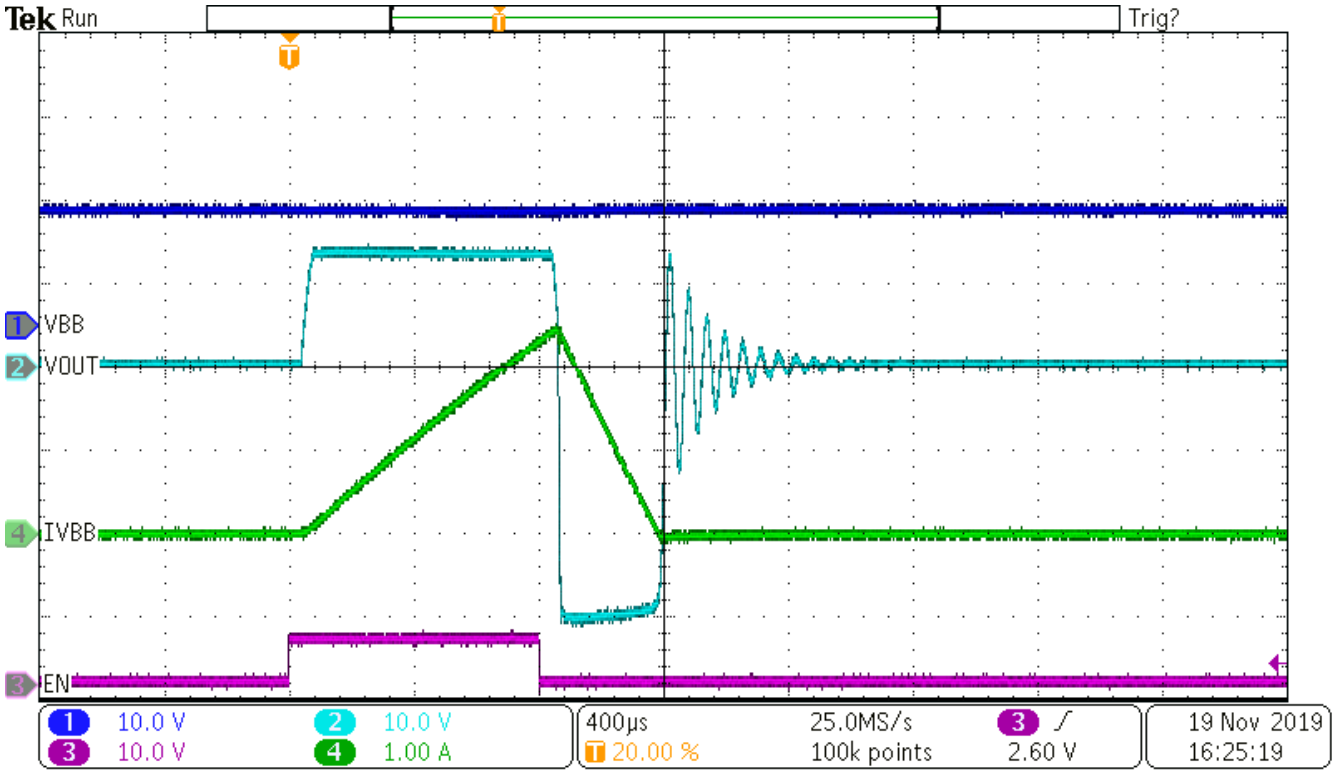


Figure 9-3. TPS1HB50-Q1 Inductive Discharge (5 mH)

For more information on driving inductive loads, refer to TI's *How To Drive Inductive, Capacitive, and Lighting Loads With Smart High Side Switches* application report.

9.3.1.4 Reverse Battery

In the reverse battery condition, the switch will automatically be enabled regardless of the state of EN to prevent excess power dissipation inside the MOSFET body diode. In many applications (for example, resistive loads), the full load current may be present during reverse battery. In order to activate the automatic switch on feature, SEL must have a path to ground from either from the MCU or it needs to be tied to ground through R_{PROT} if unused.

There are two options for blocking reverse current in the system. The first option is to place a blocking device (FET or diode) in series with the battery supply, blocking all current paths. The second option is to place a blocking diode in series with the GND node of the high-side switch. This method will protect the controller portion of the switch (path 2), but it will not prevent current from flowing through the load (path 3). The diode used for the second option may be shared amongst multiple high-side switches.

Path 1 shown in Figure 9-4 is blocked inside of the device.

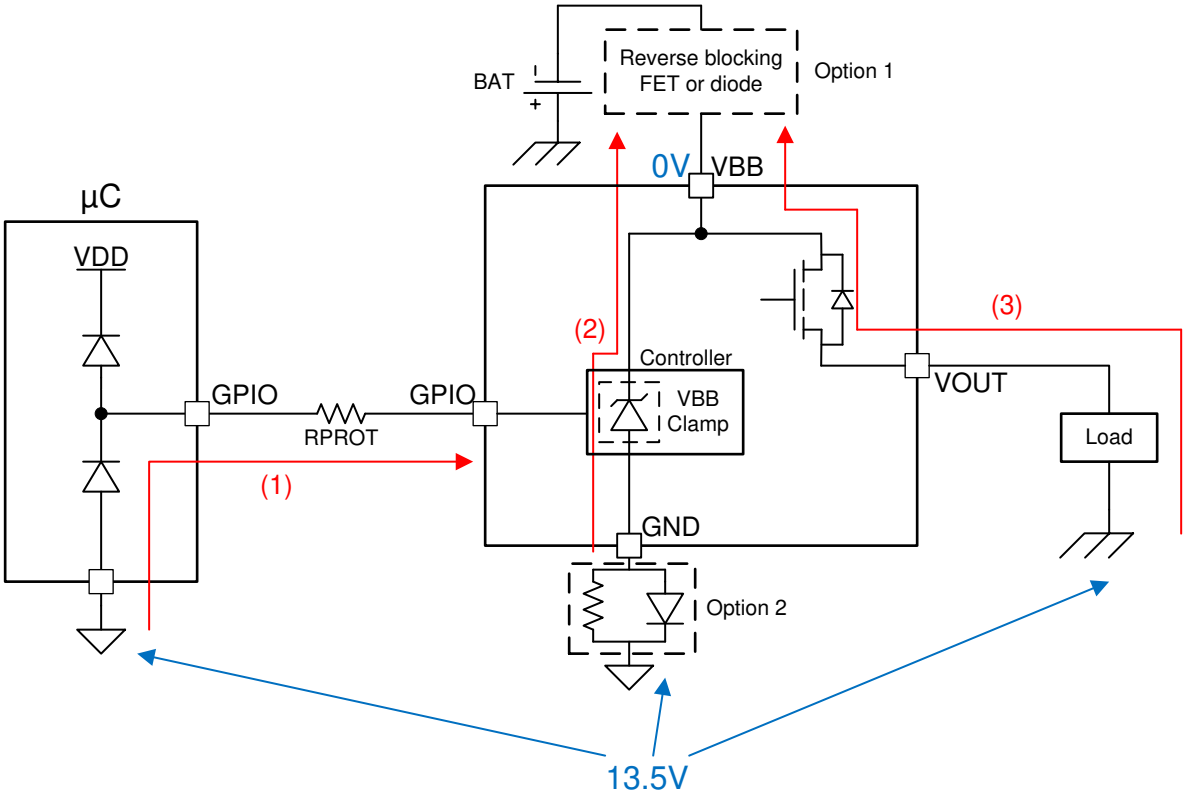


Figure 9-4. Current Path During Reverse Battery

For more information on reverse battery protection, refer to TI's *Reverse Battery Protection for High Side Switches* application note.

9.3.1.5 Fault Event – Timing Diagrams

Note

All timing diagrams assume that the SEL1 pin is low.

The LATCH, DIA_EN, and EN pins are controlled by the user. The timing diagrams represent a possible use-case.

Figure 9-5 shows the immediate current limit switch off behavior. The diagram also illustrates the retry behavior. As shown, the switch will remain latched off until the LATCH pin is low.

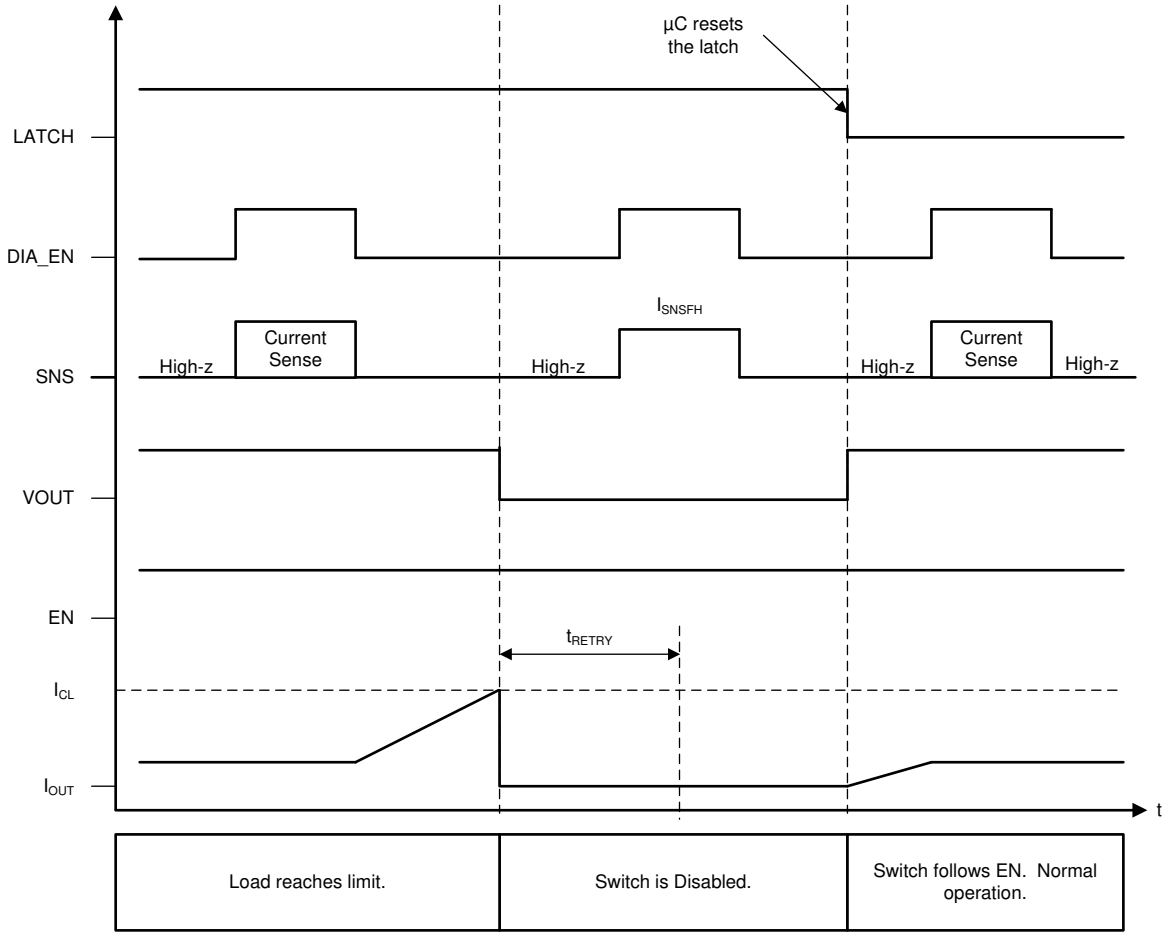


Figure 9-5. Current Limit – Version A and B - Latched Behavior

Figure 9-6 shows the immediate current limit switch off behavior. In this example, LATCH is tied to GND; hence, the switch will retry after the fault is cleared and t_{RETRY} has expired.

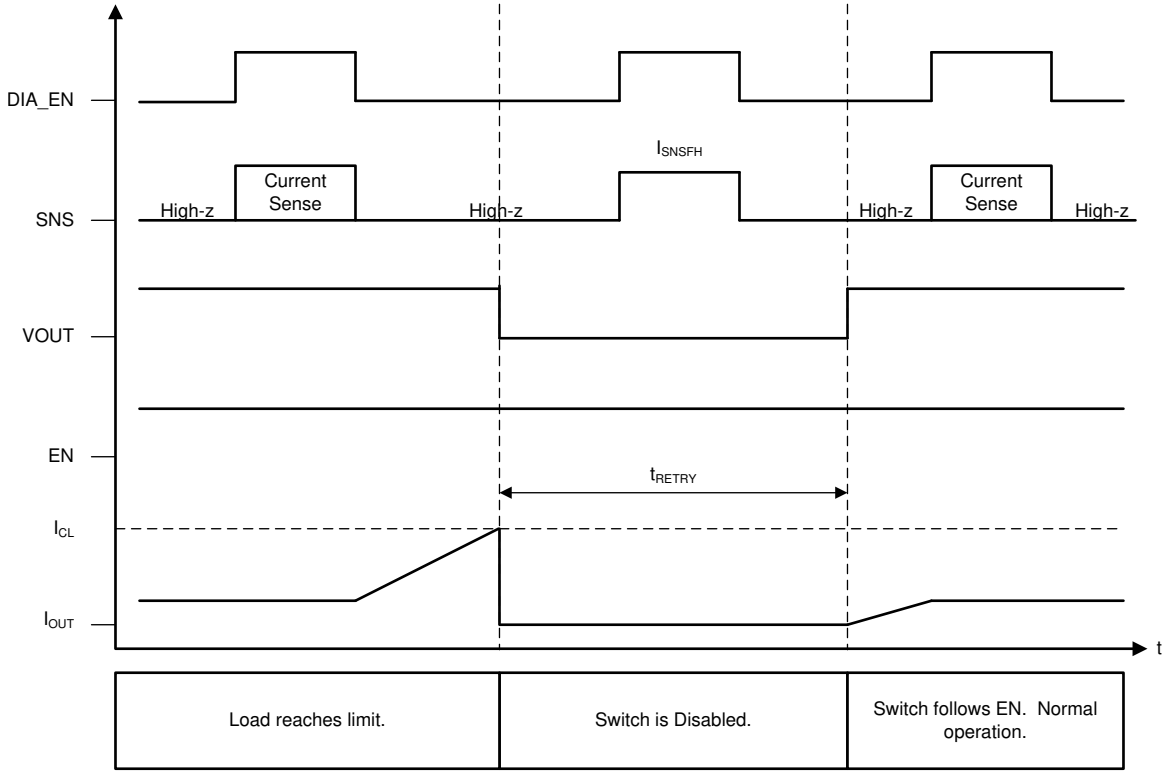


Figure 9-6. Current Limit - Version A and B - LATCH = 0

When the switch retries after a shutdown event, the SNS fault indication will remain until V_{OUT} has risen to V_{BB} – 1.8 V. Once V_{OUT} has risen, the SNS fault indication is reset and current sensing is available. If there is a short-to-ground and V_{OUT} is not able to rise, the SNS fault indication will remain indefinitely. Figure 9-7 illustrates auto-retry behavior and provides a zoomed-in view of the fault indication during retry.

Note

Figure 9-7 assumes that t_{RETRY} has expired by the time that T_J reaches the hysteresis threshold.

LATCH = 0 V and DIA_EN = 5 V

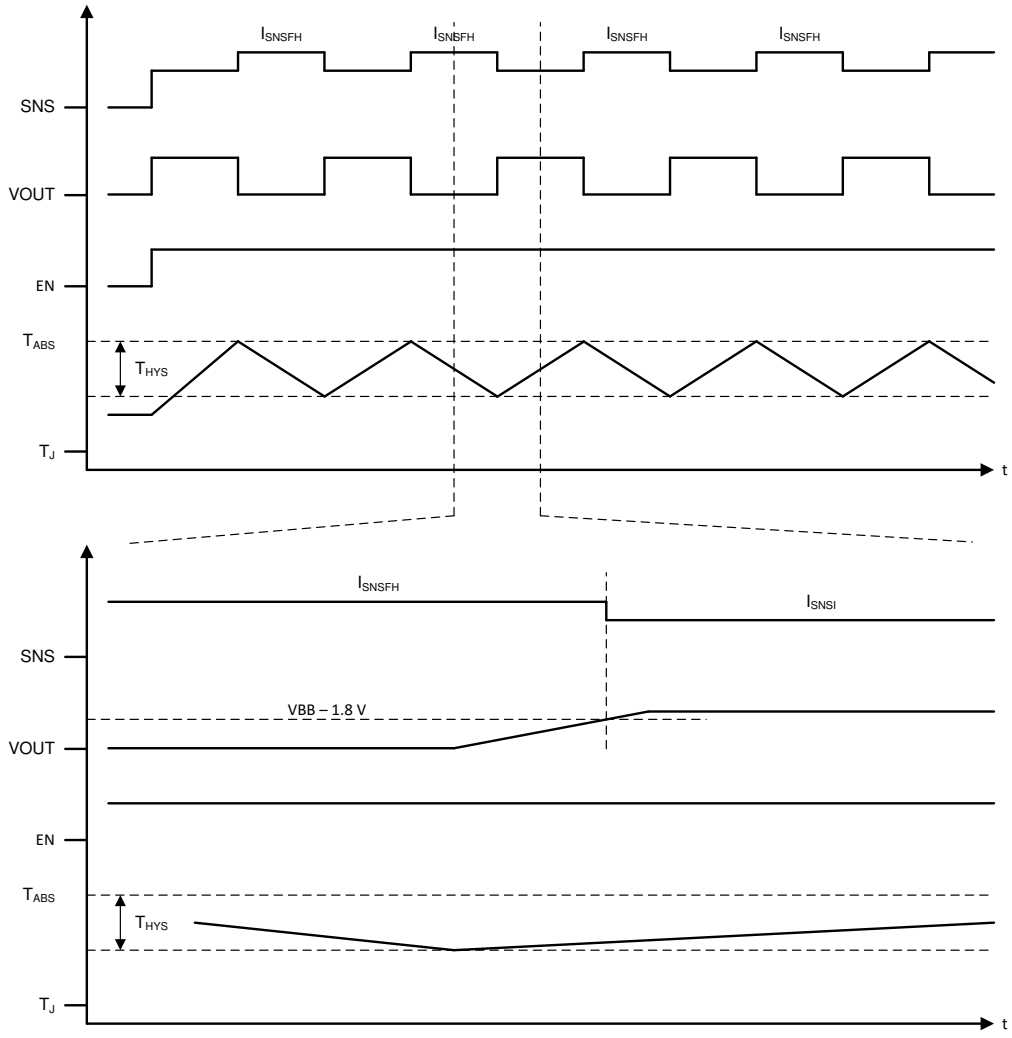


Figure 9-7. Fault Indication During Retry

9.3.2 Diagnostic Mechanisms

9.3.2.1 VOUT Short-to-Battery and Open-Load

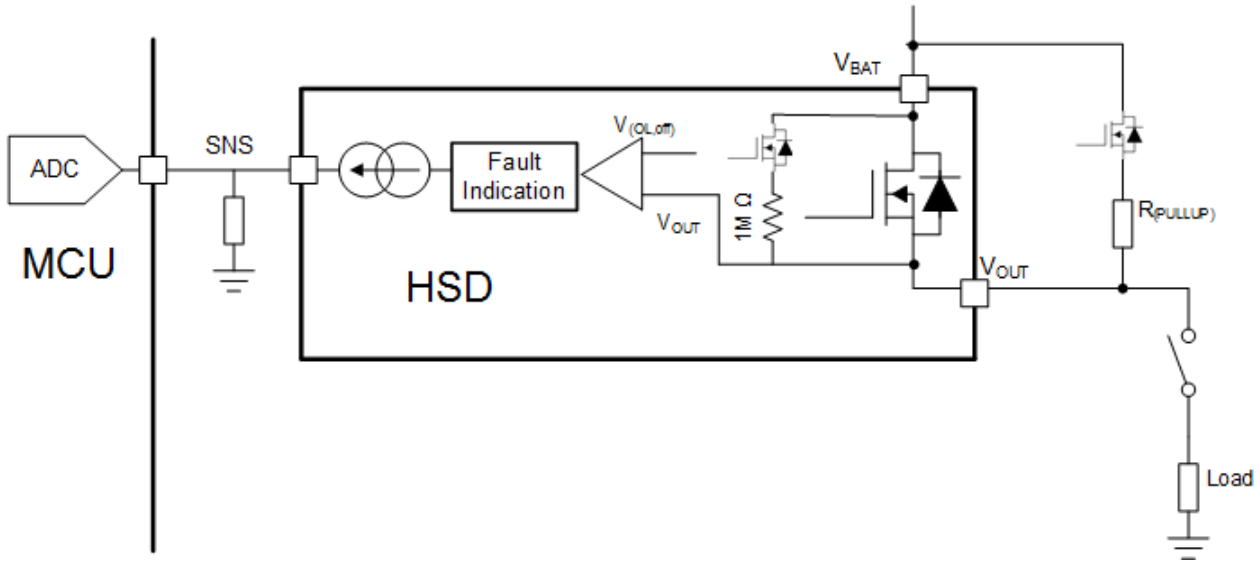
The TPS1HB50-Q1 is capable of detecting short-to-battery and open-load events regardless of whether the switch is turned on or off, however the two conditions use different methods.

9.3.2.1.1 Detection With Switch Enabled

When the switch is enabled, the VOUT short-to-battery and open-load conditions can be detected by the current sense feature. In both cases, the load current will be measured through the SNS pin as below the expected value.

9.3.2.1.2 Detection With Switch Disabled

While the switch is disabled, if DIA_EN is high, an internal comparator will detect the condition of V_{OUT}. If the load is disconnected (open load condition) or there is a short to battery the V_{OUT} voltage will be higher than the open load threshold ($V_{OL,off}$) and a fault is indicated on the SNS pin. An internal pull-up of 1 MΩ is in series with an internal MOSFET switch, so no external component is required if a completely open load must be detected. However, if there is significant leakage or other current draw even when the load is disconnected, a lower value pull-up resistor and switch can be added externally to set the V_{OUT} voltage above the $V_{OL,off}$ during open load conditions.



This figure assumes that the device ground and the load ground are at the same potential. In a real system, there may be a ground shift voltage of 1 V to 2 V.

Figure 9-8. Short to Battery and Open Load Detection

The detection circuitry is only enabled when DIA_EN = HIGH and EN = LOW. If $V_{OUT} > V_{OL}$, the SNS pin will go to the fault level, but if $V_{OUT} < V_{OL}$ there will be no fault indication. The fault indication will only occur if the SEL1 pin is low.

While the switch is disabled and DIA_EN is high, the fault indication mechanisms will continuously represent the present status. For example, if V_{OUT} decreases from greater than V_{OL} to less than V_{OL}, the fault indication is reset. Additionally, the fault indication is reset upon the falling edge of DIA_EN or the rising edge of EN.

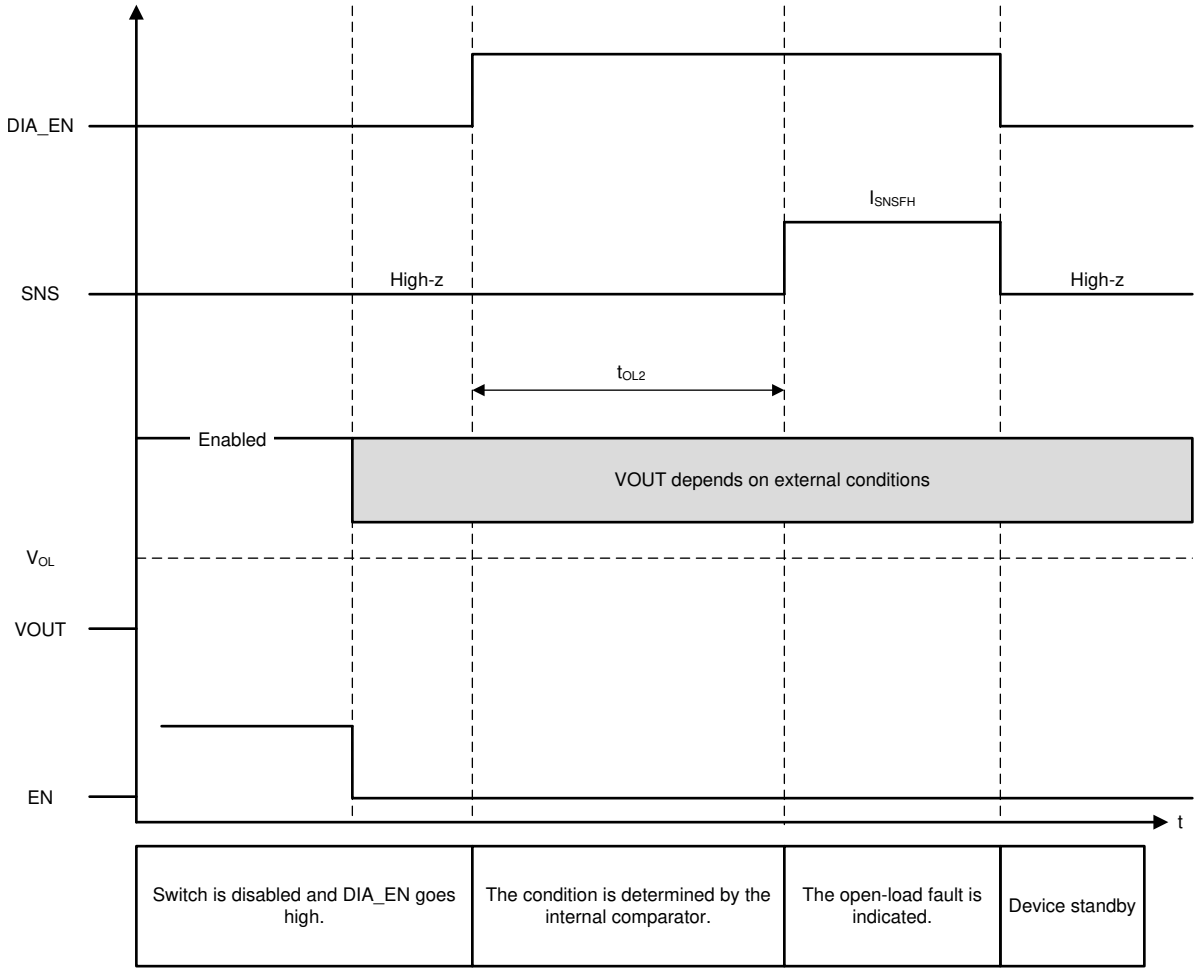


Figure 9-9. Open Load

9.3.2.2 SNS Output

The SNS output may be used to sense the load current if the SEL1 pin is low and there is no fault or device temperature if the SEL1 pin is high and there is no fault. The sense circuit will provide a current that is proportional to the selected parameter. This current will be sourced into an external resistor to create a voltage that is proportional to the selected parameter. This voltage may be measured by an ADC or comparator. In addition, the SNS pin can be used to measure the FET temperature.

To ensure accurate sensing measurement, the sensing resistor should be connected to the same ground potential as the µC ADC.

Table 9-1. Analog Sense Transfer Function

PARAMETER	TRANSFER FUNCTION
Load current	$I_{SNSI} = I_{OUT} / K_{SNS} = I_{OUT} / 1500$
Device temperature	$I_{SNST} = (T_J – 25°C) \times dI_{SNST} / dT + 0.85$

The SNS output will also be used to indicate system faults. I_{SNS} will go to the predefined level, I_{SNSFH}, when there is a fault. I_{SNSFH}, dI_{SNST}/dT, and K_{SNS} are defined in the *Specifications* section.

9.3.2.2.1 R_{SNS} Value

The following factors should be considered when selecting the R_{SNS} value:

- Current sense ratio (K_{SNS})

- Largest and smallest diagnosable load current required for application operation
- Full-scale voltage of the ADC
- Resolution of the ADC

For an example of selecting R_{ISNS} value, reference *R_{ILIM} Calculation* in the applications section of this datasheet.

9.3.2.2.1.1 High Accuracy Load Current Sense

In many automotive modules, it is required that the high-side switch provide diagnostic information about the downstream load. With more complex loads, high accuracy sensing is required. A few examples follow:

- **LED lighting**: In many architectures, the body control module (BCM) must be compatible with both incandescent bulbs and also LED modules. The bulb may be relatively simple to diagnose. However, the LED module will consume less current and also can include multiple LED strings in parallel. The same BCM is used in both cases, so the high-side switch can accurately diagnose both load types.
- **Solenoid protection**: Often solenoids are precisely controlled by low-side switches. However, in a fault event, the low-side switch cannot disconnect the solenoid from the power supply. A high-side switch can be used to continuously monitor several solenoids. If the system current becomes higher than expected, the high-side switch can disable the module.

9.3.2.2.1.2 SNS Output Filter

To achieve the most accurate current sense value, it is recommended to filter the SNS output. There are two methods of filtering:

- Low-Pass RC filter between the SNS pin and the ADC input. This filter is illustrated in Figure 10-1 with typical values for the resistor and capacitor. The designer should select a C_{SNS} capacitor value based on system requirements. A larger value will provide improved filtering but a smaller value will allow for faster transient response.
- The ADC and microcontroller can also be used for filtering. It is recommended that the ADC collects several measurements of the SNS output. The median value of this data set should be considered as the most accurate result. By performing this median calculation, the microcontroller can filter out any noise or outlier data.

9.3.2.3 Fault Indication and SNS Mux

The following faults will be communicated through the SNS output:

- Switch shutdown, due to:
  - Thermal Shutdown
  - Current limit
- Open-Load and V_{OUT} shorted-to-battery

Open-load and Short-to-battery are not indicated while the switch is enabled, although these conditions can still be detected through the sense current. Hence, if there is a fault indication while the channel is enabled, then it must be either due to an overcurrent or overtemperature event.

The SNS pin will only indicate the fault if the SEL1 pins is low. When the SEL1 pin is high and the device is set to measure temperature, the pin will be measuring the channel FET temperature.

Table 9-2. Device Version A/B SNS Mux

INPUTS			OUTPUTS
DIA_EN	SEL1	FAULT DETECT(1)	SNS
0	X	X	High-z
1	0	0	Output current
1	1	0	Device temperature
1	0	1	I_{SNSFH}
1	1	1	Device temperature

(1) Fault Detect encompasses multiple conditions:
- Switch shutdown and waiting for retry
- Open Load and Short To Battery

9.3.2.4 Resistor Sharing

Multiple high-side devices may use the same SNS resistor as shown in Figure 9-10. This reduces the total number of passive components in the system and the number of ADC terminals that are required of the microcontroller.

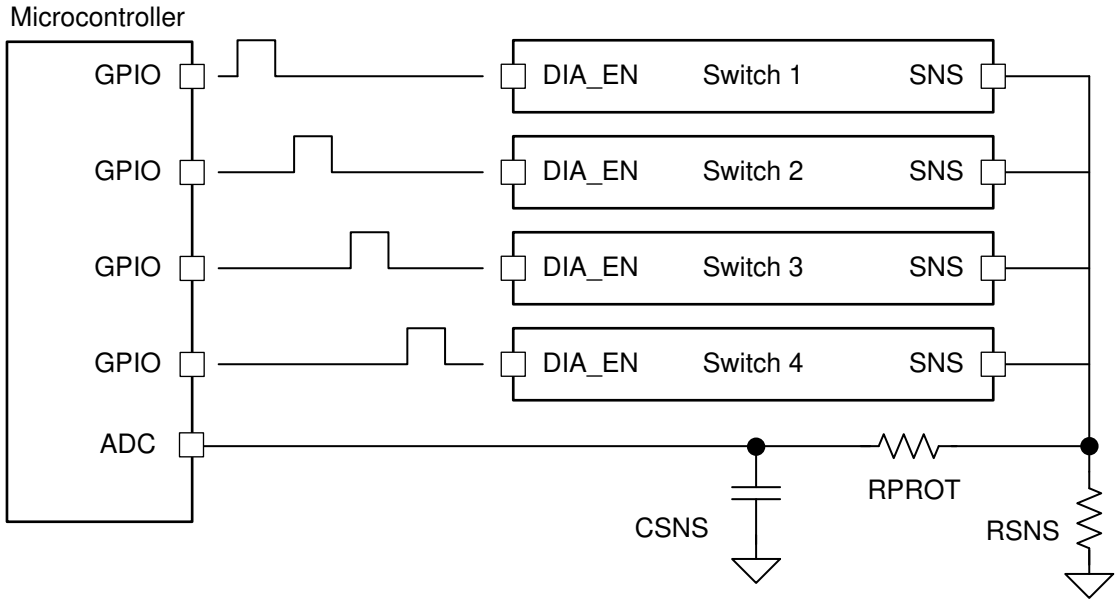


Figure 9-10. Sharing R_{SNS} Among Multiple Devices

9.3.2.5 High-Frequency, Low Duty-Cycle Current Sensing

Some applications will operate with a high-frequency, low duty-cycle PWM or require fast settling of the SNS output. For example, a 250-Hz, 5% duty cycle PWM will have an on-time of only 200 µs that must be accommodated. The micro-controller ADC may sample the SNS signal after the defined settling time $t_{SNSION3}$.

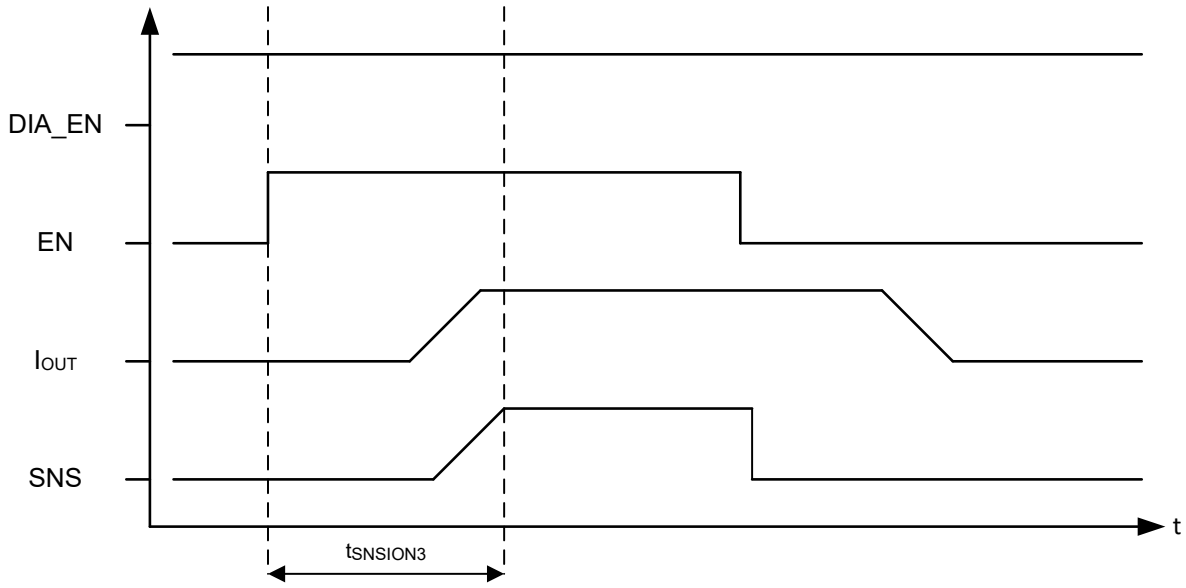


Figure 9-11. Current Sensing in Low-Duty Cycle Applications

9.4 Device Functional Modes

During typical operation, the TPS1HB50-Q1 can operate in a number of states that are described below and shown as a state diagram in Figure 9-12.

9.4.1 Off

Off state occurs when the device is not powered.

9.4.2 Standby

Standby state is a low-power mode used to reduce power consumption to the lowest level. Diagnostic capabilities are not available in Standby mode.

9.4.3 Diagnostic

Diagnostic state may be used to perform diagnostics while the switch is disabled.

9.4.4 Standby Delay

The Standby Delay state is entered when EN and DIA_EN are low. After t_{STBY}, if the EN and DIA_EN pins are still low, the device will go to Standby State.

9.4.5 Active

In Active state, the switch is enabled. The diagnostic functions may be turned on or off during Active state.

9.4.6 Fault

The Fault state is entered if a fault shutdown occurs (thermal shutdown or current limit). After all faults are cleared, the LATCH pin is low, and the retry timer has expired, the device will transition out of Fault state. If the EN pin is high, the switch will re-enable. If the EN pin is low, the switch will remain off.

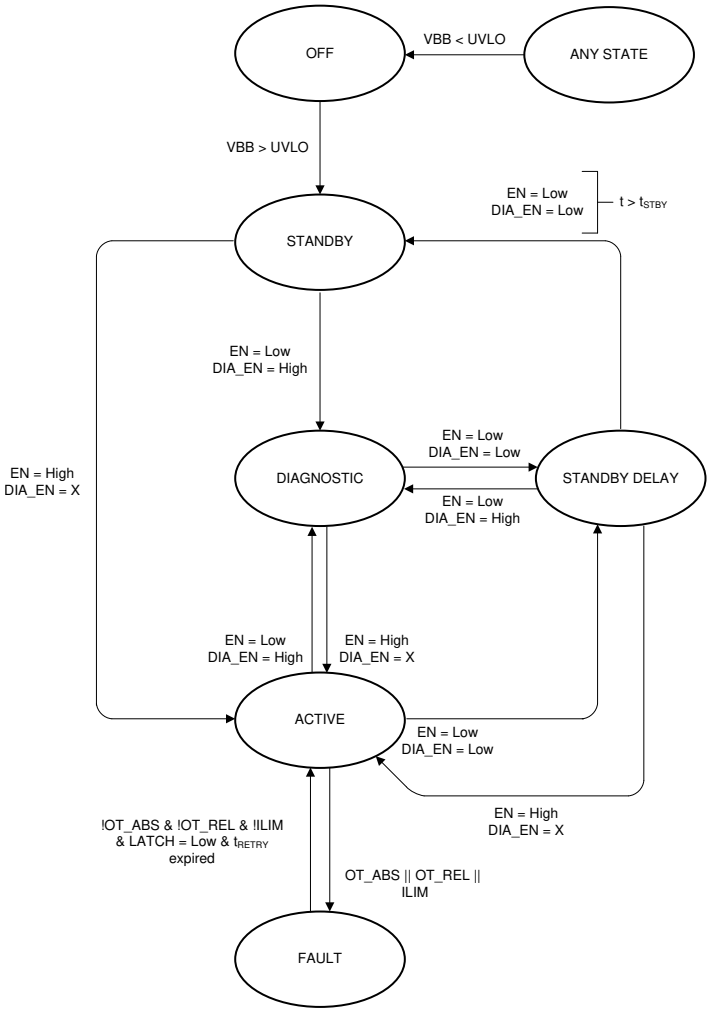


Figure 9-12. State Diagram

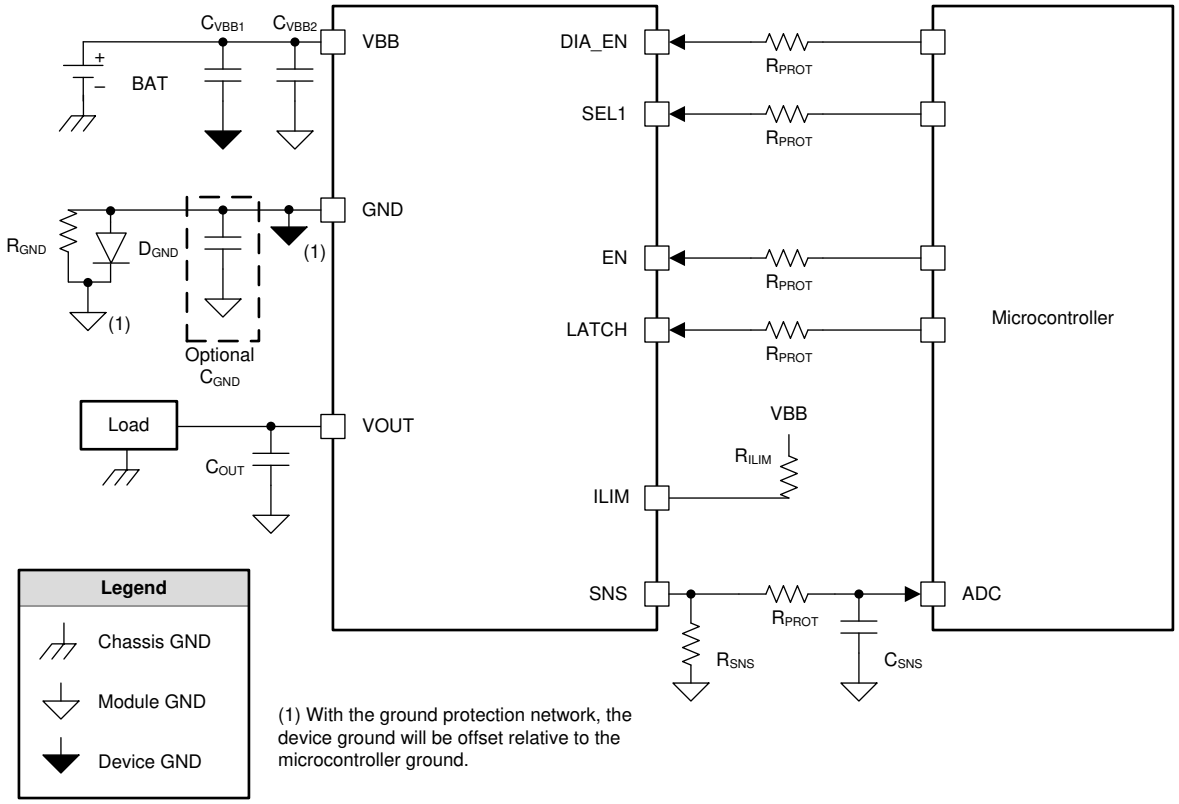
10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Figure 10-1 shows the schematic of a typical application of the TPS1HB50-Q1. It includes all standard external components. This section of the datasheet discusses the considerations in implementing commonly required application functionality.



With the ground protection network, the device ground will be offset relative to the microcontroller ground.

Figure 10-1. System Diagram

Table 10-1. Recommended External Components

COMPONENT	TYPICAL VALUE	PURPOSE
R_{PROT}	15 kΩ	Protect microcontroller and device I/O pins.
R_{SNS}	1 kΩ	Translate the sense current into sense voltage.
C_{SNS}	100 pF - 10 nF	Low-pass filter for the ADC input.
R_{GND}	4.7 kΩ	Stabilize GND potential during turn-off of inductive load.
D_{GND}	BAS21 Diode	Protects device during reverse battery.
R_{ILIM}	5 kΩ - 25 kΩ	Set current limit threshold.
C_{VBB1}	4.7 nF to Device GND	Filtering of voltage transients (for example, ESD, ISO7637-2) and improved emissions.
C_{VBB2}	220 nF to Module GND	Stabilize the input supply and filter out low frequency noise.

Table 10-1. Recommended External Components (continued)

COMPONENT	TYPICAL VALUE	PURPOSE
C_{OUT}	220 nF	Filtering of voltage transients (for example, ESD, ISO7637-2).

10.1.1 Ground Protection Network

As discussed in the *Reverse Battery* section, D_{GND} may be used to prevent excessive reverse current from flowing into the device during a reverse battery event. Additionally, R_{GND} is placed in parallel with D_{GND} if the switch is used to drive an inductive load. The ground protection network (D_{GND} and R_{GND}) may be shared amongst multiple high-side switches.

A minimum value for R_{GND} may be calculated by using the absolute maximum rating for I_{GND}. During the reverse battery condition, $I_{GND} = V_{BB} / R_{GND}$:

$$R_{GND} \geq V_{BB} / I_{GND} \quad (2)$$

- Set V_{BB} = –13.5 V
- Set I_{GND} = –50 mA (absolute maximum rating)

$R_{GND} \geq$ –13.5 V / –50 mA = 270 Ω

In this example, it is found that R_{GND} must be at least 270 Ω. It is also necessary to consider the power dissipation in R_{GND} during the reverse battery event:

$$P_{RGND} = V_{BB}^{\ 2} / R_{GND} \quad (3)$$

$P_{RGND} = (13.5\ V)^2 / 270\ \Omega = 0.675$ W

In practice, R_{GND} may not be rated for such a high power. In this case, a larger resistor value should be selected.

10.1.2 Interface With Microcontroller

The ground protection network will cause the device ground to be at a higher potential than the module ground (and microcontroller ground). This offset will impact the interface between the device and the microcontroller.

Logic pin voltage will be offset by the forward voltage of the diode. For input pins (for example, EN), the designer must consider the V_{IH} specification of the switch and the V_{OH} specification of the microcontroller. For a system that *does not* include D_{GND}, it is required that $V_{OH} > V_{IH}$. For a system that *does* include D_{GND}, it is required that $V_{OH} > (V_{IH} + V_F)$. V_F is the forward voltage of D_{GND}.

The sense resistor, R_{SNS}, should be terminated to the microcontroller ground. In this case, the ADC can accurately measure the SNS signal even if there is an offset between the microcontroller ground and the device ground.

10.1.3 I/O Protection

R_{PROT} is used to protect the microcontroller I/O pins during system-level voltage transients such as ISO pulses or reverse battery. The SNS pin voltage can exceed the ADC input pin maximum voltage if the fault or saturation current causes a high enough voltage drop across the sense resistor. If that can occur in the design (for example, by switching to a high value R_{SNS} to improve ADC input level), then an appropriate external clamp has to be designed to prevent a high voltage at the SNS output and the ADC input.

10.1.4 Inverse Current

Inverse current occurs when 0 V < V_{BB} < V_{OUT}. In this case, current may flow from V_{OUT} to V_{BB}. Inverse current cannot be caused by a purely resistive load. However, a capacitive or inductive load can cause inverse current. For example, if there is a significant amount of load capacitance and the V_{BB} node has a transient droop, V_{OUT} may be greater than V_{BB}.

The TPS1HB50-Q1 will not detect inverse current. When the switch is enabled, inverse current will pass through the switch. When the switch is disabled, inverse current may pass through the MOSFET body diode. The device will continue operating in the normal manner during an inverse current event.

10.1.5 Loss of GND

The ground connection may be lost either on the device level or on the module level. If the ground connection is lost, the switch will be disabled. If the switch was already disabled when the ground connection was lost, the switch will remain disabled. When the ground is reconnected, normal operation will resume.

10.1.6 Automotive Standards

The TPS1HB50-Q1 is designed to be protected against all relevant automotive standards to ensure reliable operations when connected to a 12-V automotive battery.

10.1.6.1 ISO7637-2

The TPS1HB50-Q1 is tested according to the ISO7637-2:2011 (E) standard. The test pulses are applied both with the switch enabled and disabled. The test setup includes only the DUT and minimal external components: C_{VBB}, C_{OUT}, D_{GND}, and R_{GND}.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as: “The function does not perform as designed during the test but returns automatically to normal operation after the test”. See Table 10-2 for ISO7637-2:2011 (E) expected results.

Table 10-2. ISO7637-2:2011 (E) Results

TEST PULSE	TEST PULSE SEVERITY LEVEL WITH STATUS II FUNCTIONAL PERFORMANCE		MINIMUM NUMBER OF PULSES OR TEST TIME	BURST CYCLE / PULSE REPETITION TIME	
	LEVEL	US		MIN	MAX
1	III	–112 V	500 pulses	0.5 s	--
2a(1)	III	+55 V	500 pulses	0.20	5 s
2b	IV	+10 V	10 pulses	0.5 s	5 s
3a	IV	–220 V	1 hour	90 ms	100 ms
3b	IV	+150 V	1 hour	90 ms	100 ms

(1) 1-µF capacitance on C_{VBB} is required for passing level 3 ISO7637 pulse 2 A.

10.1.6.2 AEC-Q100-012 Short Circuit Reliability

The TPS1HB50-Q1 is tested according to the AEC-Q100-012 Short Circuit Reliability standard. This test is performed to demonstrate the robustness of the device against V_{OUT} short-to-ground events. Test conditions and test procedures are summarized in Table 10-3. For further details, refer to the AEC-Q100-012 standard document.

Test conditions:

- LATCH = 0 V
- R_{ILIM} = 5 kΩ
- 10 units from 3 separate lots for a total of 30 units.
- L_{supply} = 5 µH, R_{supply} = 10 mΩ
- V_{BB} = 14 V

Test procedure:

- Parametric data is collected on each unit pre-stress
- Each unit is enabled into a short-circuit with the required short circuit cycles or duration as specified
- Functional testing is performed on each unit post-stress to verify that the part still operates as expected

The cold repetitive test is run at 85°C which is the worst case condition for the device to sustain a short circuit. The cold repetitive test refers to the device being given time to cool down between pulses, rather than being run at a cold temperature. The load short circuit is the worst case situation, since the energy stored in the cable inductance can cause additional harm. The fast response of the device ensures current limiting occurs quickly and at a current close to the load short condition. In addition, the hot repetitive test is performed as well.

Table 10-3. AEC-Q100-012 Test Results

TEST	LOCATION OF SHORT	DEVICE VERSION	NO. OF CYCLES / DURATION	NO. OF UNITS	NO. OF FAILS
Cold Repetitive - Long Pulse(1)	Load Short Circuit, L_{short} = 5 µH, R_{short} = 200 mΩ, T_A = 85°C	B	100 k cycles	30	0
Hot Repetitive - Long Pulse	Load Short Circuit, L_{short} = 5 µH, R_{short} = 100 mΩ, T_A = 25°C	B	100 hours	30	0

(1) For Cold Repetitive short, 200-mΩ R_{short} is used so that the device is at a higher junction temperature before the short circuit event, increasing the harshness of the test.

10.1.7 Thermal Information

When outputting current, the TPS1HB50-Q1 will heat up due to the power dissipation. The transient thermal impedance curve can be used to determine the device temperature during a pulse of a given length. This $Z_{\theta JA}$ value corresponds to a JEDEC standard 2s2p thermal test PCB with thermal vias.

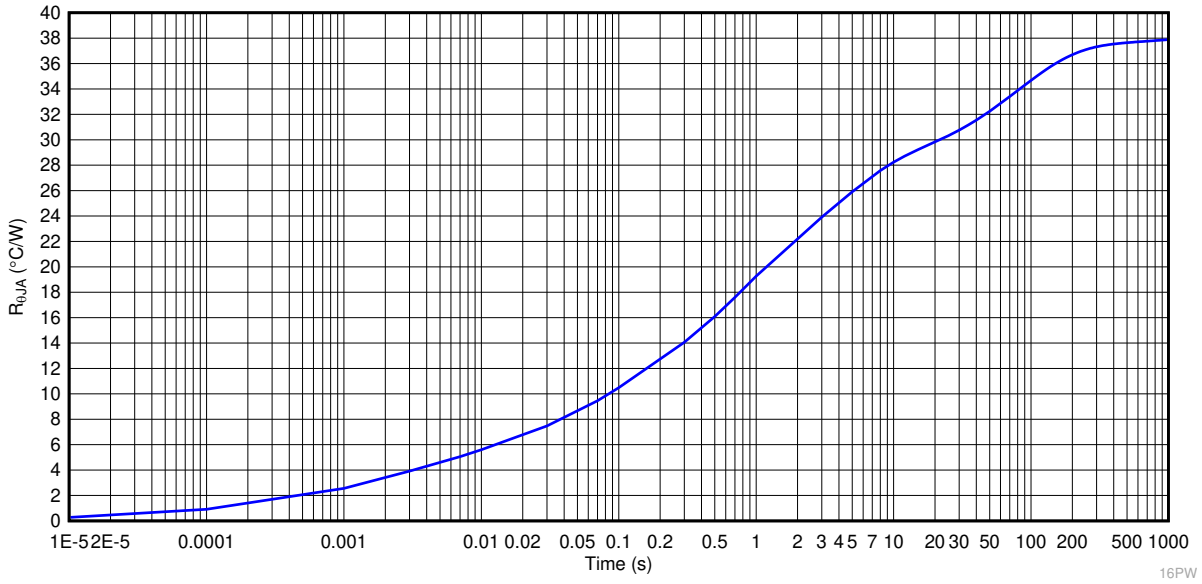


Figure 10-2. TPS1HB50-Q1 Transient Thermal Impedance

10.2 Typical Application

This application example demonstrates how the TPS1HB50-Q1 device can be used to power resistive heater loads in automotive seats. In this example, we consider a heater load that is powered by the device. This is just one example of the many applications where this device can fit.

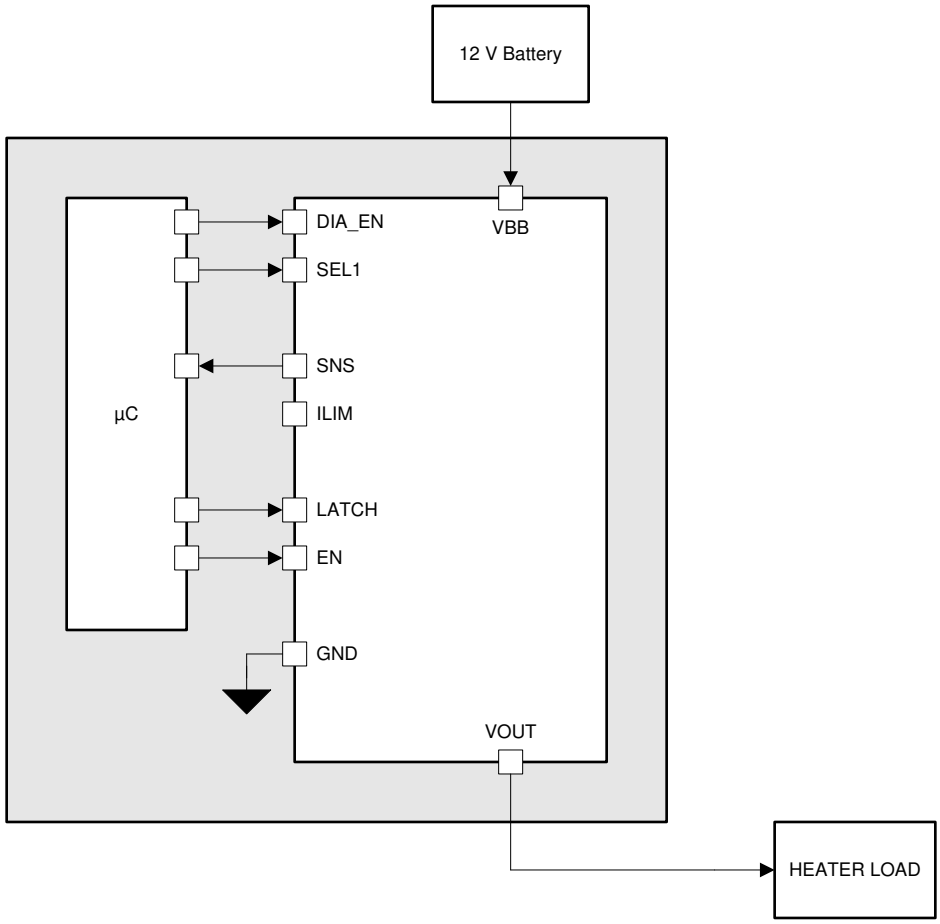


Figure 10-3. Block Diagram for Powering Heater Load

10.2.1 Design Requirements

For this design example, use the input parameters shown in Table 10-4.

Table 10-4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{BB}	13.5 V
Load - Heater	45 W max
Load Current Sense	30 mA to 6 A
I_{LIM}	4.5 A
Ambient temperature	70°C
$R_{\theta JA}$	37°C/W (depending on PCB)
Device Version	A

10.2.2 Detailed Design Procedure

10.2.2.1 Thermal Considerations

The 45 W heater load will cause a DC current in the channel under maximum load power condition of around 3.3 A. Therefore, this current at 13.5 V will assume worst case heating.

Power dissipation in the switch is calculated in Equation 4. R_{ON} is assumed to be 100 mΩ because this is the maximum specification at high temperature. In practice, R_{ON} will almost always be lower.

$$P_{FET} = I^2 \times R_{ON} \quad (4)$$

$$P_{FET} = (3.3\ A)^2 \times 100\ m\Omega = 1.09\ W \quad (5)$$

This means that the maximum FET power dissipation is 1.09 W. The junction temperature of the device can be calculated using Equation 6 and the $R_{\theta JA}$ value from the *Specifications* section.

$$T_J = T_A + R_{\theta JA} \times P_{FET} \quad (6)$$

$$T_J = 70°C + 37°C/W \times 1.09\ W = 110.3°C$$

The maximum junction temperature rating for the TPS1HB50-Q1 is T_J = 150°C. Based on the above example calculation, the device temperature will stay below the maximum rating even at this high level of current.

10.2.2.2 R_{ILIM} Calculation

In this application, the TPS1HB50-Q1 must allow for the maximum DC current with margin but minimize the energy in the switch during a fault condition by minimizing the current limit. For this application, the best I_{LIM} set point is approximately 4.5. Equation 7 allows you to calculate the R_{ILIM} value that is placed from the I_{LIM} pins to V_{BB}. R_{ILIM} is calculated in kΩ.

$$R_{ILIM} = K_{CL} / I_{CL} \quad (8)$$

Because this device is version A, the K_{CL} value in the *Specifications* section is A × kΩ.

$$R_{ILIM} = 40\ (A \times k\Omega) / 4.5\ A = 8.89\ k\Omega \quad (9)$$

For a I_{LIM} of 4.5 A, the R_{ILIM} value should be set at around 8.89 kΩ.

10.2.2.3 Diagnostics

If the resistive heating load is disconnected (heater malfunction), an alert is desired. Open-load detection can be performed in the switch-enabled state with the current sense feature of the TPS1HB50-Q1 device. Under open load condition, the current in the SNS pin will be the fault current and the can be detected from the sense voltage measurement.

10.2.2.3.1 Selecting the R_{ISNS} Value

Table 10-5 shows the requirements for the load current sense in this application. The K_{SNS} value is specified for the device and can be found in the *Specifications* section.

Table 10-5. R_{SNS} Calculation Parameters

PARAMETER	EXAMPLE VALUE
Current Sense Ratio (K_{SNS})	1500
Largest diagnosable load current	6 A
Smallest diagnosable load current	30 mA
Full-scale ADC voltage	5 V
ADC resolution	10 bit

The load current measurement requirements of 6 A ensures that even in the event of a overcurrent surpassing the set current limit, the MCU can register and react by shutting down the TPS1HB50-Q1, while the low level of 30 mA allows for accurate measurement of low load currents.

The R_{SNS} resistor value should be selected such that the largest diagnosable load current puts V_{SNS} at about 95% of the ADC full-scale. With this design, any ADC value above 95% can be considered a fault. Additionally, the R_{SNS} resistor value should ensure that the smallest diagnosable load current does not cause V_{SNS} to fall below 1 LSB of the ADC. With the given example values, a 1.2-kΩ sense resistor satisfies both requirements shown in Table 10-6.

Table 10-6. V_{SNS} Calculation

LOAD (A)	SENSE RATIO	I_{SNS} (mA)	R_{SNS} (Ω)	V_{SNS} (V)	% of 5-V ADC
0.03	1500	0.02	1200	0.024	0.5%
6	1500	4	1200	4.800	96.0%

11 Power Supply Recommendations

The TPS1HB50-Q1 device is designed to operate in a 12-V automotive system. The nominal supply voltage range is 6 V to 18 V as measured at the V_{BB} pin with respect to the GND pin of the device. In this range the device meets full parametric specifications as listed in the *Electrical Characteristics* table. The device is also designed to withstand voltage transients beyond this range. When operating outside of the nominal voltage range but within the operating voltage range, the device will exhibit normal functional behavior. However, parametric specifications may not be specified outside the nominal supply voltage range.

Table 11-1. Operating Voltage Range

V_{BB} Voltage Range	Note
3 V to 6 V	Transients such as cold crank and start-stop, functional operation are specified but some parametric specifications may not apply. The device is completely short-circuit protected up to 125°C.
6 V to 18 V	Nominal supply voltage, all parametric specifications apply. The device is completely short-circuit protected up to 125°C.
18 V to 40 V	Transients such as jump-start and load-dump, functional operation specified but some parametric specifications may not apply.

12 Layout

12.1 Layout Guidelines

To achieve optimal thermal performance, connect the exposed pad to a large copper pour. On the top PCB layer, the pour may extend beyond the package dimensions as shown in the example below. In addition to this, it is recommended to also have a V_{BB} plane either on one of the internal PCB layers or on the bottom layer.

Vias should connect this plane to the top V_{BB} pour.

Ensure that all external components are placed close to the pins. Device current limiting performance can be harmed if the R_{ILIM} is far from the pins and extra parasitics are introduced.

12.2 Layout Example

The layout example is for device versions A/B.

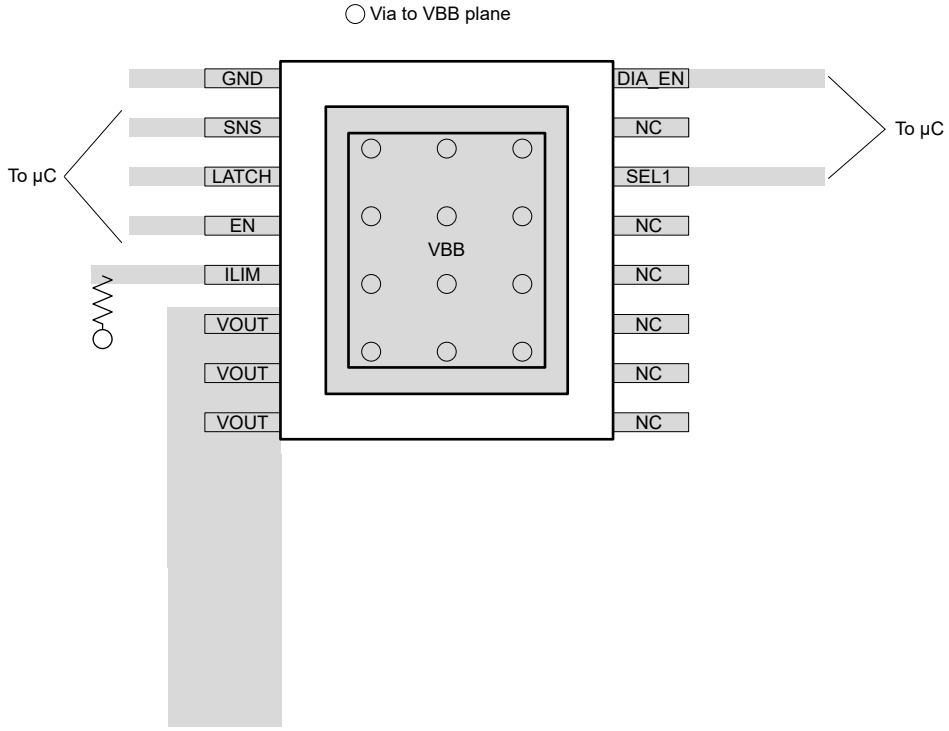


Figure 12-1. 16-PWP Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- TI's *How To Drive Inductive, Capacitive, and Lighting Loads with Smart High Side Switches*
- TI's *Short-Circuit Reliability Test for Smart Power Switch*
- TI's *Reverse Battery Protection for High Side Switches*
- TI's *Adjustable Current Limit of Smart Power Switches*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS1HB50AQPWPRQ1	ACTIVE	HTSSOP	PWP	16	3000	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HB50AQ	Samples
TPS1HB50BQPWPRQ1	ACTIVE	HTSSOP	PWP	16	3000	RoHS-Exempt & Green	NIPDAU	Level-3-260C-168HRS	-40 to 125	1HB50BQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

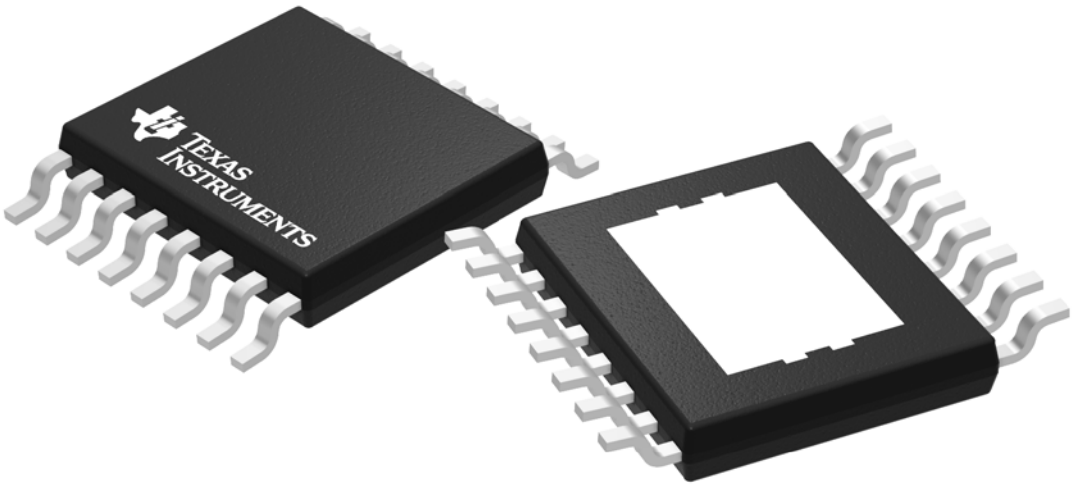
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



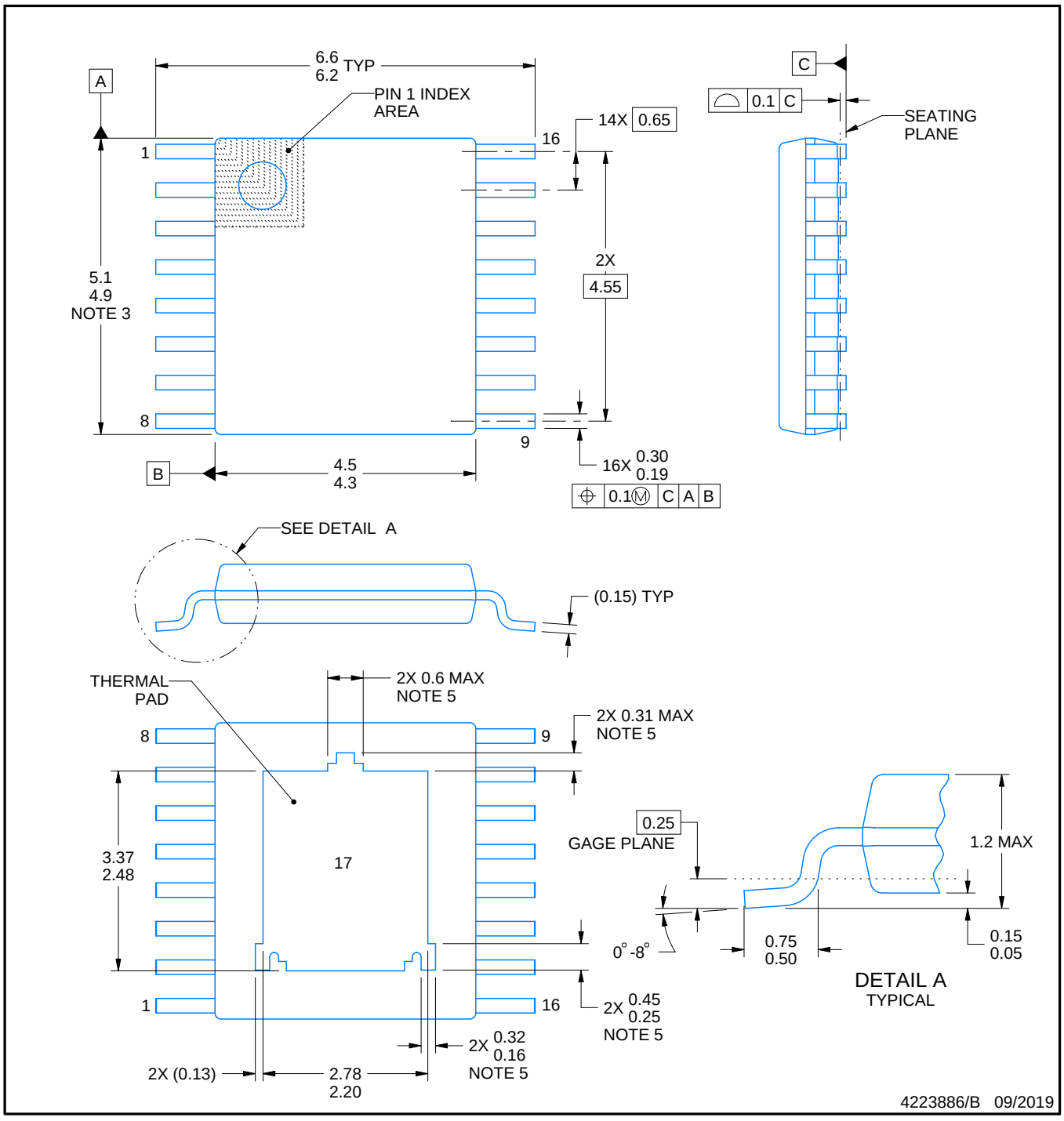
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PWP0016M

PowerPAD™ TSSOP - 1.2 mm max height

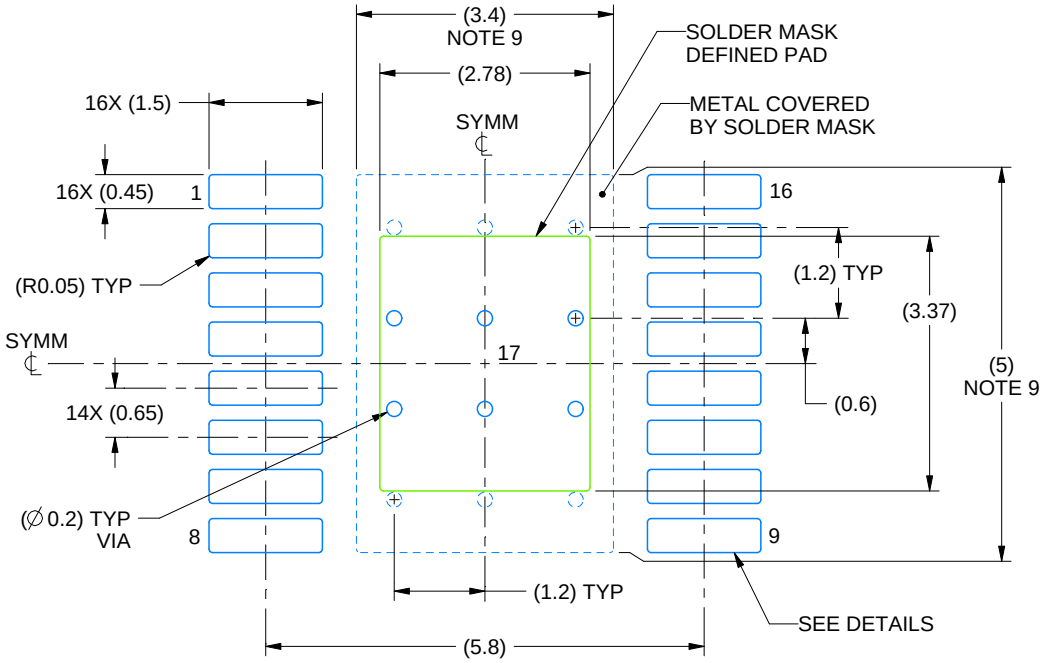
SMALL OUTLINE PACKAGE



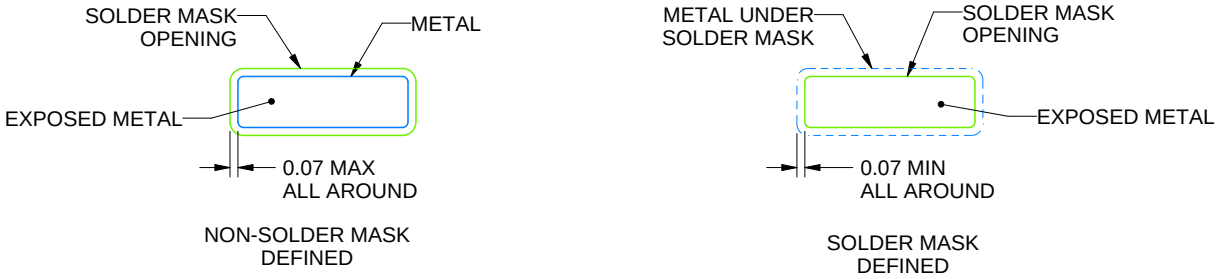
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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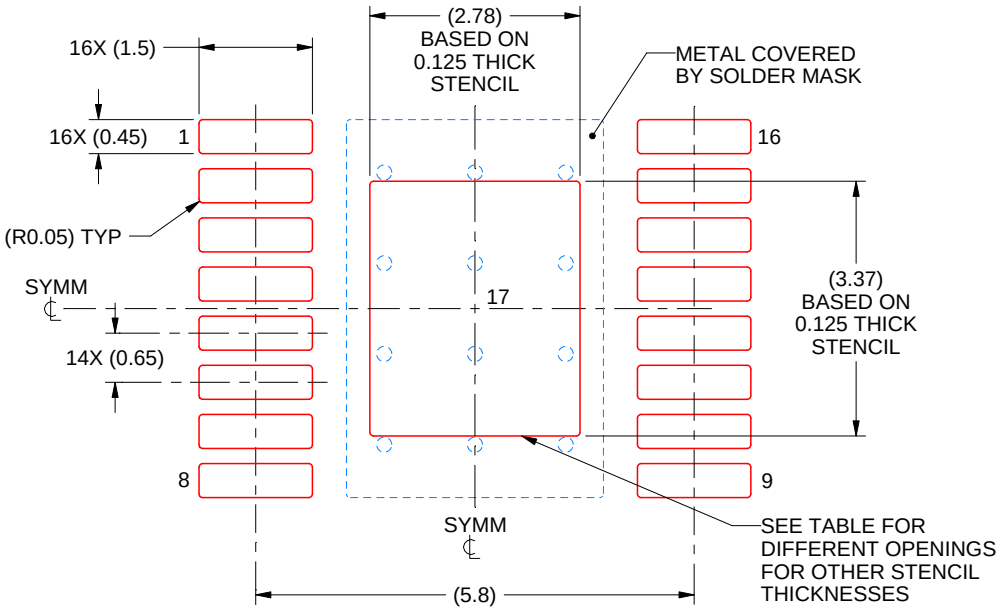
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.11 X 3.77
0.125	2.78 X 3.37 (SHOWN)
0.15	2.54 X 3.08
0.175	2.35 X 2.85

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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