# 4-CHANNEL ESD SOLUTION FOR USB-HS/USB OTG/USB CHARGER INTERFACE

**Check for Samples: TPD4S012**

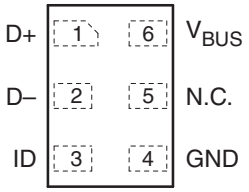
## FEATURES

- **Integrated ESD Clamps for D+, D–, $V_{BUS}$, and ID Pins to Provide Single-Chip ESD Protection for USB High Speed, USB-OTG, and USB Charger Interface**
- **Special Snap Back Technology Allows High-voltage Tolerance During Normal Operation while Reducing the Clamp Voltage during System Level ESD Stress**
- **USB Signal Pins (D+, D–, ID)**
  - **0.8-pF Line Capacitance**
  - **Tolerates 6 V Signal**
- **$V_{BUS}$ Line ($V_{BUS}$)**
  - **11-pF Line Capacitance**
  - **Tolerates 20 V Signal**
- **Flow-Through Pin Mapping for the High-Speed Lines Ensures Zero Additional Skew Due to Board Layout While Placing the ESD Protection Chip Near the Connector**
- **Supports Data Rates in Excess of 480 Mbps**
- **IEC 61000-4-2 (Level 4) System Level ESD Compliance Measured at the D+, D–, and ID Pins**
  - **Â±10-kV IEC 61000-4-2 Contact Discharge**
  - **Â±10-kV IEC 61000-4-2 Air-Gap Discharge**
- **3 Amps Peak Pulse Current (8/20 µs Pulse) for $V_{BUS}$ and D+, D–, and ID Lines**
- **Industrial Temperature Range: –40°C to 85°C**

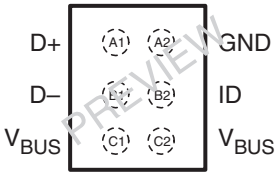
## APPLICATIONS

- **Cellular Phones**
- **Digital Cameras**
- **Global Positioning Systems (GPS)**
- **Portable Digital Assistants (PDA)**
- **Portable Computers**

**DRY PACKAGE**
**(TOP VIEW)**




**YFP PACKAGE**
**(TOP VIEW)**






N.C. – Not internally connected

D+, D–, and ID pins are exact equivalent ESD clamp circuits. Any of these pins can be connected to any other D+, D–, or ID pin if it becomes easier to route the traces from the USB connector.

## DESCRIPTION

The TPD4S012 is a four-channel electrostatic discharge (ESD) solution for USB charger or USB on-the-go (OTG) interface. In many cell phone applications, the USB connector is the de facto communication port for external communications like high-speed data transfer, audio signal, charging, car-kit, etc. In order to support different interfaces, the USB port needs to handle different voltage levels. For example, some chargers require the $V_{BUS}$ port of the USB connector to handle in excess of the normal $V_{BUS}$ voltage per USB specifications. The TPD4S012 offers combinations of two different clamp voltages to match the voltage tolerances of the different signal interfaces using the common USB connector. Refer to Figure 5-6 & Figure 9-12, special snap back technology allows high-voltage tolerance during normal operation while reducing the clamp voltage during system level ESD stress.

The TPD4S012 conforms to IEC61000-4-2 (Level 4) ESD. The device is offered in space-saving packages with flow-through pin mapping.

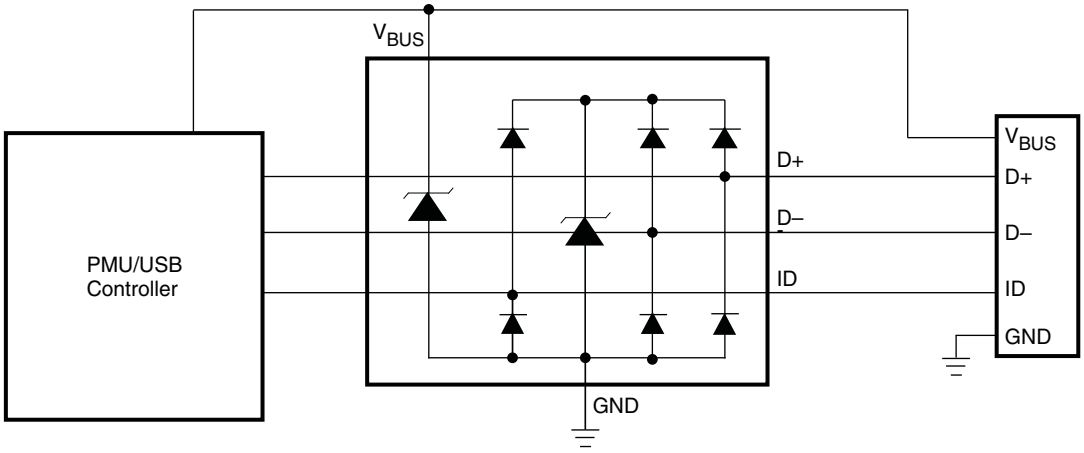
The TPD4S012 is characterized for operation over ambient air temperature of –40°C to 85°C.

## ORDERING INFORMATION

| $T_A$ | PACKAGE (1) (2) | | NOMINAL DIMENSIONS (mm) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|---|
| –40°C to 85°C | SON – DRY | Reel of 3000 | W = 1.0, L = 1.45, H = 0.55, Pitch = 0.5 | TPD4S012DRYR | 3B |
| | WCSP – XXX | Reel of 3000 | W = 0.8, L = 1.2, H = 0.5, Pitch = 0.4 | TPD4S012XXXR | TBD |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## APPLICATION SCHEMATIC




If the ID pin is not used, it can be left floating.

## Board Layout Recommendations

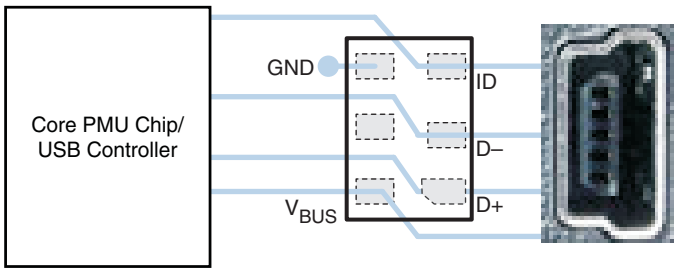



**Figure 1. Using DRY Package**

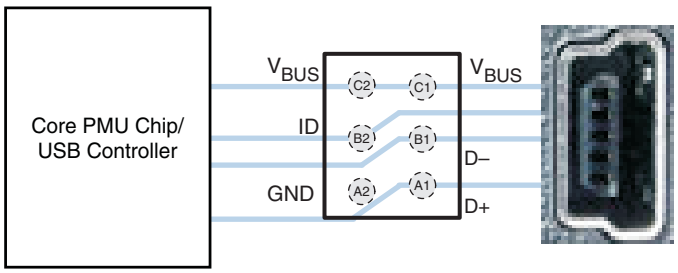
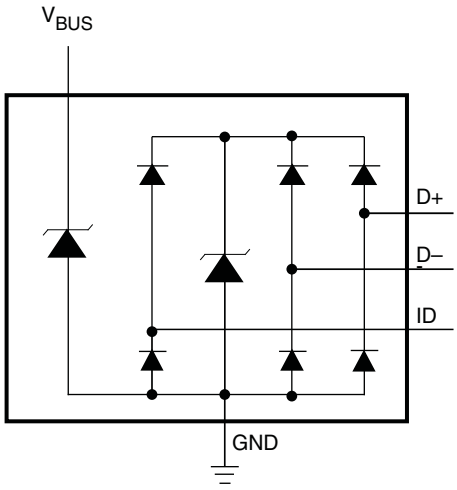



**Figure 2. Using YFP Package**

The TPD4S012 can provide system-level ESD protection to the high-speed differential ports. The flow-through package offers flexibility for board routing. Figure 1 and Figure 2 show the board layout scheme for the D+ and D– lines of a single differential pair. It allows the differential signal pairs couple together right after they touch the ESD ports of the TPD4S012.

## CIRCUIT DIAGRAM




## TERMINAL FUNCTIONS

| TERMINAL | | | TYPE | DESCRIPTION |
|---|---|---|---|---|
| DRY PIN NO. | XXX BALL NO. | NAME | | |
| 1 | A1 | D+ | ESD clamp | Provides ESD protection to the high-speed differential data lines |
| 2 | B1 | D– | ESD clamp | Provides ESD protection to the high-speed differential data lines |
| 3 | B2 | ID | ESD clamp | Provides ESD protection to the high-speed differential data lines |
| 4 | A2 | GND | Pwr | Ground |
| 5 | – | N.C. | – | Not internally connected |
| 6 | C1, C2 | $V_{BUS}$ | ESD clamp | ESD clamp for high-voltage tolerant $V_{BUS}$ line(s) |

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| | $V_{BUS}$ voltage tolerance | $V_{BUS}$ pin | –0.3 | 20 | V |
| | IO voltage tolerance | D+, D–, ID pins | –0.3 | 6 | V |
| $T_{stg}$ | Storage temperature range | | –65 | 125 | °C |
| $T_A$ | Operating free-air temperature range | | –40 | 85 | °C |
| | IEC 61000-4-2 Contact Discharge | D+, D–, ID | | ±10 | kV |
| | IEC 61000-4-2 Air-Gap Discharge | D+, D–, ID | | ±10 | kV |
| | IEC 61000-4-2 Contact Discharge | $V_{BUS}$ pin | | ±10 | kV |
| | IEC 61000-4-2 Air-Gap Discharge | $V_{BUS}$ pin | | ±9 | kV |
| | Peak pulse power ($t_p$ = 8/20 µs) | D+, D–, ID, $V_{BUS}$ pins | | 60 | W |
| | Peak pulse current ($t_p$ = 8/20 µs) | D+, D–, ID, $V_{BUS}$ pins | | 3 | A |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{VBUS}$ | $V_{BUS}$ operating current | $V_{BUS}$ = 5 V | D+, D–, ID pins open | | | | μA |
| | | $V_{BUS}$ = 19 V | | | 0.1 | 0.5 | |
| $I_{IO}$ | IO port current | $V_{IO}$ = 2.5 V, $V_{BUS}$ = 5 V | D+, D–, ID pins | | 0.1 | 0.5 | μA |
| $V_D$ | Diode forward voltage | $I_{IO}$ = 8 mA | D+, D–, ID pins (lower clamp diode) | 0.6 | 0.8 | 0.95 | V |
| $C_{VBUS}$ | $V_{BUS}$ pin capacitance | $V_{BUS}$ = 5 V | | | 11 | 15 | pF |
| $C_{IO}$ | IO capacitance | $V_{IO}$ = 2.5 V | D+, D–, ID pins (DRY package) | | 0.8 | 1 | pF |
| $R_{DYN}$ | Dynamic resistance | $I_{IO}$ = 1.5 A | D+, D–, ID, and $V_{BUS}$ pins, including central clamp dioded during positive ESD pulse | | 1.2 | | Ω |
| | | $I_{IO}$ = 1 A | D+, D–, ID, and $V_{BUS}$ pins, including central clamp diode during negative ESD pulse | | 1 | | |
| $V_{BR}$ | Breakdown voltage | $I_{IO}$ = 1 mA | D+, D–, ID pins | 6 | 9 | | V |
| | | | $V_{BUS}$ pin(s) | 20 | 24 | | |

## TYPICAL CHARACTERISTICS

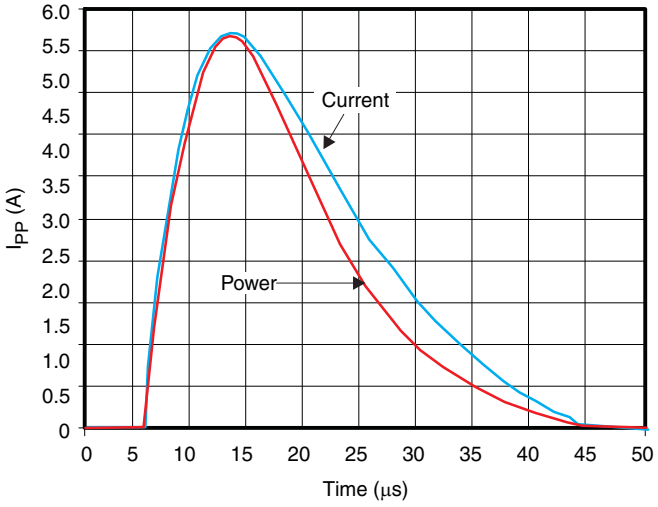



**Figure 3. Peak Pulse Power Waveform at the D+, D–, or ID Pin**

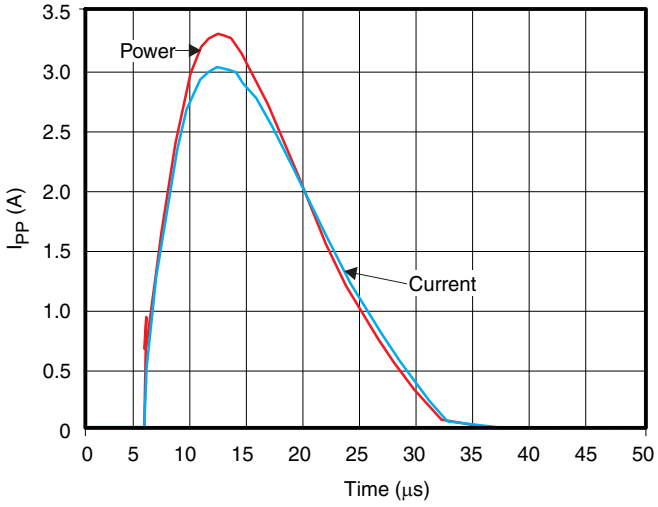



**Figure 4. Peak Pulse Power Waveform at the $V_{BUS}$ Pin**

## TYPICAL CHARACTERISTICS (continued)

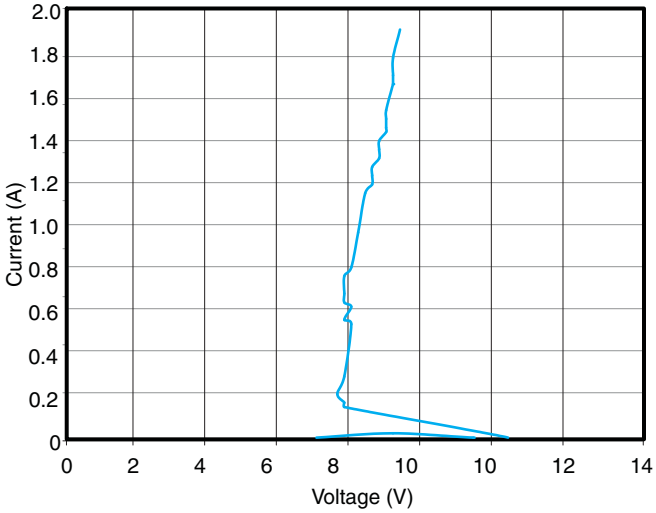



**Figure 5. D+, D–, or ID Clamp Voltage Under ESD Event**

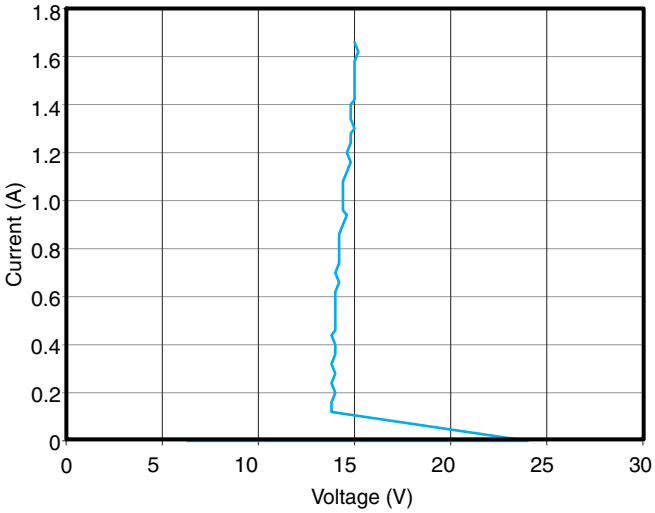



**Figure 6. $V_{BUS}$ Clamp Voltage Under ESD Event**

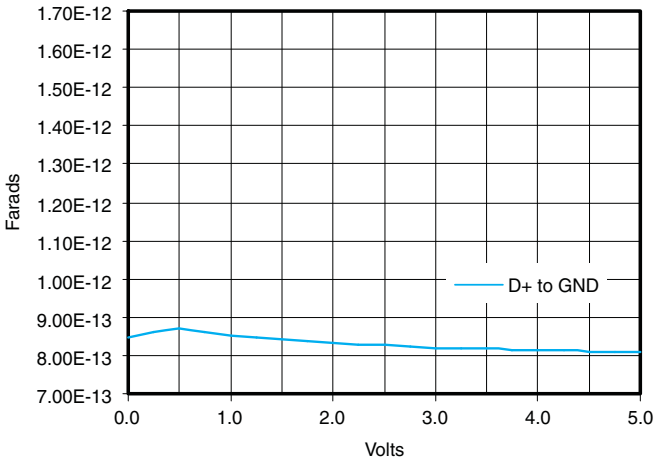



**Figure 7. D+, D–, or ID Capacitance, $T_A$ = 27°C**

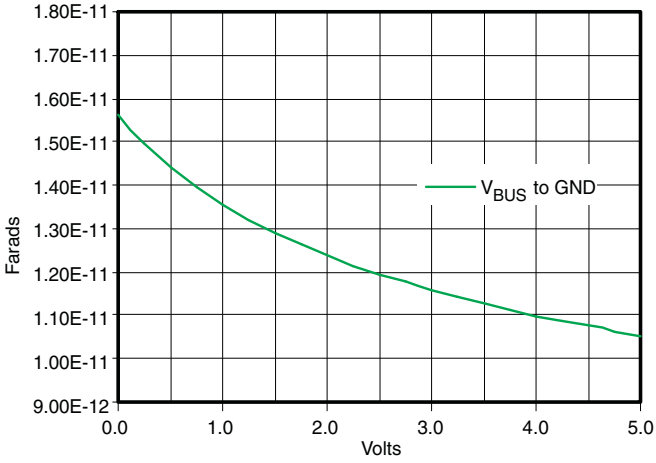



**Figure 8. $V_{BUS}$ Capacitance, $T_A$ = 27°C**

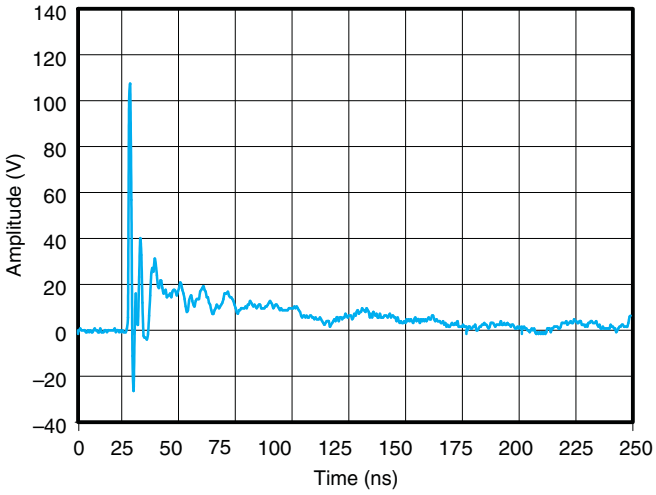



**Figure 9. IEC Clamping Waveform, 8 kV Contact, D+, 25 ns/div**

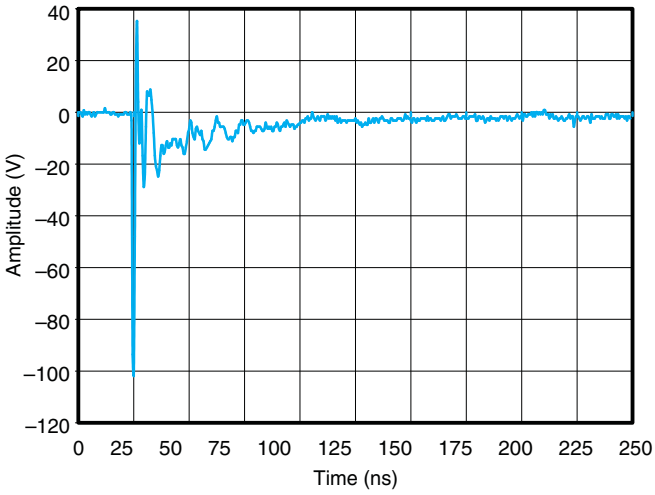



**Figure 10. IEC Clamping Waveform, –8 kV Contact, D+, 25 ns/div**

## TYPICAL CHARACTERISTICS (continued)

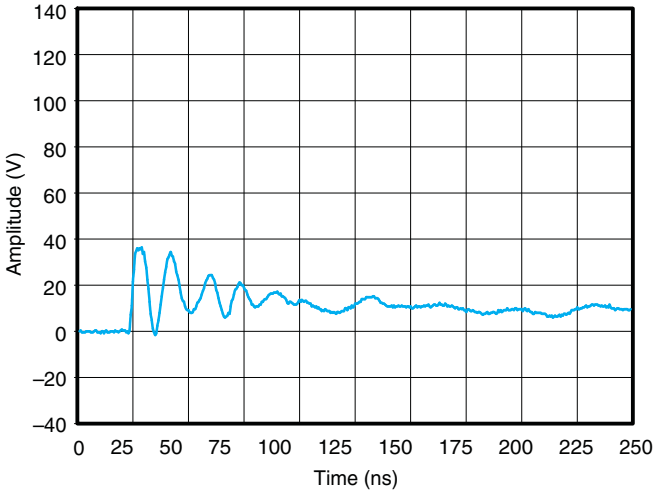



**Figure 11. $V_{BUS}$ IEC Clamping Waveform, 8 kV Contact, D+, 25 ns/div**

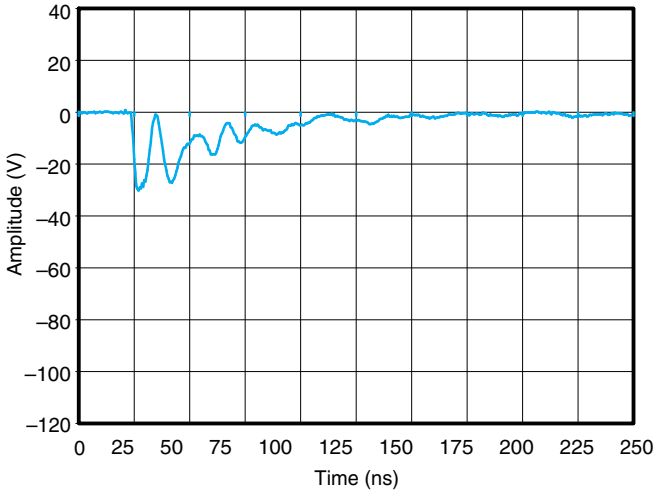



**Figure 12. $V_{BUS}$ IEC Clamping Waveform, –8 kV Contact, D+, 25 ns/div**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4S012DRYR | ACTIVE | SON | DRY | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 3B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

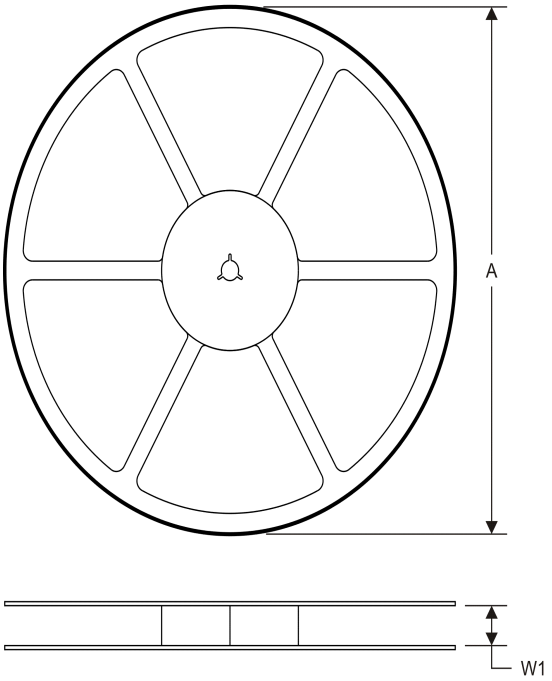
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

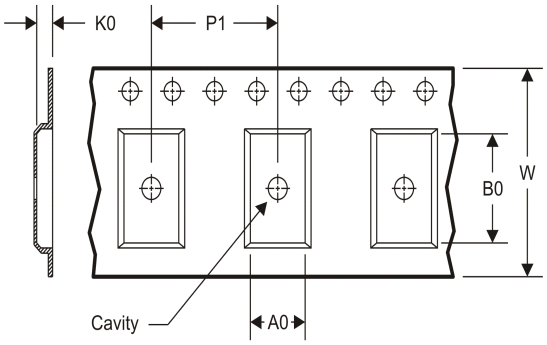
(4) Only one of markings shown within the brackets will appear on the physical device.

## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



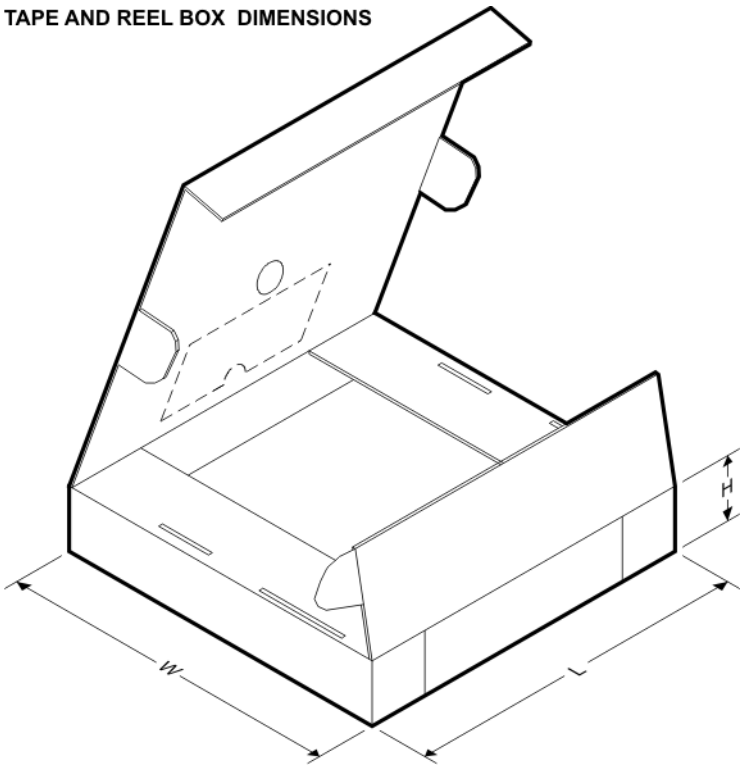

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPD4S012DRYR | SON | DRY | 6 | 5000 | 179.0 | 8.4 | 1.2 | 1.65 | 0.7 | 4.0 | 8.0 | Q1 |

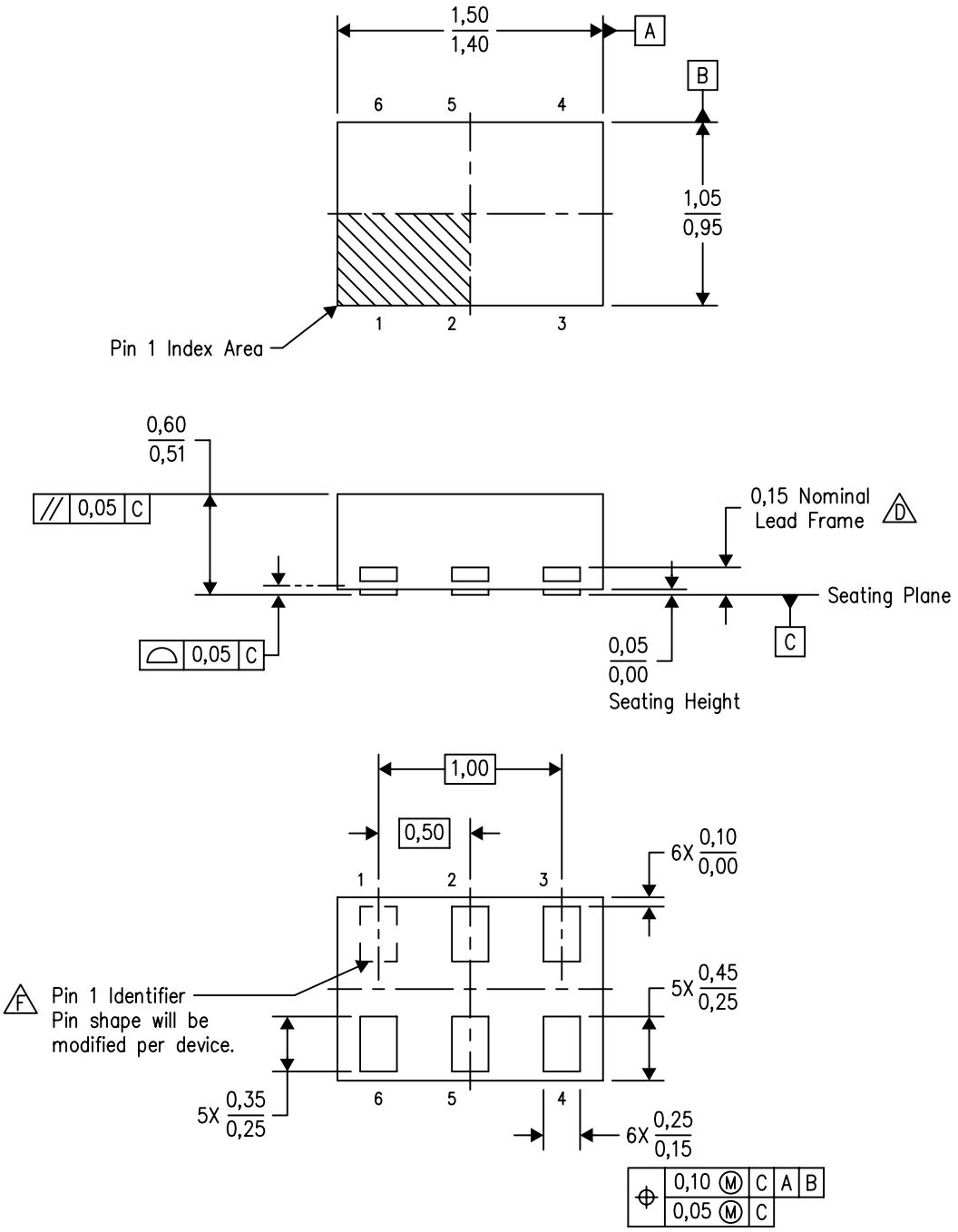
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPD4S012DRYR | SON | DRY | 6 | 5000 | 203.0 | 203.0 | 35.0 |

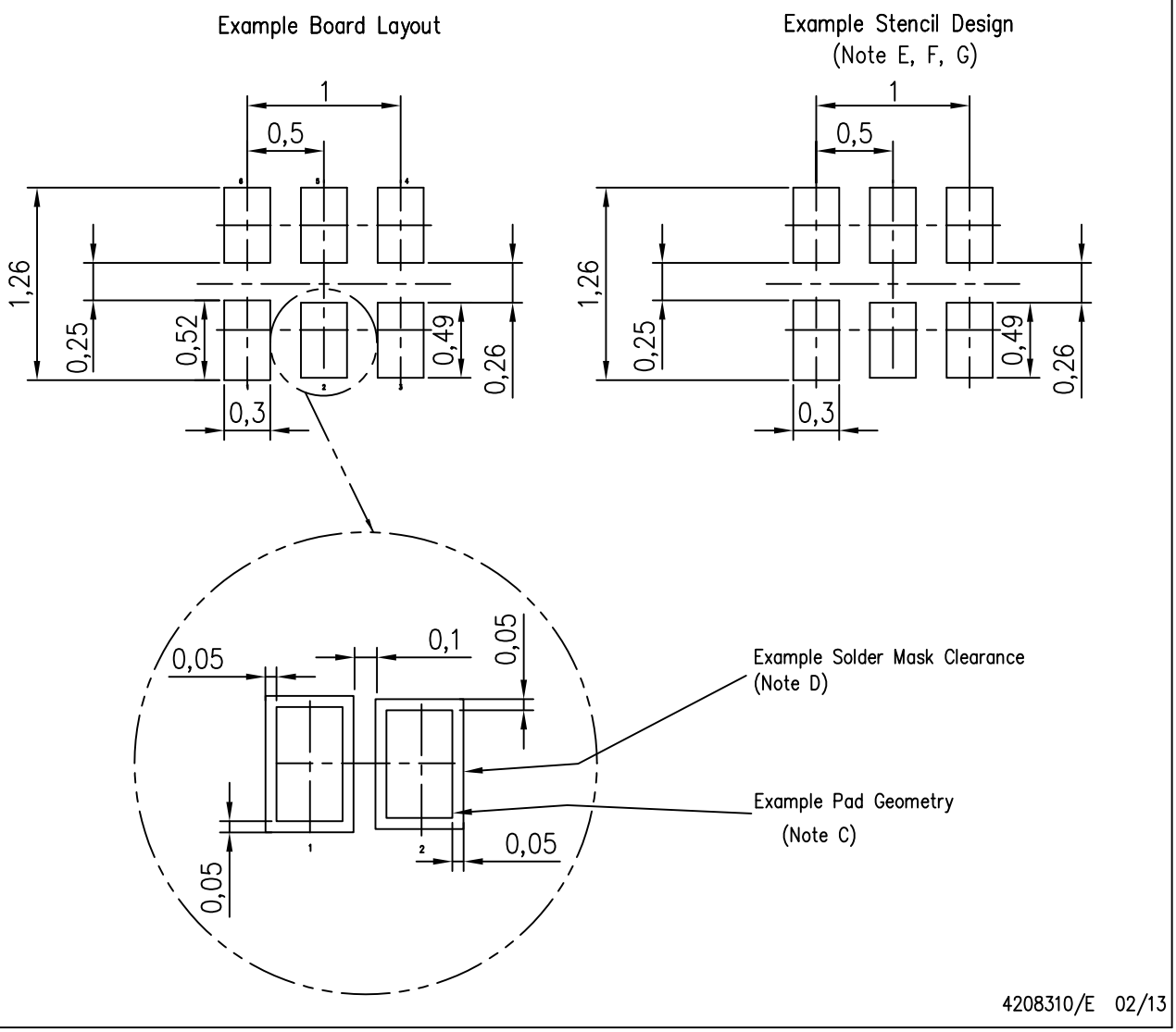
DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




4207181/F 12/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.
E. This package complies to JEDEC MO–287 variation UFAD.
F. See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.

DRY (R–PUSON–N6) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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