DUAL CHANNEL HIGH SPEED ESD PROTECTION DEVICE

Check for Samples: TPD2E1B06

FEATURES

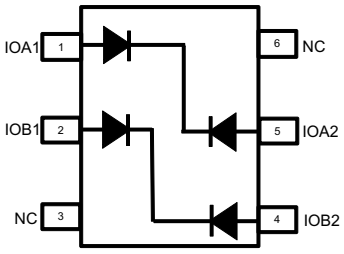
- **Provides System Level ESD Protection for Low Voltage IO Interface**
- **IEC 61000-4-2 Level 4 ESD Rating**
- **IO Capacitance 1pF (Typ)**
- **DC Breakdown Voltage 7V (Min)**
- **Ultra low Leakage Current 10nA (Max)**
- **Low ESD Clamping Voltage**
- **Automotive Temperature Range: –40°C to 125°C**
- **Small Easy-to-Route DRL package**

APPLICATIONS

- **Gaming Machines**
- **eBook**
- **Portable Media Players**
- **Digital Camera**

DESCRIPTION

The TPD2E1B06 is a dual channel ultra low cap ESD protection device. It offers ±10KV IEC contact ESD protection. Its 1pF line capacitance makes it suitable for a wide range of applications. Typical application interfaces are USB2.0, LVDS, and I2C. There are two common layout methods for TPD2E1B06 and both are highlighted in the Application Information section.



DRL
1.6 mm x 1.2 mm x 0.55mm
(0.5-mm pitch)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

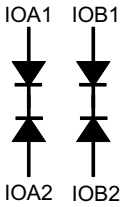


Figure 1. CIRCUIT SCHEMATIC DIAGRAM

TERMINAL FUNCTIONS

PIN		PIN TYPE	DESCRIPTION	USAGE
NAME	NO.			
IOA1	1	I/O	ESD protected channel	Please refer to the Application Information Section.
IOA2	5	I/O		
IOB1	2	I/O		
IOB2	4	I/O		
NC	3, 6	NC	No connect	Can be left floating, grounded, or connected to VCC

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Operating temperature range	–40 to 125	°C
	Storage temperature	–65 to 155	°C
	IEC 61000-4-2 contact ESD(1)	±10	kV
	IEC 61000-4-2 air gap ESD(1)	±15	kV
I_{PP}	Peak pulse current (tp = 8/20μs)(1)	2.5	A
P_{PP}	Peak pulse power (tp = 8/20μs)(1)	35	W

(1) Using Routing Option 1 or 2 as shown in Figure 2 or Figure 3.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPD2E1B06 DRL (6) PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	349.7	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	120.5	
θ_{JB}	Junction-to-board thermal resistance	171.4	
ψ_{JT}	Junction-to-top characterization parameter	10.8	
ψ_{JB}	Junction-to-board characterization parameter	169.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range. (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, I/O to GND (1)(2)		11		V
		I_{PP} = 5 A, TLP, I/O to GND (1)(2)		15		V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, GND to I/O (1)(2)		11		V
		I_{PP} = 5 A, TLP, GND to I/O (1)(2)		15		V
R_{DYN}	Dynamic resistance			0.9		Ω
C_{L1}	Pin 2 and 5 capacitance	Pin 1 and 4 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(3)		0.85		pF
C_{L2}	Pin 1 and 4 capacitance	Pin 2 and 5 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(4)		1.05		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	7		9.5	V
I_{LEAK}	Leakage current	V_{BIAS} = +2.5 V		1	10	nA

(1) Transmission line pulse with rise time 10ns and pulse width 100ns.
(2) T_A = 25°C
(3) Using Routing Option 1, Figure 2.
(4) Using Routing Option 2, Figure 3.

APPLICATION INFORMATION

There are 2 channels of back-to-back diodes in TPD2E1B06DRL. The device should be routed in one of the two ways shown below. Routing option 1 is recommended because TPD2E1B06 is designed to maximize signal integrity in this configuration while still comply with IEC 61000-4-2 level 4 contact ESD rating.

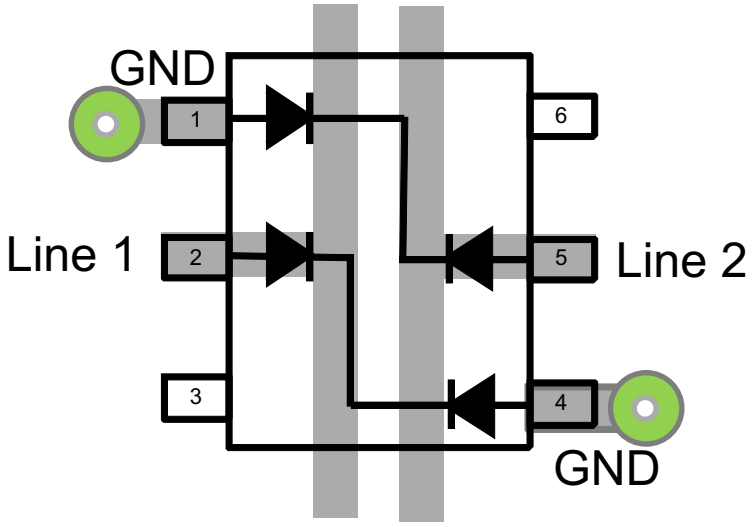


Figure 2. Routing Option 1

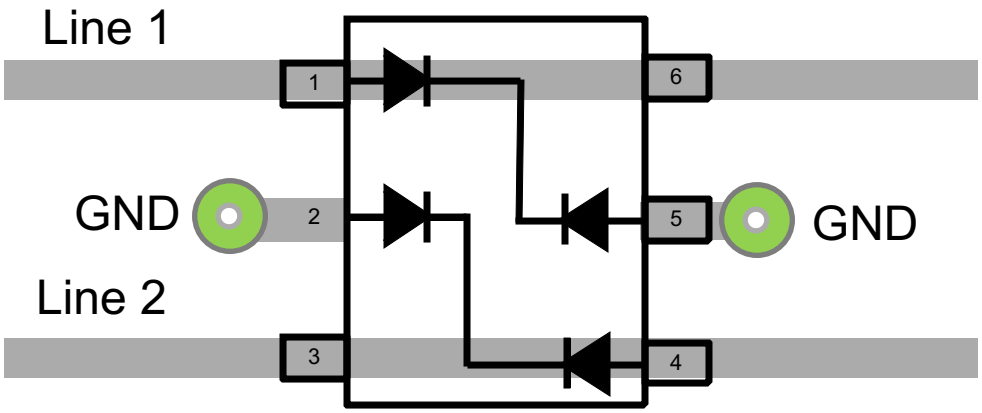


Figure 3. Routing Option 2

TYPICAL CHARACTERISTICS

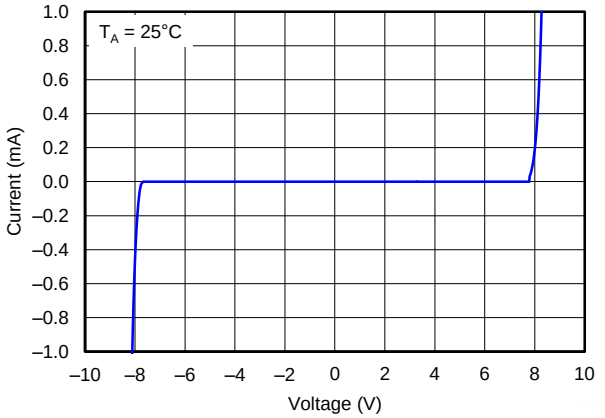


Figure 4. IV Curve

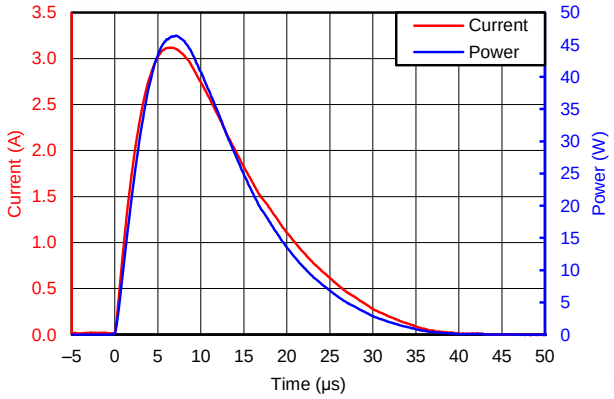


Figure 5. Max Surge Rating

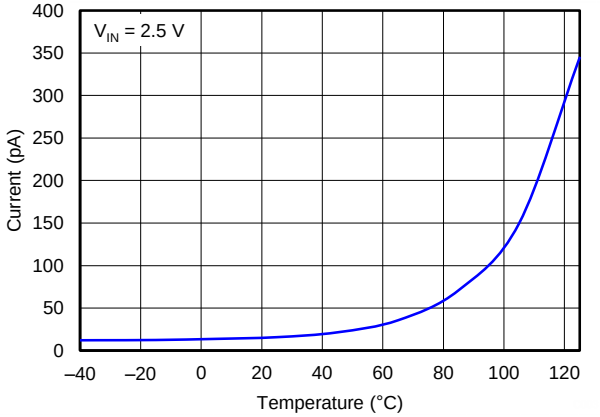


Figure 6. ILeak vs Temperature

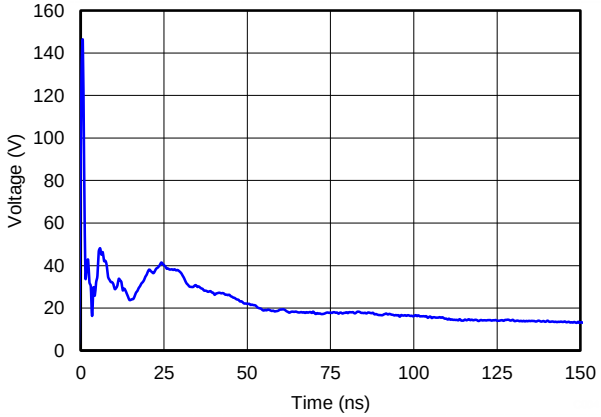


Figure 7. +8kV Contact ESD Clamping

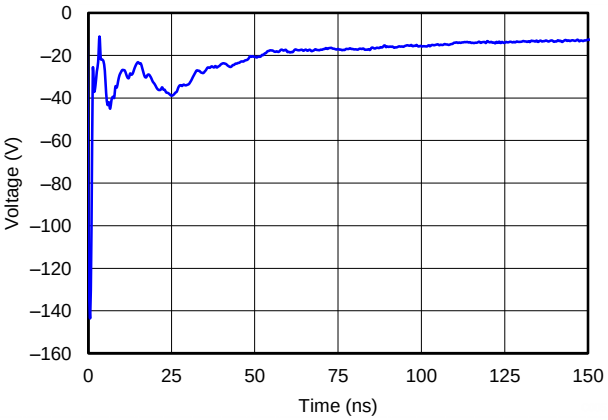


Figure 8. –8kV Contact ESD Clamping

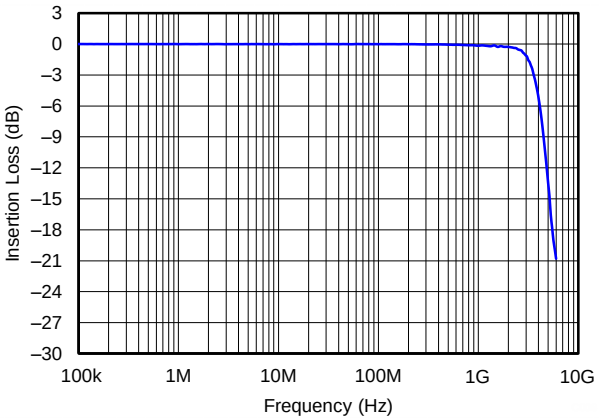


Figure 9. Insertion Loss

TYPICAL CHARACTERISTICS (continued)

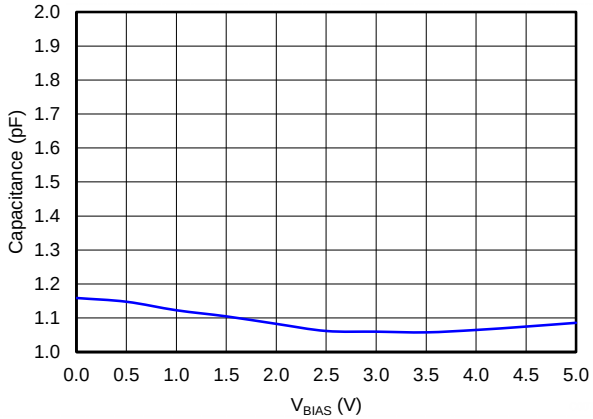


Figure 10. Capacitance vs Vbias

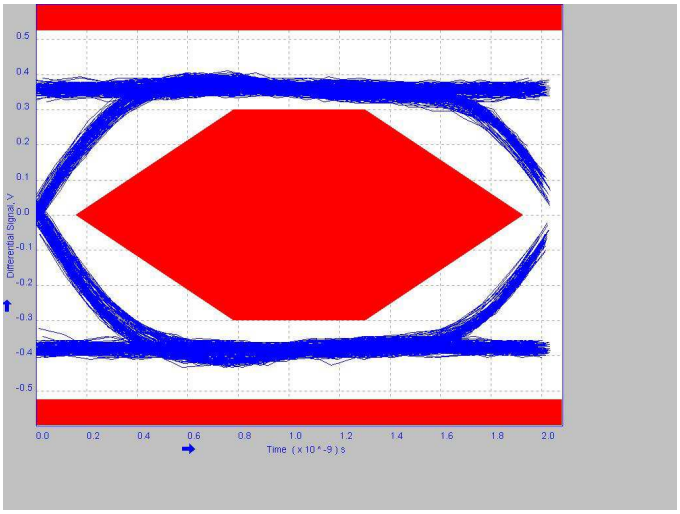


Figure 11. Eye Diagram Without TPD2E1B06DRL on EVM

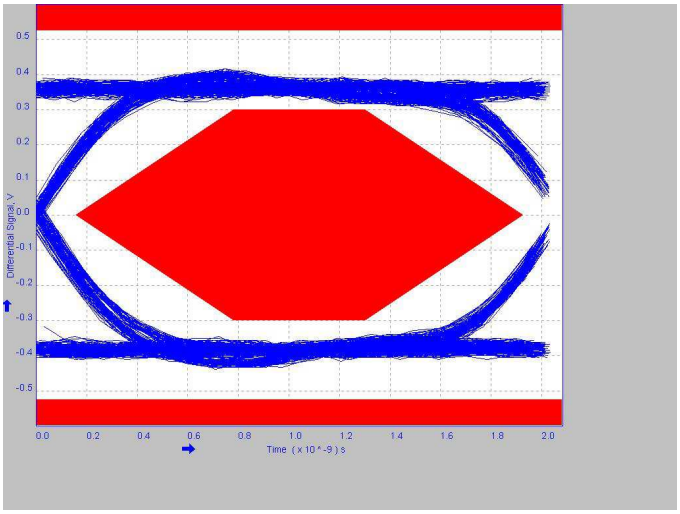


Figure 12. Eye Diagram With TPD2E1B06DRL on EVM

REVISION HISTORY

Changes from Original (July 2013) to Revision A	Page
• Revised document from PREVIEW to PRODUCTION DATA.	1

Changes from Revision A (August 2013) to Revision B	Page
• Added TYPICAL CHARACTERISTICS section.	5

Changes from Revision B (September 2013) to Revision C	Page
• Added air gap ESD specification to the ABSOLUTE MAXIMUM RATINGS table.	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E1B06DRLR	ACTIVE	SOT	DRL	6	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		DUL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

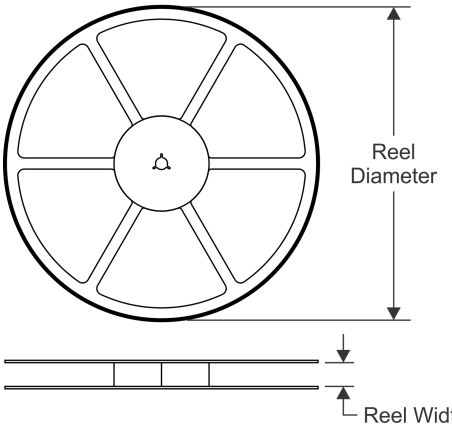
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

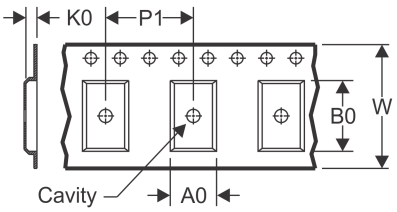
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

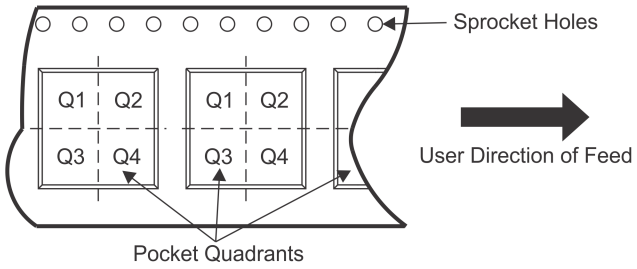


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

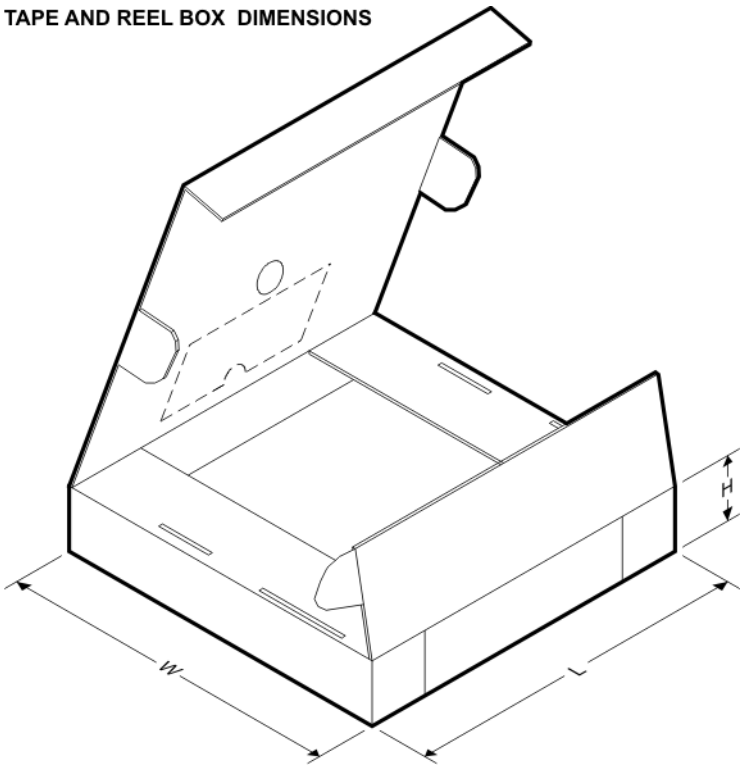
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

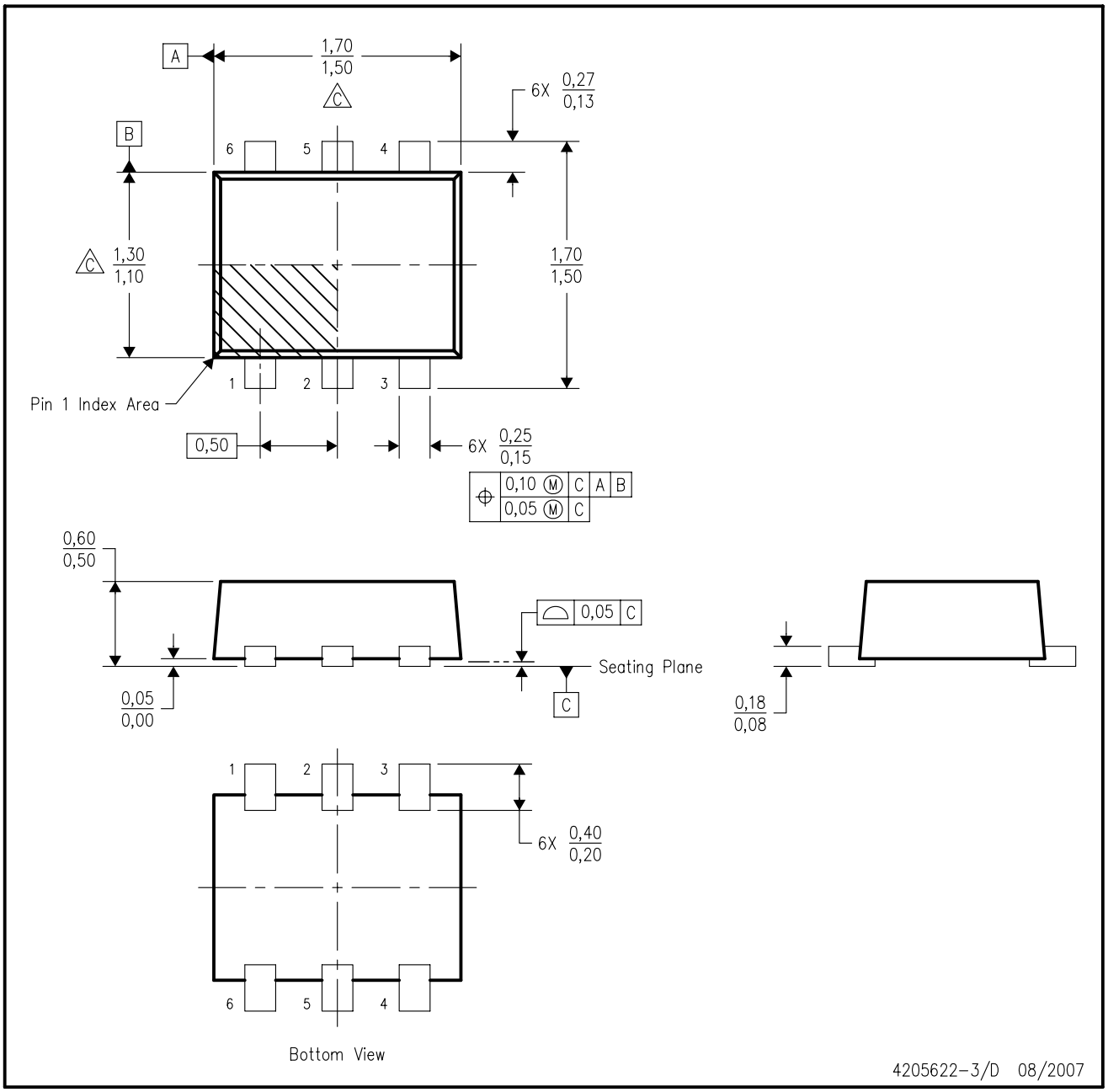
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E1B06DRLR	SOT	DRL	6	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



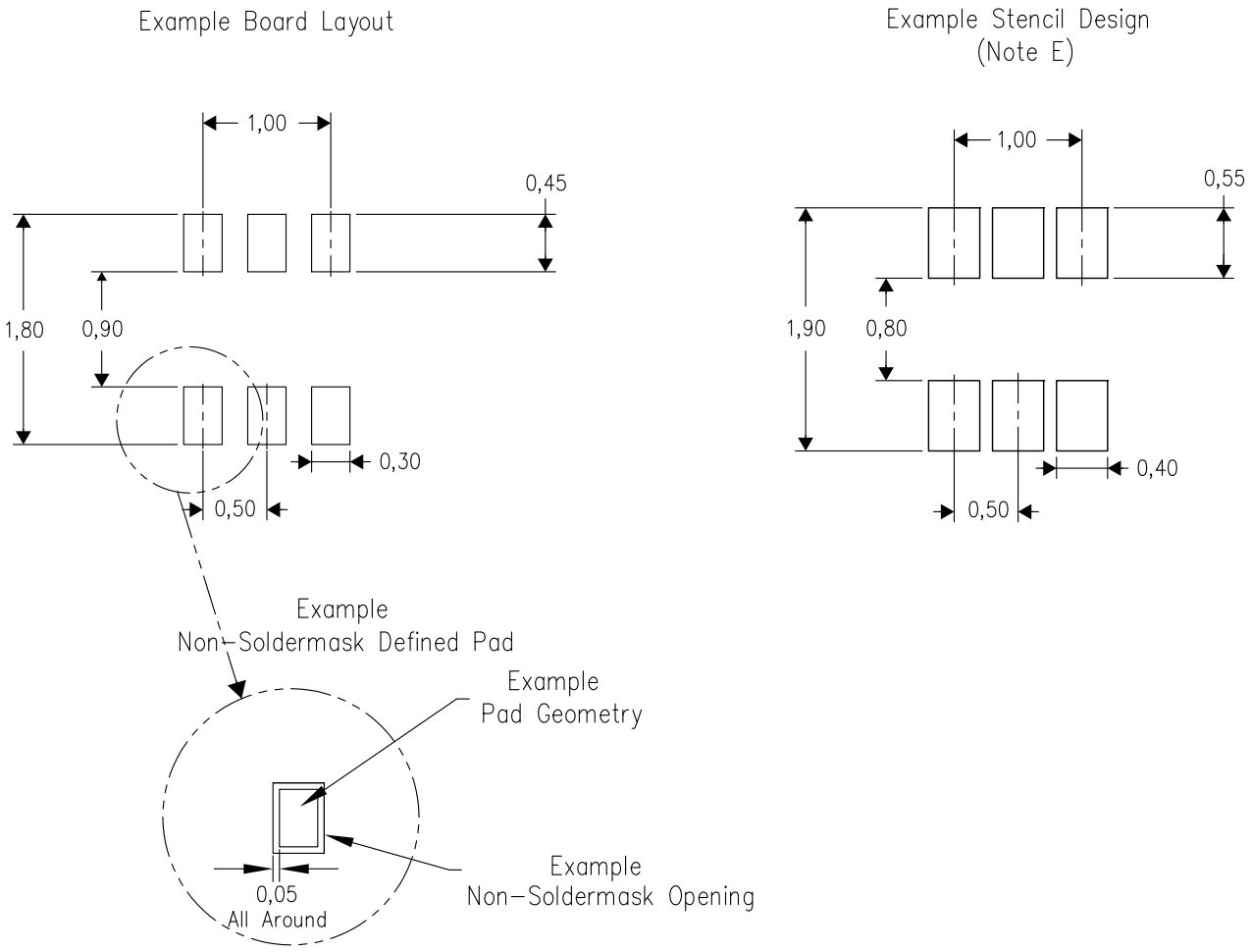
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E1B06DRLR	SOT	DRL	6	4000	180.0	180.0	30.0



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N6) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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