TPD1E01B04 1-Channel ESD Protection Diode for USB Type-C and Thunderbolt 3

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±15-kV Contact Discharge
  - ±17-kV Air Gap Discharge
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- IO Capacitance:
  - 0.18 pF (Typical)
  - 0.2 pF (Maximum)
- DC Breakdown Voltage: 6.4 V (Typical)
- Ultra Low Leakage Current: 10-nA (Maximum)
- Low ESD Clamping Voltage: 15 V at 16 A TLP
- Low Insertion Loss: 26.9 GHz (–3 dB Bandwidth)
- Supports High Speed Interfaces up to 20 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Ultra-small 0201 footprint

2 Applications

- End Equipment
  - Laptops and Desktops
  - Mobile and Tablets
  - Set-Top Boxes
  - TV and Monitors
  - USB Dongles
  - Docking Stations
- Interfaces
  - USB Type-C
  - Thunderbolt 3
  - USB 3.1 Gen 2
  - HDMI 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - PCI Express 3

3 Description

The TPD1E01B04 is a bidirectional TVS ESD protection diode array for USB Type-C and Thunderbolt 3 circuit protection. The TPD1E01B04 is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

This device features a 0.18-pF (typical) IO capacitance making it ideal for protecting high-speed interfaces up to 20 Gbps such as USB 3.1 Gen2 and Thunderbolt 3. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

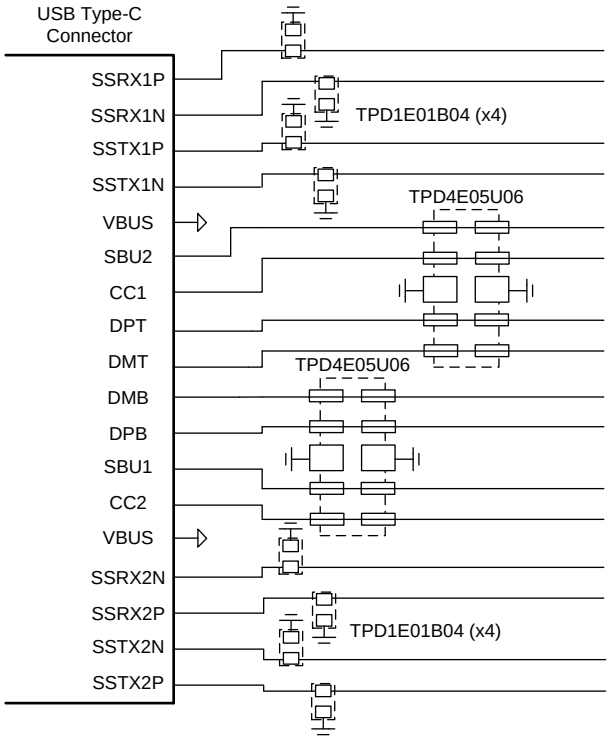
The TPD1E01B04 is offered in the industry standard 0201 (DPL) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD1E01B04	X2SON (2)	0.60 mm x 0.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2016) to Revision B **Page**

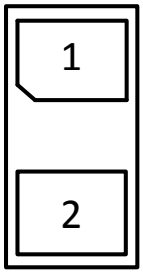
- Made changes to the *Electrical Characteristics* table. Updated limits for V_{HOLD} ... 1

Changes from Original (March 2016) to Revision A **Page**

- Changed device status from *Product Preview* to *Production Data* ... 1

5 Pin Configuration and Functions

DPL Package
2-Pin X2SON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs)		27	W
	IEC 61000-4-5 current (t_p - 8/20 µs)		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		IEC 61000-4-2 air-gap discharge	±17000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E01B04 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	582	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	264.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	394.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	36.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	394.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to IO pin			–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	5.9	6.5	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		7		V
		I_{PP} = 5 A, TLP, from IO to GND		9.2		
		I_{PP} = 16 A, TLP, from IO to GND		15		
		I_{PP} = 1 A, TLP, from GND to IO		7		
		I_{PP} = 5 A, TLP, from GND to IO		9.2		
		I_{PP} = 16 A, TLP, from GND to IO		15		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.57		Ω
		GND to IO		0.57		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND T_A = 25°C		0.18	0.20	pF

6.7 Typical Characteristics

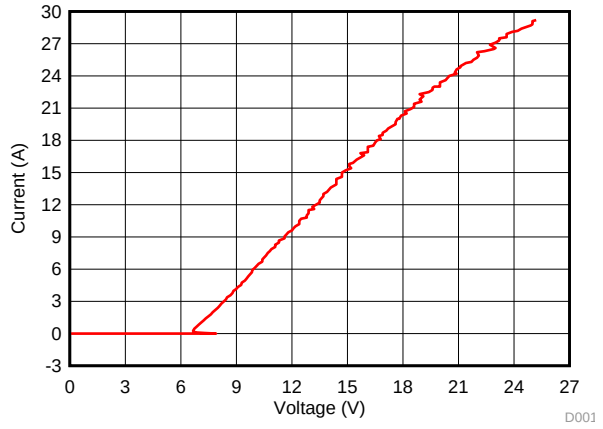


Figure 1. Positive TLP Curve

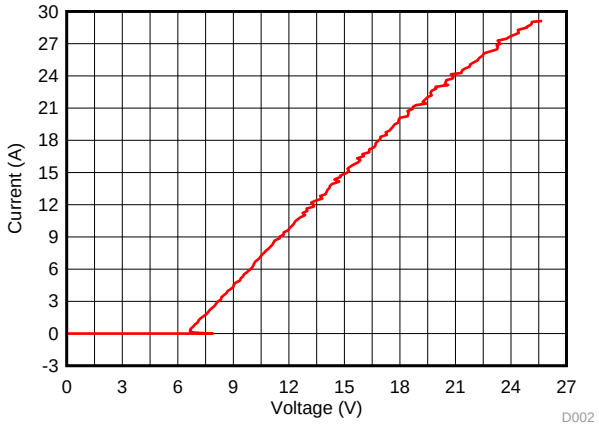


Figure 2. Negative TLP Curve

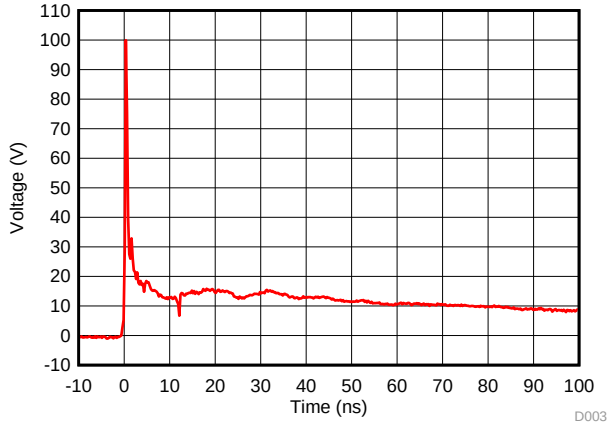


Figure 3. 8-kV IEC Waveform

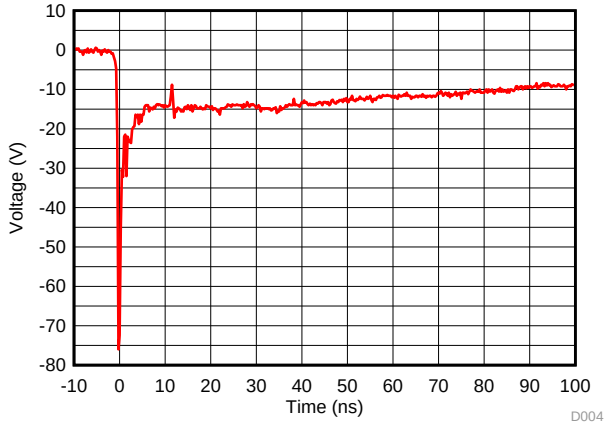


Figure 4. –8-kV IEC Waveform

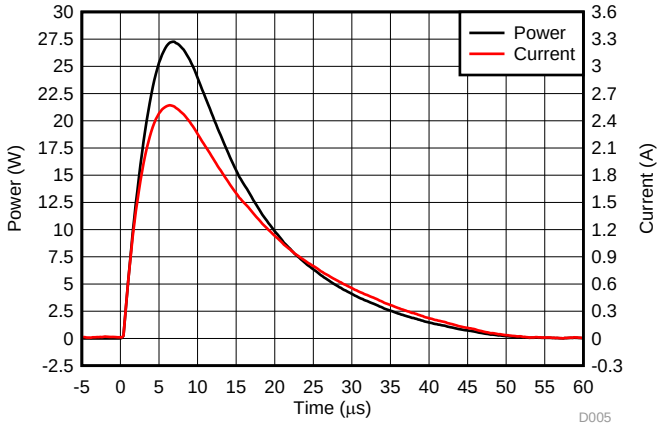


Figure 5. Surge Curve (t_p = 8/20µs), IO pin to GND

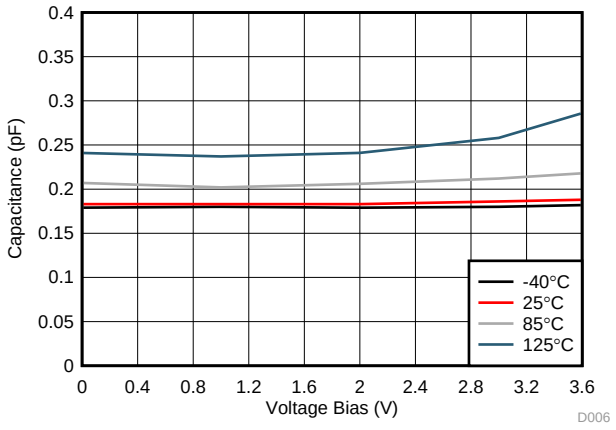


Figure 6. Capacitance vs. Bias Voltage

Typical Characteristics (continued)

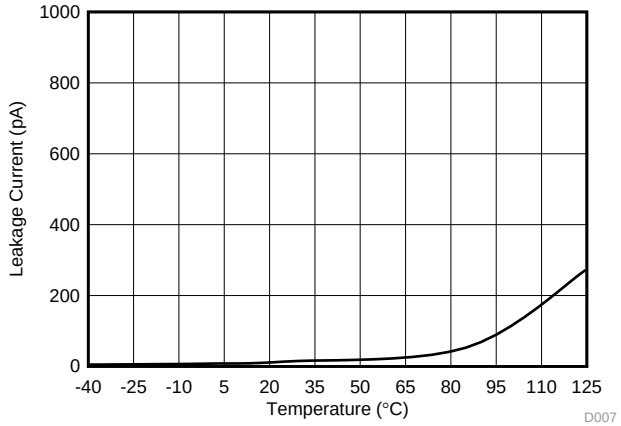


Figure 7. Leakage Current vs. Temperature

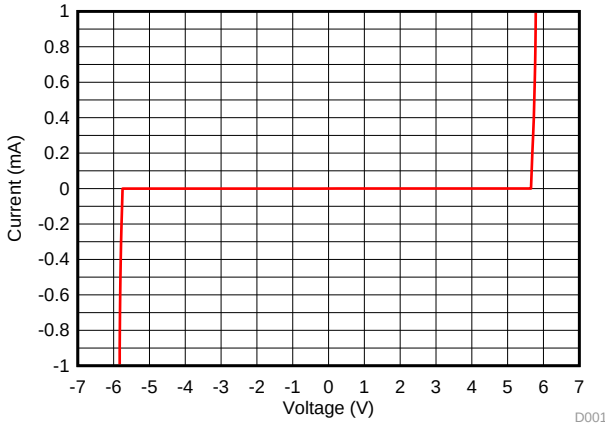


Figure 8. DC Voltage Sweep I-V Curve

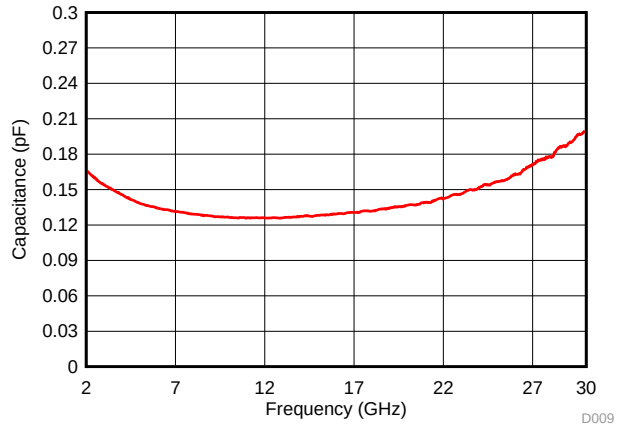


Figure 9. Capacitance vs. Frequency

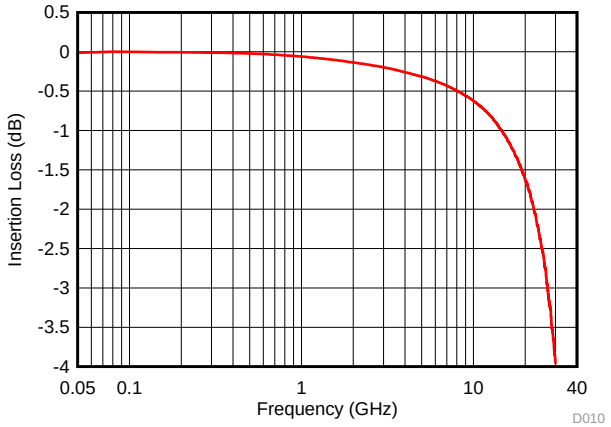


Figure 10. Insertion Loss

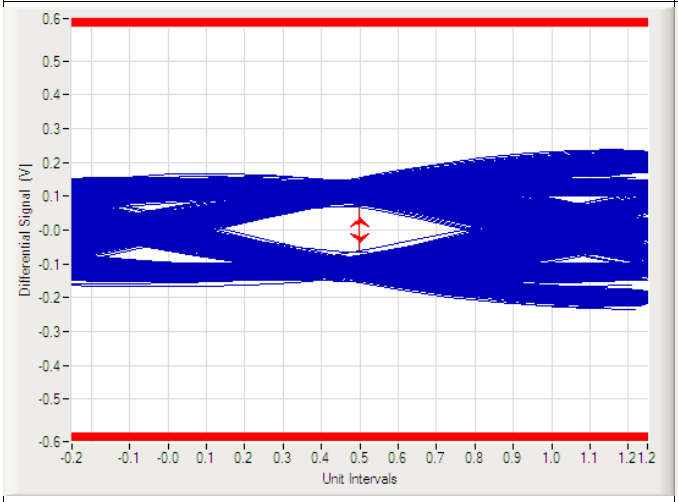


Figure 11. USB3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

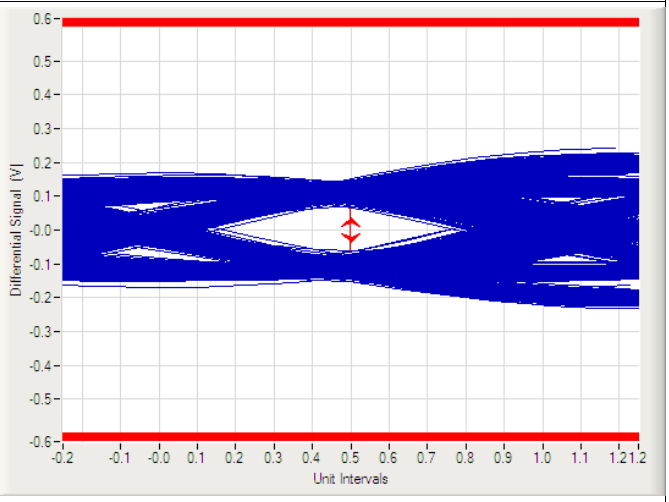


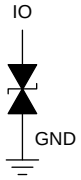
Figure 12. USB3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04)

7 Detailed Description

7.1 Overview

The TPD1E01B04 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins including Thunderbolt 3. The low capacitance allows for extremely low losses even at RF frequencies such as USB 3.1 Gen 2, Thunderbolt 3, or antenna applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±15-kV contact and ±17-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 27 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.18 pF (typical) and 0.20 pF (maximum). This device supports data rates up to 20 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V (typical). This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±2.5 V

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.2 V (I_{PP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 20 Gbps, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

Feature Description (continued)

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E01B04 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E01B04 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E01B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

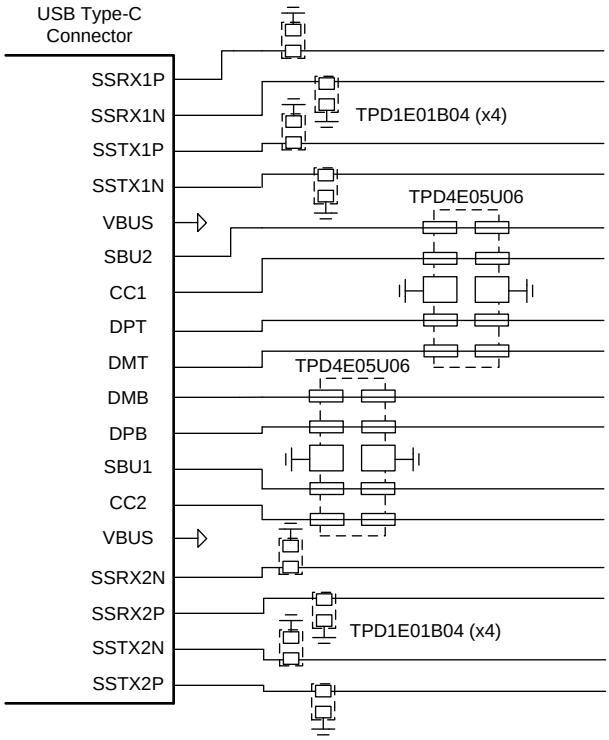


Figure 13. USB Type-C for Thunderbolt 3 ESD Schematic

8.2.1 Design Requirements

For this design example eight TPD1E01B04 devices and two TPD4E05U06 devices are being used in a USB Type-C for Thunderbolt 3 application. This provides a complete ESD protection scheme.

Given the Thunderbolt 3 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on superspeed Lines	0 V to 3.6 V
Operating frequency on superspeed Lines	up to 10 GHz
Signal range on CC, SBU, and DP/DM Lines	0 V to 5 V

Typical Application (continued)

Table 1. Design Parameters (continued)

DESIGN PARAMETER	VALUE
Operating frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E01B04 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP-DM lines.

8.2.2.2 Operating Frequency

The TPD1E01B04 has a 0.18 pF (typical) capacitance, which supports the Thunderbolt 3 data rates of 20 Gbps. The TPD4E05U06 has a 0.5-pF (typical) capacitance, which easily supports the CC, SBU, and DP-DM data rates.

8.2.3 Application Curves

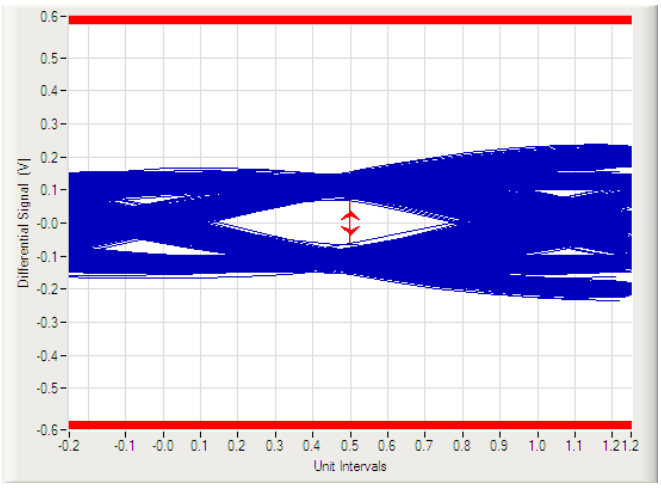


Figure 14. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

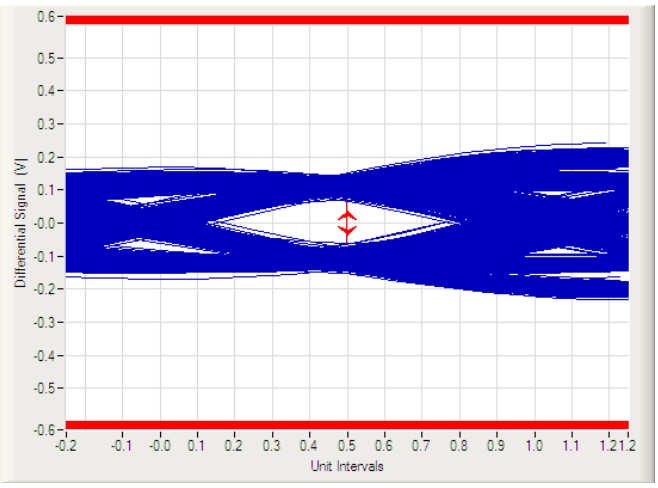


Figure 15. USB 3.1 Gen 2 10-Gbps Eye Diagram (with TPD1E01B04)

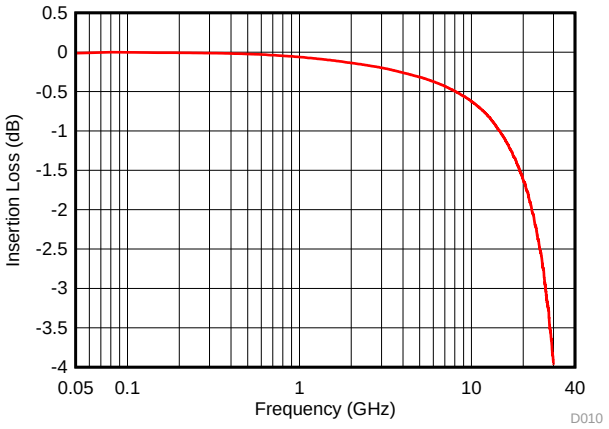


Figure 16. Insertion Loss

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

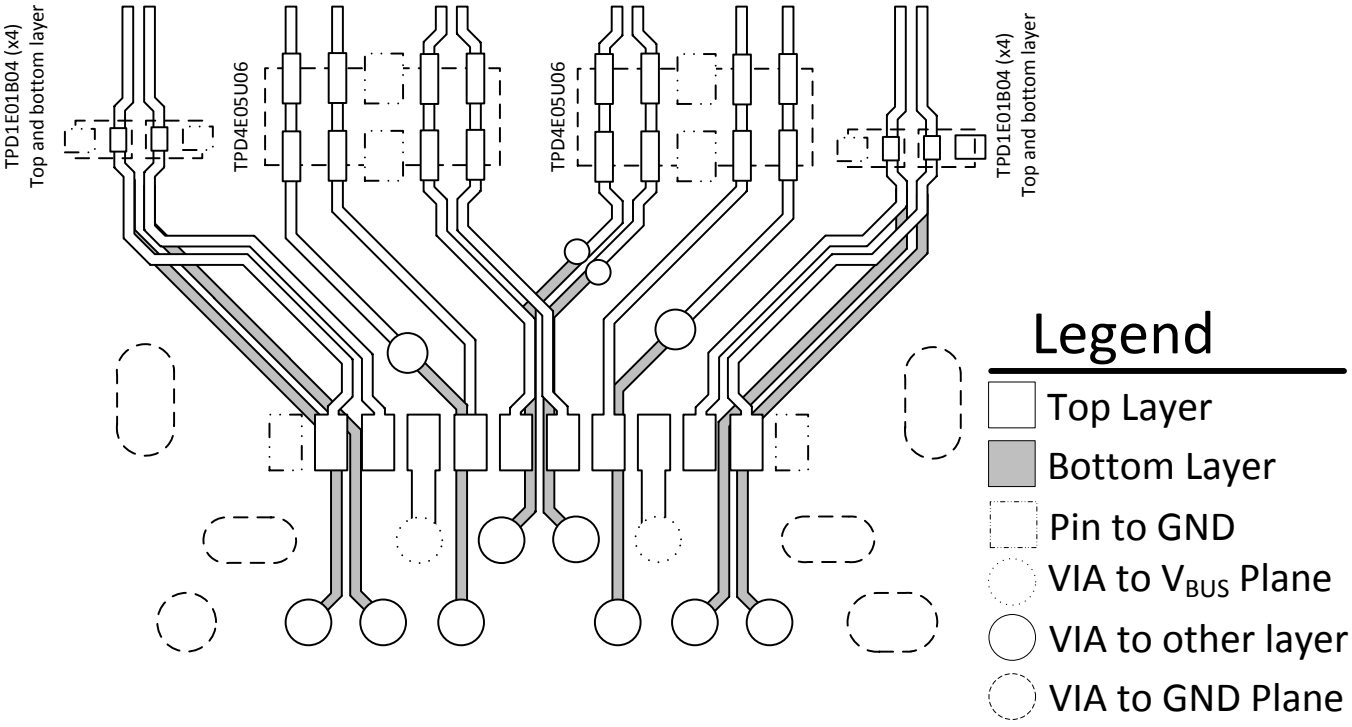


Figure 17. USB Type-C Mid-Mount, Hybrid Connector ESD Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

TPD1E01B04 Evaluation Module User's Guide, SLVUAN5

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E01B04DPLR	ACTIVE	X2SON	DPL	2	15000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TPD1E01B04DPLT	ACTIVE	X2SON	DPL	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7	Samples
TPD1E01B04DPYR	PREVIEW	X1SON	DPY	2	10000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5C	
TPD1E01B04DPYT	PREVIEW	X1SON	DPY	2	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5C	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

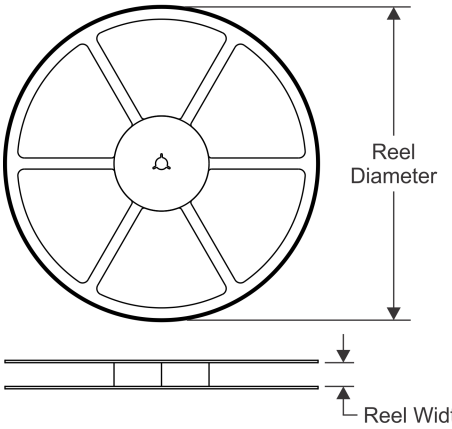
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

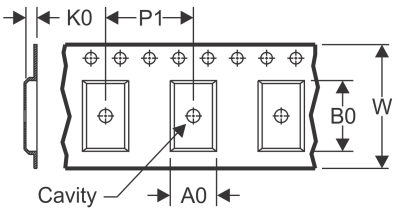
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

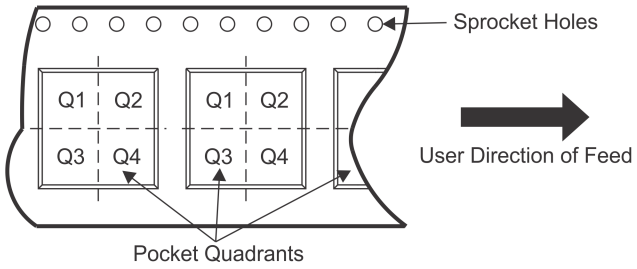


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

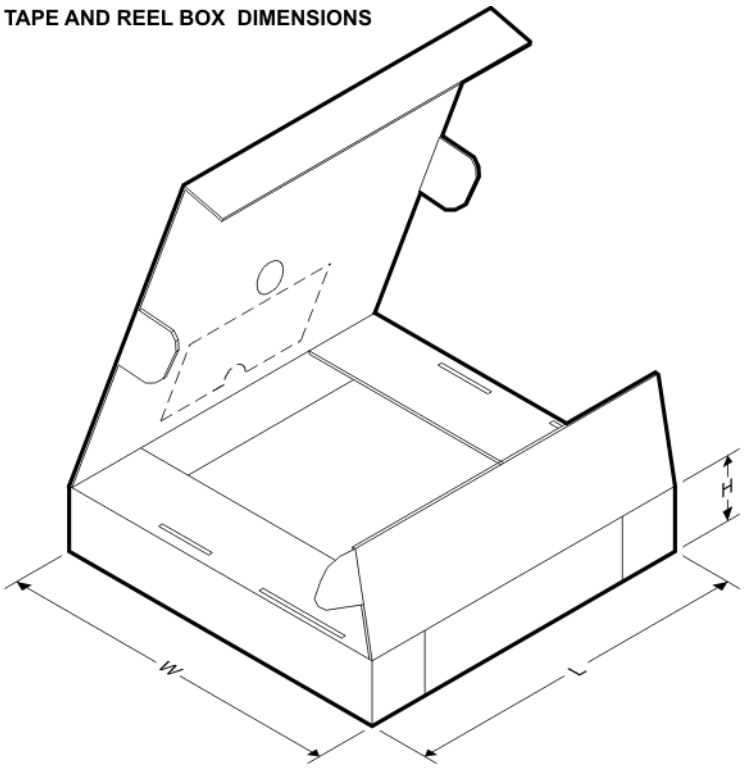
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E01B04DPLR	X2SON	DPL	2	15000	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1
TPD1E01B04DPLT	X2SON	DPL	2	250	178.0	8.4	0.36	0.66	0.33	2.0	8.0	Q1

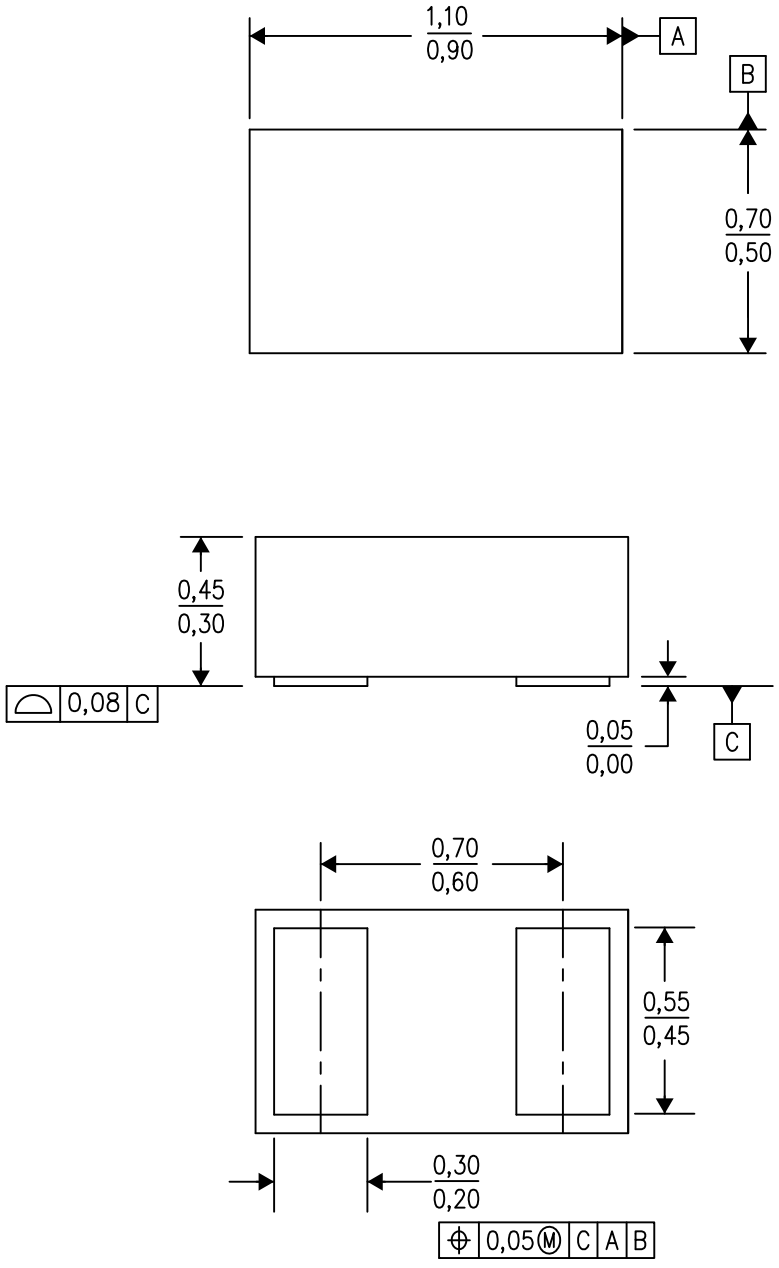
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E01B04DPLR	X2SON	DPL	2	15000	205.0	200.0	33.0
TPD1E01B04DPLT	X2SON	DPL	2	250	205.0	200.0	33.0

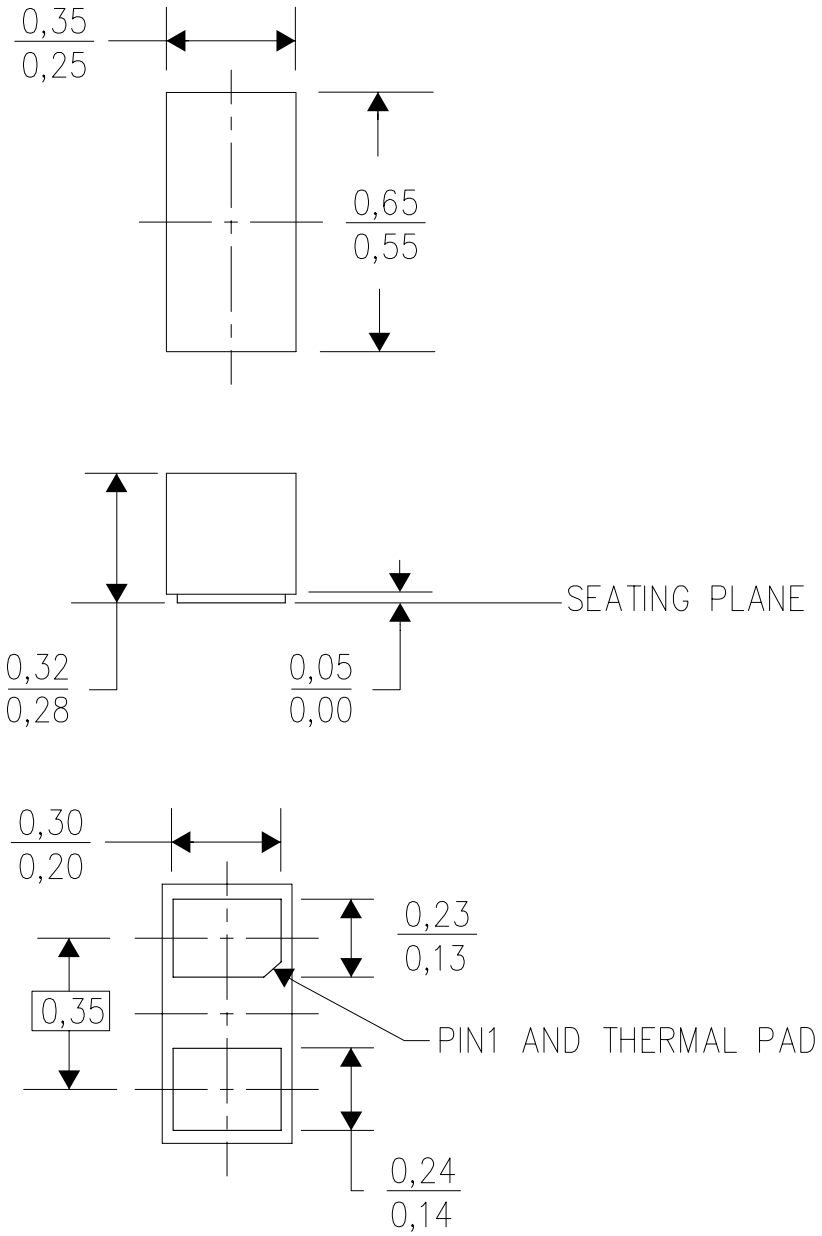
DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD

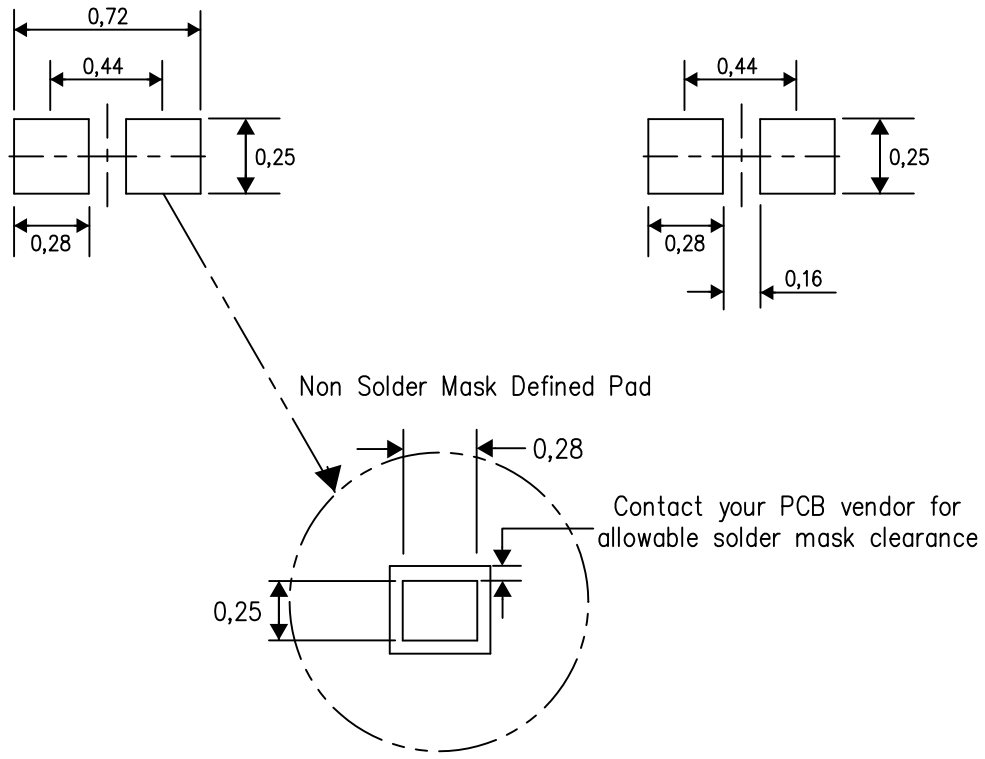


4212149/B 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

DPL (R–PX2SON–N2) SMALL PACKAGE OUTLINE NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)

4217903/A 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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