TMUX1511 Low-Capacitance, 1:1 (SPST) 4-Channel, Powered-Off Protected Switch with 1.8 V Logic

1 Features

- Wide Supply Range: 1.5 V to 5.5 V
- Low On-Capacitance: 3.3 pF
- Low On-Resistance: 2 Ω
- High Bandwidth: 2 GHz
- 1.8 V Logic Compatible
- Supports input voltage beyond supply
- Bidirectional Signal Path
- Fail-Safe Logic
- -40°C to +125°C Operating Temperature
- Powered-off Protection up to 3.6 V Signals
  - Pinout compatible to SN74CBTLV3126
  - Pinout compatible (logic variant) of SN74CBTLV3125

2 Applications

- Servers
- Data Center Switches & Routers
- PC/Notebooks
- Building Automation
- ePOS
- Motor Drives
- Appliances
- Battery-Powered Equipment
- JTAG Isolation
- SPI Isolation

3 Description

The TMUX1511 is a complementary metal-oxide semiconductor (CMOS) analog switch. The TMUX1511 offers 1:1 SPST switch configuration with 4-channels. Wide operating supply of 1.5 V to 5.5 V allows for use in a wide array of applications from servers and communication equipment to industrial applications. The device supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins and can pass signals above supply up to V_{DD} x 2, with a maximum of 5.5 V.

Powered-off Protection up to 3.6 V on the signal path of the TMUX1511 provides isolation when the supply voltage is removed (V_{DD} = 0 V). Without this protection feature, switches can back-power the supply rail through an internal ESD diode and cause potential damage to the system.

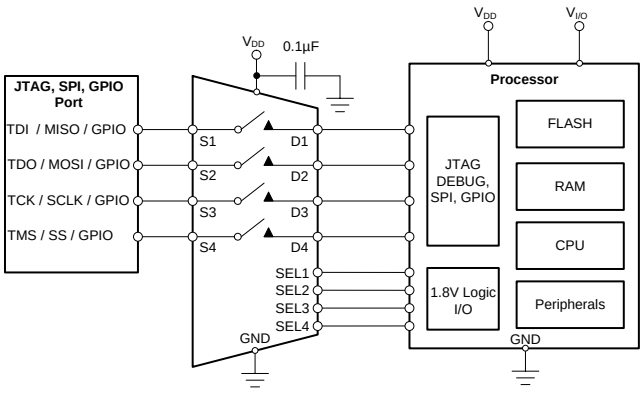
Fail-Safe Logic circuitry allows voltages on the digital control pins to be applied before the supply pin, protecting the device from potential damage. All digital control inputs have 1.8 V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

Device Information(1)

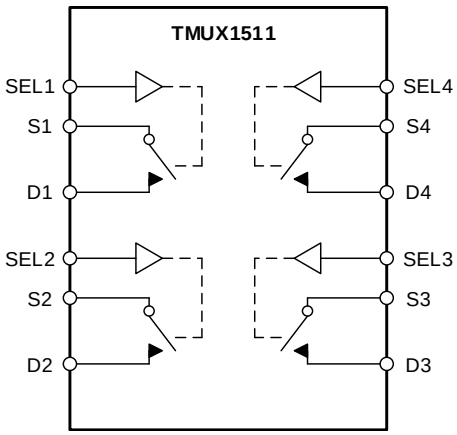
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX1511	TSSOP (14)	5.00 mm × 4.40 mm
	QFN (16)	2.60 mm x 1.80 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Application Example



Simplified Schematic



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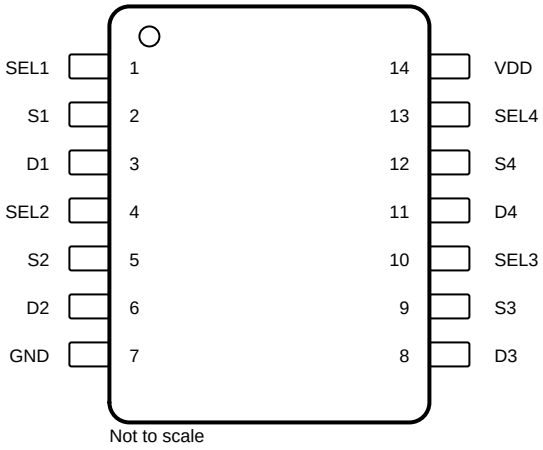
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2018	*	Preliminary release.

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



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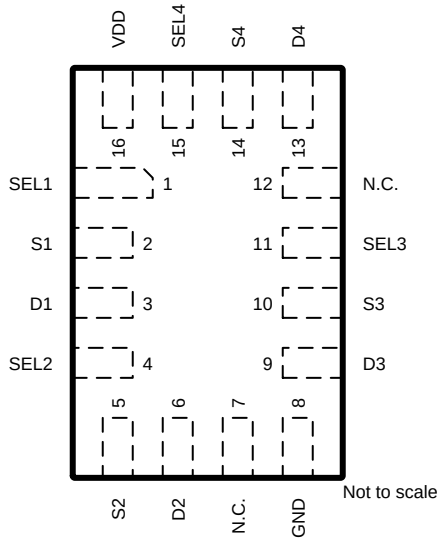
RSV Package
16-Pin QFN
Top View



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Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	UQFN		
SEL1	1	1	I	Select pin 1: controls state of switch #1 (logic low = OFF, logic high = ON)
S1	2	2	I/O	Source pin 1. Can be an input or output.
D1	3	3	I/O	Drain pin 1. Can be an input or output.
SEL2	4	4	I	Select pin 2: controls state of switch #2 (logic low = OFF, logic high = ON)
S2	5	5	I/O	Source pin 2. Can be an input or output.
D2	6	6	I/O	Drain pin 2. Can be an input or output.
N.C.	-	7	Not Connected	Not Connected - Can be shorted to GND or left floating
GND	7	8	P	Ground (0 V) reference
D3	8	9	I/O	Drain pin 3. Can be an input or output.
S3	9	10	I/O	Source pin 3. Can be an input or output.
SEL3	10	11	I	Select pin 3: controls state of switch #3 (logic low = OFF, logic high = ON)
N.C.	-	12	Not Connected	Not Connected - Can be shorted to GND or left floating
D4	11	13	I/O	Drain pin 4. Can be an input or output.
S4	12	14	I/O	Source pin 4. Can be an input or output.
SEL4	13	15	I	Select pin 4: controls state of switch #4 (logic low = OFF, logic high = ON)
VDD	14	16	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.

(1) I = input, O = output, I/O = input and output, P = power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage(3)	–0.5	6	V
V_{SEL}	Logic control input pin voltage (SEL1, SEL2, SEL3, SEL4)(3)	–0.5	6	V
I_{SEL}	Logic control input pin current (SEL1, SEL2, SEL3, SEL4)	-30	30	mA
V_S or V_D	Source or drain pin voltage(3)	–0.5	6	V
I_S or $I_{D\ (CONT)}$	Source and drain pin continuous current: (S1 to S4, D1 to D4)	-25	25	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.5	5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin), $V_{DD} \geq 1.5$ V	0	5.5	V
V_{S_off} or V_{D_off}	Signal path input/output voltage (source or drain pin), $V_{DD} < 1.5$ V(1)	0	3.6	V
V_{SEL}	Control input voltage (SELx pins)	0	5.5	V
T_A	Ambient temperature	–40	125	ºC

(1) V_{S_off} and V_{D_off} refers to the voltage at the source or drain pins when supply is less than 1.5 V

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE PW (TSSOP) 14 PINS	DEVICE RSV (UQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	129.4	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.6	TBD	°C/W
Y_{JB}	Junction-to-board characterization parameter	71.9	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics

V_{DD} = 1.5 V to 5.5 V, GND = 0V, T_A = -40°C to +125°C, Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{DD}	Power supply voltage		1.5		5.5	V
I_{DD}	Active supply current	V_{IN} = 0 V, 1.4 V or V_{DD} V_S = 0 V to 5.5 V		37	70	µA
DC Characteristics						
R_{ON}	ON-state resistance	V_S = 0 V to V_{DD} I_{DS} = 8 mA Refer to ON-State Resistance Figure		2	5	Ω
R_{ON}	ON-state resistance	V_S = V_{DD}*2 $V_{S(max)}$ = 5.5 V I_{DS} = 8 mA Refer to ON-State Resistance Figure		2	5	Ω
ΔR_{ON}	ON-state resistance match between channels	V_S = V_{DD} I_{DS} = 8 mA Refer to ON-State Resistance Figure		0.07		Ω
R_{ON} (FLAT)	ON-state resistance flatness	V_S = 0 V to V_{DD} I_{DS} = 8 mA Refer to ON-State Resistance Figure		3.5		Ω
I_{POFF}	Power-off I/O pin leakage current	V_{DD} = 0 V V_S = 0 V to 3.6 V V_D = 0 V Refer to Ipoff Leakage Figure	-2	0	2	µA
$I_{S(OFF)}$ $I_{D(OFF)}$	Powered I/O pin leakage current	Switch Off V_D = 0.8*V_{DD} / 0.2*V_{DD} or V_S = 0.2*V_{DD} / 0.8*V_{DD} Refer to Off Leakage Figure	-1	0	1	µA
$I_{D(ON)}$ $I_{S(ON)}$	ON leakage current	Switch On V_D = 0.8*V_{DD} / 0.2*V_{DD}, S pins floating or V_S = 0.8*V_{DD} / 0.2*V_{DD}, D pins floating Refer to On Leakage Figure	-50	1	50	nA
Digital Characteristics						
V_{IH}	Input logic high		1.4		5.5	V
V_{IL}	Input logic low		0		0.5	V
I_{IH}	Input high leakage current	V_{SEL} = 1.8 V, V_{DD}	-1	1	2	µA
I_{IL}	Input low leakage current	V_{SEL} = 0 V	-1	±0.2	2	µA
R_{PD}	Internal pull-down resistor on digital input pins			6		MΩ
C_I	Digital input capacitance	V_{SEL} = 0 V, 1.8 V or V_{DD} f = 1 MHz		3		pF

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6.6 Dynamic Characteristics

V_{DD} = 1.5 V to 5.5 V, GND = 0V, T_A = -40°C to +125°C, Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	Source and drain off capacitance	$V_S = V_{DD} / 2$ V_{SEL}= 0 V f = 1 MHz Refer to Capacitance Figure	Switch OFF		2.5	5	pF
C_{ON}	Source and drain on capacitance	$V_S = V_{DD} / 2$ V_{SEL}= V_{DD} f = 1 MHz Refer to Capacitance Figure	Switch ON		3.3	5	pF
Q_C	Charge Injection	$V_S = V_{DD} / 2$ R_S = 0 Ω, C_L =1 nF Refer to Charge Injection Figure	Switch ON		10		pC
O_{ISO}	Off isolation	R_L = 50 Ω f = 100 kHz Refer to Off Isolation Figure	Switch OFF		-90		dB
		R_L = 50 Ω f = 1 MHz Refer to Off Isolation Figure	Switch OFF		-60		dB
X_{TALK}	Channel to Channel crosstalk	R_L = 50 Ω f = 100 kHz Refer to Crosstalk Figure	Switch ON		-90		dB
BW	Bandwidth	R_L = 50 Ω Refer to BW and Insertion Loss Figure	Switch ON		2		GHz
I_{LOSS}	Insertion loss	RL = 50 Ω f = 1 MHz Refer to BW and Insertion Loss Figure	Switch ON		-0.5		dB

6.7 Timing Requirements

V_{DD} = 1.5 V to 5.5 V, GND = 0V, T_A = -40°C to +125°C, Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ON(VDD)}$	Device turn on time (V_{DD} to output)	$V_S = V_{DD}$, V_{DD} rise time = 1us R_L = 200 Ω, C_L = 15pF Refer to Ton-Vdd & Toff-Vdd Figure		20	60	us
$t_{OFF(VDD)}$	Device turn off time (V_{DD} to output)	$V_S = V_{DD}$ V_{DD} fall time = 1us R_L = 200 Ω, C_L = 15pF Refer to Ton-Vdd & Toff-Vdd Figure		1.2	4	µs
t_{TRAN}	Transition time from control input	V_{DD} < 2.3 V $V_S = V_{DD}$ R_L = 200 Ω, C_L = 15pF Refer to Transition Time Figure		50	80	ns
t_{TRAN}	Transition time from control input	V_{DD} = 2.3 V to 5.5 V $V_S = V_{DD}$ R_L = 200 Ω, C_L = 15pF Refer to Transition Time Figure		25	50	ns

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7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 1 . Voltage (V) and current (I_{DS}) are measured using this setup, and R_{ON} is computed as shown below with $R_{ON} = V / I_{SD}$:

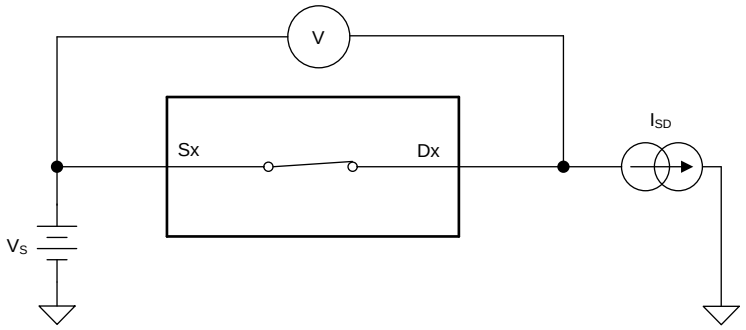

Figure 1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in Figure 2.

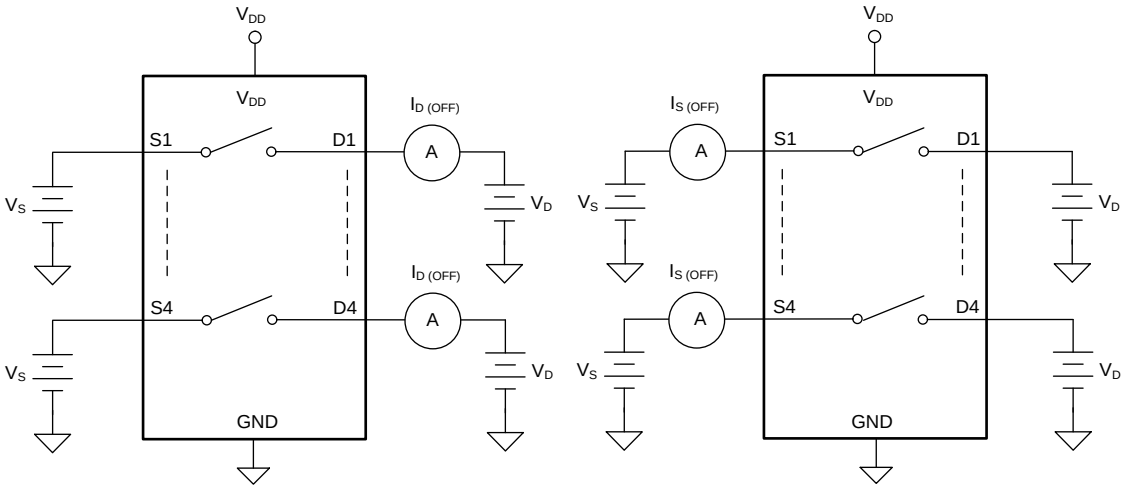

Figure 2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

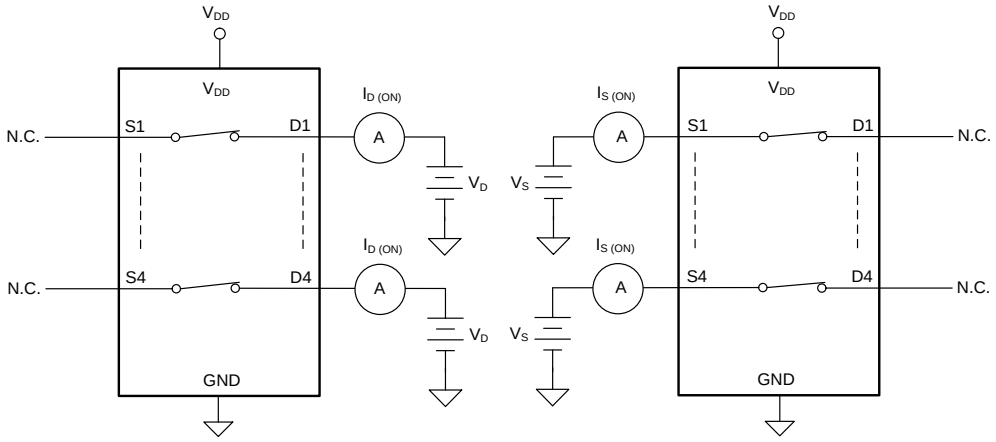

Figure 3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the control select signal has risen or fallen past the digital logic threshold. The 10% transition measurement is utilized to provide the timing of the device. The time constant from the load resistance and load capacitance can be added to the transition time to calculate system level timing. Figure 4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

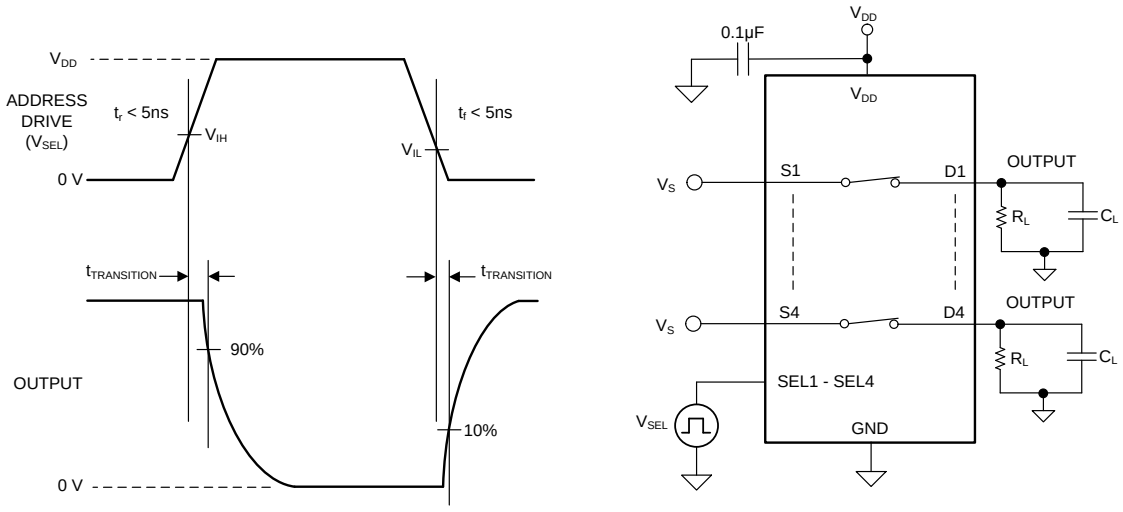

Figure 4. Transition-Time Measurement Setup

7.5 $T_{ON\ (VDD)}$ and $T_{OFF\ (VDD)}$ Time

$T_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is utilized to provide the timing of the device turning on in the system. The time constant from the load resistance and load capacitance can be added to the turn-on-VDD time to calculate system level timing. Figure 5 shows the setup used to measure transition time, denoted by the symbol $t_{ON\ (VDD)}$.

$T_{OFF\ (VDD)}$ time is defined as the time taken by the output of the device to fall to 90% after the enable has fallen past the supply threshold. The 90% measurement is utilized to provide the timing of the device turning off in the system. The time constant from the load resistance and load capacitance can be added to the turn-off-VDD time to calculate system level timing. Figure 5 shows the setup used to measure transition time, denoted by the symbol $t_{OFF\ (VDD)}$.

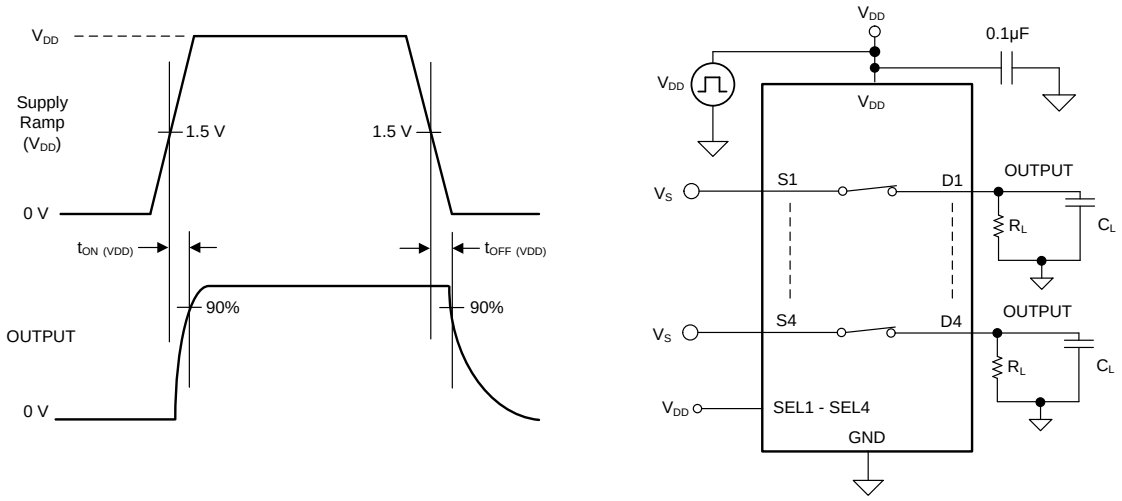

Figure 5. Turn-On-VDD and Turn-Off-VDD Time Measurement Setup

7.6 Charge Injection

The amount of charge injected into the source or drain of the device during the falling or rising edge of the gate signal is known as charge injection, and is denoted by the symbol Q_C. Figure 6 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

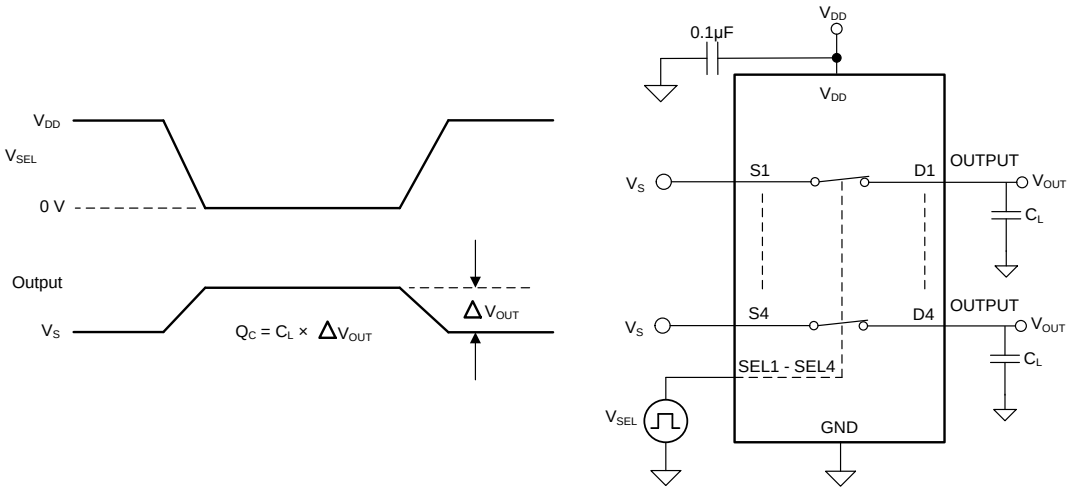

Figure 6. Charge-Injection Measurement Setup

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7.7 Capacitance

The parasitic capacitance of the device is captured at the source (Sx), drain (Dx), and select (SELx) pins. The capacitance is measured in both the on and off state and is denoted by the symbol C_{ON} and C_{OFF}. Figure 7 shows the setup used to measure capacitance.

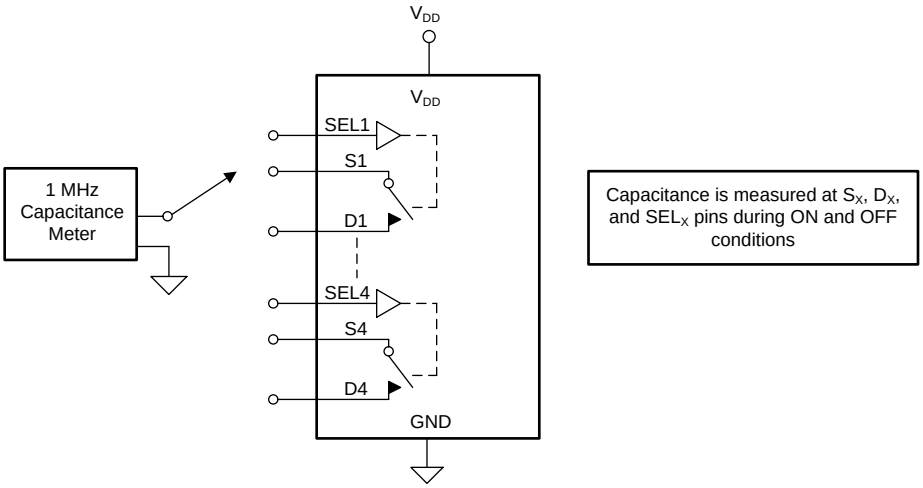

Figure 7. Capacitance Measurement Setup

7.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 8 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

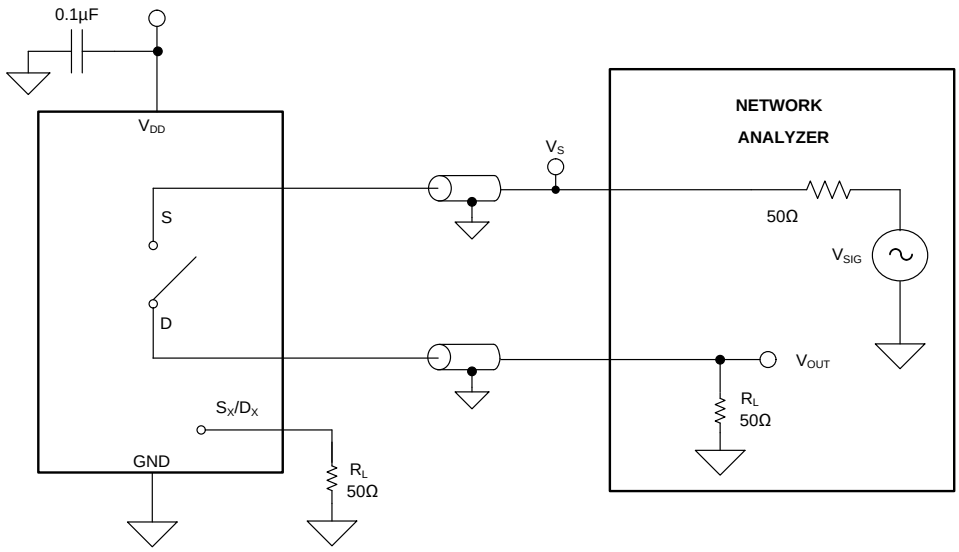

Figure 8. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.9 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 9 shows the setup used to measure, and the equation used to compute crosstalk.

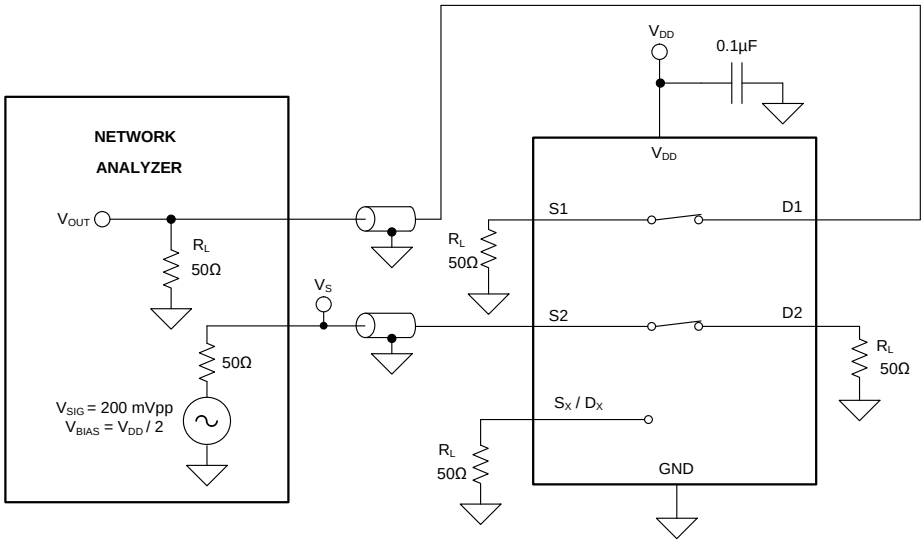

Figure 9. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.10 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. Figure 10 shows the setup used to measure bandwidth.

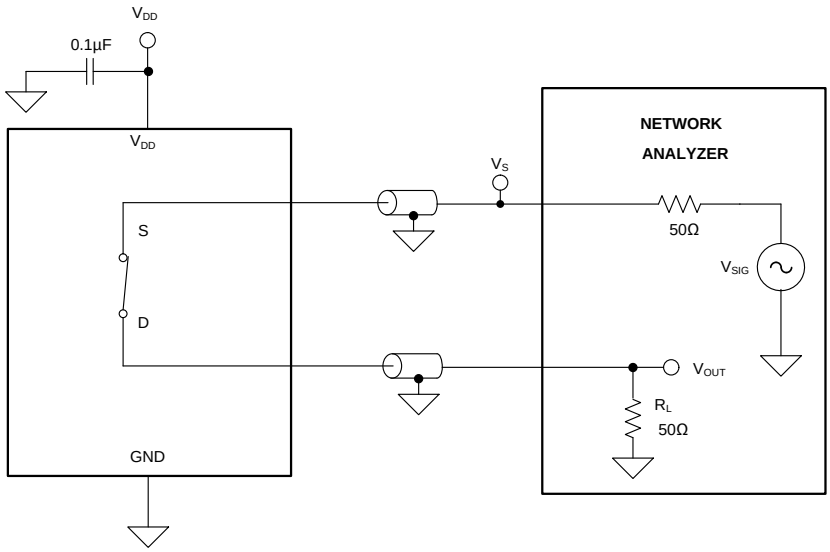

Figure 10. Bandwidth Measurement Setup

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8 Detailed Description

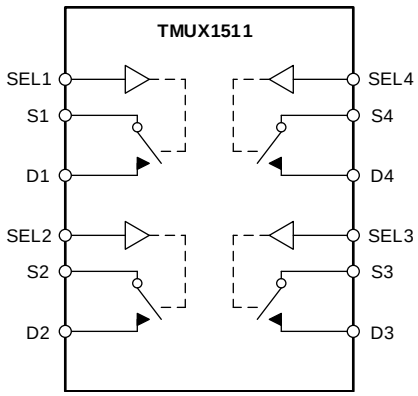
8.1 Overview

The TMUX1511 is a high speed 1:1 (SPST) 4-ch. analog switch with powered-off protection up to 3.6 V. Wide operating supply of 1.5 V to 5.5 V allows for use in a wide array of applications from servers and communication equipment to industrial applications. The device supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins. The wide bandwidth of this switch allows little or no attenuation of the high-speed signals at the outputs to pass with minimum edge and phase distortion as well as propagation delay.

The select (SELx) pins are active-high logic pins that control the connection between the source (Sx) and drain (Dx) pins of the device. Each channel of the TMUX1511 can be controlled independently through the associated select pin, or all four select pins can be tied together for simultaneous control of all channels with a single GPIO. Fail-Safe Logic circuitry allows voltages on the digital control pins to be applied before the supply pin, protecting the device from potential damage. All digital control inputs have 1.8V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range.

Powered-off protection up to 3.6 V on the signal path of the TMUX1511 provides isolation when the supply voltage is removed (V_{DD} = 0 V). Without this protection feature, the system can back-power the supply rail through an internal ESD diode and cause potential damage to the system.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX1511 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Beyond Supply Operation

The valid signal path input/output voltage for TMUX1511 ranges from GND to V_{DD} x 2, with a maximum of 5.5 V.

8.3.3 1.8 V Logic Compatible Inputs

The TMUX1511 has 1.8-V logic compatible control inputs for all switch channels. Regardless of the V_{DD} voltage the control input thresholds remained fixed, allowing a 1.8-V processor GPIO to control the TMUX1511 without the need for an external translator. This saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

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Feature Description (continued)

8.3.4 Powered-off Protection

Powered-off protection up to 3.6 V on the signal path of the TMUX1511 provides isolation when the supply voltage is removed (V_{DD} = 0 V). When the TMUX1511 is powered-off the I/Os of the device remain in a high-Z state. Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on 1.8 V logic implementations refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*

8.3.5 Fail-Safe Logic

The TMUX1511 support Fail-Safe Logic on the control input pins (SELx) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the digital control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1511 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1511 with V_{DD} = 1.5 V while allowing the select pins to interface with a logic level of another device up to 5.5 V.

8.4 Device Functional Modes

The select (SELx) pins are active-high logic pins that control the connection between the source (Sx) and drain (Dx) pins of the device. The TMUX1511 has internal weak pull-down resistors (6 MΩ) to GND so that it powers-on with the switches disabled. When a given select pin of the TMUX1511 is pulled high, the corresponding switch conducts from the source to drain. When any of the select pins are pulled low, the corresponding switch is in an open state (HI-Z). Each channel of the TMUX1511 can be controlled independently through the associated select pin, or all four select pins can be tied together for simultaneous control of all channels with a single GPIO.

8.5 Truth Tables

Table 1 shows the truth table for the TMUX1511.

Table 1. TMUX1511 Truth Table

SELx	Sx / Dx: STATE
0	Hi-Z (OFF)
1	Conducting (ON)

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX15xx family offers high-speed system performance across a wide operating supply (1.5 V to 5.5 V) and operating temperature (-40°C to +125°C). The TMUX1511 supports a number of features that improve system performance such as 1.8 V logic compatibility, supports input voltages beyond supply, Fail-Safe Logic, and Powered-off Protection up to 3.6 V. These features make the TMUX15xx a family of protection multiplexers and switches that can reduce system complexity, board size, and overall system cost.

9.2 Typical Application

One useful application to take advantage of the TMUX1511 features is isolating various protocols from a possessor or MCU such as JTAG, SPI, or standard GPIO signals. The device provides good isolation performance when the device is powered, and unpowered with source (Sx) and drain (Dx) pins below 3.6 V. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications.

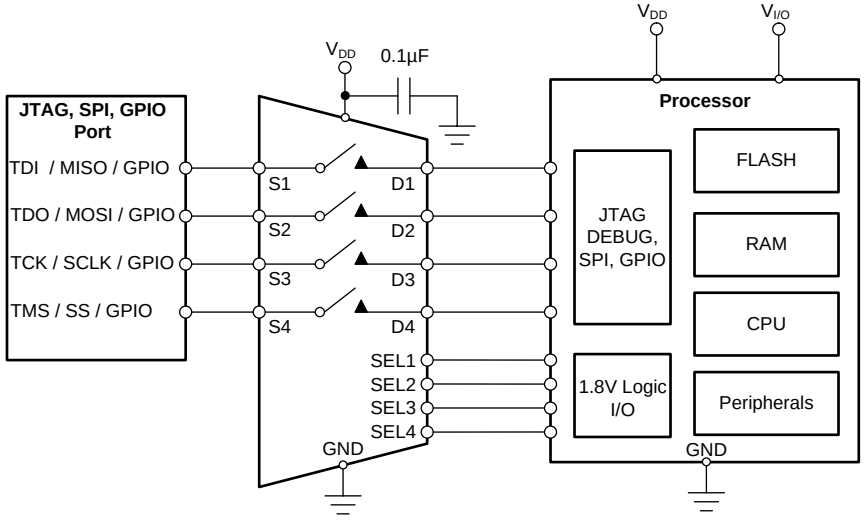


Figure 11. Isolation of JTAG, SPI, and GPIO Signals

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input / Output signal range	0 V to 3.3 V
Control logic thresholds	1.8 V compatible

9.2.2 Detailed Design Procedure

The TMUX1511 can be operated without any external components except for the supply decoupling capacitors. The TMUX1511 has internal weak pull-down resistors (6 MΩ) to GND so that it powers-on with the switches disabled. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX1511 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 5.5 V when the device is powered. This example can also utilize the Powered-off Protectionfeature and the inputs can range from 0 V to 3.6 V when V_{DD} = 0 V. The max continuous current can be 25 mA. Due to the voltage range and high speed capability, the TMUX1511example is suitable for use in JTAG and SPI applications beyond the 100 MHz maximum in a typical application.

10 Power Supply Recommendations

The TMUX1511 operates across a wide supply range of 1.5 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.Figure 12 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

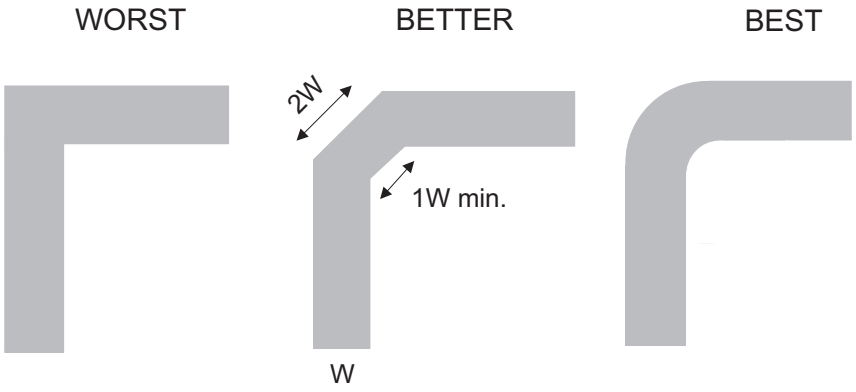


Figure 12. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed signals traces because they cause signal reflections.

Route all high-speed signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 13.

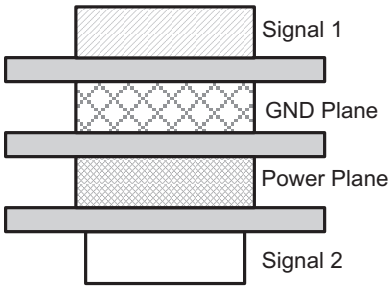


Figure 13. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

Figure 14 illustrates an example of a PCB layout with the TMUX1511. Some key considerations are:

Layout Guidelines (continued)

Decouple the V_{DD} pin with a 0.1-μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

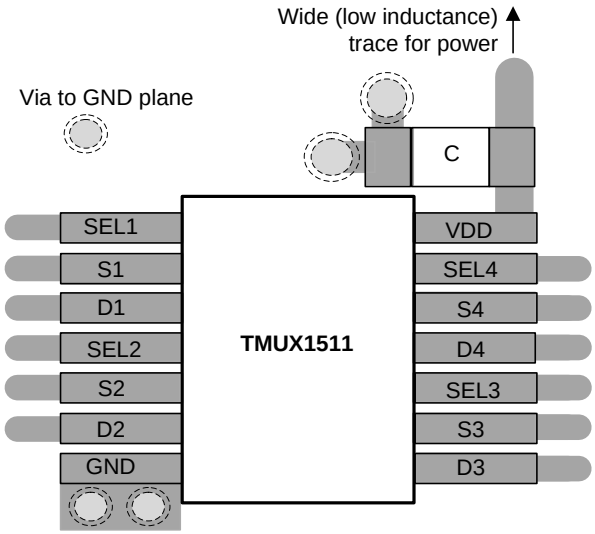


Figure 14. Example Layout

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *High-Speed Interface Layout Guidelines*.

Texas Instruments, *High-Speed Layout Guidelines*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX1511PWR	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX1511PWR	PREVIEW	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX1511	
TMUX1511RSVR	PREVIEW	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1511	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

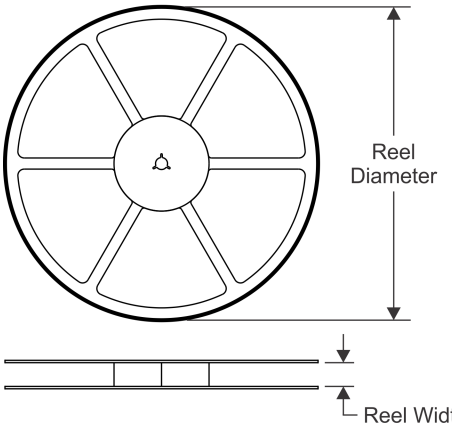
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

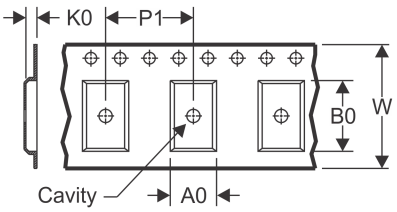
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

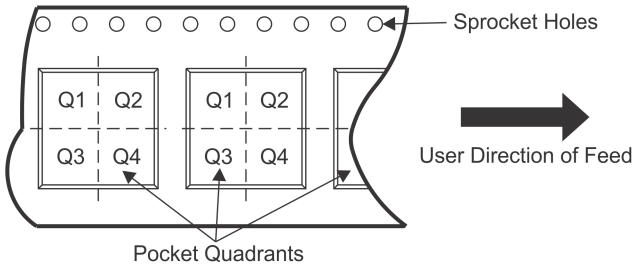


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

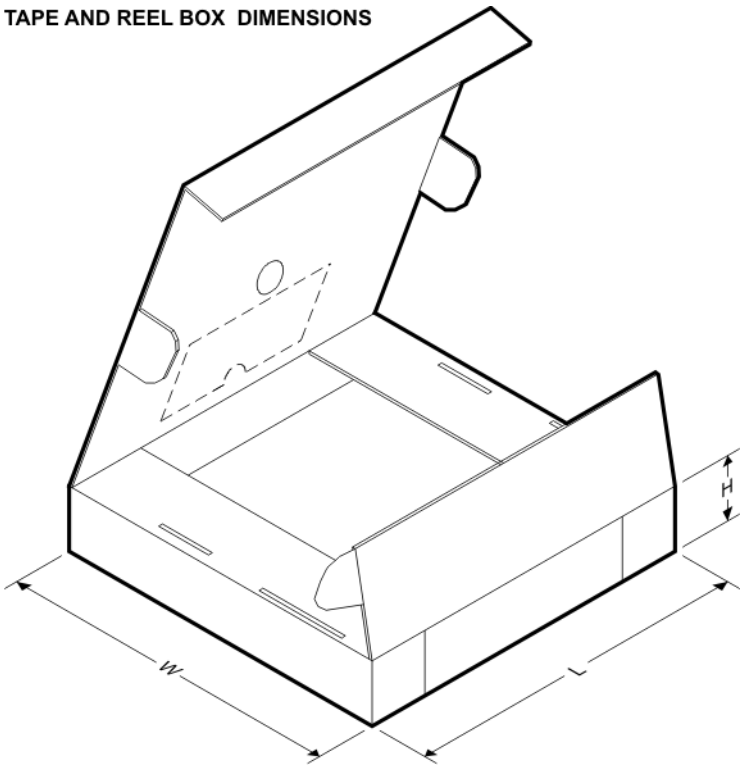
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1511PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX1511RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

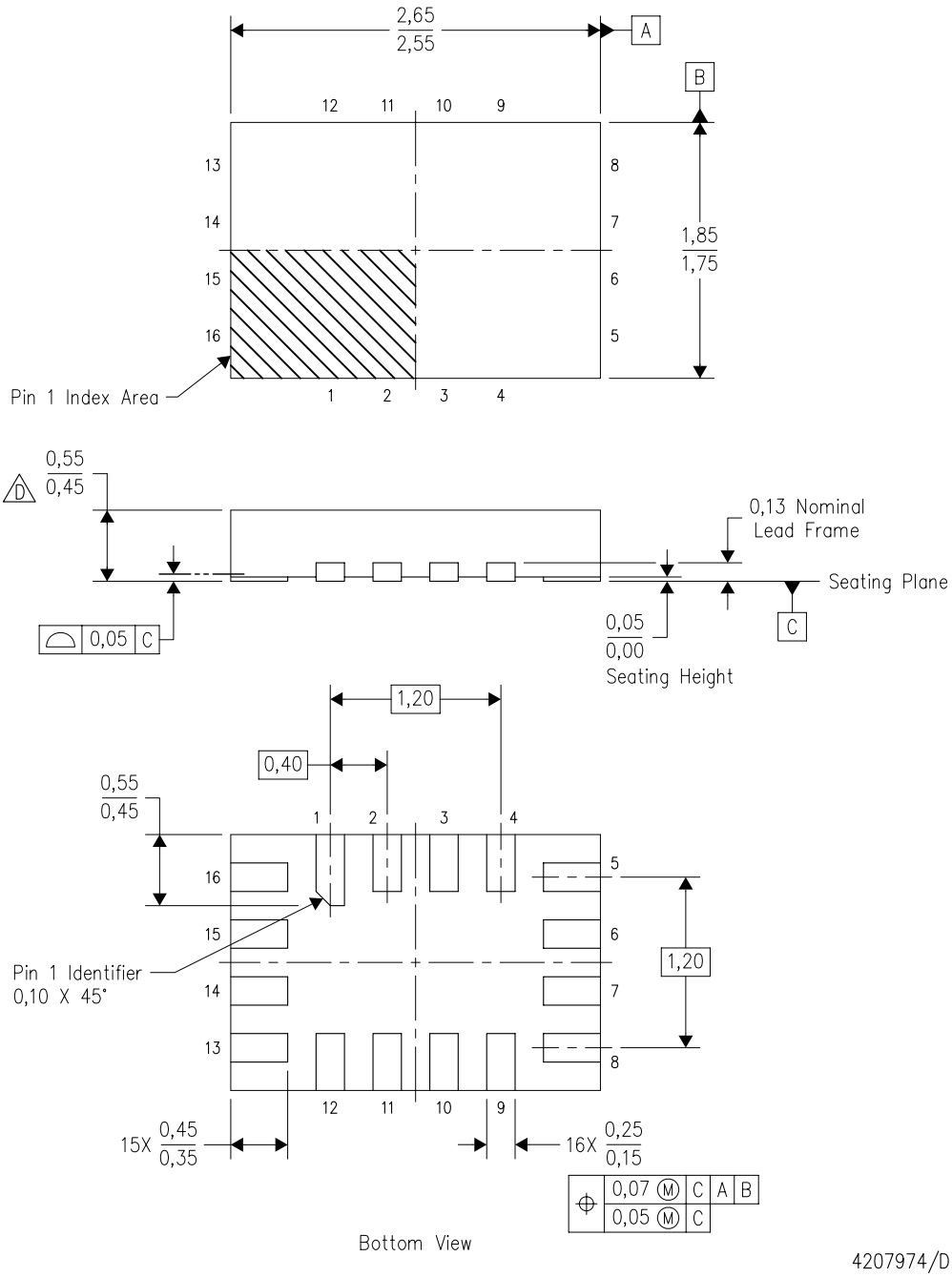
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

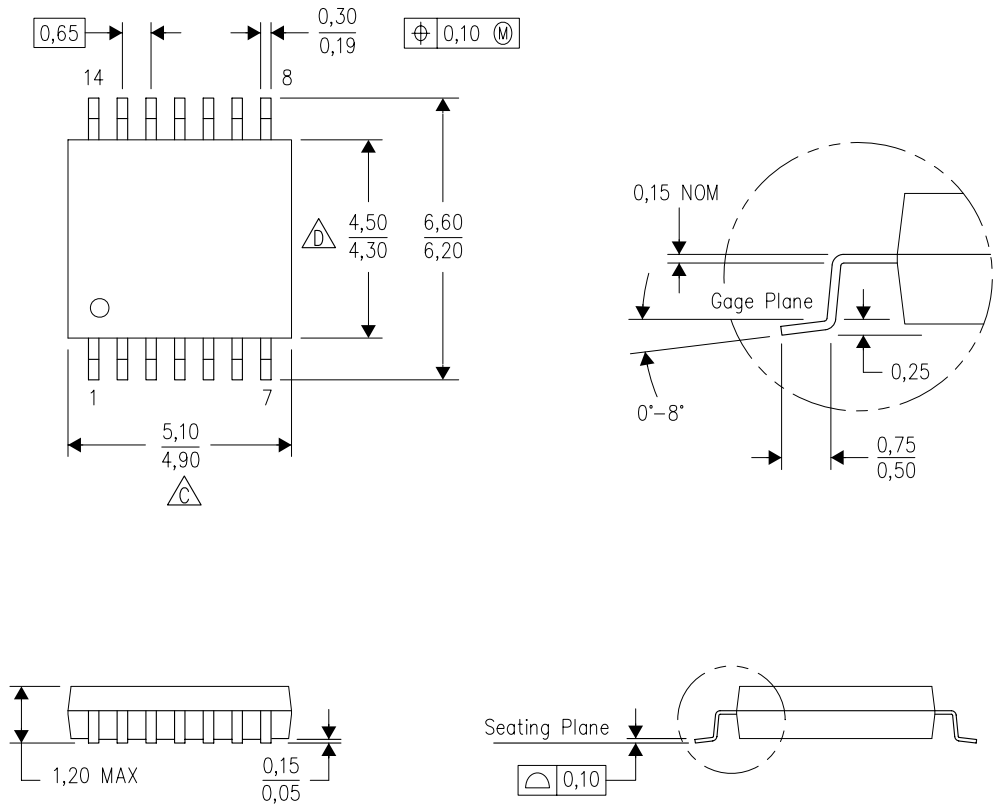
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1511PWR	TSSOP	PW	14	2000	367.0	367.0	35.0
TMUX1511RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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