Capacitor-Free, Dual, 150-mA, Low-Dropout Voltage Regulator (LDO) in 1,2-mm × 1,2-mm SON Package

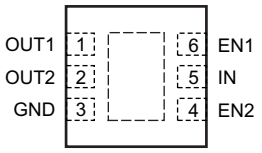
FEATURES

- **No Input or Output Capacitors Required**
- **Inrush Current Control**
- **Low Crosstalk**
- **Accuracy: 1%**
- **Input Voltage Range: 1.4 V to 5.5 V**
- **Multiple Fixed-Output Voltage Combinations Possible from 1.0 V to 3.3 V**
- **Foldback Current-Limit Protection**
- **Package: 1,2-mm × 1,2-mm SON-6 (DPQ)**

APPLICATIONS

- **Wireless Handsets, Smart Phones, Tablets**
- **Set-Top Boxes (STBs), Cameras, Modems**
- **Portable Battery-Powered Products**

DPQ PACKAGE
1,2-mm x 1,2-mm SON
(TOP VIEW)



DESCRIPTION

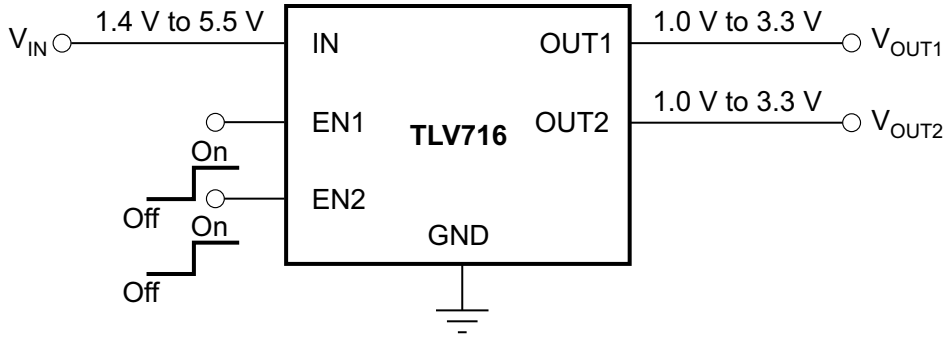
The TLV716 is a family of dual-channel, capacitor-free,150-mA, low-dropout (LDO) voltage regulators with multiple fixed-output options available from 1.0 V to 3.3 V. These devices provide an initial 1% accuracy and 1.5% accuracy over temperature.

The TLV716 family is designed to be stable with or without an input or output capacitor. Eliminating the output capacitor allows for a very small solution size. The TLV716P series provides an active pull-down circuit to quickly discharge the output voltage if the application requires an output capacitor.

The device provides inrush current control during device power-up and enabling. Inrush control provides constant-current charging of the output load during startup, thereby reducing the risk of an undesired overcurrent fault from the input supply or battery.

The TLV716 family is available in a 1,2-mm × 1,2-mm SON-6 package and is ideal for space-constrained applications.

Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TLV716**XX(X)YY(Y) PWWWZ**	**XX(X)** is the nominal output voltage of channel 1. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V and 185 = 1.85 V). **YY(Y)** is the nominal output voltage of channel 2. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 18 = 1.8 V and 185 = 1.85 V). **P** is optional. Use *P* for devices with an active output discharge. **WWW** is the package designator. **Z** is the package quantity. Use *R* for reel (3000 pieces), and *T* for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact the factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+6.0	V
	EN1, EN2	–0.3	V_{IN} + 0.3	V
	OUT1, OUT2	–0.3	+3.6 or V_{IN} + 0.3 (whichever is smaller)	V
Current	OUT1, OUT2	-30	Internally limited	mA
Output short-circuit duration		Indefinite		s
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground.

THERMAL INFORMATION(1)

THERMAL METRIC(2)(1)		TLV716, TLV716P DPQ (SON) 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	149.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	93.0	
θ_{JB}	Junction-to-board thermal resistance	110.1	
ψ_{JT}	Junction-to-top characterization parameter	3.4	
ψ_{JB}	Junction-to-board characterization parameter	114.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	91.0	

(1) See the *Power Dissipation* section for more details.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

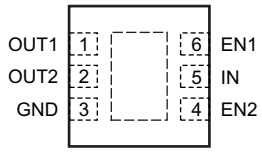
Over operating temperature range of T_A = –40°C to +85°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN1} = V_{EN2} = 0.9 V, and C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, unless otherwise noted. Typical values are at T_J = +25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		1.4		5.5	V
V_{OUT}	Output voltage accuracy	T_J = +25°C, V_{OUT} > 1.2 V	–1%	0.33%	1%	
		T_J = +25°C, V_{OUT} ≤ 1.2 V	–20		20	mV
		T_J = –40°C to +85°C, V_{OUT} > 1.2 V	–1.5%		1.5%	
		T_J = –40°C to +85°C, V_{OUT} ≤ 1.2 V	–50		50	mV
I_{OUT}	Output current	Each channel	150			mA
ΔV_{OUT} / ΔV_{IN}	Line regulation	V_{OUT} + 0.5 V < V_{IN} ≤ 5.5 V		0.02	0.2	%/V
ΔV_{OUT} / ΔI_{OUT}	Load regulation	1 mA < I_{OUT} < 150 mA		0.07	0.2	mV/mA
ΔV_{OUT} / ΔI_{OUT}	Cross load regulation	1 mA < I_{OUT} < 150 mA		0.005	0.066	mV/mA
V_{DO}	Dropout voltage	I_{OUT} = 150 mA, 1.0 V ≤ V_{OUT} < 1.2 V		0.78	1	V
		I_{OUT} = 150 mA, 1.2 V ≤ V_{OUT} < 1.8 V		0.6	0.9	V
		I_{OUT} = 150 mA, 1.8 V ≤ V_{OUT} < 2.1 V		0.35	0.575	V
		I_{OUT} = 150 mA, 2.1 V ≤ V_{OUT} < 2.5 V		0.29	0.48	V
		I_{OUT} = 150 mA, 2.5 V ≤ V_{OUT} < 3.0 V		0.23	0.45	V
		I_{OUT} = 150 mA, 3.0 V ≤ V_{OUT} < 3.3 V		0.21	0.42	V
V_{HI}	Enable high voltage		0.9		V_{IN}	V
V_{LO}	Enable low voltage		0		0.4	V
R_{PD}	Output pull-down resistance	TLV716P only		120		Ω
I_{CL}	Output current limit	V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.1 V (whichever is greater)	160		500	mA
I_{SC}	Output short current limit	V_{OUT} = 0 V		40		mA
I_{GND}	Ground pin current	Per channel, I_{OUT} = 0 mA, V_{IN} = 5.5 V		50	75	µA
$I_{SHUTDOWN}$	Shutdown current	Per channel, V_{IN} = 5.5 V, T_J = +25°C		0.1	1	µA
PSRR	Power-supply rejection ratio	f = 100 Hz, V_{OUT} = 2.8 V, I_{OUT} = 30 mA		80		dB
		f = 10 kHz, V_{OUT} = 2.8 V, I_{OUT} = 30 mA		46		dB
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.8 V, V_{IN} = 2.3 V, I_{OUT} = 10 mA		70		μV_{RMS}
t_{STR}	Startup time(1)	V_{OUT} = 1.0 V, I_{OUT} = 150 mA		170		µs
		V_{OUT} = 3.3 V, I_{OUT} = 150 mA		900		µs
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+158		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating Junction Temperature		–40		+125	°C

(1) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

PIN CONFIGURATION

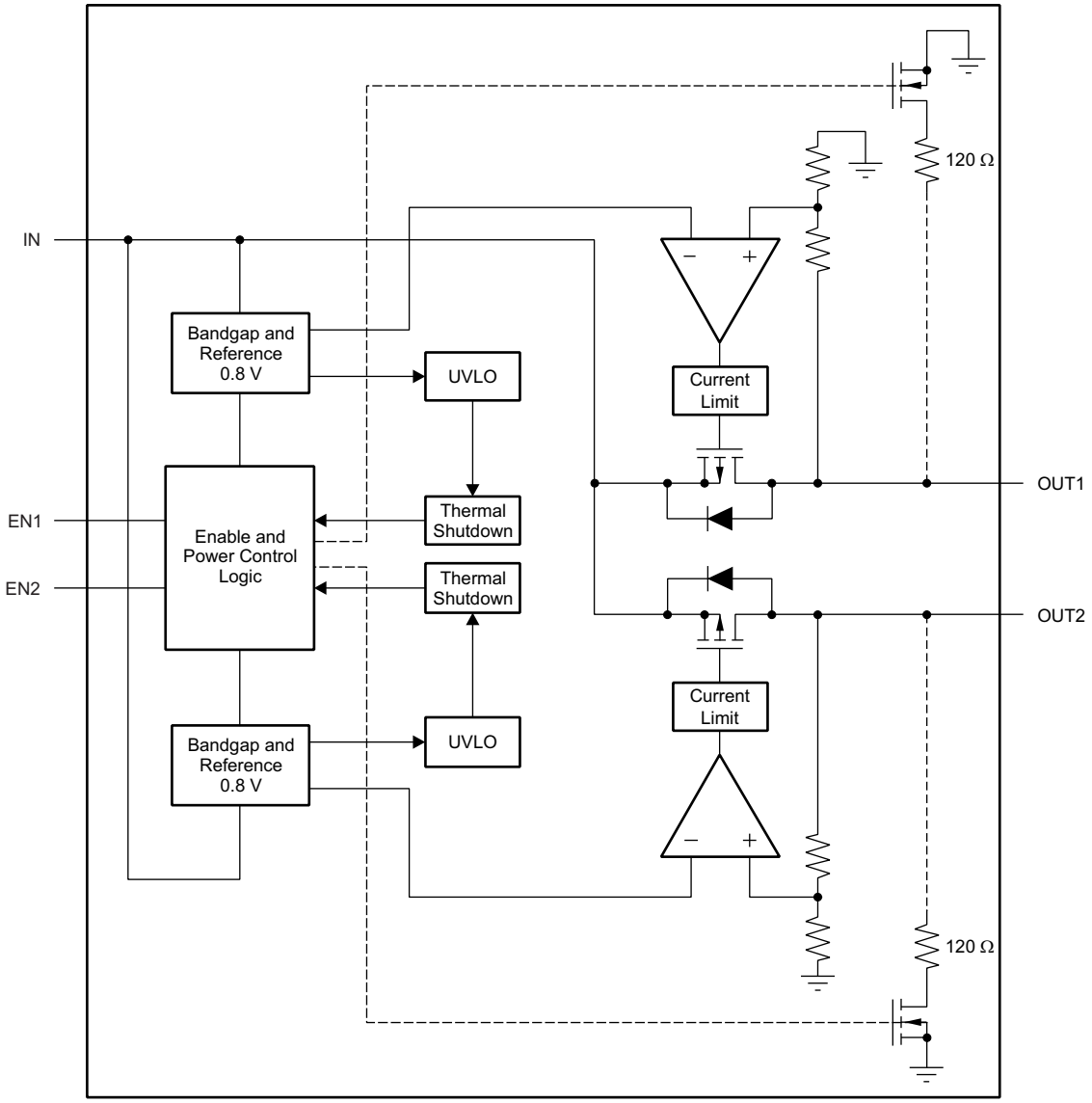
DPQ PACKAGE
1,2-mm × 1,2-mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
OUT1	1	Regulated output voltage pin. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
OUT2	2	Regulated output voltage pin. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
GND	3	Ground pin.
EN2	4	Enable pin for regulator 2. Driving EN2 over 0.9 V turns on regulator 2. Driving EN2 below 0.4 V places regulator 2 into shutdown mode.
IN	5	Input pin. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
EN1	6	Enable pin for regulator 1. Driving EN1 over 0.9 V turns on regulator 1. Driving EN1 below 0.4 V places regulator 1 into shutdown mode.
—	PAD	Connecting the thermal pad to the ground plane improves the thermal performance.

FUNCTIONAL BLOCK DIAGRAM



NOTE: Dashed lines are for the TLV716P only.

TYPICAL CHARACTERISTICS

Over operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater), V_{EN1} = V_{EN2} = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at T_J = +25°C.

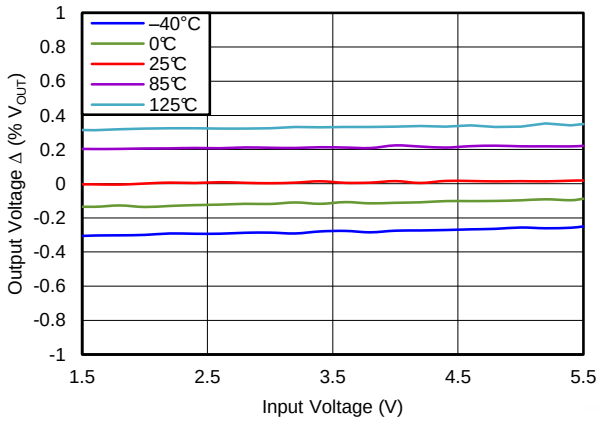


Figure 1. LINE REGULATION %V_{OUT} DEVIATION vs V_{IN} (V_{OUT} = 1.0 V)

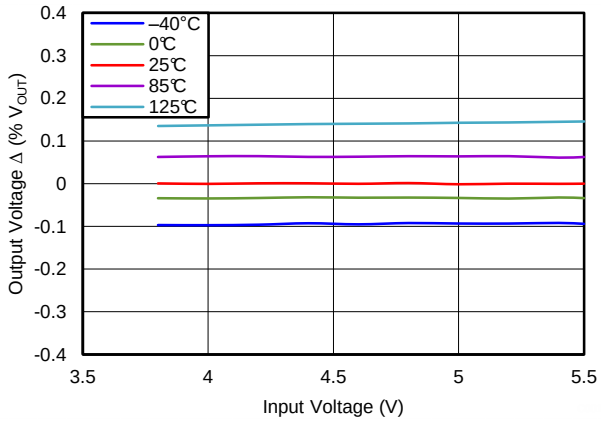


Figure 2. LINE REGULATION %V_{OUT} DEVIATION vs V_{IN} (V_{OUT} = 3.3 V)

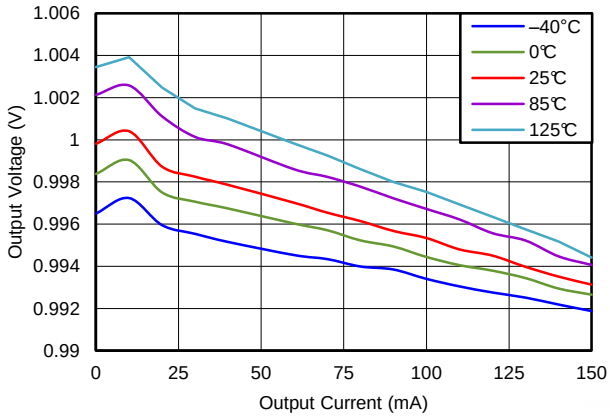


Figure 3. LOAD REGULATION V_{OUT} vs I_{OUT} (V_{OUT} = 1.0 V)

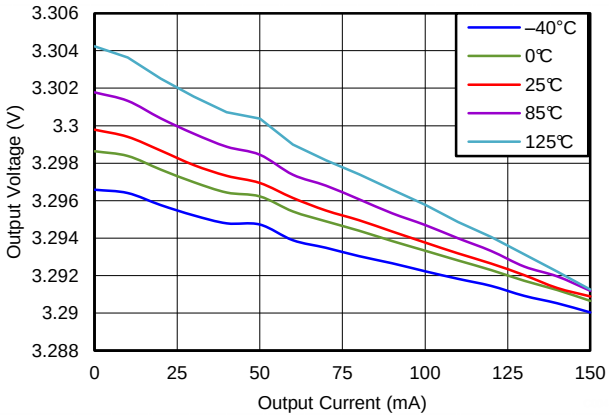


Figure 4. LOAD REGULATION V_{OUT} vs I_{OUT} (V_{OUT} = 3.3 V)

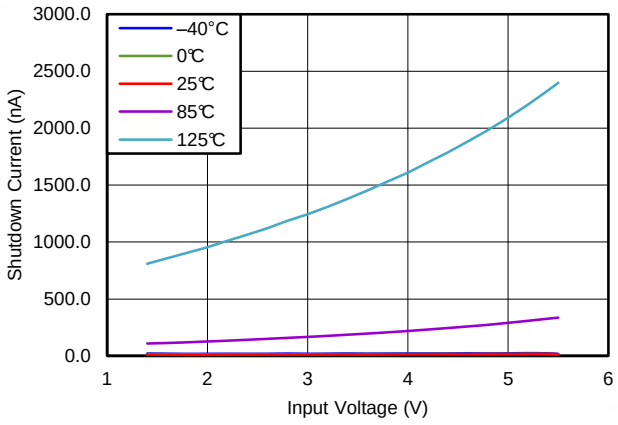


Figure 5. SHUTDOWN CURRENT vs V_{IN}

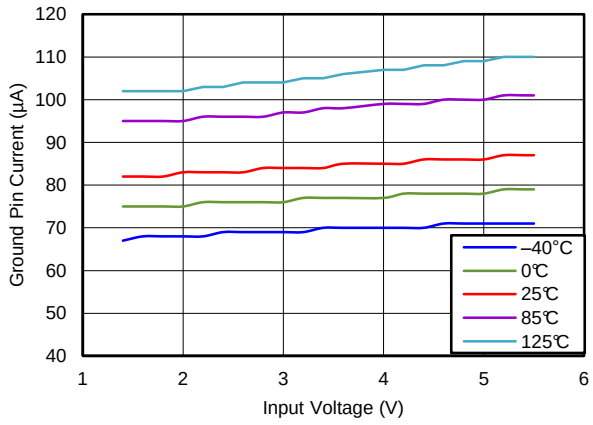


Figure 6. GROUND PIN CURRENT vs V_{IN}

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater), V_{EN1} = V_{EN2} = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at T_J = +25°C.

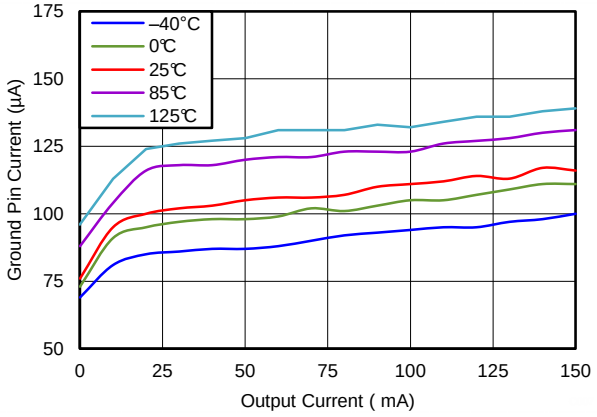


Figure 7. GROUND PIN CURRENT vs I_{OUT}

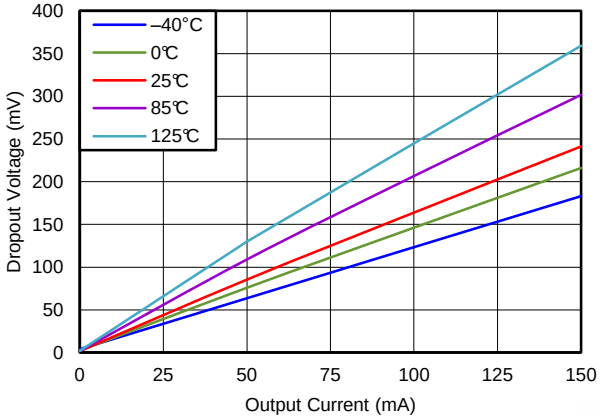


Figure 8. DROPOUT VOLTAGE vs I_{OUT} (V_{OUT} = 3.3 V)

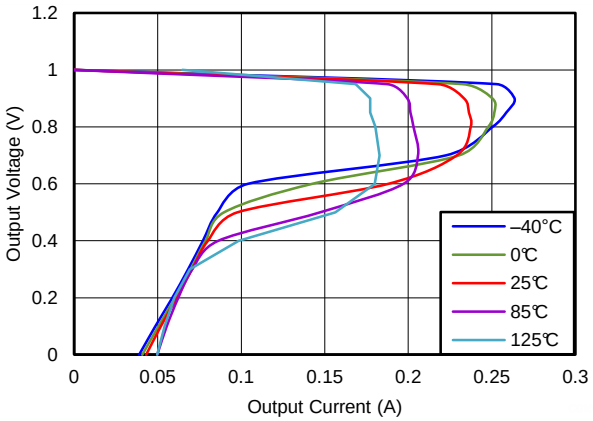


Figure 9. OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{OUT} = 1.0 V) (Foldback Current Limit)

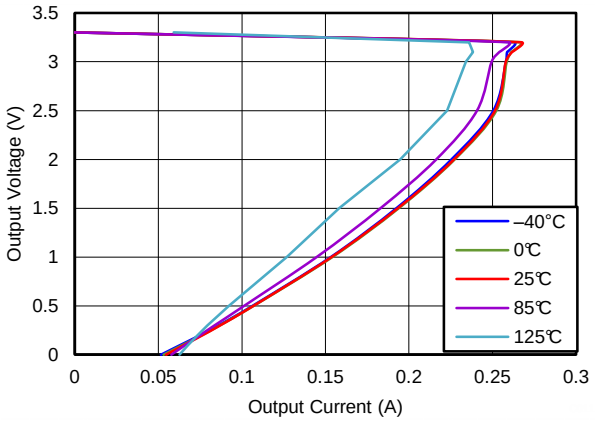


Figure 10. OUTPUT VOLTAGE vs OUTPUT CURRENT (V_{OUT} = 3.3 V) (Foldback Current Limit)

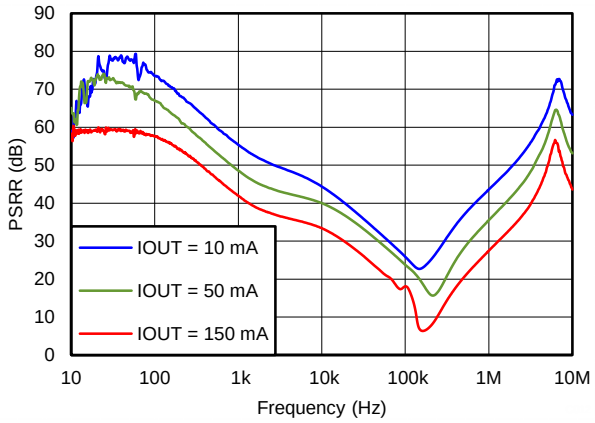


Figure 11. POWER-SUPPLY REJECTION RATIO vs FREQUENCY (V_{OUT} = 3.3 V)

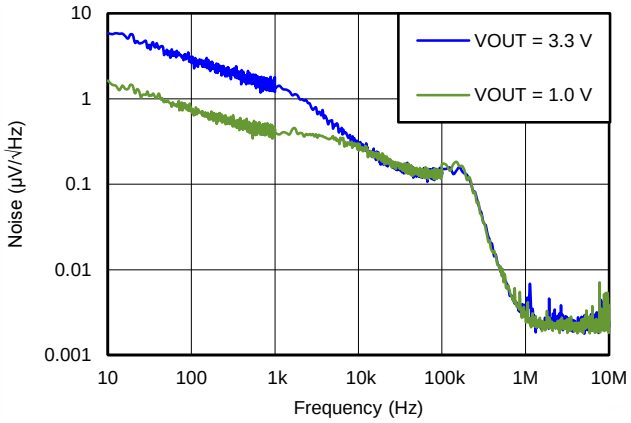


Figure 12. OUTPUT SPECTRAL NOISE DENSITY

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater), V_{EN1} = V_{EN2} = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at T_J = +25°C.

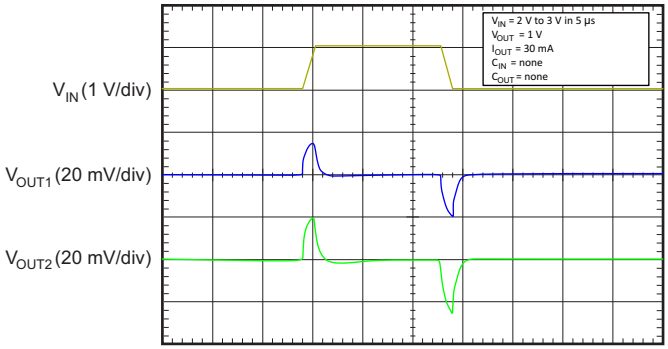


Figure 13. LINE TRANSIENT

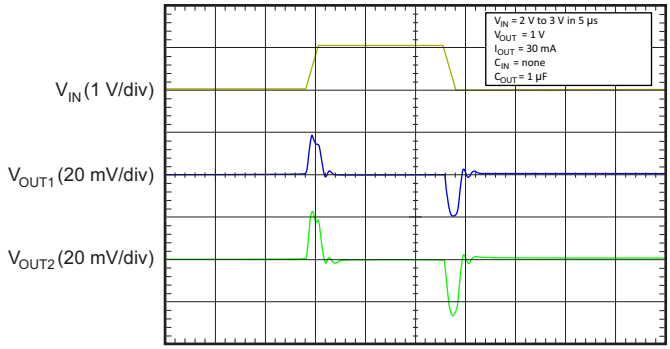


Figure 14. LINE TRANSIENT

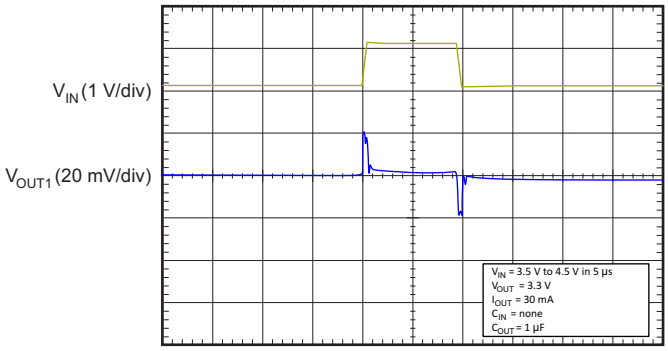


Figure 15. LINE TRANSIENT

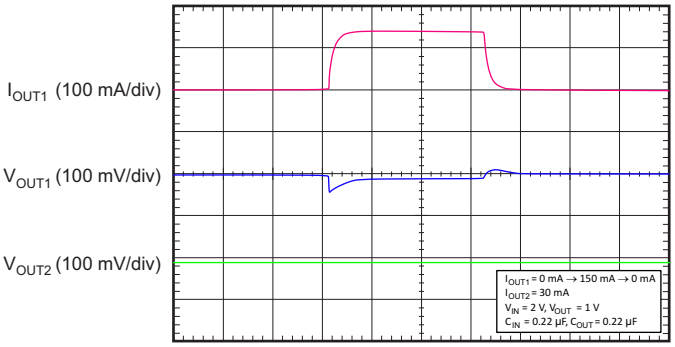


Figure 16. LOAD TRANSIENT

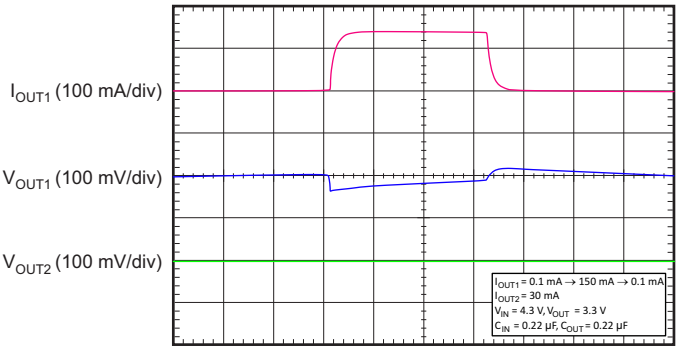


Figure 17. LOAD TRANSIENT

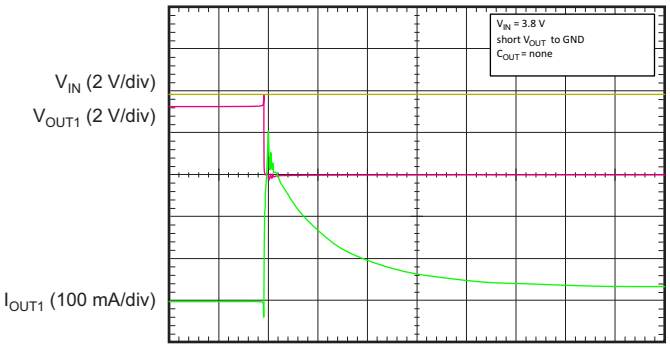


Figure 18. FOLDBACK CURRENT LIMIT

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2.0 V (whichever is greater), V_{EN1} = V_{EN2} = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = 1 µF, C_{OUT1} = 1 µF, and C_{OUT2} = 1 µF, unless otherwise noted. Output current plots show typical performance with a single output current sweep. Typical values are at T_J = +25°C.

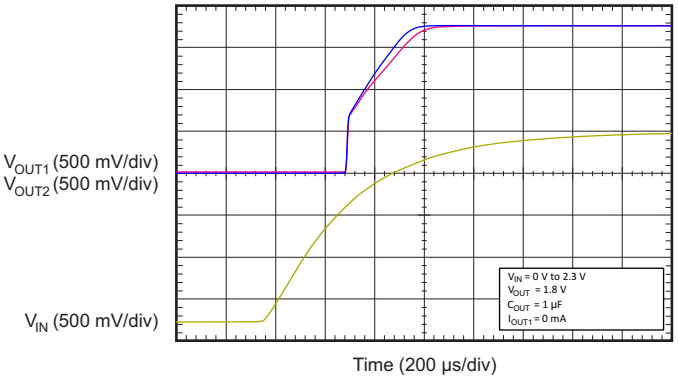


Figure 19. STARTUP

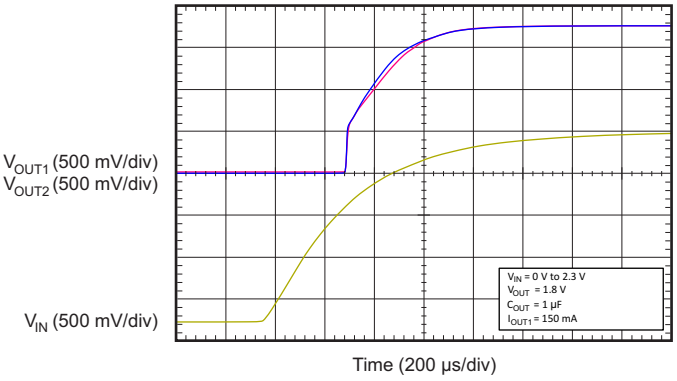


Figure 20. STARTUP

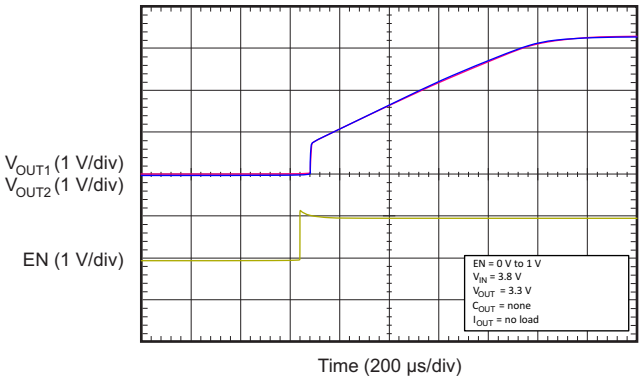


Figure 21. STARTUP WITH EN

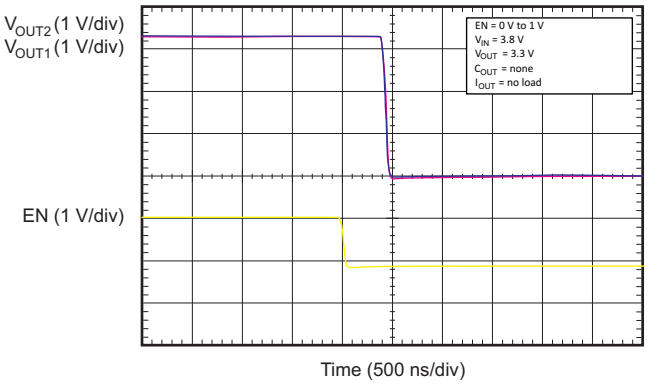


Figure 22. SHUTDOWN WITH EN

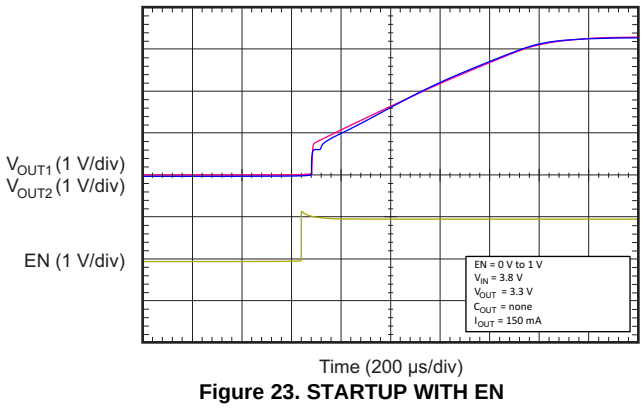
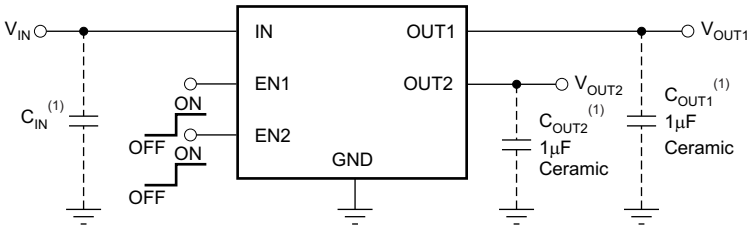


Figure 23. STARTUP WITH EN

APPLICATION INFORMATION

The TLV716 and TLV716P belong to a family of dual-channel, capacitor-free, 150-mA, low-dropout voltage (LDO) regulators. These devices can be used with or without external capacitors and are available in a 1,2-mm × 1,2-mm package, making these devices a very small solution size for dual-channel, low-dropout (LDO) regulators. This family of LDO regulators offers current-limit and thermal protection, and is specified from –40°C to +85°C. Figure 24 shows an application circuit for this family of devices.



(1) Optional.

Figure 24. Typical Application Circuit

CAPACITOR-FREE OPERATION

The TLV716 is stable without the use of input or output capacitors. This functionality results in a reduction of component count, cost, and solution size. In addition, without the need of external capacitors, the TLV716 ultra-small, 1,2-mm × 1,2-mm DPQ package optimizes the solution size for board space-constrained applications. To optimize device ac performance, an input and output capacitor is recommended, as described in the *Input and Output Capacitor Requirements* section.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

The TLV716 uses an advanced internal control loop to obtain stable operation both with or without the use of input or output capacitors as high as 100-µF. The dynamic performance of the device is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts input source impedance and improves supply transient response, input ripple, and PSRR. A higher value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

If used, place the input and output capacitors as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that for V_{IN} and V_{OUT}, the ground planes are connected only at the GND pin of the device. In addition, connect the ground connection for the output capacitor directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TLV716 has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device gradually reduces while the output voltage decreases. When the output is connected to ground, the LDO supplies a typical current of 40 mA. When in current limit, the output voltage is not regulated and $V_{OUT} = I_{OUT} \times R_{LOAD}$; see Figure 10 and Figure 11. The PMOS pass transistor dissipates $[(V_{IN} – V_{OUT}) \times I_{LIMIT}]$ until thermal shutdown is triggered and the device turns off. When the device cools down, the internal thermal shutdown circuit turns on the device. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV716 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended. A small schottky diode connected with the anode to OUT and the cathode to IN can accomplish this limiting.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the EN pin goes above 0.9 V. This relatively low value of voltage required to turn the LDO regulator on can be used to enable the device with the general-purpose input/output (GPIO) of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, the EN pin can connected to the IN pin. The TLV716P will pull down the output with a 120Ω resistor when the EN pin falls below 0.4 V.

DROPOUT VOLTAGE

The TLV716 and TLV716P use a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} – V_{OUT})$ approaches dropout.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV716 and TLV716P use an undervoltage lockout circuit (1.3 V, typical) to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +158°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. The ambient temperature at which thermal shutdown occurs on the device is 33°C higher (158°C - 125°C) than the maximum recommended operating conditions.

The internal protection circuitry of the TLV716 and TLV716P is designed to protect against overload conditions. This circuitry is not intended to replace proper PCB layout and heatsinking. Continuously running the device into thermal shutdown degrades reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The copper PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in the Thermal Information table. Using heavier copper increases effectiveness in removing heat from the device.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across both output pass elements, as shown in Equation 1:

$$P_D = (V_{IN} – V_{OUT1}) \times I_{OUT1} + (V_{IN} – V_{OUT2}) \times I_{OUT2} \quad (1)$$

The maximum ambient temperature that the device can operate within the maximum T_J operating temperature of +125°C depends on the thermal impedance and the total power dissipated within the device. Figure 25 and Figure 26 show maximum ambient temperature verses output current for two different LDO configurations. Figure 25 shows the maximum ambient temperature with V_{IN} = 3.3 V, V_{OUT1} = 1.8 V, and V_{OUT2} = 1.0 V versus I_{OUT1}. Figure 26 shows the maximum ambient temperature with V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, and V_{OUT2} = 1.8 V versus I_{OUT1}.

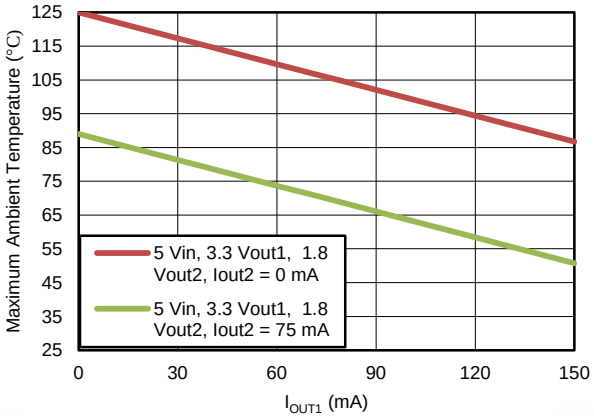


Figure 25. Maximum Ambient Temperature vs Output Current (V_{IN} = 5.0 V, V_{OUT1} = 3.3 V, V_{OUT2} = 1.8 V)

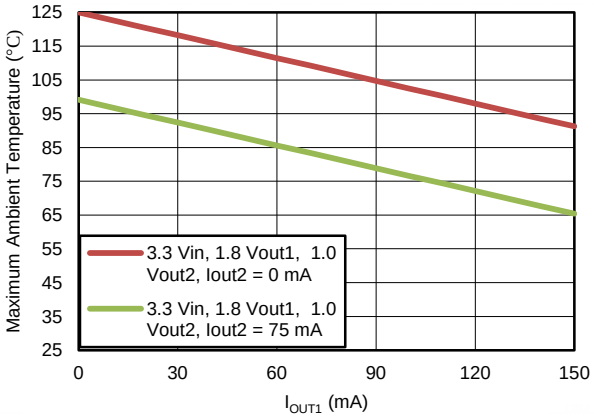


Figure 26. Maximum Ambient Temperature vs Output Current (V_{IN} = 3.3 V, V_{OUT1} = 1.8 V, V_{OUT2} = 1.0 V)

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2013) to Revision A	Page
• Changed document status from Product Preview to Production Data; pre-RTM changes made throughout	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV716120275PDPQR	ACTIVE	X2SON	DPQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI	Samples
TLV716120275PDPQT	ACTIVE	X2SON	DPQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	EI	Samples
TLV7162818PDPQR	ACTIVE	X2SON	DPQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW	Samples
TLV7162818PDPQT	ACTIVE	X2SON	DPQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CW	Samples
TLV7162828PDPQR	ACTIVE	X2SON	DPQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX	Samples
TLV7162828PDPQT	ACTIVE	X2SON	DPQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CX	Samples
TLV7163030PDPQR	ACTIVE	X2SON	DPQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY	Samples
TLV7163030PDPQT	ACTIVE	X2SON	DPQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CY	Samples
TLV7163318PDPQR	ACTIVE	X2SON	DPQ	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ	Samples
TLV7163318PDPQT	ACTIVE	X2SON	DPQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

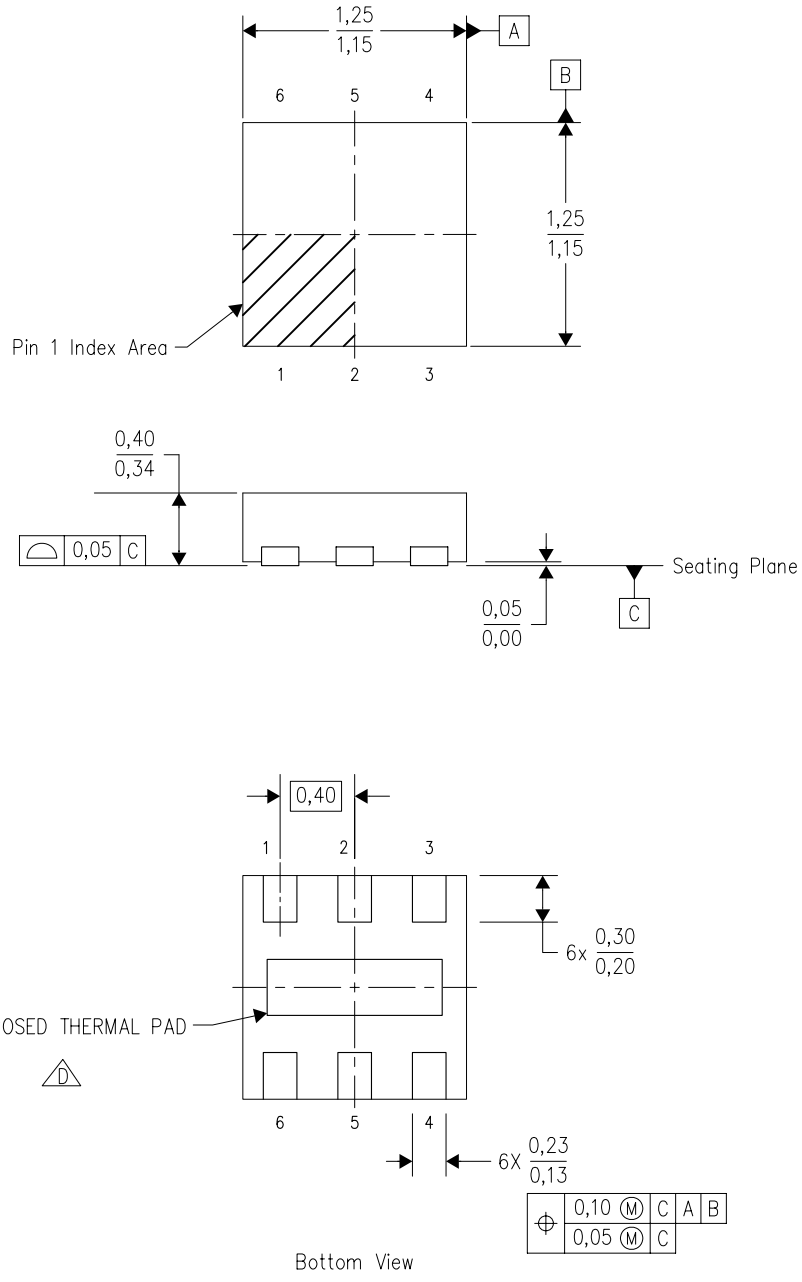
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

DPQ (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4211511/A 12/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

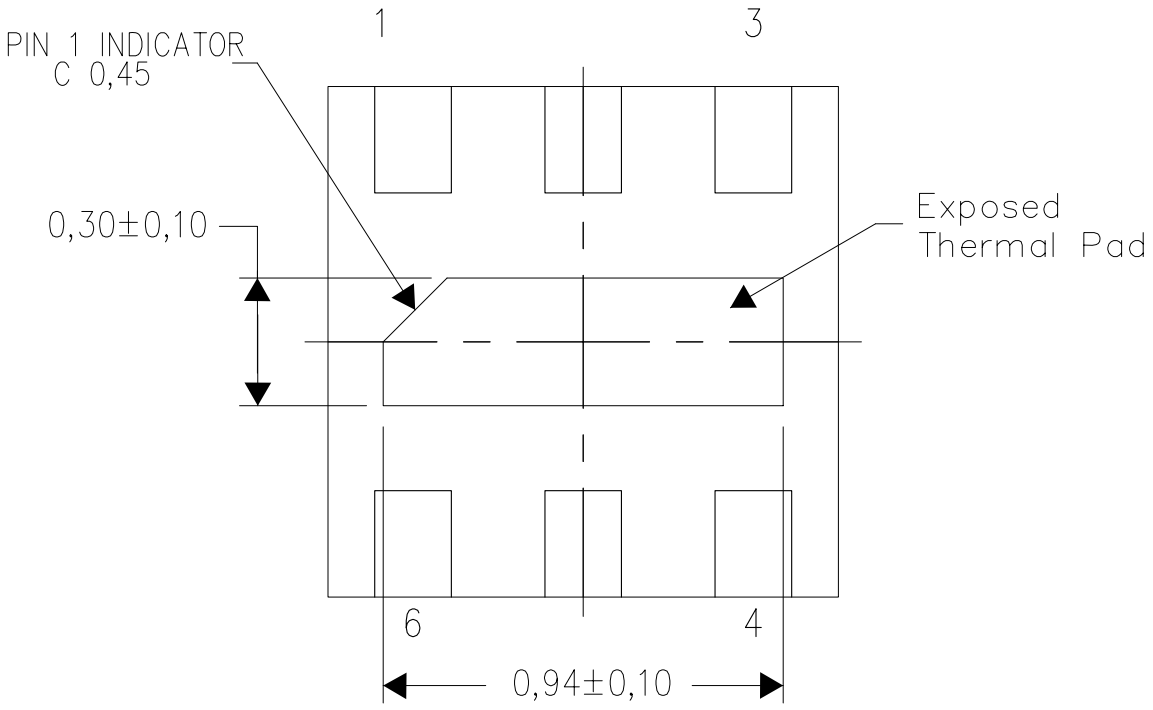
DPQ (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



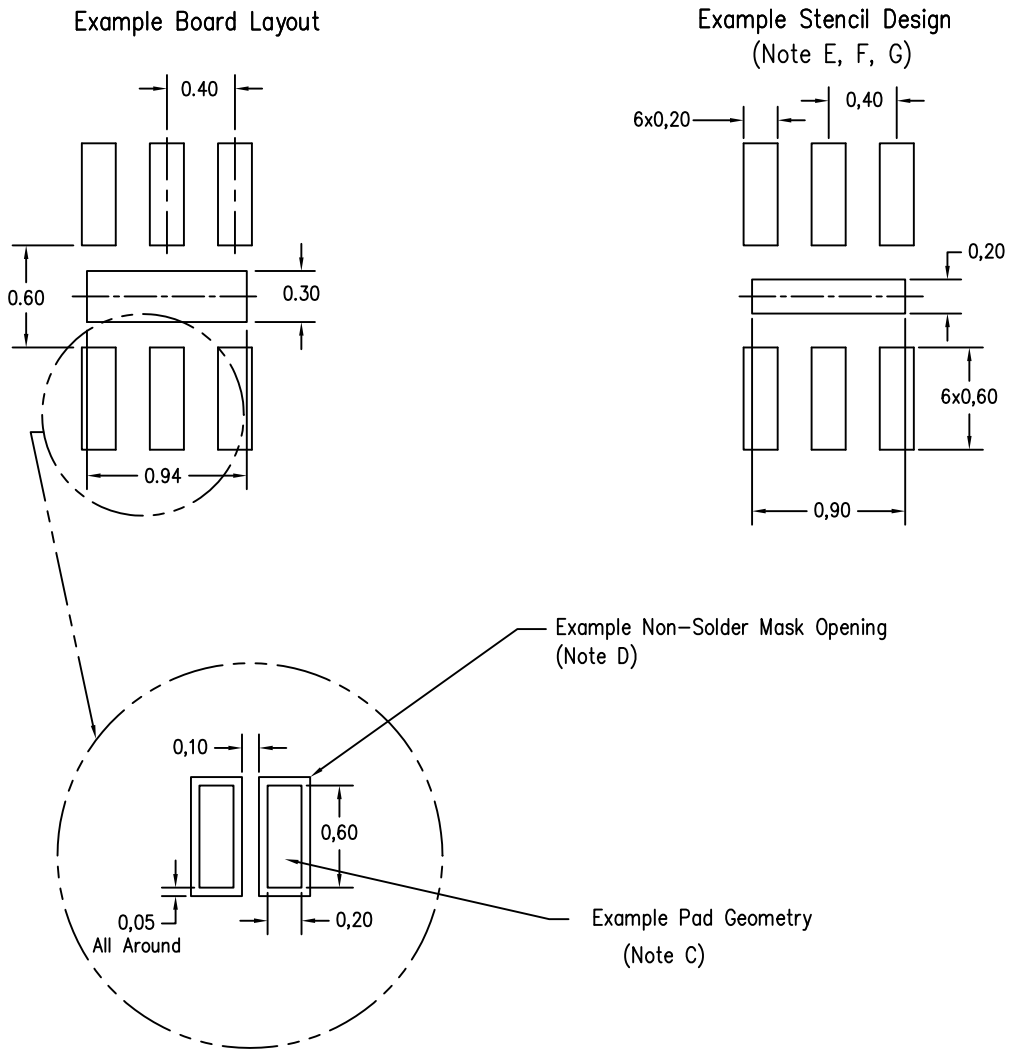
Bottom View

Exposed Thermal Pad Dimensions

4211579/B 02/12

NOTES: All linear dimensions are in millimeters

DPQ (S–PX2SON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265