Capacitor-Free, 150-mA, Low-Dropout Regulator with Foldback Current Limit for Portable Devices

Check for Samples: TLV713, TLV713P

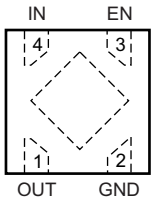
FEATURES

- **Stable Operation With or Without Capacitors**
- **Foldback Overcurrent Protection**
- **Package: SOT23-5 and X2SON**
- **Very Low Dropout: 230 mV at 150 mA**
- **Accuracy: 1%**
- **Low I_Q: 50 µA**
- **Input Voltage Range: 1.4 V to 5.5 V**
- **Available in Fixed-Output Voltages: 1.0 V to 3.3 V**
- **High PSRR: 65 dB at 1 kHz**

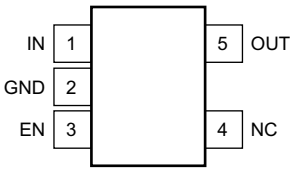
APPLICATIONS

- **PDAs and Battery-Powered Portable Devices**
- **MP3 Players and Other Hand-Held Products**
- **WLAN and Other PC Add-On Cards**

DQN Package
1-mm x 1-mm X2SON
(Top View)



DBV PACKAGE
SOT23-5
(Top View)



DESCRIPTION

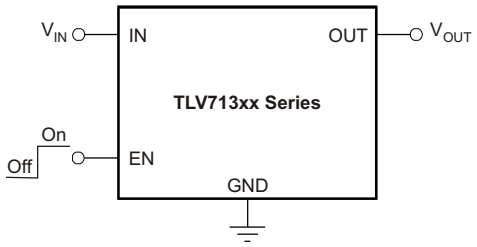
The TLV713 series of low-dropout (LDO) linear regulators are low quiescent current LDOs with excellent line and load transient performance and are designed for power-sensitive applications. These devices provide a typical accuracy of 1%.

The TLV713 series is designed to be stable without an output capacitor. The removal of the output capacitor allows for a very small solution size. However, the TLV713 series is also stable with any output capacitor if an output capacitor is used.

The TLV713 also provides inrush current control during device power-up and enabling. The TLV713 limits the input current to the defined current limit to avoid large currents from flowing from the input power source. This functionality is especially important in battery-operated devices.

The TLV713 series is available in standard DQN and DBV packages. The TLV713P provides an active pull-down circuit to quickly discharge output loads.

Typical Application Circuit



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)(2)

PRODUCT	V_{OUT}
TLV713**xx(x)Pyyyz**	**XX(X)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 475 = 4.75 V). **P** is optional; devices with P have an LDO regulator with an active output discharge. **YYY** is the package designator. **Z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = +25°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	Input range, V_{IN}	–0.3	6.0	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	V
	Output range, V_{OUT}	–0.3	6.0	V
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Total power dissipation	Continuous, P_{DISS}	See Thermal Information table		
Temperature	Junction range, T_J	–55	+85	°C
	Storage junction range, T_{stg}	–55	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2000	V
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TLV713xx TLV713xxP		UNITS
		DQN (X2SON)	DBV (SOT23)	
		4 PINS	5 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	255.8	213.1	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	159.3	110.9	
θ_{JB}	Junction-to-board thermal resistance	208.2	97.4	
ψ_{JT}	Junction-to-top characterization parameter	16.2	22.0	
ψ_{JB}	Junction-to-board characterization parameter	208.1	78.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	148.6	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

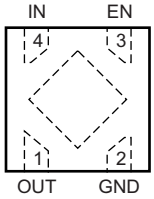
At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{OUT} = 0.47 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV713			UNIT
				MIN	TYP	MAX	
V_{IN}	Input voltage range			1.4		5.5	V
V_{OUT}	Output voltage range			1.0		3.3	V
	DC output accuracy	V_{OUT} ≥ 1.8 V, T_A = +25°C		–1		1	%
		V_{OUT} < 1.8 V, T_A = +25°C		–20		20	mV
		V_{OUT} ≥ 1.2 V, –40°C ≤ T_A ≤ +85°C		–1.5		1.5	%
		V_{OUT} < 1.2 V, –40°C ≤ T_A ≤ +85°C		–50		50	mV
$\Delta V_O/V_{IN}$	Line regulation				1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	30	mV
V_{DO}	Dropout voltage	V_{OUT} = 0.98 × $V_{OUT(NOM)}$	1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 30 mA		70		mV
			1.8 V ≤ V_{OUT} < 2.1 V, I_{OUT} = 150 mA		350	575	mV
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 30 mA		90		mV
			2.1 V ≤ V_{OUT} < 2.5 V, I_{OUT} = 150 mA		290	481	mV
			2.5 V ≤ V_{OUT} < 3.0 V, I_{OUT} = 30 mA		50		mV
			2.5 V ≤ V_{OUT} < 3.0 V, I_{OUT} = 150 mA		246	445	mV
			3.3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 30 mA		46		mV
			3.3 V ≤ V_{OUT} < 3.6 V, I_{OUT} = 150 mA		230	420	mV
			1.0 V ≤ V_{OUT} < 1.8 V, I_{OUT} = 150 mA		600	900	mV
			V_{OUT} = 1.1 V, I_{OUT} = 100 mA		470	600	mV
I_{GND}	Ground pin current	I_{OUT} = 0 mA			50	75	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 5.5 V, T_A = +25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 100 Hz		70		dB
			f = 10 kHz		55		dB
			f = 1 MHz		55		dB
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 150 mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pull-down resistor (TLV713P only)	V_{IN} = 4 V			120		Ω
T_J	Operating junction temperature			–40		+125	°C
I_{LIM}	Output current limit	V_{IN} = 3.8 V, V_{OUT} = 3.3 V		180			mA
		V_{IN} = 2.25 V, V_{OUT} = 1.8 V		180			mA
		V_{IN} = 2.0 V, V_{OUT} = 1.2 V		180			mA
I_{SC}	Short-circuit current	V_{OUT} = 0 V			40		mA
T_{SD}	Thermal shutdown	Shutdown, temperature increasing			158		°C
		Reset, temperature decreasing			140		°C

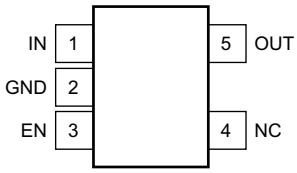
(1) Startup time is the time from EN assertion to (0.98 × $V_{OUT(nom)}$).

PIN CONFIGURATIONS

DQN PACKAGE
1-mm × 1-mm X2SON
(Top View)



DBV PACKAGE
SOT23-5
(Top View)



PIN DESCRIPTIONS

PIN			DESCRIPTION
NAME	DQN	SOT23-5	
EN	3	3	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	2	Ground pin
IN	4	1	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
NC	—	4	No internal connection
OUT	1	5	Regulated output voltage pin. For best transient response, a small 1-µF ceramic capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Requirements* section in the *Application Information* for more details.
Thermal pad	—	—	TI recommends connecting this pin to GND for improved thermal performance.

FUNCTIONAL BLOCK DIAGRAMS

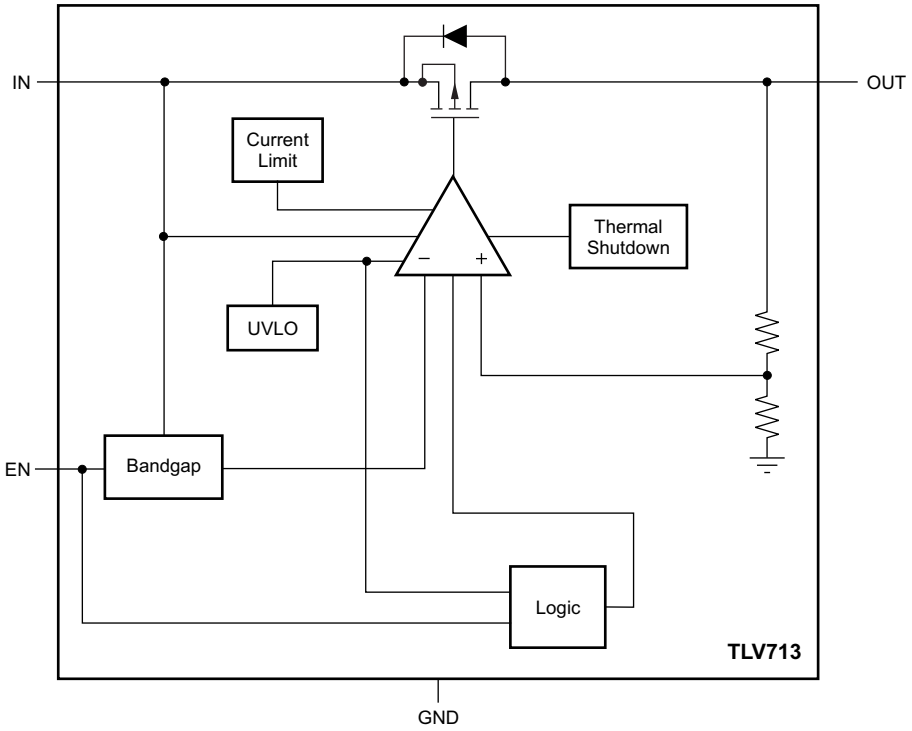


Figure 1. TLV713 Block Diagram

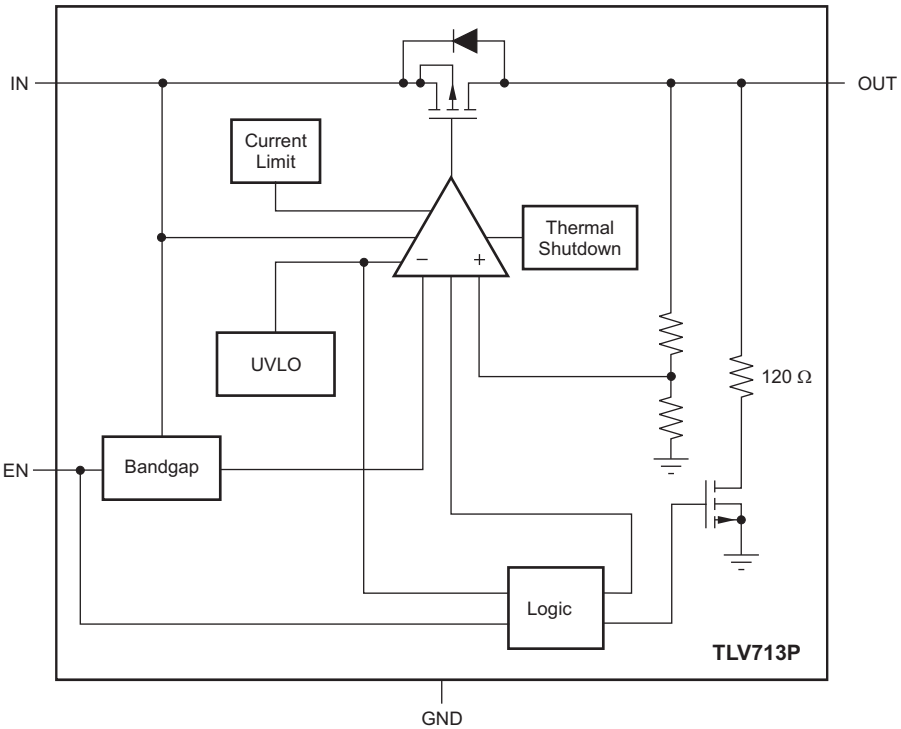


Figure 2. TLV713P Block Diagram

TYPICAL CHARACTERISTICS

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

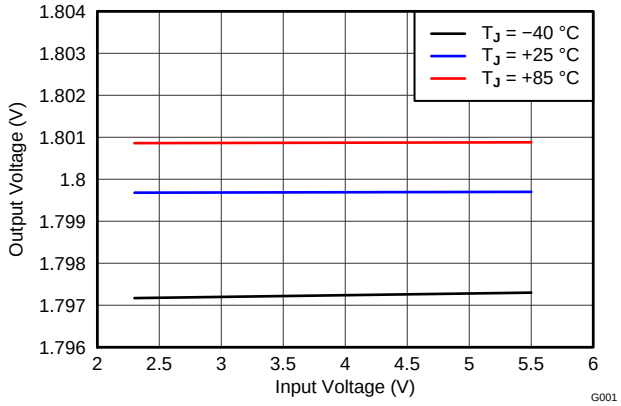


Figure 3. 1.8-V LINE REGULATION vs V_{IN} AND TEMPERATURE

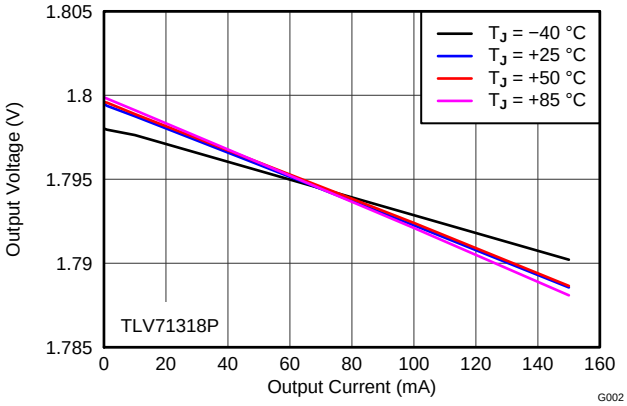


Figure 4. 1.8-V LOAD REGULATION vs I_{OUT} AND TEMPERATURE

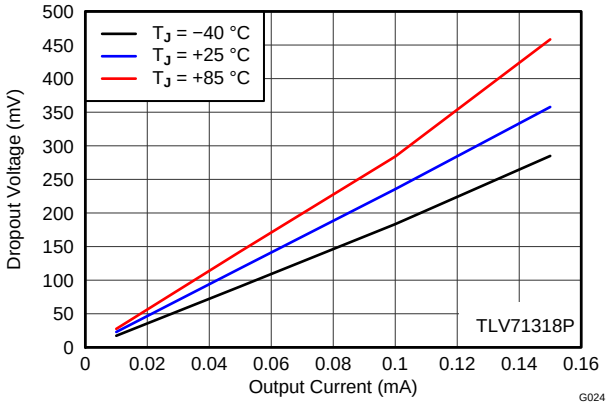


Figure 5. 1.8-V DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE

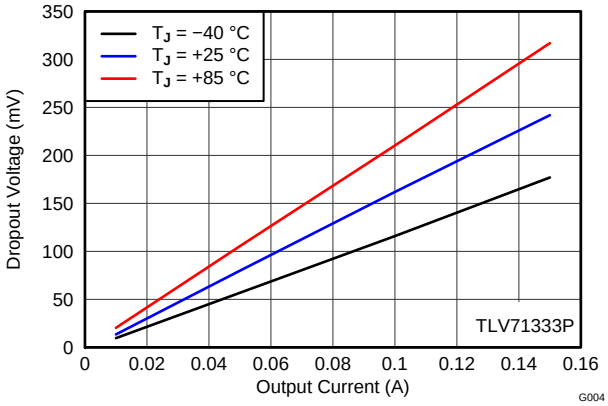


Figure 6. 3.3-V DROPOUT VOLTAGE vs I_{OUT} AND TEMPERATURE

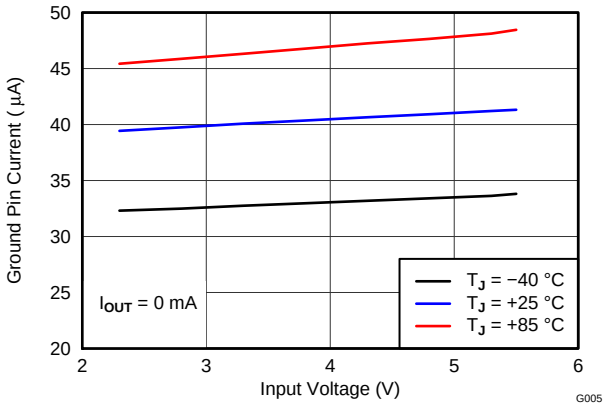


Figure 7. GROUND PIN CURRENT vs V_{IN} AND TEMPERATURE

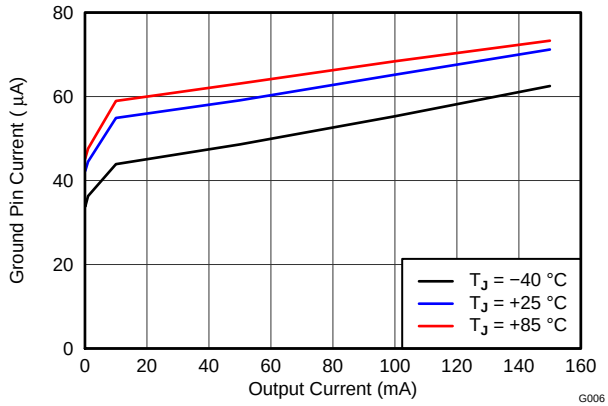


Figure 8. GROUND PIN CURRENT vs I_{OUT} AND TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

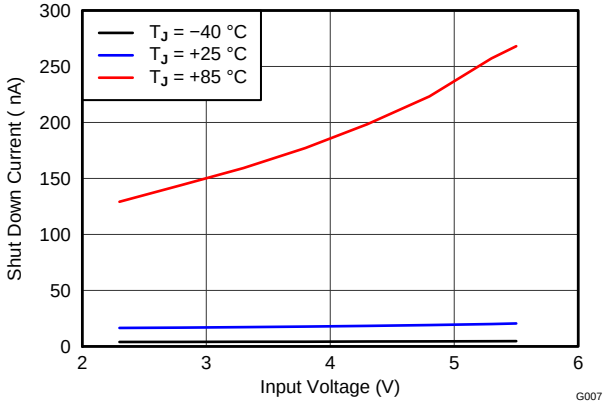


Figure 9. SHUTDOWN CURRENT vs V_{IN} AND TEMPERATURE

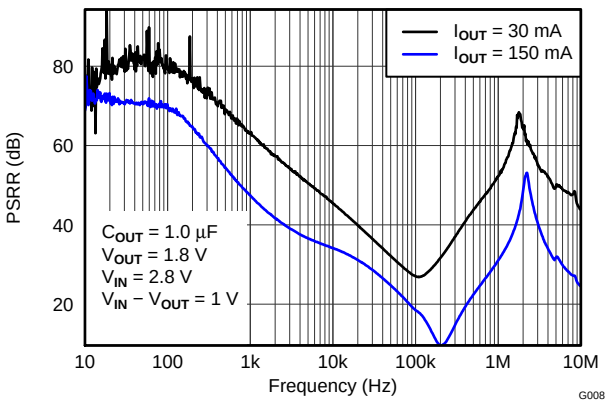


Figure 10. POWER-SUPPLY REJECTION RATIO vs FREQUENCY

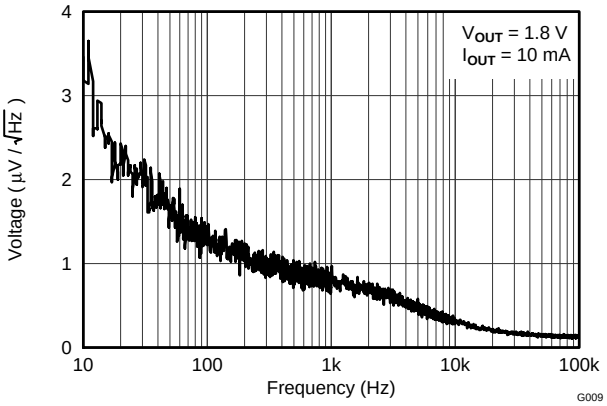


Figure 11. OUTPUT SPECTRAL NOISE DENSITY

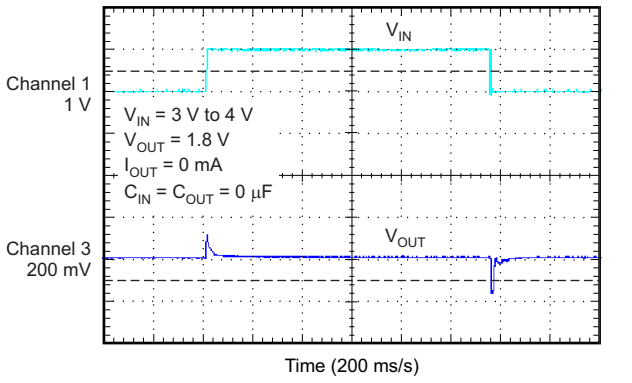


Figure 12. LINE TRANSIENT

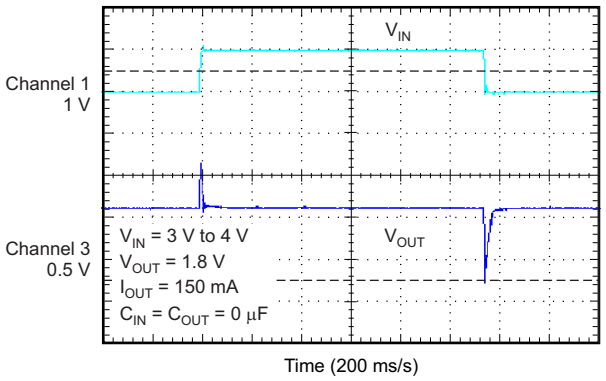


Figure 13. LINE TRANSIENT

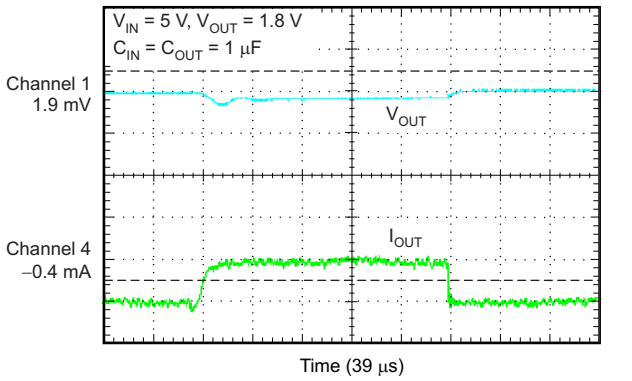


Figure 14. 0-mA to 20-mA LOAD TRANSIENT

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

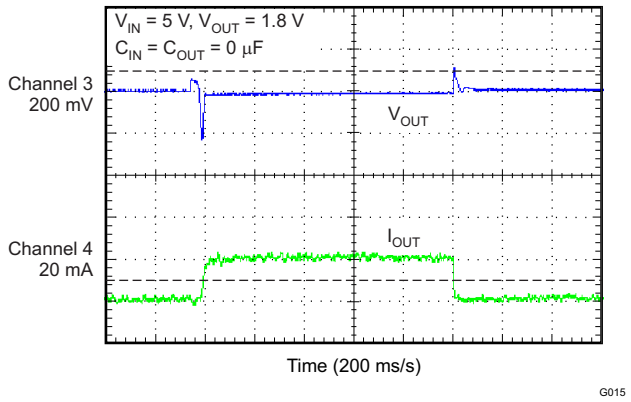


Figure 15. 0-mA to 20-mA LOAD TRANSIENT

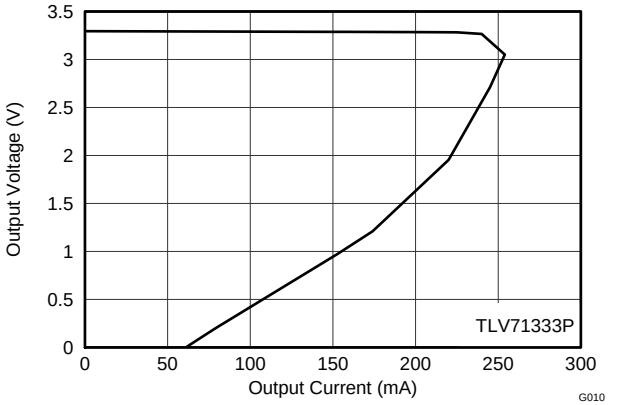


Figure 16. 3.3-V OUTPUT VOLTAGE vs OUTPUT CURRENT (Foldback Current Limit)

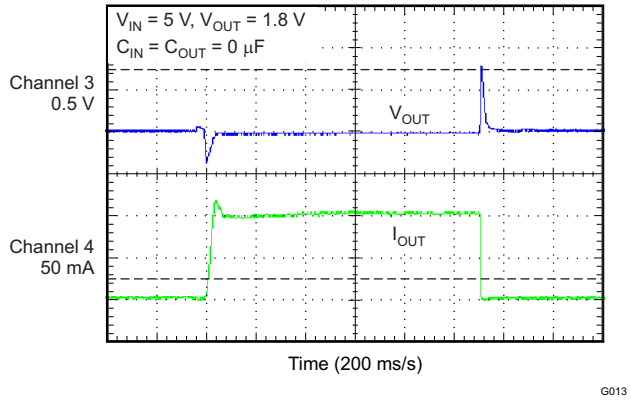


Figure 17. 0-mA to 100-mA LOAD TRANSIENT

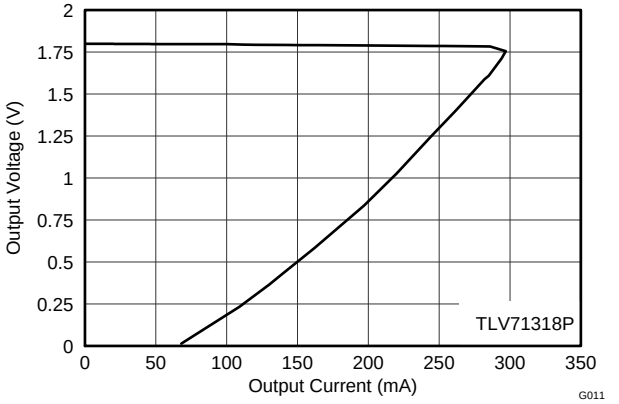


Figure 18. 1.8-V OUTPUT VOLTAGE vs OUTPUT CURRENT (Foldback Current Limit)

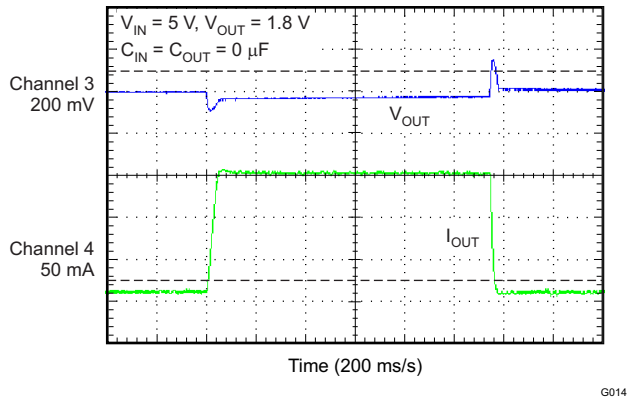


Figure 19. 10-mA to 150-mA LOAD TRANSIENT

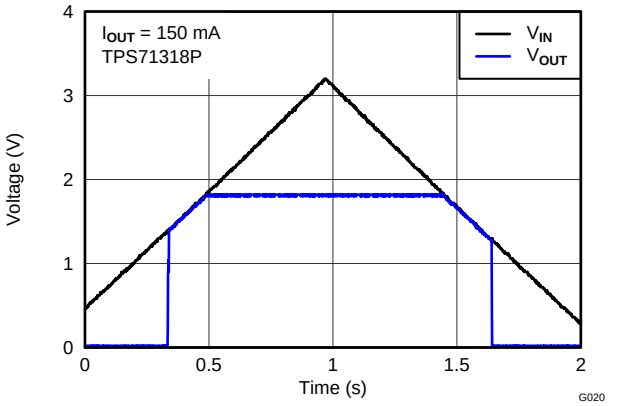


Figure 20. V_{IN} POWER-UP AND POWER-DOWN

TYPICAL CHARACTERISTICS (continued)

At operating temperature range (T_A = –40°C to +85°C), T_A = +25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

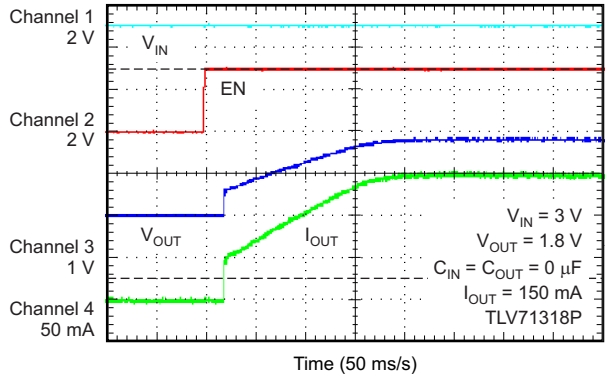


Figure 21. STARTUP WITH EN

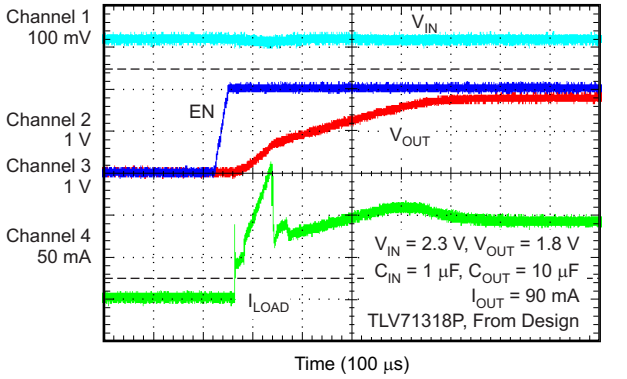


Figure 22. STARTUP WITH EN

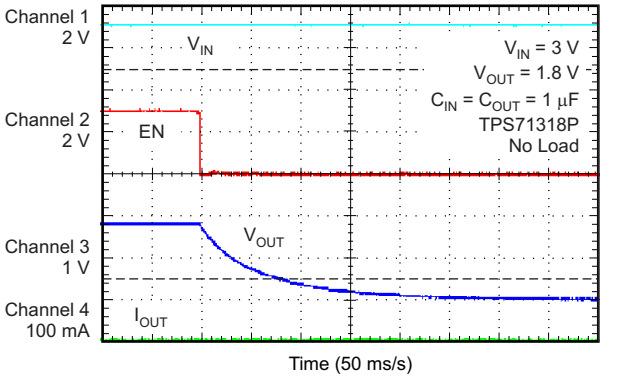


Figure 23. SHUTDOWN RESPONSE WITH ENABLE

APPLICATION INFORMATION

The TLV713 belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current limit and thermal protection. Device operating junction temperature is –40°C to +85°C.

INPUT AND OUTPUT CAPACITOR CONSIDERATIONS

The TLV713 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. The TLV713xx dynamic performance is improved with the use of an output capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated or if the device is located several inches from the input power source.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

INTERNAL CURRENT LIMIT

The TLV713 has an internal foldback current limit that helps protect the regulator during fault conditions. The current supplied by the device is gradually throttled down while the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is (V_{OUT} = I_{LIMIT} × R_{LOAD}). The PMOS pass transistor dissipates [(V_{IN} – V_{OUT}) × I_{LIMIT}] until thermal shutdown is triggered and the device turns off. While the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The TLV713 PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

POWERING THE MSP430 MICROCONTROLLER

Figure 24 shows a diagram of the TLV713 powering an MSP430 microcontroller. Several versions of the TPS713 are ideal for powering the MSP430 microcontroller. Table 1 shows potential applications of some voltage versions.

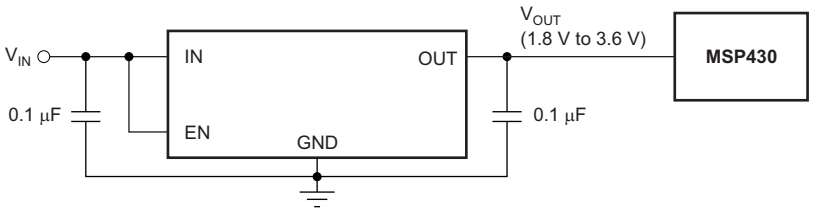


Figure 24. TLV713 Powering a Microcontroller

Table 1. Typical MSP430 Applications

DEVICE	V_{OUT} (Typ)	APPLICATION
TLV71319	1.9 V	V_{OUT}, minimum > 1.8 V required by many MSP430s, allows lowest power consumption operation
TLV71323	2.3 V	V_{OUT}, minimum > 2.2 V required by some MSP430s FLASH operation
TLV71330	3.0 V	V_{OUT}, minimum > 2.7 V required by some MSP430s FLASH operation

DROPOUT VOLTAGE

The TLV713 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV713 uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV713 internal protection circuitry is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TLV713 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in the Thermal Information table. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. P_D is equal to the product of the output current and voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2013) to Revision D — **Page**

- Changed document status from Mixed Status to Production Data 1
- Deleted DPW package from document 1
- Deleted DPW pin out drawing from front-page graphic 1
- Deleted footnote for page 1 graphic 1
- Deleted reference to DPW package from last sentence of *Description* section 1
- Deleted footnote 3 of Ordering Information table 2
- Deleted DPW data from Thermal Information table 2
- Deleted DPW pin out drawing from Pin Configurations section 4
- Deleted reference to DPW package from Pin Descriptions table 4

Changes from Revision B (December 2012) to Revision C — **Page**

- Changed last Features bullet 1
- Added Typical Application Circuit 1
- Changed last two rows of the V_{DO} parameter in the Electrical Characteristics table 3

Changes from Revision A (October 2012) to Revision B — **Page**

- Changed footnote for page 1 graphic 1
- Changed footnote 3 of Ordering Information table 2
- Added DBV data to Thermal Information table 2

Changes from Original (September 2012) to Revision A — **Page**

- Reordered Features bullets 1
- Changed dropout range in fourth Features bullet 1
- Changed *Package* and *Fixed-Output Voltage* Features bullets 1
- Updated DQN pin out drawing 1
- Added second and third paragraphs to *Description* section 1
- Changed DQN header row in Thermal Information table 2
- Changed V_{OUT} maximum specification in Electrical Characteristics table 3
- Combined all V_{DO} rows together in Electrical Characteristics table 3
- Changed V_{DO} specifications in Electrical Characteristics table 3
- Changed I_{SHDN} test conditions in Electrical Characteristics table 3
- Changed DQN pin out caption in Pin Configurations section 4
- Changed 1.2 V to 0.9 V in description of EN pin in Pin Descriptions table 4
- Updated Figure 1 5
- Changed Typical Characteristics conditions 6
- Added curves 6
- Changed junction temperature range in second paragraph of *Application Information* section 10
- Changed second paragraph of *Input and Output Capacitor Considerations* section 10
- Deleted curve reference from *Dropout Voltage* section 11
- Deleted third paragraph from *Thermal Information* section 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71310PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUQI	Samples
TLV71310PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUQI	Samples
TLV71310PDQNR	PREVIEW	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ET	
TLV71310PDQNT	PREVIEW	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ET	
TLV71311PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUPI	Samples
TLV71311PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUPI	Samples
TLV71312PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUEI	Samples
TLV71312PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUEI	Samples
TLV71312PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AF	Samples
TLV71312PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AF	Samples
TLV71315PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUGI	Samples
TLV71315PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUGI	Samples
TLV71315PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AY	Samples
TLV71315PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AY	Samples
TLV713185PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUII	Samples
TLV713185PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUII	Samples
TLV713185PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A1	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV713185PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A1	Samples
TLV71318PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUDI	Samples
TLV71318PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUDI	Samples
TLV71318PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AW	Samples
TLV71318PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AW	Samples
TLV71320DQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2	Samples
TLV71320DQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2	Samples
TLV71325PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUJI	Samples
TLV71325PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUJI	Samples
TLV71325PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZ	Samples
TLV71325PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZ	Samples
TLV713285PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VULI	Samples
TLV713285PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VULI	Samples
TLV713285PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A2	Samples
TLV713285PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	A2	Samples
TLV71328PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUKI	Samples
TLV71328PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUKI	Samples
TLV71328PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AK	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71328PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AK	Samples
TLV71330PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUMI	Samples
TLV71330PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUMI	Samples
TLV71330PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AL	Samples
TLV71330PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AL	Samples
TLV71333PDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUFI	Samples
TLV71333PDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	VUFI	Samples
TLV71333PDQNR	ACTIVE	X2SON	DQN	4	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH	Samples
TLV71333PDQNT	ACTIVE	X2SON	DQN	4	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

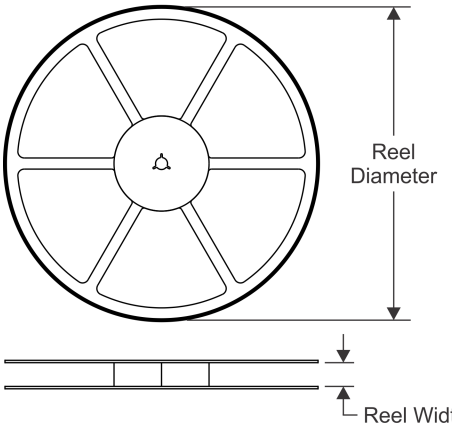
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

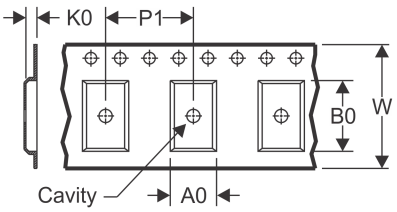
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

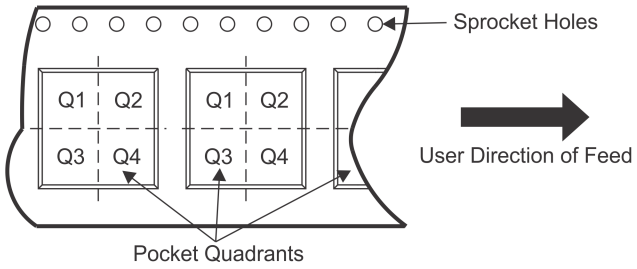


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

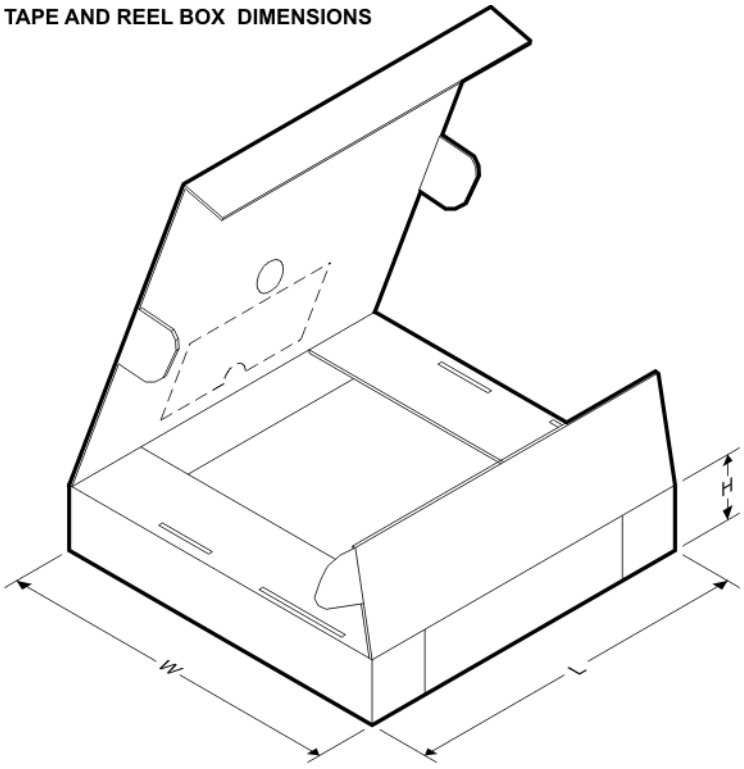


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71310PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71311PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71312PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71312PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71312PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71315PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71315PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71315PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV713185PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV713185PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV713185PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71318PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71318PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71318PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71320DQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71320DQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71325PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71325PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71325PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV713285PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV713285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV713285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71328PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71328PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71328PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71330PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71330PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71330PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71333PDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV71333PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2
TLV71333PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

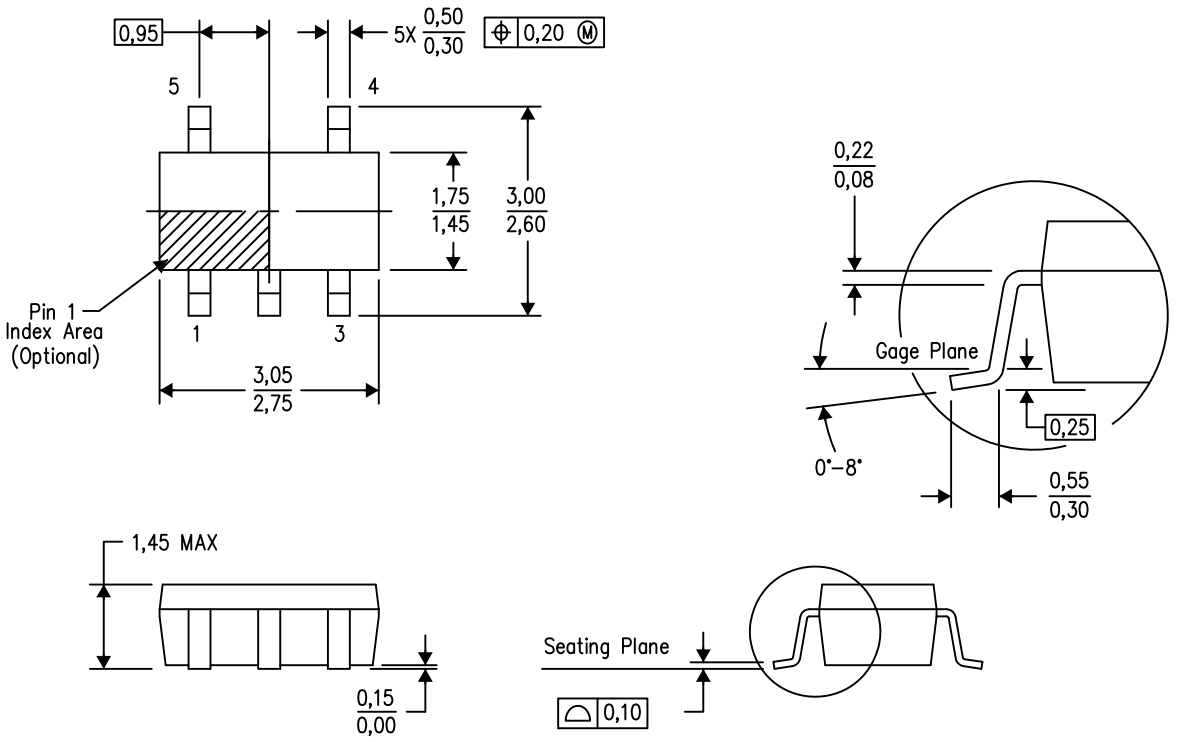


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71310PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71311PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71312PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71312PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71312PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71315PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71315PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71315PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV713185PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV713185PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV713185PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71318PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71318PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71318PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71320DQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71320DQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71325PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71325PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71325PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV713285PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV713285PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV713285PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71328PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71328PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71328PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71330PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71330PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71330PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0
TLV71333PDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV71333PDQNR	X2SON	DQN	4	3000	180.0	180.0	30.0
TLV71333PDQNT	X2SON	DQN	4	250	180.0	180.0	30.0

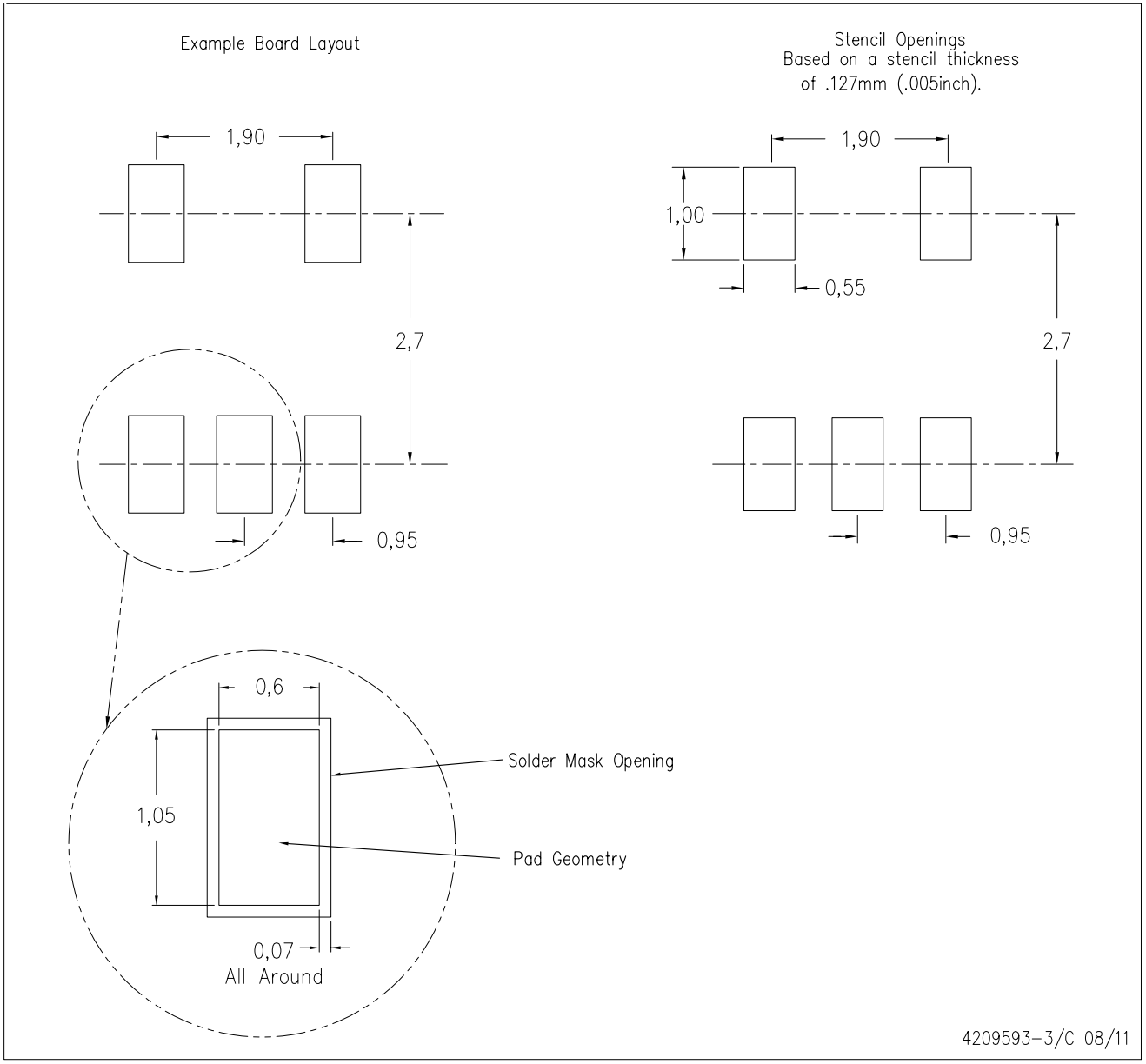
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/L 08/2013

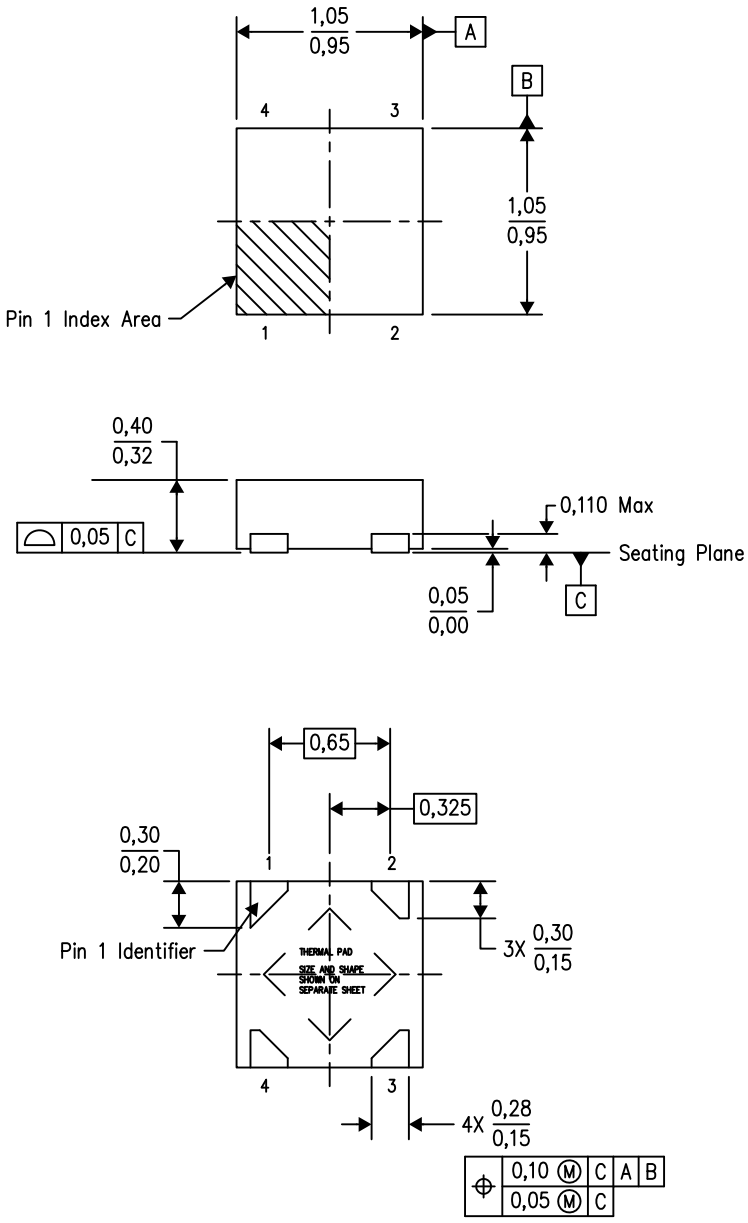
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



4210367/D 09/2012

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

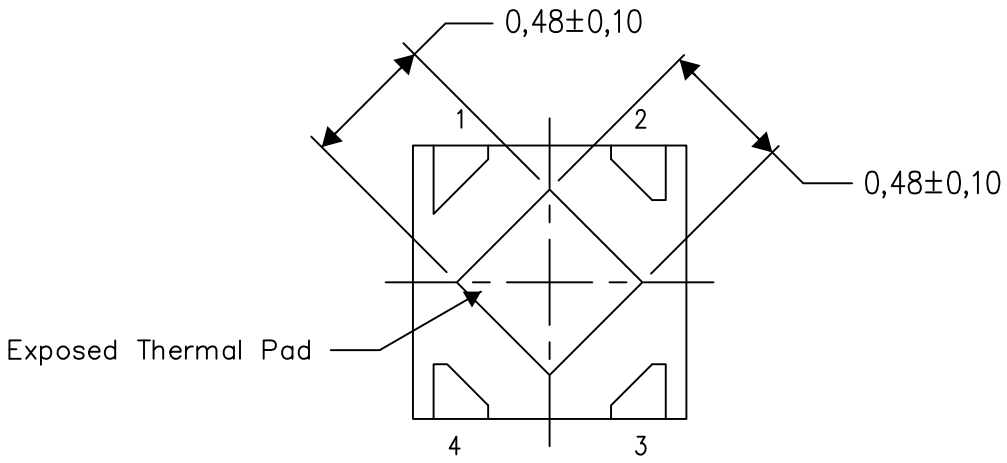
DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



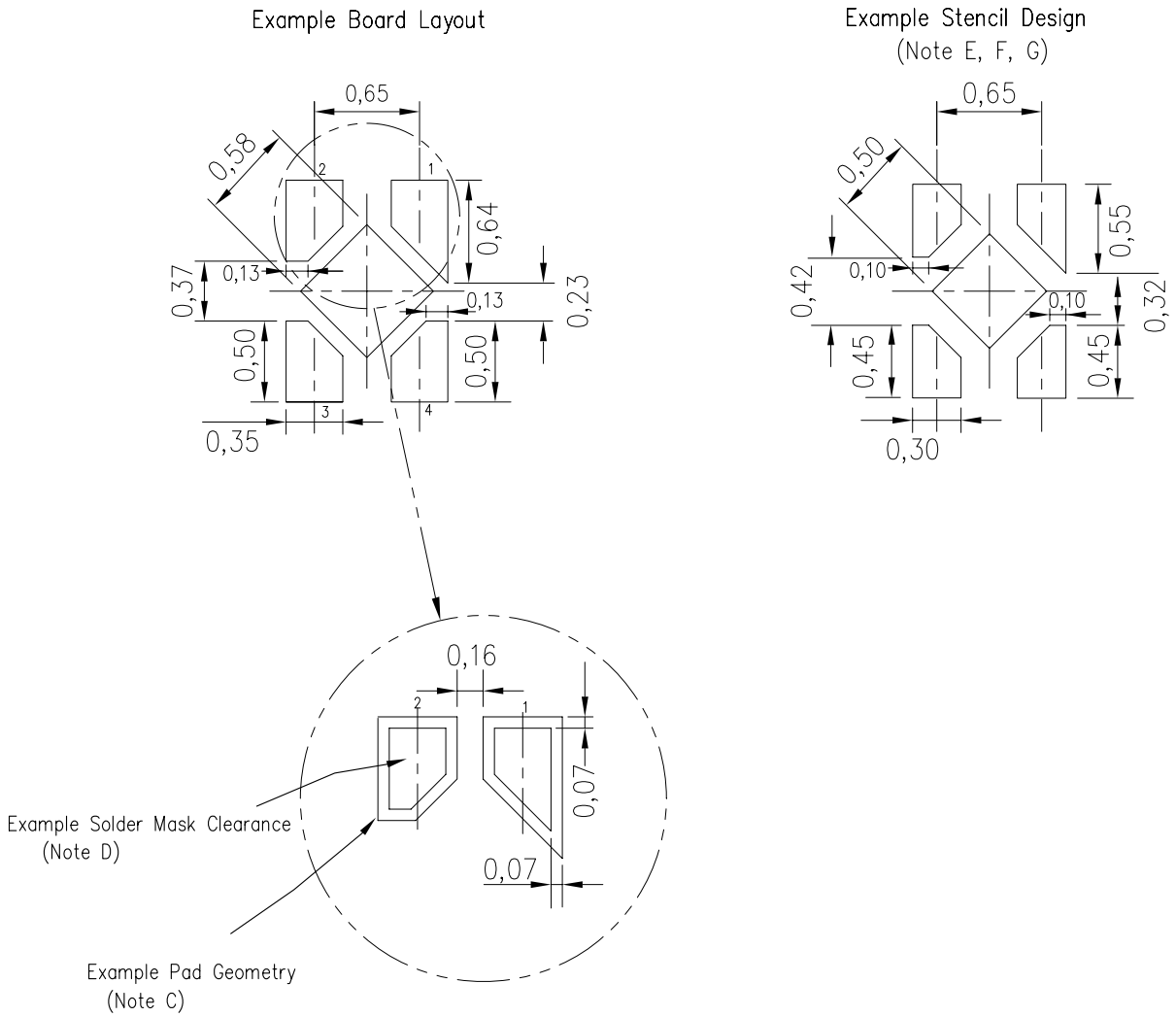
Bottom View

Exposed Thermal Pad Dimensions

4210393–3/E 04/12

NOTE: All linear dimensions are in millimeters

DQN (S–PX2SON–N4) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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