TEXAS INSTRUMENTS

TLV70018-Q1, TLV70012-Q1

SLVSB67B – NOVEMBER 2011 – REVISED JANUARY 2016

TLV700xx-Q1 300-mA, Low-I_Q, Low-Dropout Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- 2% Accuracy
- Low I_Q: 35 µA
- Fixed-Output Voltage Combinations Possible from 1.2 V to 4.8 V
- High PSRR: 68 dB at 1 kHz
- Stable With Effective Capacitance of 0.1 µF(1)
- Thermal Shutdown and Overcurrent Protection

(1) See the *Input and Output Capacitor Requirements*.

2 Applications

- MP3 Players
- ZigBee® Networks
- Bluetooth® Devices
- Li-Ion Operated Handheld Products

3 Description

The TLV700xx-Q1 series of low-dropout (LDO) linear regulators are low quiescent current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy. Low output noise, high power-supply rejection ratio (PSRR), and low-dropout voltage make this series of devices ideal for a wide selection of battery-operated handheld equipment. All device versions have thermal shutdown and current limit for safety.

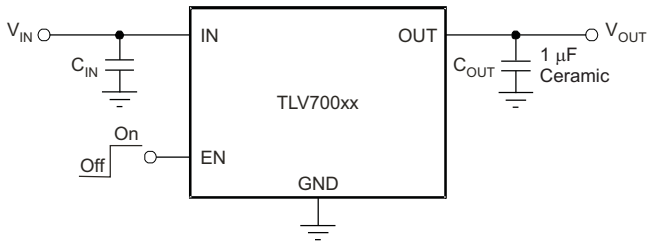
Furthermore, these devices are stable with an effective output capacitance of only 0.1 µF. This feature enables the use of cost-effective capacitors that have higher bias voltages and temperature derating. The devices regulate to specified accuracy with no output load.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV70018-Q1	SOT (5)	2.90 mm × 1.60 mm
TLV70012-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application (Fixed-Voltage Version)



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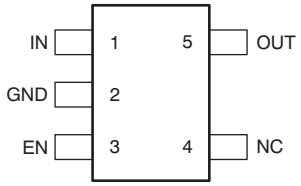
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2012) to Revision B	Page
• Added *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Detailed Description* section, *Application and Implementation* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted the *Dissipation Ratings* table	4

5 Pin Configuration and Functions

DDC Package
5-Pin SOT
Top View



Pin Functions

PIN		DESCRIPTION
NO.	NAME	
1	IN	Input pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability and good transient performance. (1)
2	GND	Ground pin
3	EN	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode and reduces operating current to 1 µA, nominal.
4	NC	No connection. This pin can be tied to ground to improve thermal dissipation.
5	OUT	Regulated output voltage pin. A small 1-µF ceramic capacitor is needed from this pin to ground to assure stability. (1)

(1) See *Input and Output Capacitor Requirements* section for more details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage(2)	IN	–0.3	6.0	V
	EN	–0.3	6.0	V
	OUT	–0.3	6.0	V
Current (source)	OUT	Internally Limited		
Output short-circuit duration		Indefinite		
Operating virtual junction, T_J		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range, unless otherwise noted.

			MIN	MAX	UNIT
V_I	Input voltage	IN	2	5.5	V
		EN	0	5.5	
		OUT	0	5.5	
	Current output		0	300	mA
T_J	Operating junction temperature		–40	150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV70018-Q1 DDC (SOTC23) 5 PINS	TLV70012-Q1 DDC (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.9	262.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.1	68.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.4	81.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.5	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.2	80.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

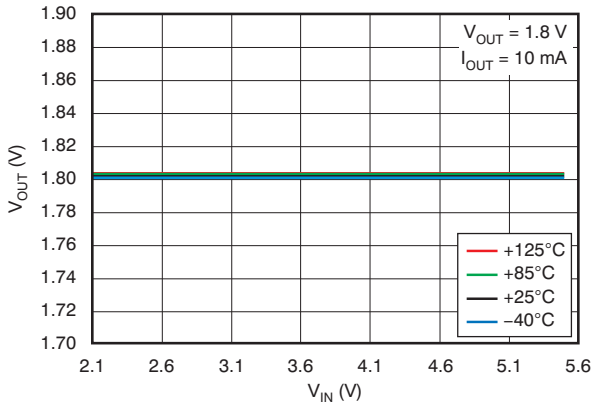
At V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V (whichever is greater); I_{OUT} = 10 mA, V_{EN} = 0.9 V, C_{OUT} = 1.0 µF, and T_A = –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2		5.5	V
V_{OUT}	DC output accuracy	–40°C ≤ T_A ≤ 125°C	–2%	0.5%	2%	
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 300 mA, TLV70018-Q1		1	15	mV
		0 mA ≤ I_{OUT} ≤ 300 mA, TLV70012-Q1		1	20	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	320	500	860	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA		35	55	µA
		I_{OUT} = 300 mA, V_{IN} = V_{OUT} + 0.5 V		370		µA
I_{SHDN}	Ground pin current (shutdown)	V_{EN} ≤ 0.4 V, V_{IN} = 2.0 V		400		nA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V, T_A = –40°C to 85°C		1	2	µA
		V_{EN} ≤ 0.4 V, 2.0 V ≤ V_{IN} ≤ 4.5 V, T_A = 85°C to 125°C		1	2.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA, f = 1 kHz		68		dB
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA		48		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0 µF, I_{OUT} = 300 mA		100		µs
$V_{EN(HI)}$	Enable pin high (enabled)		0.9		V_{IN}	V
$V_{EN(LO)}$	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	V_{IN} = V_{EN} = 5.5 V		0.04		µA
UVLO	Undervoltage lockout	V_{IN} rising		1.9		V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
		Reset, temperature decreasing		145		°C
T_A	Operating temperature		–40		125	°C

(1) Startup time = time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

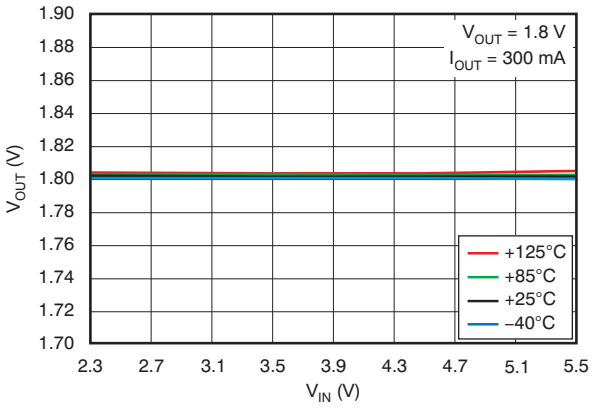
6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = 25°C.



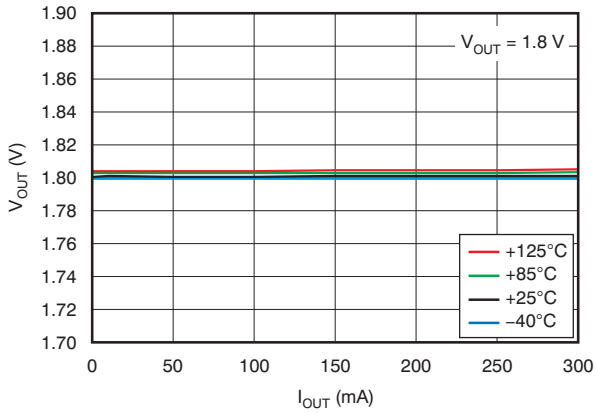
V_{OUT} = 1.8 V I_{OUT} = 10 mA

Figure 1. Line Regulation 10 mA



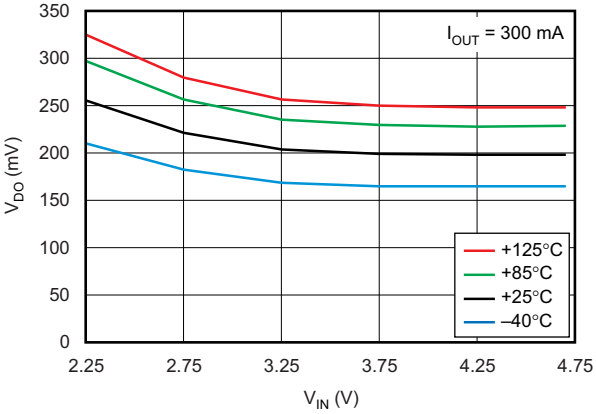
V_{OUT} = 1.8 V I_{OUT} = 300 mA

Figure 2. Line Regulation 300 mA



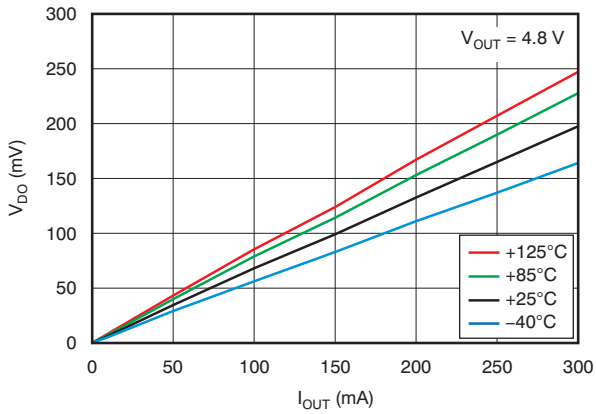
V_{OUT} = 1.8 V

Figure 3. Load Regulation



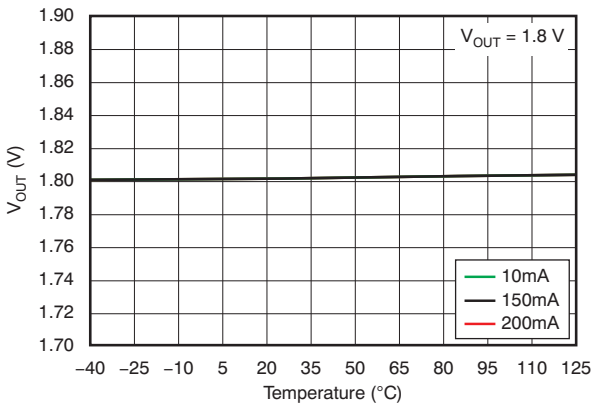
I_{OUT} = 300 mA

Figure 4. Dropout Voltage vs Input Voltage



V_{OUT} = 4.8 V

Figure 5. Dropout Voltage vs Output Current

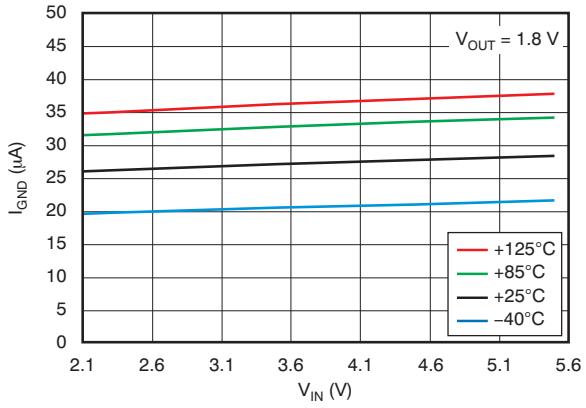


V_{OUT} = 1.8 V

Figure 6. Output Voltage vs Temperature

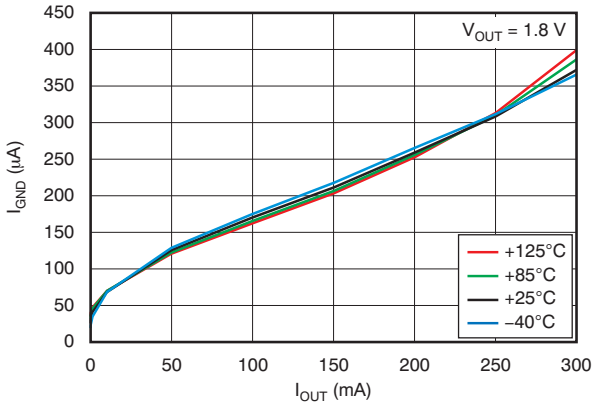
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = 25°C.



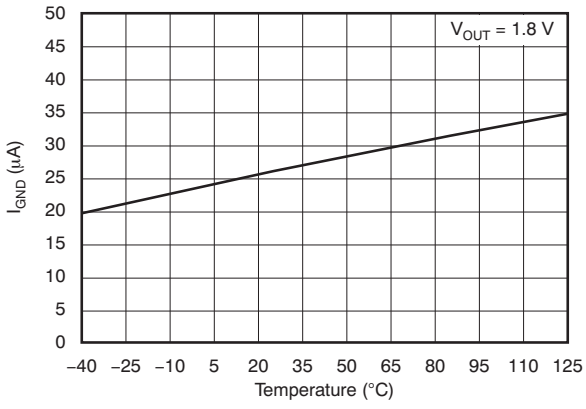
V_{OUT} = 1.8 V

Figure 7. Ground Pin Current vs Input Voltage



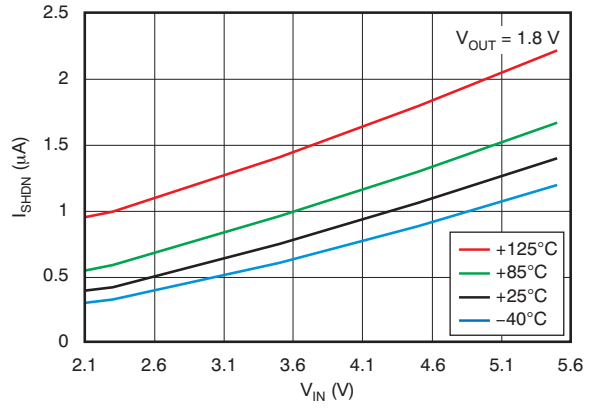
V_{OUT} = 1.8 V

Figure 8. Ground Pin Current vs Load



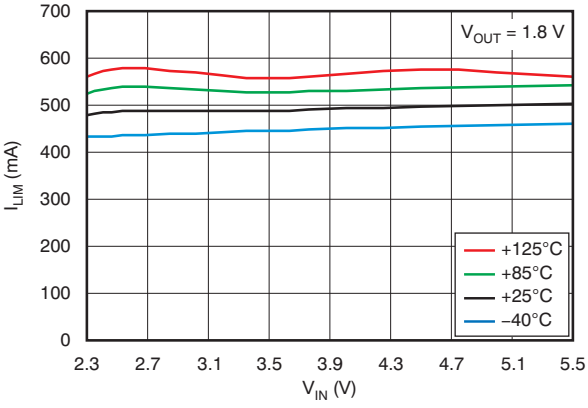
V_{OUT} = 1.8 V

Figure 9. Ground Pin Current vs Temperature



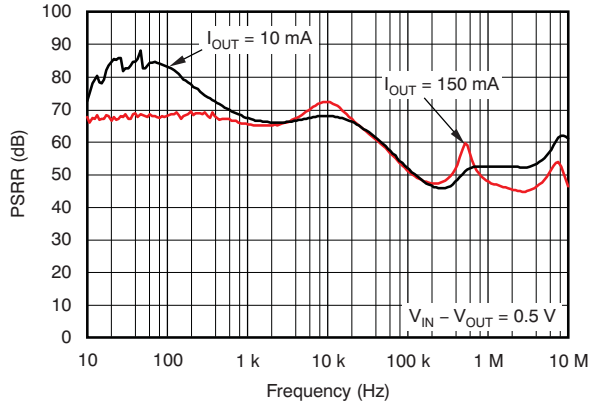
V_{OUT} = 1.8 V

Figure 10. Shutdown Current vs Input Voltage



V_{OUT} = 1.8 V

Figure 11. Current Limit vs Input Voltage

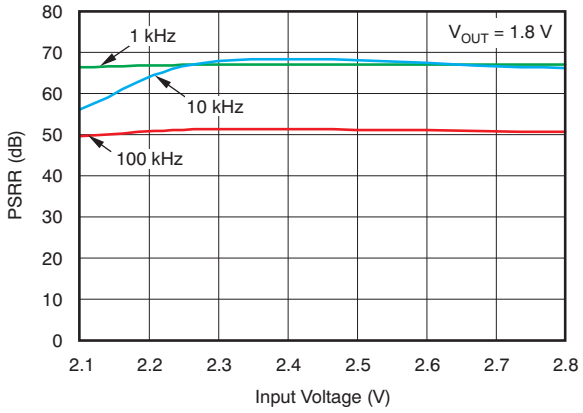


V_{IN} – V_{OUT} = 0.5 V

Figure 12. Power-Supply Ripple Rejection vs Frequency

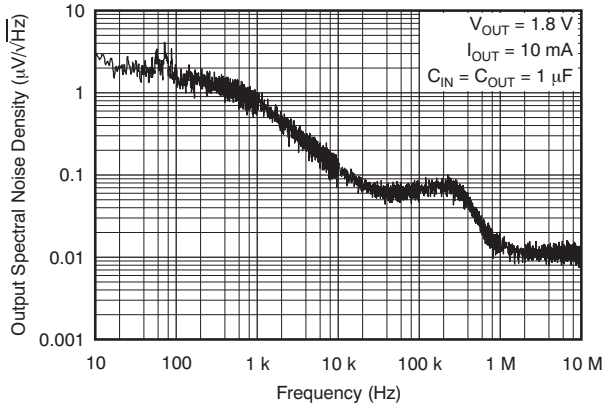
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = 25°C.



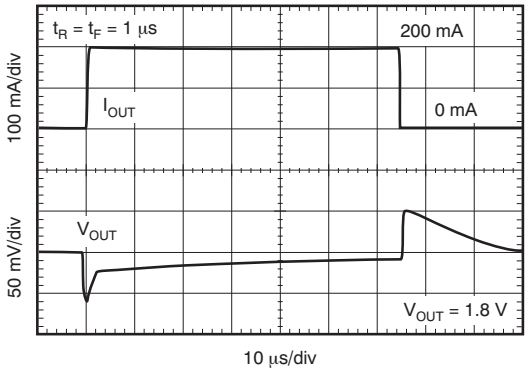
V_{OUT} = 1.8 V

Figure 13. Power-Supply Ripple Rejection vs Input Voltage



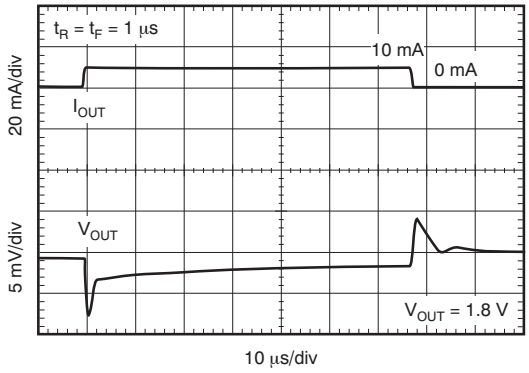
V_{OUT} = 1.8 V I_{OUT} = 10 mA C_{OUT} = 1 µF
C_{IN} = 1 µF

Figure 14. Output Spectral Noise Density vs Frequency



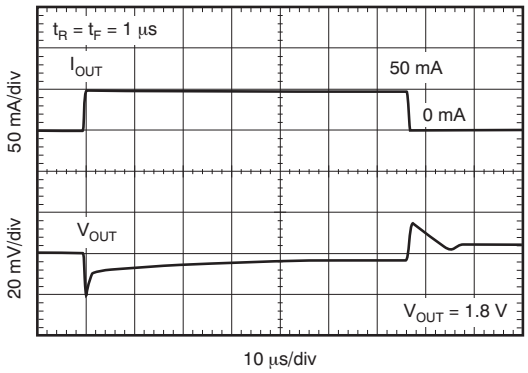
V_{OUT} = 1.8 V

Figure 15. Load Transient Response



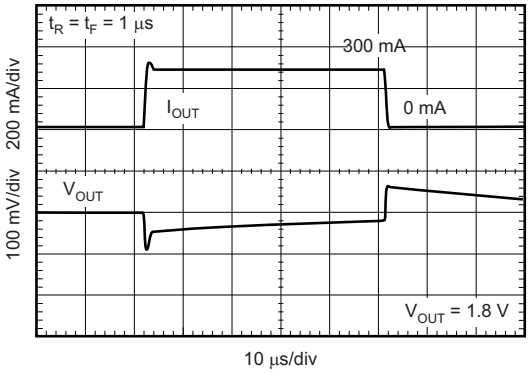
V_{OUT} = 1.8 V

Figure 16. Load Transient Response



V_{OUT} = 1.8 V

Figure 17. Load Transient Response

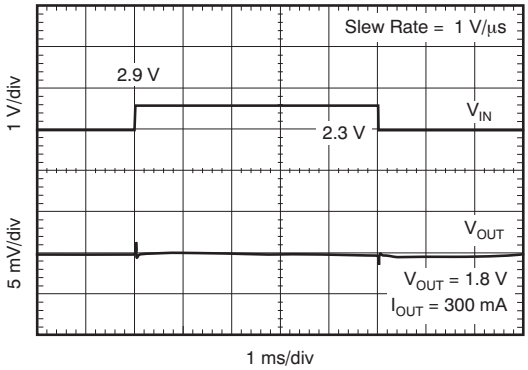


V_{OUT} = 1.8 V

Figure 18. Load Transient Response

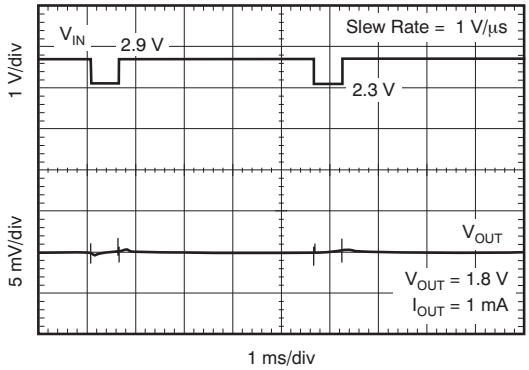
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.5 V or 2 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, C_{OUT} = 1.0 µF, unless otherwise noted. Typical values are at T_J = 25°C.



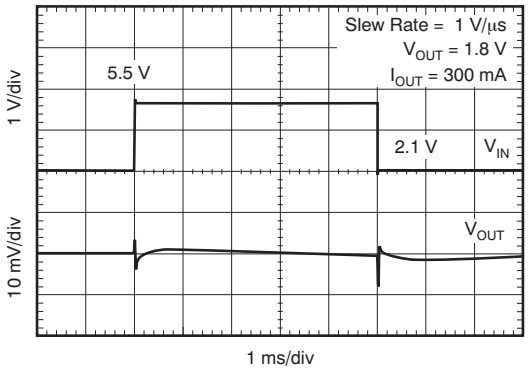
V_{OUT} = 1.8 V I_{OUT} = 300 mA

Figure 19. Line Transient Response



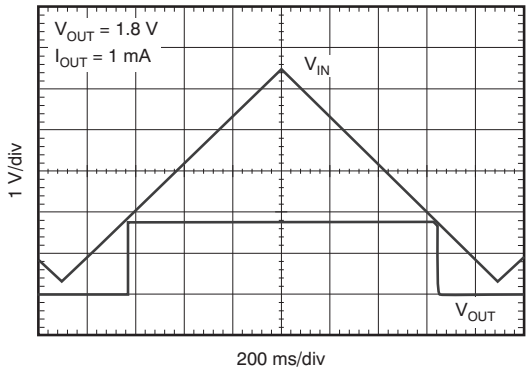
V_{OUT} = 1.8 V I_{OUT} = 1 mA

Figure 20. Line Transient Response



Slew Rate = 1 V / µs V_{OUT} = 1.8 V I_{OUT} = 300 mA

Figure 21. Line Transient Response



V_{OUT} = 1.8 V I_{OUT} = 1 mA

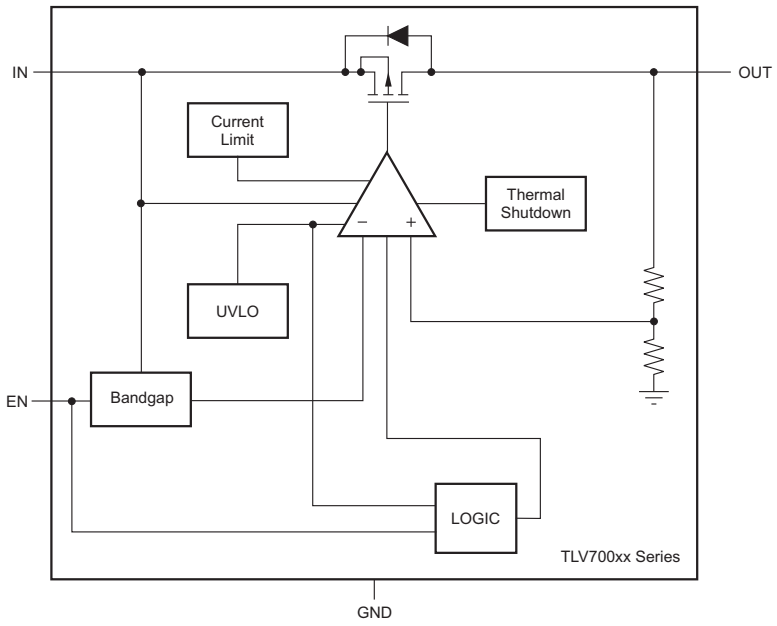
Figure 22. V_{IN} Ramp Up, Ramp Down Response

7 Detailed Description

7.1 Overview

The TLV700xx-Q1 family of low-dropout (LDO) linear regulators are low-quiescent-current devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provides overall 2% accuracy together with low output noise, very high power-supply rejection ratio (PSRR), and low dropout voltage.

7.2 Functional Block Diagrams



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV70018-Q1 internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device turns off. As the device cools, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Considerations* section for more details.

The PMOS pass element in the TLV70018-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

7.3.2 Dropout Voltage

The TLV70018-Q1 uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as $(V_{IN} – V_{OUT})$ approaches dropout. This effect is shown in Figure 13.

Feature Description (continued)

7.3.3 Undervoltage Lockout (UVLO)

The TLV70018-Q1 uses an undervoltage lockout circuit to keep the output shut off until internal circuitry is operating properly.

7.3.4 Thermal Shutdown

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV700xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV700xx-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Shutdown

The enable pin (EN) is active high. The device is enabled when voltage at EN pin goes above 0.9 V. This relatively lower value of voltage required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO Logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

7.4.2 Operation with V_{IN} Less than 2 V

The TLV700xx-Q1 family of devices operates with input voltages above 2 V. The typical UVLO voltage is 1.9 V and the device operates at an input voltage above 2 V. When input voltage falls below UVLO voltage, the device will shutdown.

7.4.3 Operation with V_{IN} Greater than 2 V

When V_{IN} is greater than 2 V, if input voltage is higher than desired output voltage plus dropout voltage, the output voltage is equal to the desired value. Otherwise, output voltage will be V_{IN} minus dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV700xx-Q1 belongs to a new family of next-generation value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for portable RF applications. This family of regulators offers current limit and thermal protection, and is specified from –40°C to 125°C.

The TLV700xx is a 200-mA, low quiescent current, low noise, high PSRR, fast start-up LDO linear regulator with excellent line and load transient response. The TLV700xxEVM-503 evaluation module (EVM) helps designers evaluate the operation and performance of the TLV700xx family.

8.2 Typical Application

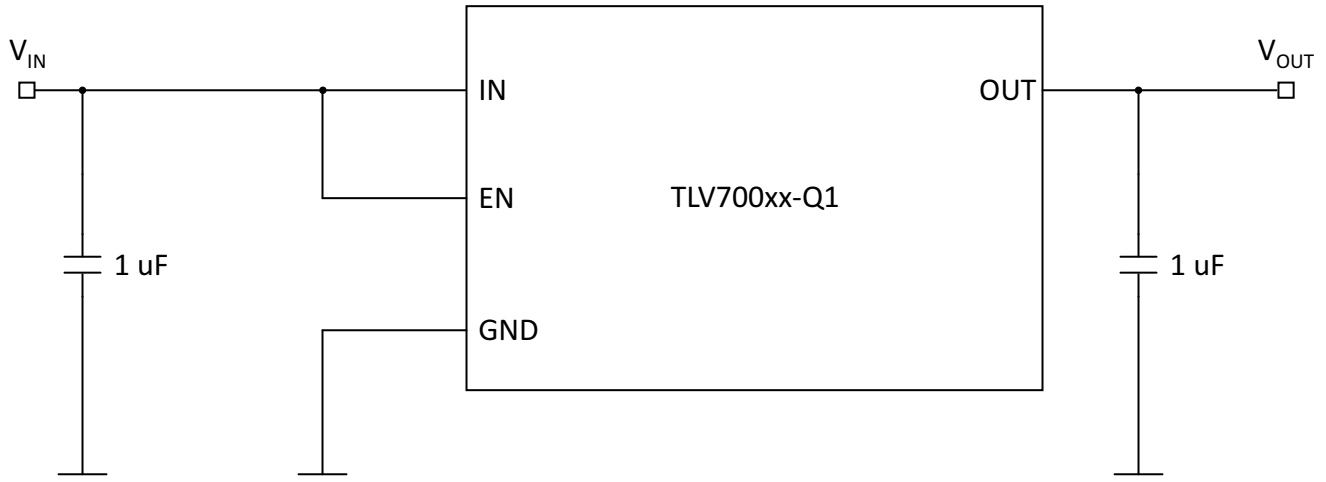


Figure 23. Simplified Schematic

8.2.1 Design Requirements

For this design example use, the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage Range	2 V to 5.5 V
Output Voltage	1.2 V, 2.5 V, 2.8 V, 3.0 V, 3.2 V, 3.3 V
Output Current Rating	200 mA
Effective Output Capacitor Range	>0.1 µF
Maximum Output Capacitor ESR Range	<200 mΩ

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

1.0-µF X5R- and X7R-type ceramic capacitors are recommended because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV70018-Q1 is designed to be stable with an *effective capacitance* of 0.1 µF or larger at the output. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of lower-cost dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller-footprint capacitors that have higher derating in size- and space-constrained applications.

NOTE

Using a 0.1-µF rated capacitor at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1.0-µF, low ESR capacitor across the IN pin and GND pin of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

8.2.2.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot or undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curve

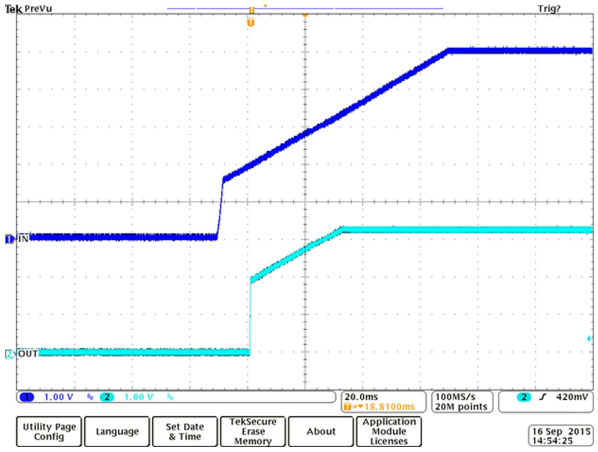


Figure 24. Power Up

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 2 V and 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, TI recommends adding a capacitor with a value of 0.1 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR performance.

10.2 Layout Example

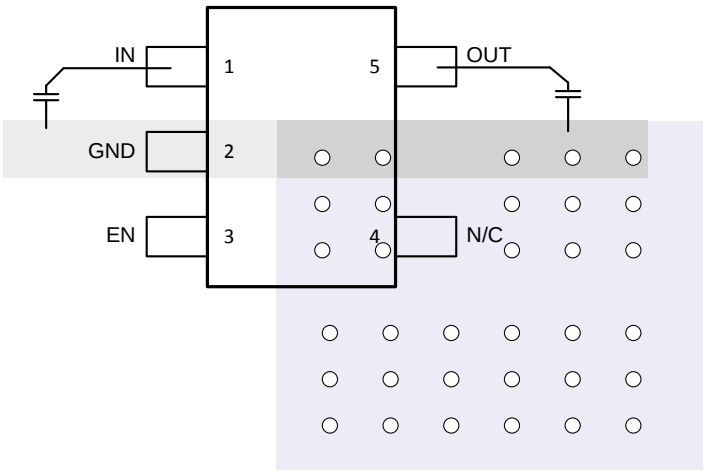


Figure 25. TLV700xx Layout Example

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum.

To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The internal protection circuitry of the TLV70018-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV70018-Q1 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Thermal performance data for TLV70018-Q1 were gathered using the TLV700 evaluation module (EVM), a 2-layer board with two ounces of copper per side. The dimensions and layout for the SOT23-5 (DBV) EVM are shown in and . Corresponding thermal performance data are given in *Thermal Information*. Note that this board has provision for soldering not only the SOT23-5 package on the bottom layer, but also the SC-70 package on the top layer. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power Dissipation (continued)

10.4.1 Thermal Calculations

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN}$$

where

- P_D is continuous power dissipation
- I_{OUT} is output current
- V_{IN} is input voltage
- V_{OUT} is output voltage

(1)

Since I_Q << I_{OUT}, the term $I_Q \times V_{IN}$ is always ignored.

For a device under operation at a given ambient air temperature (T_A), use Equation 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (Z_{\Theta JA} \times P_D)$$

where

- $Z_{\theta JA}$ is the junction-to-ambient air temperature thermal impedance

(2)

Use Equation 3 to calculate the rise in junction temperature due to power dissipation.

$$\Delta T = T_J - T_A = (Z_{\Theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature ($T_{J(MAX)}$, use Equation 4 to calculate the maximum ambient air temperature ($T_{A(MAX)}$ at which the device can operate.

$$T_{Amax} = T_{Jmax} - (Z_{\Theta JA} \times P_D) \quad (4)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Package Mounting

Solder pad footprint recommendations for the TLV70018-Q1 are available from the Texas Instruments web site at www.ti.com.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

TLV700 evaluation module

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV70018-Q1	Click here	Click here	Click here	Click here	Click here
TLV70012-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG.
ZigBee is a registered trademark of ZigBee Alliance.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLV70012QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDO	Samples
TLV70018QDDCRQ1	ACTIVE	SOT	DDC	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

OTHER QUALIFIED VERSIONS OF TLV70012-Q1, TLV70018-Q1 :

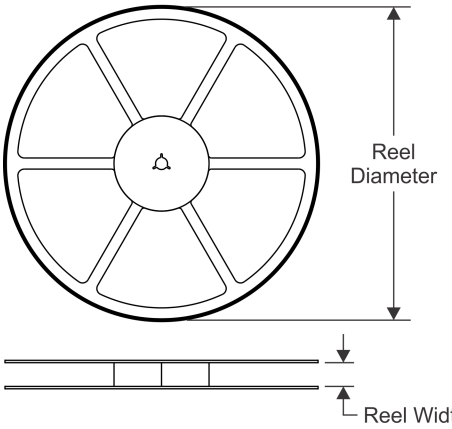
- Catalog: TLV70012, TLV70018

NOTE: Qualified Version Definitions:

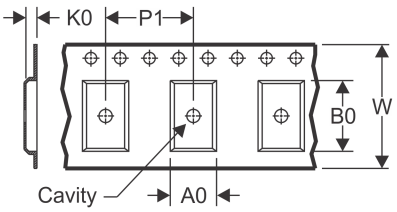
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

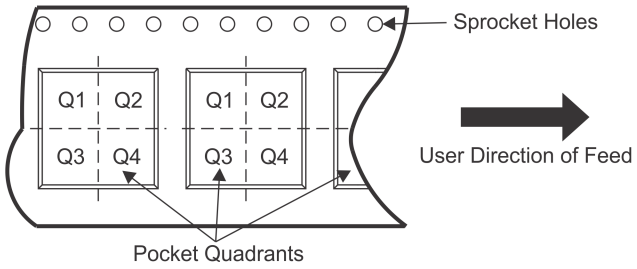


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

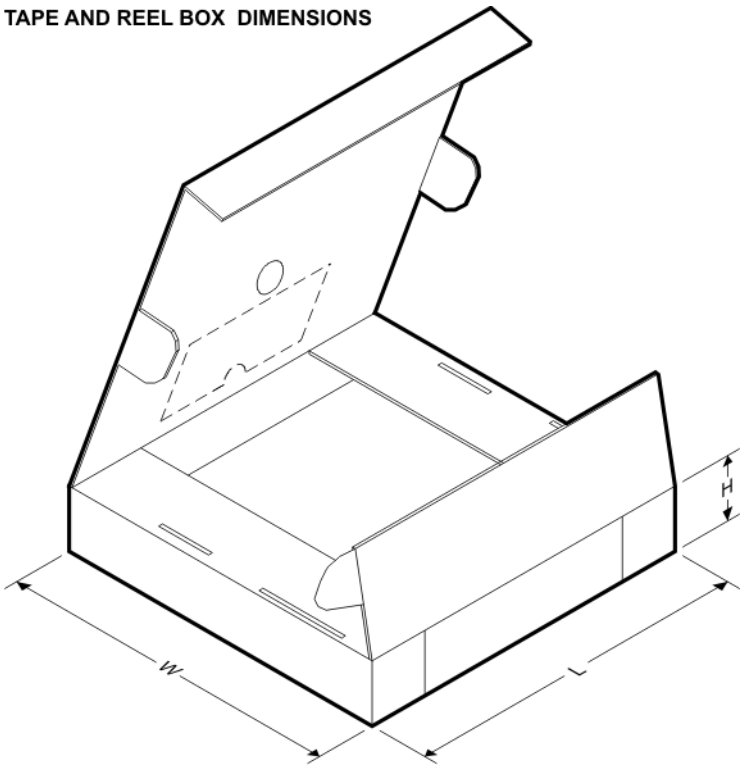
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV70012QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV70018QDDCRQ1	SOT	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

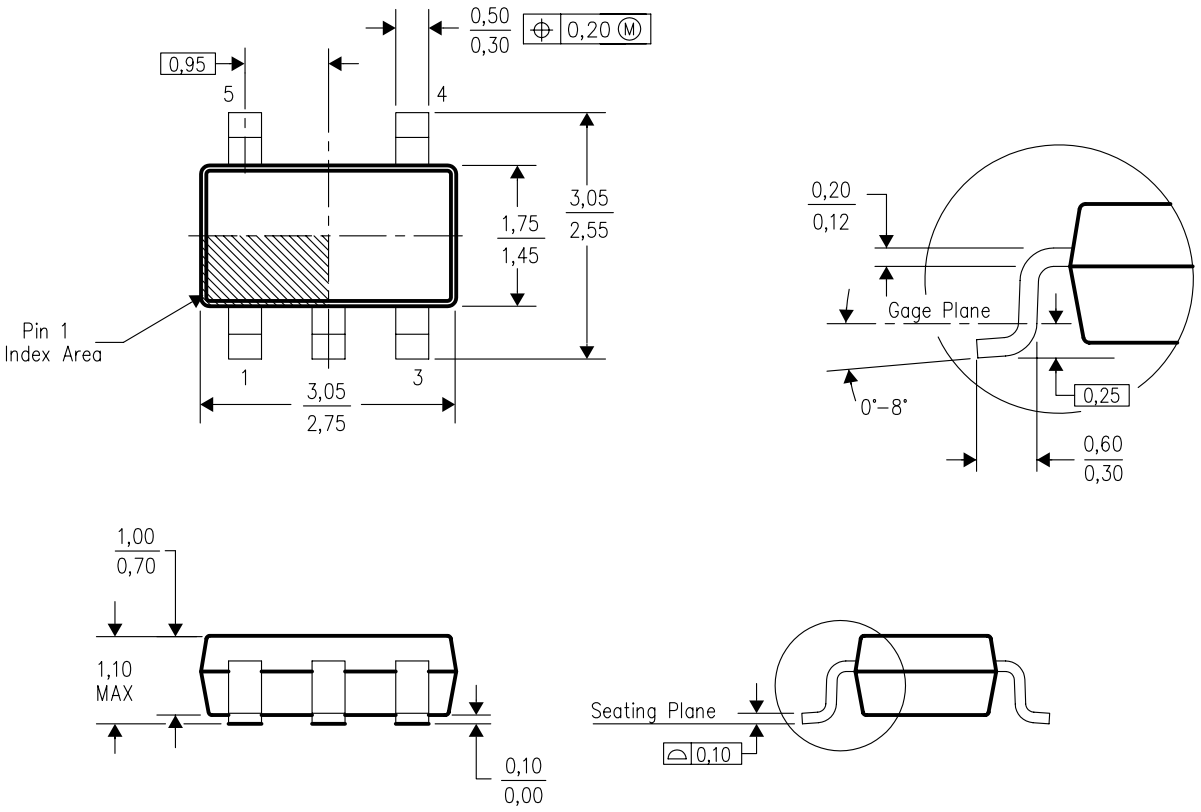
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV70012QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0
TLV70018QDDCRQ1	SOT	DDC	5	3000	195.0	200.0	45.0

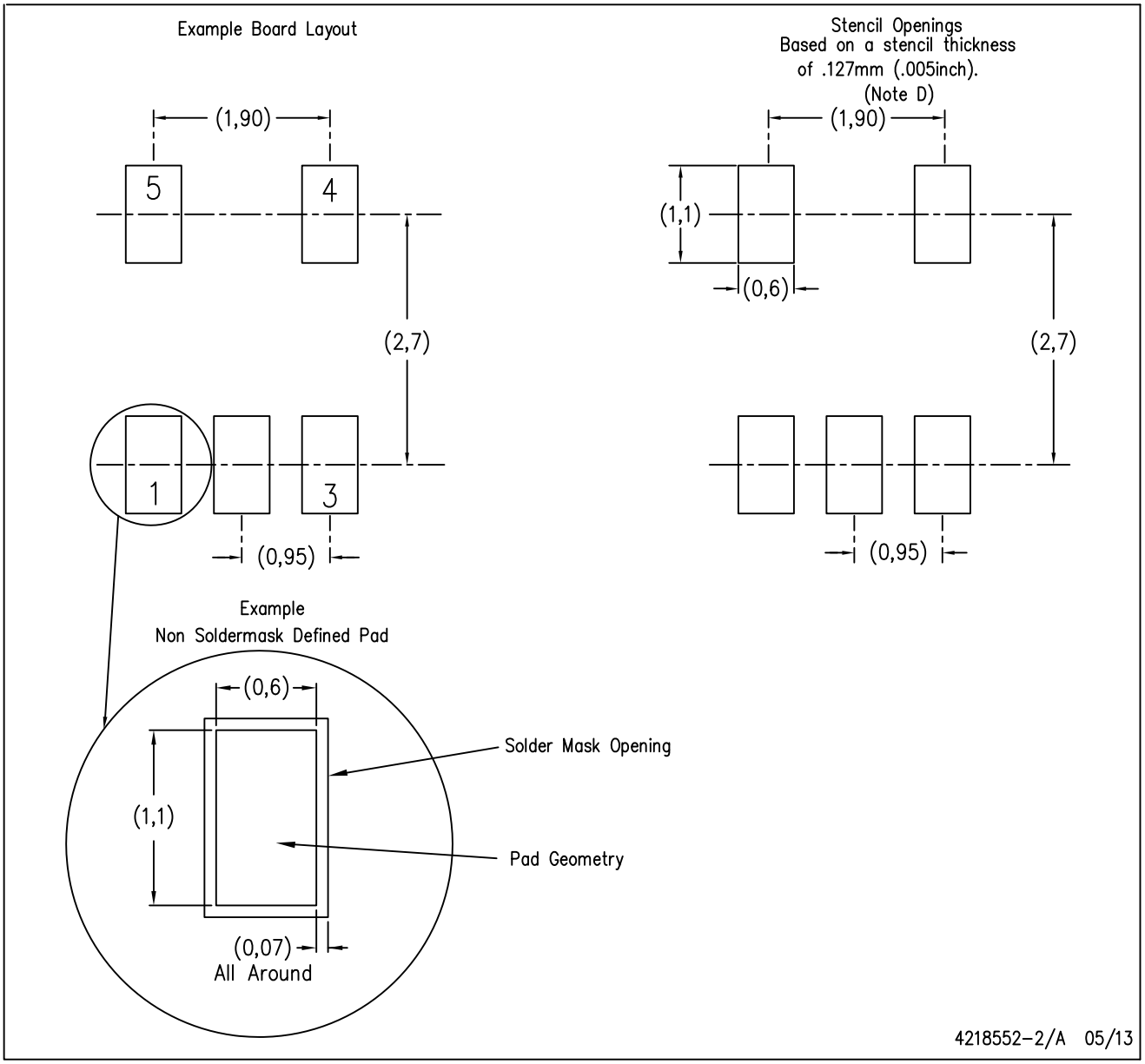
DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



4204403–2/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

DDC (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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