3-MHz 2-A Step-Down Converter in 2-mm x 2-mm SON Package

Check for Samples: TLV62065-Q1

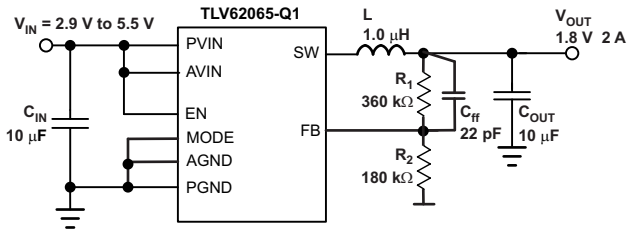
FEATURES

- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance With the Following Results:**
  - **Device Temperature Grade 2: –40°C to 105°C Ambient Operating Temperature Range**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C3B**
- **V_{IN} Range from 2.9 V to 5.5 V**
- **Up to 97% Efficiency**
- **Power-Save Mode / - MHz Fixed PWM Mode**
- **Output Voltage Accuracy in PWM Mode ±2.0%**
- **Output Capacitor Discharge Function**
- **Typical 18-µA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **For Improved Feature Set See TPS62065**
- **Available in a 2-mm × 2-mm × 0.75-mm SON**

APPLICATIONS

- **Point of Load (POL)**
- **Notebooks, Pocket PCs**
- **Portable Media Players**
- **Set Top Box**

TYPICAL APPLICATION CIRCUIT



DESCRIPTION

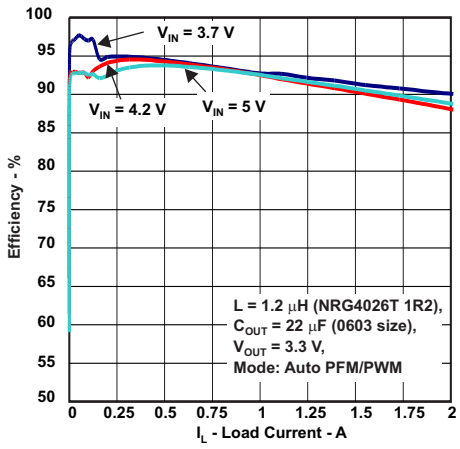
The TLV62065-Q1 is a highly efficient, synchronous step-down, dc-dc converter with a 1.2-V fixed output voltage.. It provides up to 2 A of output current.

With an input voltage range of 2.9 V to 5.5 V, the device is a perfect fit for power conversion from a 5-V or 3.3-V system supply rail. The TLV62065-Q1 operates at 3-MHz fixed frequency and enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. For low-noise applications, the TLV62065-Q1 can be forced into fixed-frequency PWM mode by pulling the MODE pin high.

In the shutdown mode, the current consumption is reduced to less than 1 µA and an internal circuit discharges the output capacitor.

The TLV62065-Q1 operates with a 1-µH inductor and 10-µF output capacitor.

The TLV62065-Q1 is available in a small 2-mm × 2-mm × 0.75-mm 8-pin SON package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	WSON -DSG	Reel of 3000	TLV62065TDSGRQ1	SCD

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range (2)	AVIN, PVIN	–0.3	7	V
	EN, MODE, FB	–0.3 to	V_{IN} + 0.3 < 7	
	SW	–0.3	7	
Current (source)	Peak output	Internally limited		A
ESD rating	Human-body model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged-device model (CDM) AEC-Q100 Classification Level C3B		750	V
Temperature	T_J	–40	140	°C
	T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

THERMAL INFORMATION

THERMAL METRIC		TLV62065-Q1 DSG 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	92.2	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	70.4	
θ_{JB}	Junction-to-board thermal resistance	46.6	
ψ_{JT}	Junction-to-top characterization parameter	1.7	
ψ_{JB}	Junction-to-board characterization parameter	46.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	39.7	

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		5.5	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		V_{IN}	V
L	Effective inductance range	0.7	1	1.6	µH
C_{OUT}	Effective output-capacitance range	4.5	10	22	µF
T_A	Operating ambient temperature (1)	–40		105	°C
T_J	Operating junction temperature	–40		140	°C

(1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application (PD(max)), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$

ELECTRICAL CHARACTERISTICS

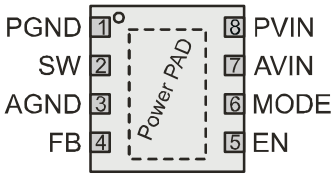
Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH, see the parameter measurement information.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		5.5	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and not device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN combined		0.1	5	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High-level input voltage	2.9 V ≤ V_{IN} ≤ 5.5 V	1		5.5	V
V_{IL}	Low-level input voltage	2.9 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
I_{IN}	Input bias current	EN, MODE tied to GND or AVIN		0.01	1	µA
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		120	**180**	mΩ
		V_{IN} = 5 V (1)		95	**150**	
$r_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V (1)		90	**130**	mΩ
		V_{IN} = 5 V (1)		75	**100**	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	3 V ≤ V_{IN} ≤ 3.6 V	2300	2750		mA
T_{SD}	Thermal shutdown	Increasing junction temperature		**150**		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 5.5 V	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage, PWM mode	PWM operation, MODE = V_{IN} , 2.9 V ≤ V_{IN} ≤ 5.5 V, 0-mA load	–2.0	0	2.0	%
$V_{FB(PFM)}$	Feedback voltage, PFM mode, voltage positioning	Device in PFM mode, voltage positioning active (2)		1		
V_{FB}	Load regulation			-0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9 V ≤ V_{IN}≤ 5.5 V, 0.8 V ≤ V_{OUT}≤ 3.6 V		200		Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(1) Maximum value applies for T_J = 85°C.
(2) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.

PIN ASSIGNMENTS

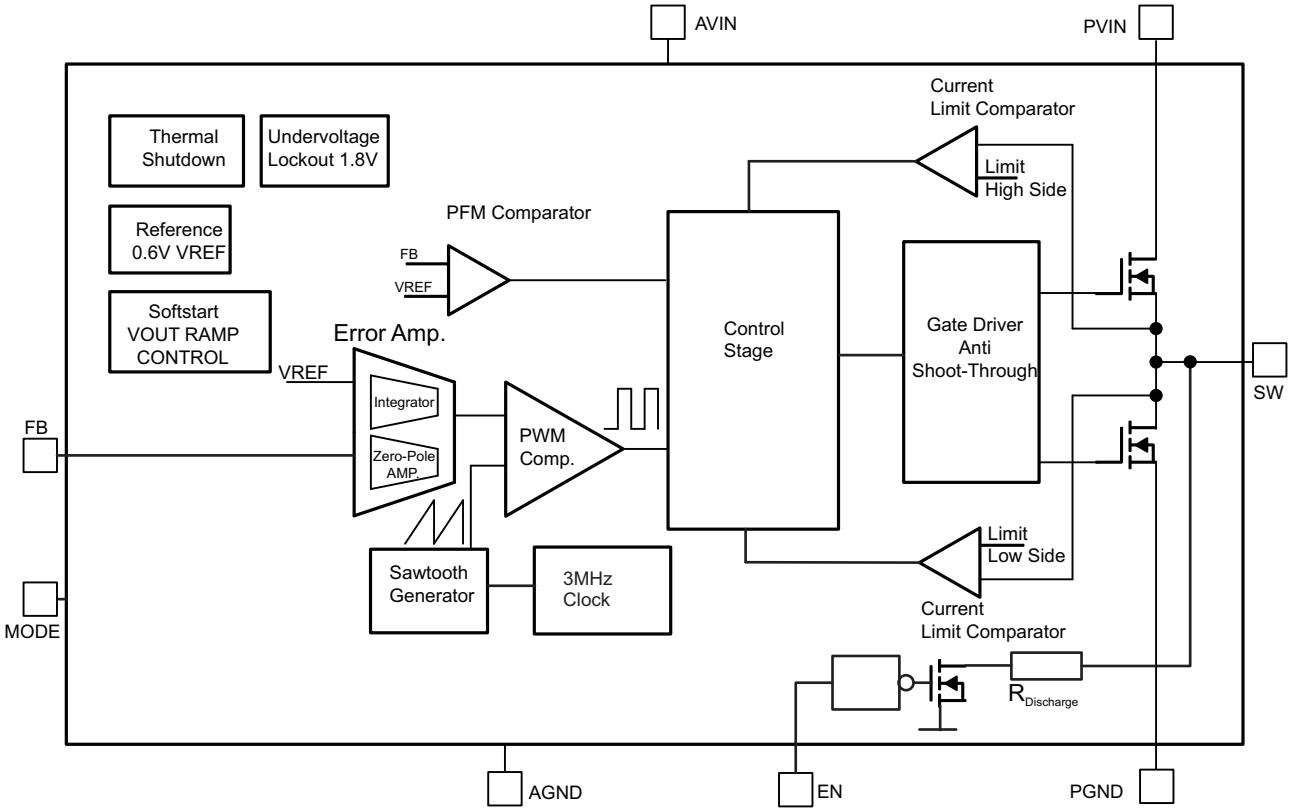
DSG PACKAGE
(TOP VIEW)



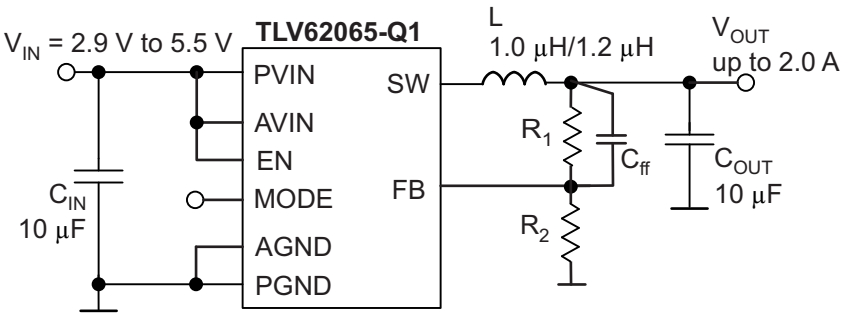
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	3	IN	Analog GND supply pin for the control circuit.
AV_{IN}	7	IN	Analog V_{IN} power supply for the control circuit. Must be connected to PVIN and input capacitor.
EN	5	IN	This is the enable pin of the device. Pulling this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must be terminated.
FB	4	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In the case of fixed output voltage option, connect this pin directly to the output capacitor.
MODE	6	IN	MODE pin = high forces the device to operate in fixed-frequency PWM mode. MODE pin = low enables the power-save mode with automatic transition from PFM mode to fixed-frequency PWM mode. This pin must be terminated.
PGND	1	PWR	GND supply pin for the output stage
PV_{IN}	8	PWR	V_{IN} power-supply pin for the output stage
SW	2	OUT	This is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
Thermal pad	–	–	For good thermal performance, this pad must be soldered to the land pattern on the PCB. This pad should be used as device GND.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



L: LQH44PN1R0NP0, L = 1.0 µH,Murata,
NRG4026T1R2, L = 1.2 µH, Taiyo Yuden
C_{IN}/C_{OUT}: GRM188R60J106U, Murata 0603 size

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

			FIGURE
η	Efficiency	Load Current, V_{OUT} = 1.2 V, Auto PF//PWM Mode, Linear Scale	Figure 1
		Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode, Linear Scale	Figure 2
		Load Current, V_{OUT} = 3.3 V, PFM/PWM Mode, Linear Scale	Figure 3
		Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale	Figure 4
	Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM/PWM Mode	Figure 5
		Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	Figure 6
	Shutdown Current	Input Voltage and Ambient Temperature	Figure 7
	Quiescent Current	Input Voltage	Figure 8
	Oscillator Frequency	Input Voltage	Figure 9
	Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	Figure 10
		Input Voltage, High-Side Switch	Figure 11
	$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	Figure 12
	Typical Operation	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 500 mA, L = 1.2 µH, C_{OUT} = 10µF	Figure 13
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 20 mA, L = 1.2 µH, C_{OUT} = 10µF	Figure 14
	Load Transient	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 0.2 mA to 1 A	Figure 15
		PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 20 mA to 250 mA	Figure 16
		V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 200 mA to 1500 mA	Figure 17
	Line Transient	PWM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 18
		PFM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	Figure 19
	Startup into Load	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Load = 2.2-Ω	Figure 20
	Output Discharge	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, No Load	Figure 21

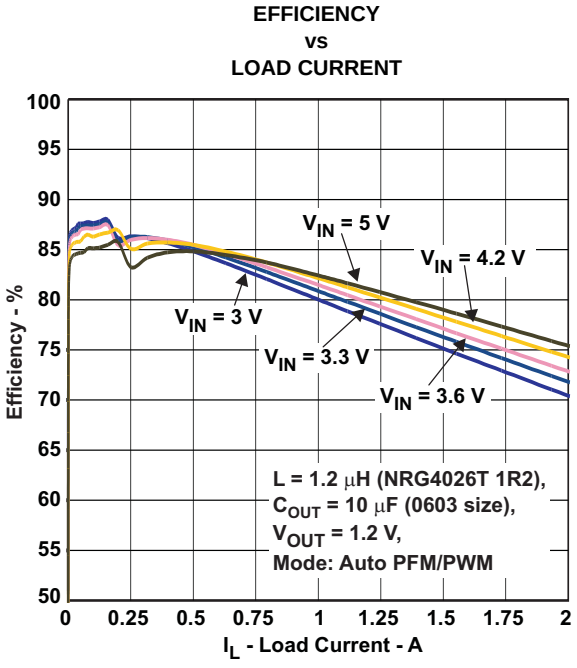


Figure 1. V_{OUT} = 1.2V, Auto PFM/PWM Mode, Linear Scale

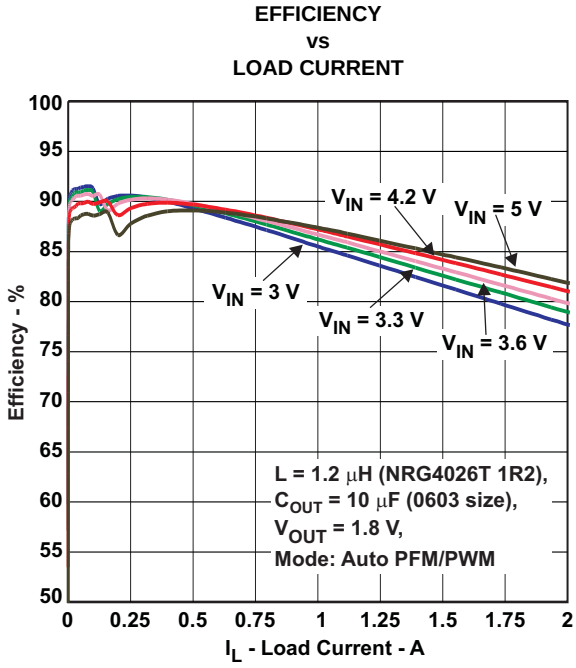


Figure 2. V_{OUT} = 1.8V, Auto PFM/PWM Mode, Linear Scale

EFFICIENCY
vs
LOAD CURRENT

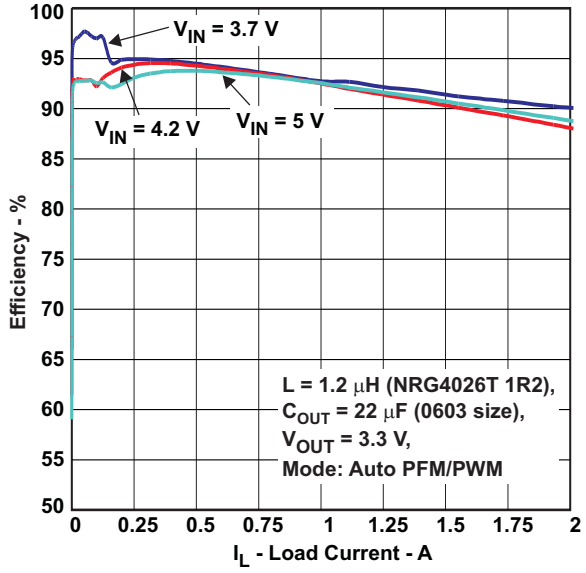


Figure 3. V_{OUT} = 3.3V, Auto PFM/PWM Mode, Linear Scale

EFFICIENCY
vs
LOAD CURRENT

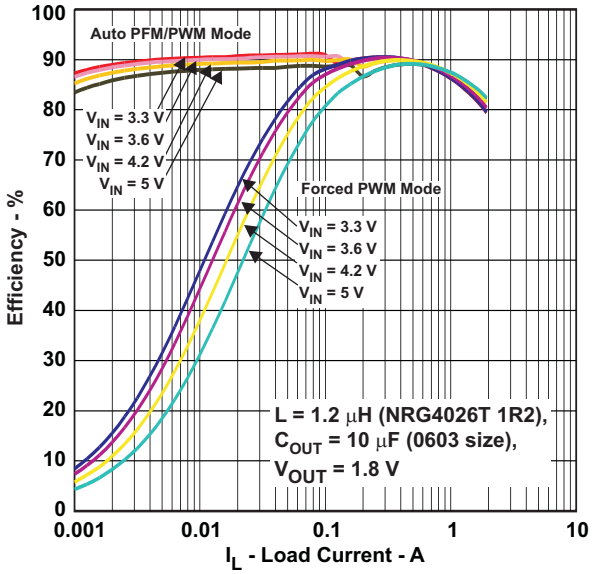


Figure 4. Auto PFM/PWM Mode vs. Forced PWM Mode, Logarithmic Scale

OUTPUT VOLTAGE ACCURACY
vs
LOAD CURRENT

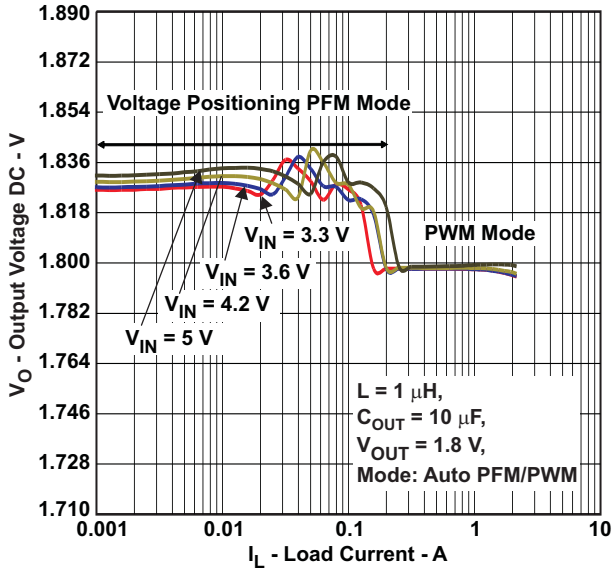


Figure 5. Auto PFM/PWM Mode

OUTPUT VOLTAGE ACCURACY
vs
LOAD CURRENT

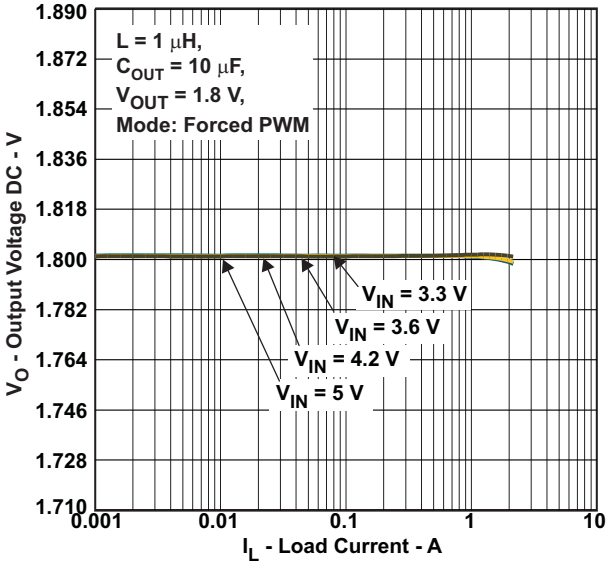


Figure 6. Forced PWM Mode

SHUTDOWN CURRENT vs INPUT VOLTAGE AND AMBIENT TEMPERATURE

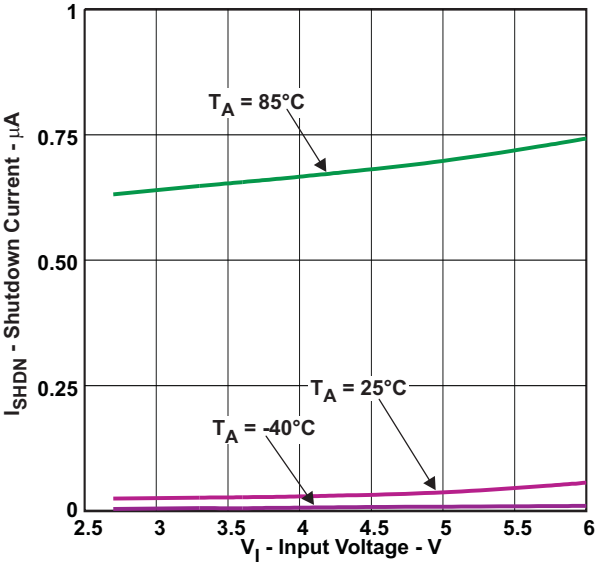


Figure 7.

QUIESCENT CURRENT vs INPUT VOLTAGE

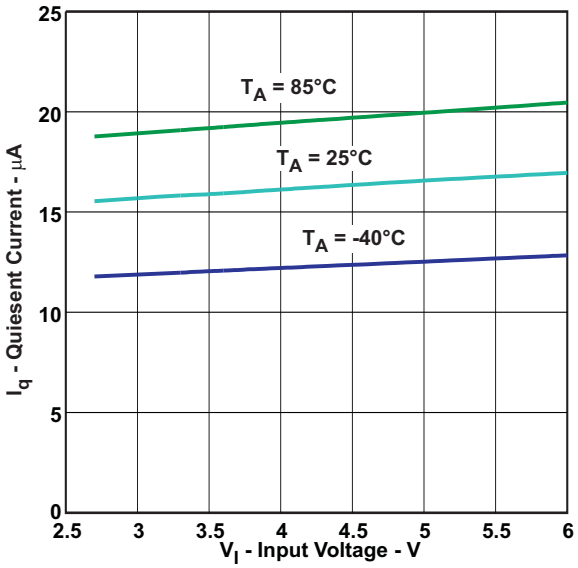


Figure 8.

OSCILLATOR FREQUENCY vs INPUT VOLTAGE

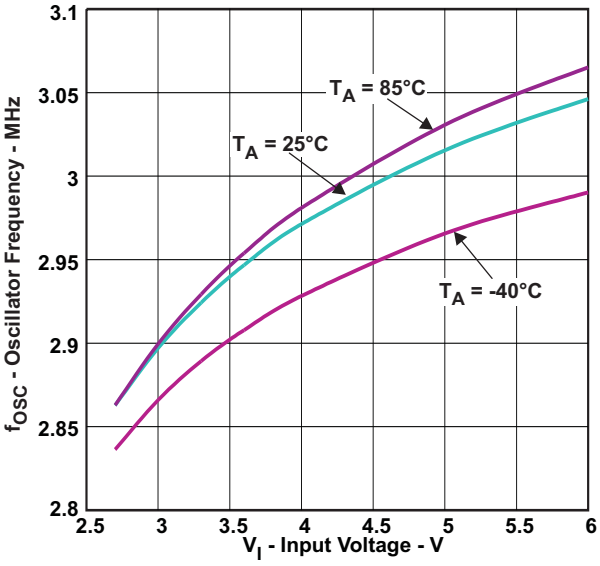


Figure 9.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs INPUT VOLTAGE

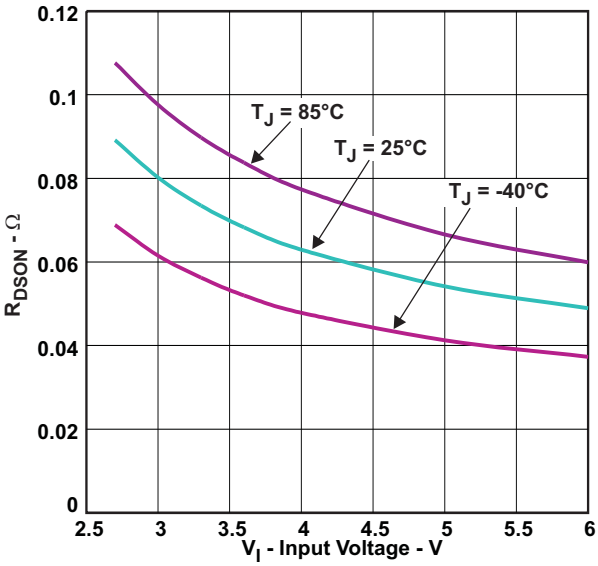


Figure 10. Low-Side Switch

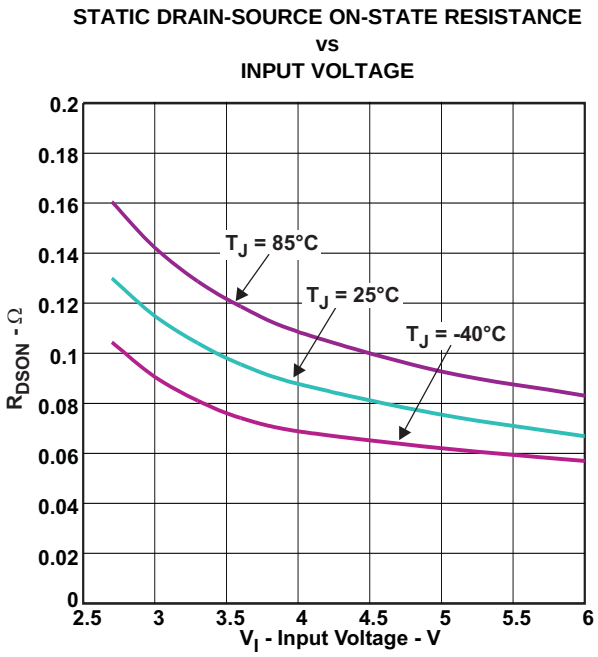


Figure 11. High-Side Switch

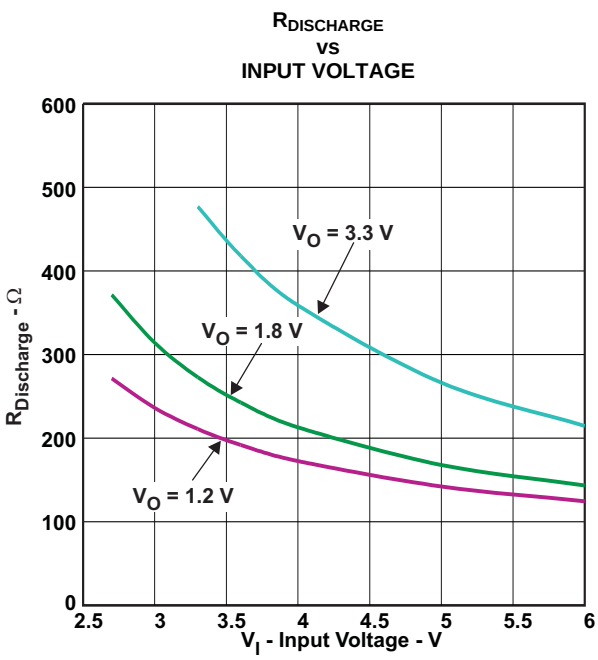


Figure 12.

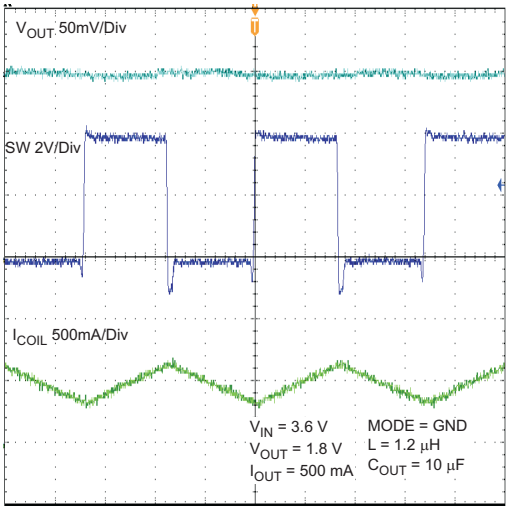


Figure 13. Typical Operation (PWM Mode)

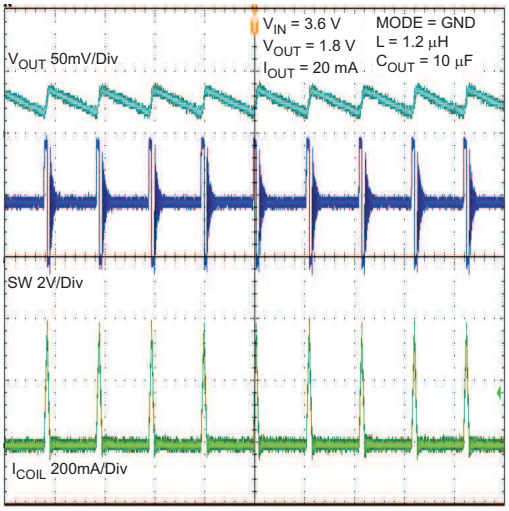


Figure 14. Typical Operation (PFM Mode)

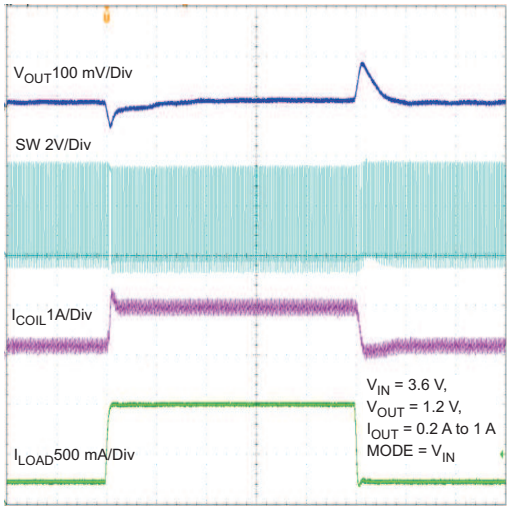


Figure 15. Load Transient Response PWM Mode 0.2A To 1A

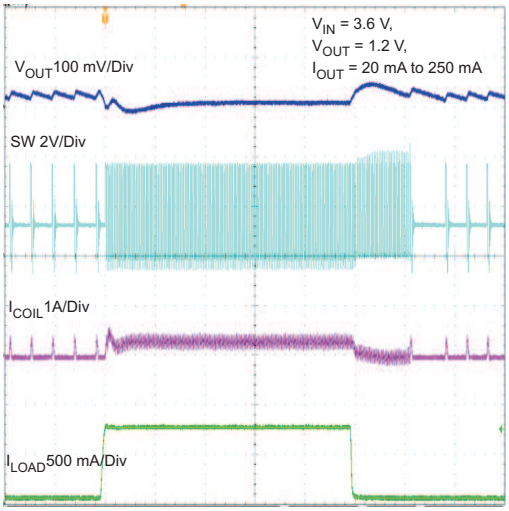


Figure 16. Load Transient PFM Mode 20 mA to 250mA

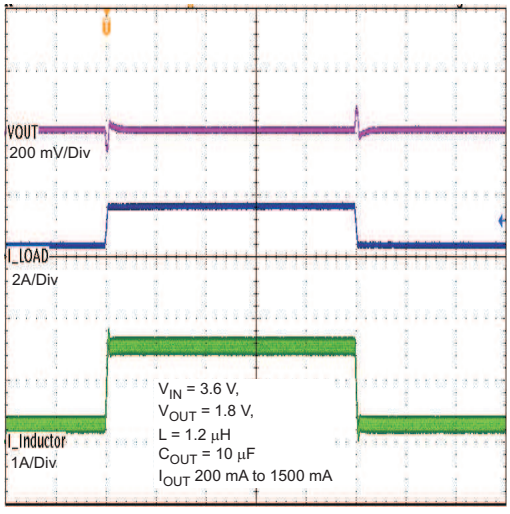


Figure 17. Load Transient Response 200 mA To 1500 mA

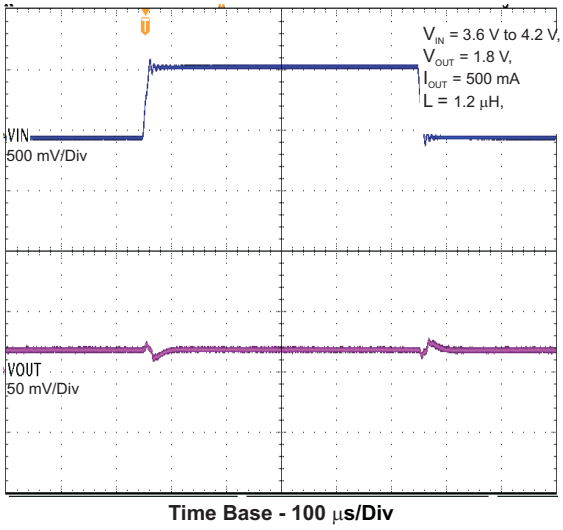


Figure 18. Line Transient Response PWM Mode

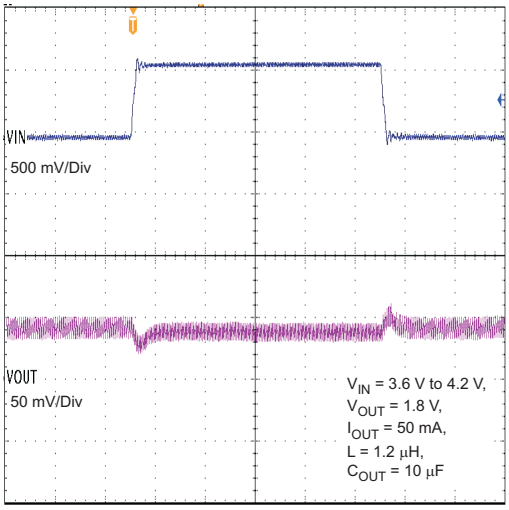


Figure 19. Line Transient PFM Mode

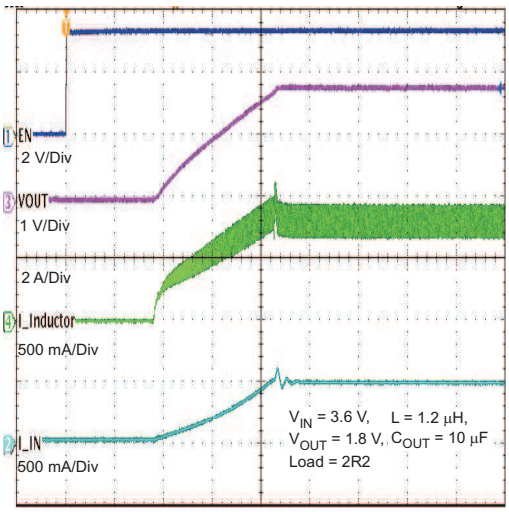


Figure 20. Start-Up Into Load – V_{OUT} 1.8 V

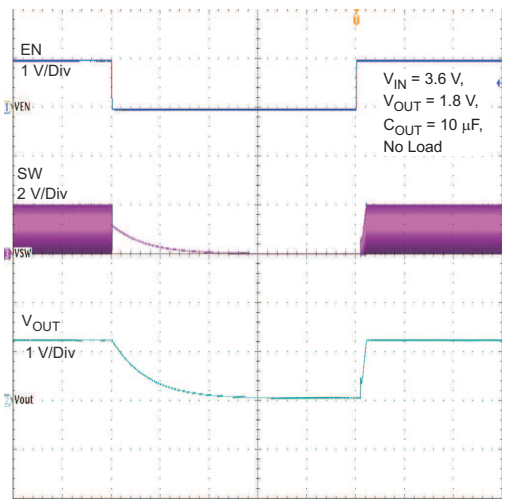


Figure 21. Output Discharge

DETAILED DESCRIPTION

OPERATION

The TLV62065-Q1 step-down converter operates with typically 3-MHz fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power-save mode, and operates then in pulse-frequency mode (PFM).

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input voltage feed-forward to achieve good line and load regulation, allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows now from the input capacitor via the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator also turns off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

POWER SAVE MODE

Pulling the TLV62065-Q1 MODE pin low enables power-save mode. If the load current decreases, the converter enters power-save mode operation automatically. In power-save mode, the converter skips switching and operates with reduced frequency in the PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage typically 1% above the nominal output voltage. This voltage-positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

In power-save mode, a PFM comparator monitors the output voltage. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ + 1%, the device starts a PFM current pulse. For this, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current, the output voltage rises. If the output voltage is equal to or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typ. 18-µA current consumption.

In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold due to the load current.

The PFM mode is exited and PWM mode entered in case the output current can no longer be supported in PFM mode.

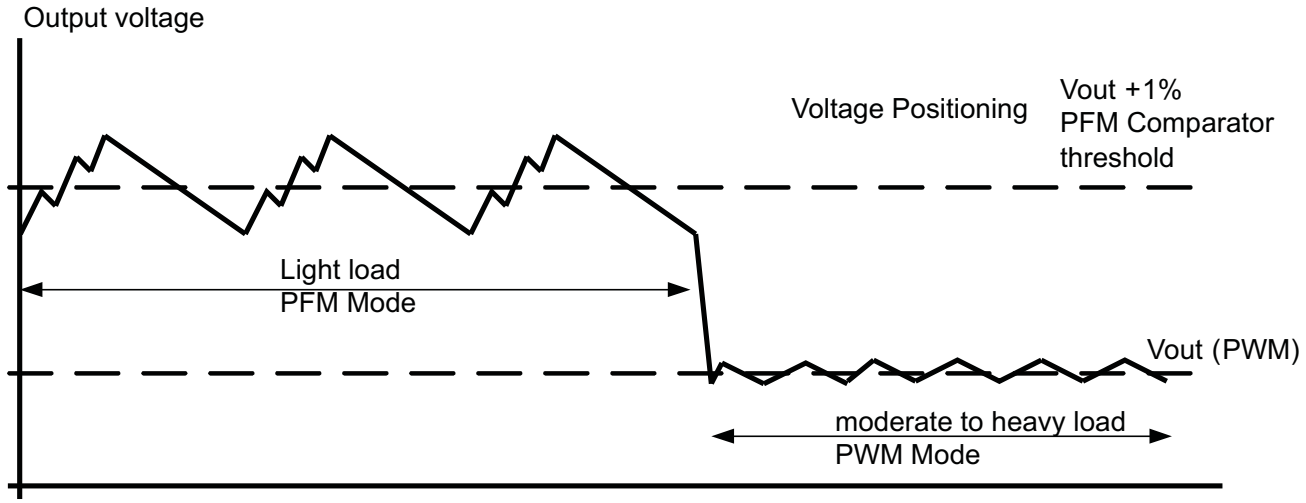


Figure 22. Power Save Mode Operation with automatic Mode transition

100% Duty Cycle Low-Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

With further decreasing VIN, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage differential. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_O max + I_O max \times (R_{DS(on)} max + R_L)$$

With:

$I_O$max = maximum output current

$R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$.

R_L = DC resistance of the inductor

$V_O$max = nominal output voltage plus maximum output voltage tolerance

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling VIN trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 1.78 V. The device starts operation once the rising V_{IN} trips the undervoltage lockout threshold V_{UVLO} again at typically 1.95 V.

Output Capacitor Discharge

With EN = GND, the device enters shutdown mode and disables all internal circuits. An internal resistor connects the SW pin is to PGND to discharge the output capacitor. This feature ensures start-up with a discharged output capacitor once the converter is enabled again and prevents *floating* charge on the output capacitor. The output voltage ramps up monotonic, starting from 0 V.

MODE SELECTION

The MODE pin allows mode selection between forced PWM mode and power-save mode.

Connecting this pin to GND enables the power-save mode with automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed-frequency PWM mode even at light load currents. This allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

ENABLE

The device is enabled by setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches 95% of its nominal value within t_{START} of typically 500 µs after the device has been enabled. The EN input can be used to control power sequencing in a system with various dc-dc converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and get a sequencing of supply rails. With EN = GND, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND via an internal resistor to discharge the output.

SOFT START

The TLV62065-Q1 has an internal soft-start circuit that controls the ramp-up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold, V_{UVLO}, the output voltage ramps up from 5% to 95% of its nominal value within t_{Ramp} of typ. 250 µs.

This limits the inrush current in the converter during start-up and prevents possible input-voltage drops when a battery or high-impedance power source is used.

During soft start, the switch current limit is reduced to 1/3 of its nominal value, I_{LIMF}, until the output voltage reaches 1/3 of its nominal value. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMF}.

INTERNAL CURRENT LIMIT / FOLD-BACK CURRENT LIMIT FOR SHORT-CIRCUIT PROTECTION

During normal operation, the high-side and low-side MOSFET switches are protected by their current limits, I_{LIMF}. Once the high-side MOSFET switch reaches its current limit, it is turned off and the low-side MOSFET switch is turned on. The high-side MOSFET switch can only turn on again once the current in the low-side MOSFET switch decreases below its current limit, I_{LIMF}. The device is capable of providing peak inductor currents up to its internal current limit $_{ILIMF.}$.

As soon as the switch-current limits are hit and the output voltage falls below 1/3 of the nominal output voltage due to an overload or short-circuit condition, the foldback current limit is enabled. In this case, the switch-current limit is reduced to 1/3 of the nominal value, I_{LIMF}.

Because the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of its nominal current limit, I_{LIMF}, until the output voltage exceeds 1/3 of the nominal output voltage. This must be considered when a load which acts as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds 150°C (typical) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues its operation with a soft start once the junction temperature falls below the thermal shutdown hysteresis.

APPLICATION INFORMATION

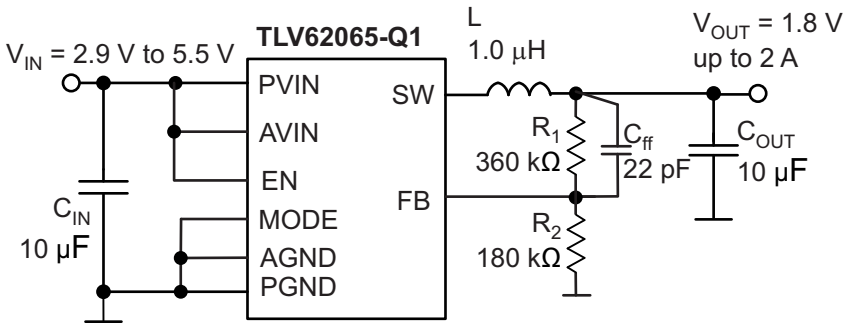


Figure 23. TLV62065-Q1 1.8V Adjustable Output Voltage Configuration

OUTPUT VOLTAGE SETTING

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

with an internal reference voltage V_{REF} typically 0.6 V.

To minimize the current through the feedback divider network, R_2 should be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 should not exceed approximately 1 MΩ, to keep the network robust against noise. An external feed-forward capacitor C_{ff} is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} place a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_c = \frac{1}{2 \times \pi \times R_2 \times C_{ff}} = 35\text{kHz}$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_2 \times 35\text{kHz}}$$

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The internal compensation network of TLV62065-Q1 is optimized for an LC output filter with a corner frequency of:

$$f_c = \frac{1}{2 \times \pi \times \sqrt{(1\mu H \times 10\mu F)}} = 50kHz$$

The part operates with nominal inductors of 1 µH to 1.2 µH and with 10 µF to 22 µF small X5R and X7R ceramic capacitors. See the lists of inductors and capacitors. The part is optimized for a 1-µH inductor and 10-µF output capacitor.

Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor must be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

Equation 1 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transients the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where:

f = Switching frequency (3 MHz typical)
L = Inductor value
ΔI_L = Peak-to-peak inductor ripple current
I_{Lmax} = Maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch-current limit $I_{LIMF}$of the converter.

The total losses of the coil have a strong impact on the efficiency of the dc-dc conversion and consist of both the losses in the dc resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

Table 2. List of Inductors

DIMENSIONS [mm]	INDUCTANCE µH	INDUCTOR TYPE	SUPPLIER
3.2 × 2.5 × 1 max.	1	LQM32PN (MLCC)	Murata
3.7 × 4 × 1.8 max.	1	LQH44 (wire wound)	Murata
4 × 4 × 2.6 max.	1.2	NRG4026T (wire wound)	Taiyo Yuden
3.5 × 3.7 × 1.8 max.	1.2	DE3518 (wire wound)	TOKO

Output Capacitor Selection

The advanced fast-response voltage-mode control scheme of the TLV62065-Q1 allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output-voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V- and Z5U-dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and may not be used. For most applications, a nominal 10-µF or 22-µF capacitor is suitable. In small ceramic capacitors, the dc-bias effect decreases the effective capacitance. Therefore a 22-µF capacitor can be used for output voltages higher than 2 V; see the list of capacitors, Table 3.

In case additional ceramic capacitors in the supplied system are connected to the output of the dc-dc converter, the output capacitor C_{OUT} must be decreased in order not to exceed the recommended effective capacitance range. In this case, a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (3)$$

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low-ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. For most applications a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability, or could even damage the part by exceeding the maximum ratings.

Table 3. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm]	SUPPLIER
10 µF	GRM188R60J106M	0603: 1.6 × 0.8 × 0.8	Murata
22 µF	GRM188R60G226M	0603: 1.6 × 0.8 × 0.8	Murata
22 µF	CL10A226MQ8NRNC	0603: 1.6 × 0.8 × 0.8	Samsung
10 µF	CL10A106MQ8NRNC	0603: 1.6 × 0.8 × 0.8	Samsung

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter, or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or wrong L-C output filter combinations. As a next step in the evaluation of the regulation loop, the transient response of the load is tested. During the time between the application of the load transient and the turnon of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta_{I(LOAD)}$ × ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta_{I(LOAD)}$ begins to charge or discharge C_O, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode at medium-to-high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

LAYOUT CONSIDERATIONS

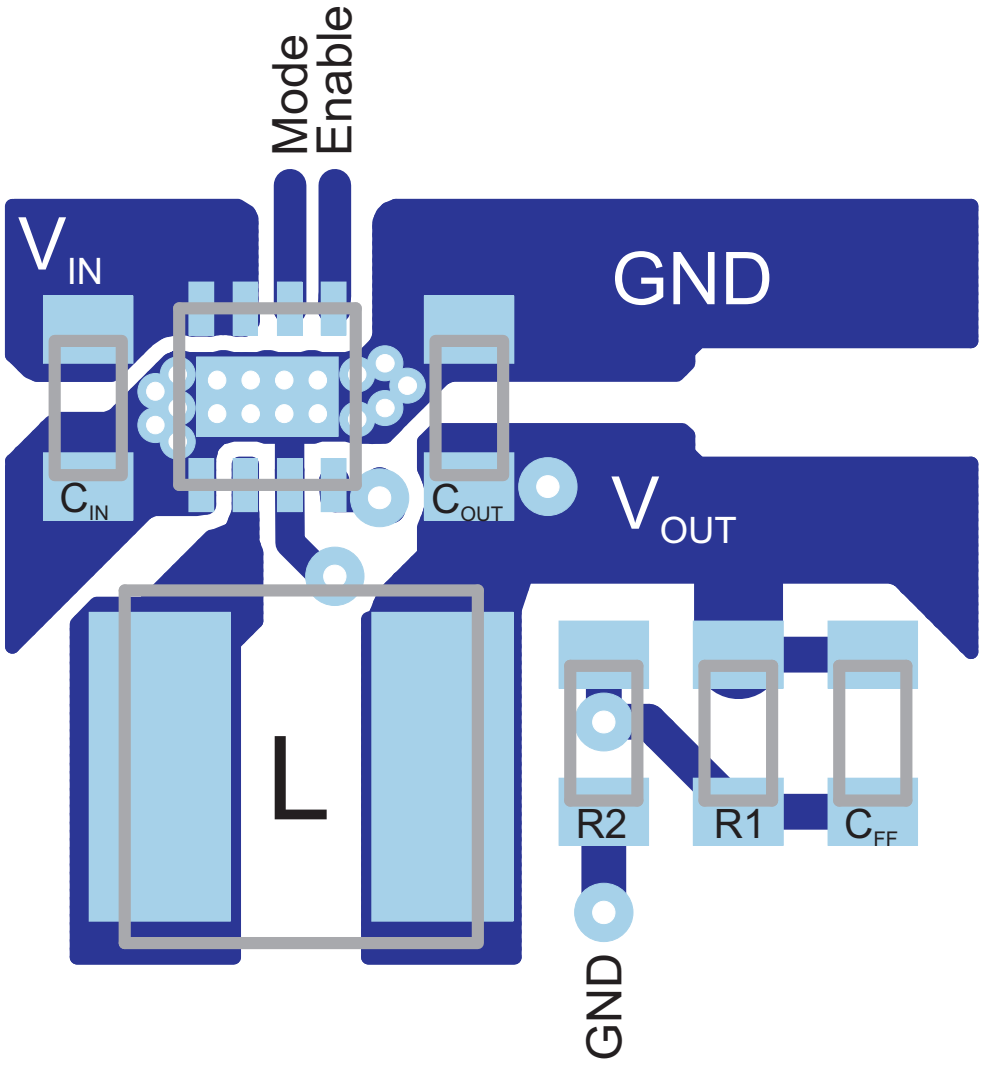


Figure 24. PCB Layout

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues, as well as EMI and thermal problems. It is critical to provide a low-inductance, low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitor as well as the inductor and output capacitor should be placed as close as possible to the IC pins.

Connect the AGND and PGND pins of the device to the PowerPAD™ land of the PCB and use this pad as a star point. Use a common power node (PGND), and a different node (AGND) for the signal, to minimize the effects of ground noise. The FB divider network should be connected directly to the output capacitor and the FB line must be routed away from noisy components and traces (for example, the SW line).

Due to the small package of this converter and the overall small solution size, the thermal performance of the PCB layout is important. For good thermal performance PCB design of at least four layers is recommended. The thermal pad of the IC must be soldered on the power pad area on the PCB to achieve proper thermal connection. Additionally, for good thermal performance, the thermal pad on the PCB must be connected to an inner GND plane with sufficient via connections. See the documentation of the evaluation kit.

Revision History

The following table summarizes the TLV62065-Q1 data sheet versions.

Note: Numbering may vary from previous versions.

Version	Literature Number	Date	Notes
*	SLVSB92	January 2011	See (1)
A	SLVSB92A	March 2012	See (2)

(1) TLV62065-Q1 Data Sheet, (SLVSB92) - Initial release.
(2) TLV62065-Q1 Data Sheet, (SLVSB92A):
  (a) - Update automotive qualitifcation description and add temperature grade
  (b) ABSOLUTE MAXIMUM RATINGS - Update Absolute Maximum Ratings
  (c) ELECTRICAL CHARACTERISTICS - Update Electrical Characteristics - Shutdown current max rating

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TLV62065TDSGRQ1	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF TLV62065-Q1 :

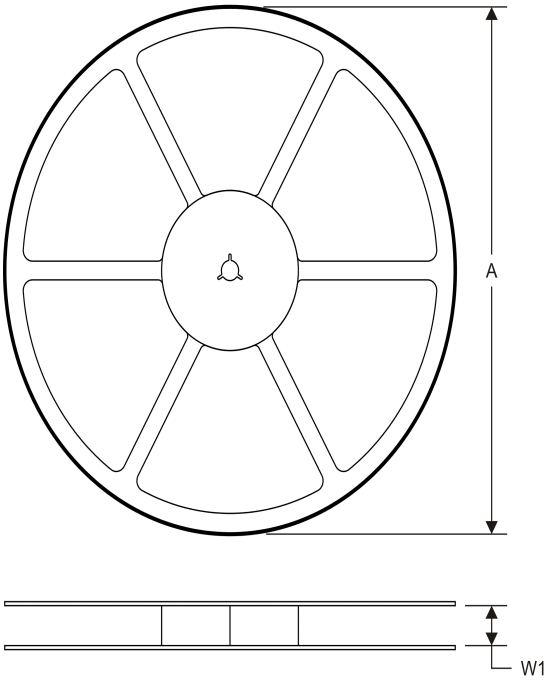
- Catalog: TLV62065

NOTE: Qualified Version Definitions:

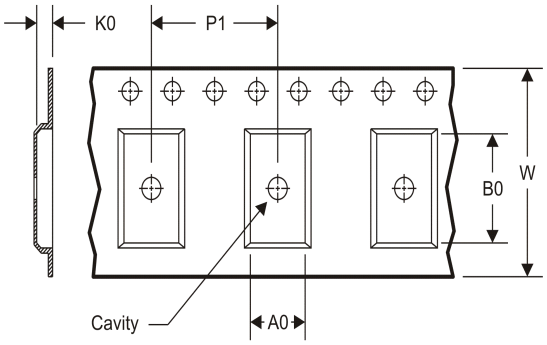
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



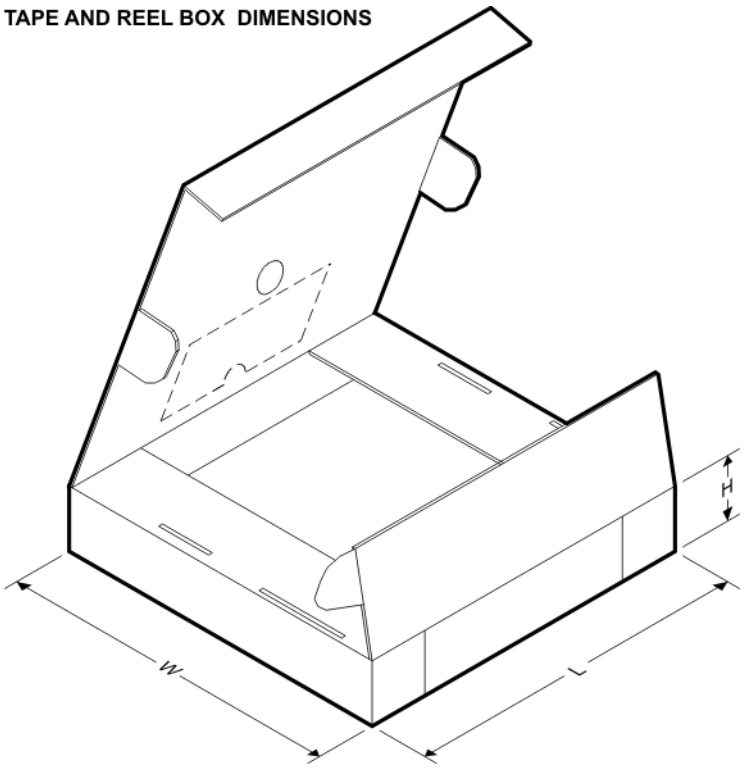
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV62065TDSGRQ1	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

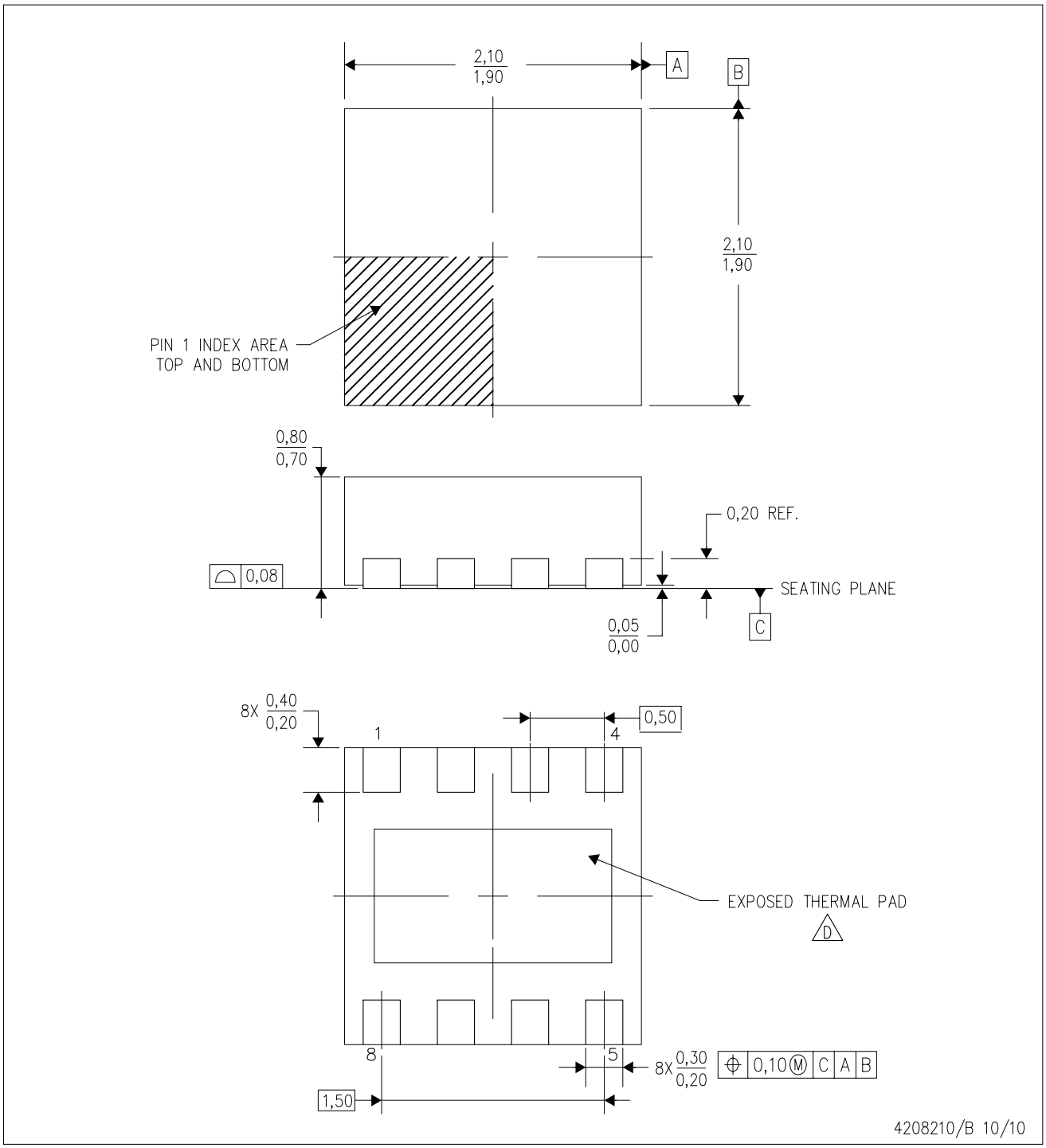
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV62065TDSGRQ1	WSON	DSG	8	3000	195.0	200.0	45.0

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

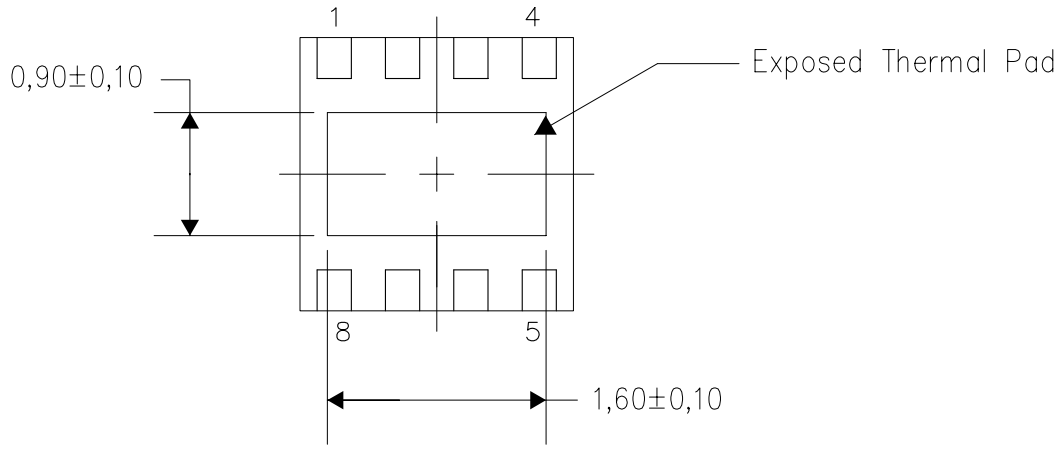
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



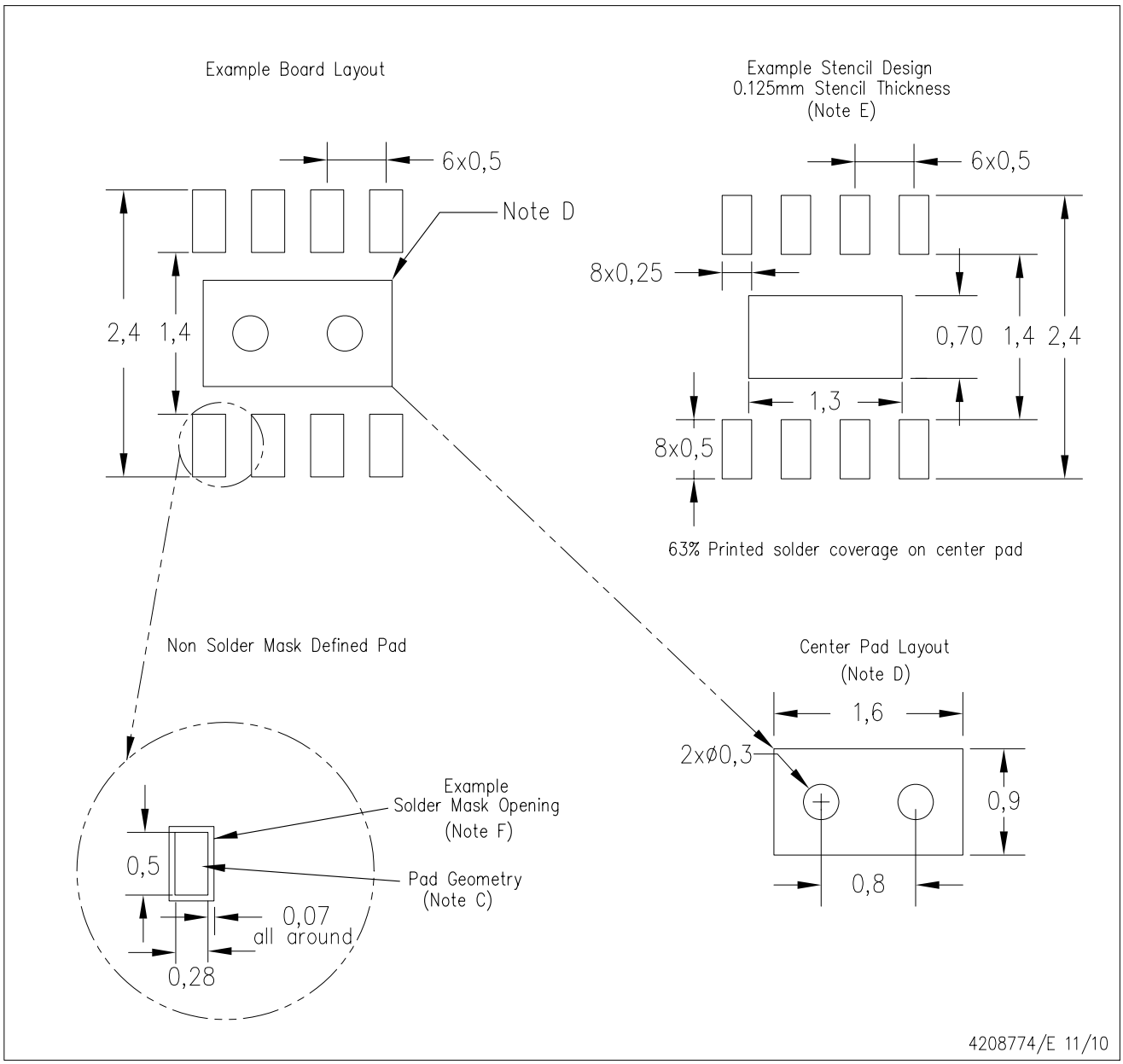
Bottom View

Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A. All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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