TLV27L2-Q1 Automotive Micropower Rail-to-Rail Output Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C6
- BiMOS Rail-to-Rail Output
- Input Bias Current: 1 pA
- High Wide Bandwidth 160 kHz
- High Slew Rate: 0.1 V/µs
- Supply Current: 7 µA (per channel)
- Input Noise Voltage: 89 nV/$\sqrt{\text{Hz}}$
- Supply Voltage Range: 2.7 V to 16 V

2 Applications

- Portable Medical
- Power Monitoring
- Low Power Security Detection Systems
- Smoke Detectors

3 Description

The TLV27L2-Q1 single-supply operational amplifiers provide rail-to-rail output capability. The TLV27L2-Q1 device takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range, while adding the rail-to-rail output swing feature. The TLV27L2-Q1 device also provides 160-kHz bandwidth from only 7 µA. The maximum recommended supply voltage is 16 V, which allows the devices to be operated from (±8-V supplies down to ±1.35 V) two rechargeable cells.

The rail-to-rail outputs make the TLV27L2-Q1 device good upgrades for the TLC27Lx family of devices which offers more bandwidth at a lower quiescent current. The TLV27L2-Q1 offset voltage is equal to that of the TLC27LxA variant. Their cost effectiveness makes them a good alternative to the TLC225x and TLV225x families of devices, where offset and noise are not of premium importance.

The TLV27L2-Q1 device is available in the commercial temperature range to enable easy migration from the equivalent TLC27Lx.

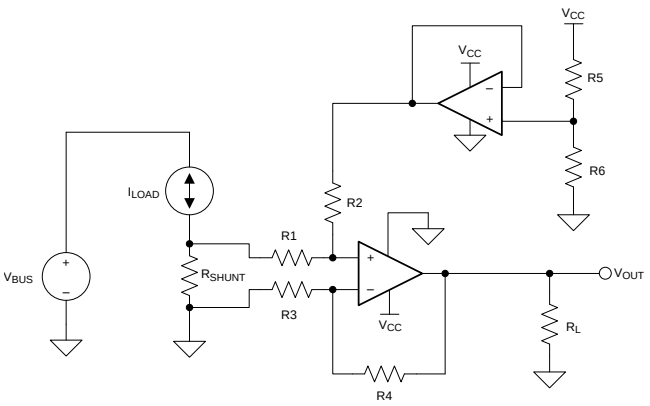
The TLV27L2-Q1 device is available in an 8-pin SOIC (D) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV27L2-Q1	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Schematic



Low and Stable Quiescent Current

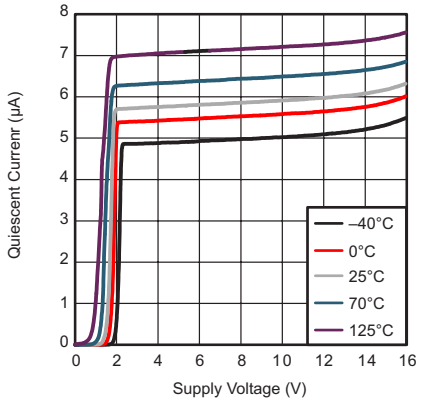


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2015) to Revision A	Page
• First public release of the data sheet.	1

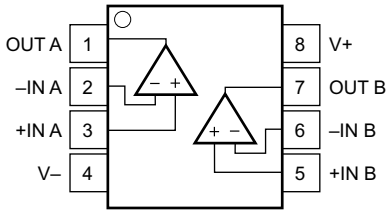
5 Selection Guide

All DC specifications are maximum values while AC specifications are typical values.

PART NUMBER	V_S (V)	I_Q/ch (µA)	V_{ICR} (V)	V_{IO} (mV)	I_{IB} (pA)	GBW (MHz)	SLEW RATE (V/µs)	Vn, 1 kHz (nV/√Hz)
TLV27L2-Q1	2.7 to 16	11	–0.2 to V_S + 1.2	5	60	0.18	0.06	89
OPAx348-Q1	2.1 to 5.5	65	–0.2 to V_S + 0.2	5	10	1	0.5	35
OPAx333-Q1	1.8 to 5.5	25	–0.1 to V_S + 0.1	0.01	200	0.35	0.16	55
OPA2314-Q1	1.8 to 5.5	180	–0.2 to V_S + 0.2	2.5	10	2.7	1.5	14
OPAx376-Q1	2.2 to 5.5	950	–0.1 to V_S + 0.1	0.025	10	5.5	2	7.5
TLV226x-Q1	2.7 to 8	500	–0.3 to V_S – 0.8	0.95	60	0.67	0.55	12

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

(1) I = input, O = output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_S	Supply voltage		16.5	V
V_I	Input voltage(2)		V_S	V
V_{ID}	Differential input voltage		V_S	V
I_O	Output current		100	mA
	Continuous total power dissipation	See the *Thermal Information* Table		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Relative to the V–.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_S	Supply voltage	Dual supply	±1.35	±8	V
		Single supply	2.7	16	
	Input common-mode voltage		–0.2	V_S – 1.2	V
T_A	Operating free-air temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV27L2-Q1 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at recommended operating conditions, V_S = 2.7 V, 5 V, and 10 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP	MAX	UNIT
DC PERFORMANCE								
V_{IO}	Input offset voltage	$V_{IC} = V_S / 2$, $V_O = V_S / 2$, R_L = 100 kΩ, R_S = 50 Ω		25°C		0.5	5	mV
				Full range			7	
α_{VIO}	Offset voltage drift	$V_{IC} = V_S / 2$, $V_O = V_S / 2$, R_L = 100 kΩ, R_S = 50 Ω		25°C		1.1		µV/°C
CMRR	Common-mode rejection ratio	V_{IC} = 0 V to V_S – 1.2 V, R_S = 50 Ω		25°C	71	86		dB
				Full range	70			
A_{VD}	Large-signal differential voltage amplification	$V_{O(PP)} = V_S / 2$, R_L = 100 kΩ,	V_S = 2.7 V, 5 V	25°C	80	100		dB
				Full range	77			
			V_S = ±5 V	25°C	77	82		
				Full range	74			
INPUT CHARACTERISTICS								
I_{IO}	Input offset current	$V_{IC} = V_S / 2$, $V_O = V_S / 2$, R_L = 100 kΩ, R_S = 50 Ω		≤ 25°C		1	60	pA
				≤ 70°C			100	
				≤ 125°C			1000	
I_{IB}	Input bias current	$V_{IC} = V_S / 2$, $V_O = V_S / 2$, R_L = 100 kΩ, R_S = 50 Ω		≤ 25°C		1	60	pA
				≤ 70°C			200	
				≤ 125°C			1000	
$r_{i(d)}$	Differential input resistance			≤ 25°C		1000		GΩ
C_{IC}	Common-mode input capacitance	f = 1 kHz		≤ 25°C		8		pF
POWER SUPPLY								
I_Q	Quiescent current (per channel)	$V_O = V_S/2$		25°C		7	11	µA
				Full range			16	
PSRR	Power supply rejection ratio ($\Delta V_S/\Delta V_{IO}$)	No load, V_S = 2.7 V to 16 V, $V_{IC} = V_S$ / 2 V		25°C	74	82		dB
				Full range	70			
OUTPUT CHARACTERISTICS								
V_O	Output voltage swing from rail	$V_{IC} = V_S / 2$, I_{OL} = 100 µA	V_S = 2.7 V	25°C		160	200	mV
				Full range			220	
			V_S = 5 V	25°C		85	120	
				Full range			200	
			V_S = ±5 V	25°C		50	120	
				Full range			150	
		$V_{IC} = V_S / 2$, I_{OL} = 500 µA	V_S = 5 V	25°C		420	800	
				Full range			900	
			V_S = ±5 V	25°C		200	400	
				Full range			500	
I_O	Output current	V_O = 0.5 V from rail, V_S = 2.7 V		25°C		400		µA
DYNAMIC PERFORMANCE								
GBP	Gain bandwidth product	R_L = 100 kΩ, C_L = 10 pF, f = 1 kHz		25°C		160		kHz
SR	Slew rate at unity gain	$V_{O(pp)}$ = 1 V, R_L = 100 kΩ, CL = 50 pF		25°C		0.06		V/µs
				–40°C		0.05		
				125°C		0.8		
φM	Phase margin	R_L = 100 kΩ, C_L = 50 pF		25°C		62		°
t_s	Settling time (0.1%)	$V_{(STEP)pp}$ = 1 V, A_V = –1, rise		25°C		62		µs
		CL = 50 pF, R_L = 100 kΩ, fall				44		
NOISE AND DISTORTION PERFORMANCE								
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		89		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.6		nV/√Hz

(1) Full range is –40°C to 125°C for I suffix.

7.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Input offset voltage (V_{IO})	vs Common-mode input voltage (V_{IC})	Figure 1, Figure 2, Figure 3
Input bias and offset current (I_{IB} and I_{IO})	vs Free-air temperature (T_A)	Figure 4
High-level output voltage (V_{OH})	vs High-level output current (I_{OH})	Figure 5, Figure 7, Figure 9
Low-level output voltage (V_{OL})	vs Low-level output current (I_{OL})	Figure 6, Figure 8, Figure 10
Quiescent current (I_Q)	vs Supply voltage (V_S)	Figure 11
	vs Free-air temperature (T_A)	Figure 12
Supply voltage and supply current ramp up		Figure 13
Differential voltage gain and phase shift (A_{VD})	vs Frequency (f)	Figure 14
Gain-bandwidth product (GBP)	vs Free-air temperature (T_A)	Figure 15
Phase margin (φ_m)	vs Load capacitance (C_L)	Figure 16
Common-mode rejection ratio (CMRR)	vs Frequency (f)	Figure 17
Power supply rejection ratio (PSRR)	vs Frequency (f)	Figure 18
Input referred noise voltage	vs Frequency (f)	Figure 19
Slew rate (SR)	vs Free-air temperature (T_A)	Figure 20
Peak-to-peak output voltage ($V_{O(PP)}$)	vs Frequency (f)	Figure 21
Inverting small-signal response		Figure 22
Inverting large-signal response		Figure 23
Crosstalk	vs Frequency (f)	Figure 24

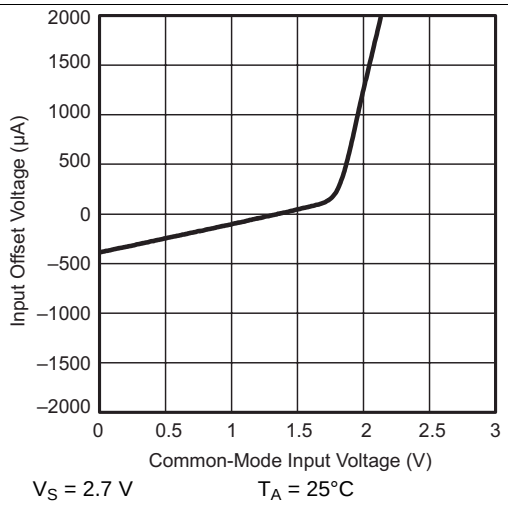


Figure 1. Input Offset Voltage vs Common-Mode Input Voltage

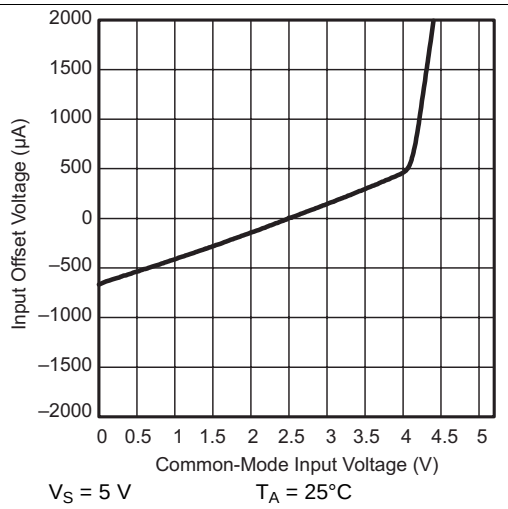
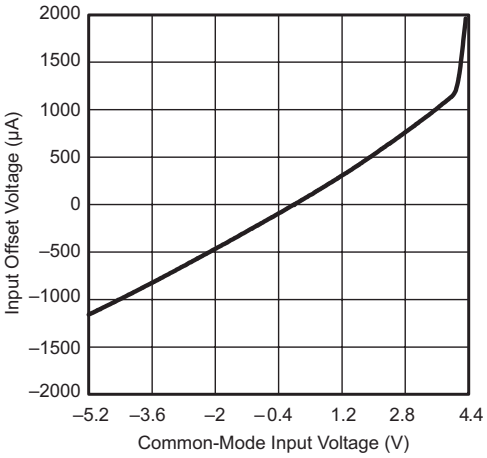
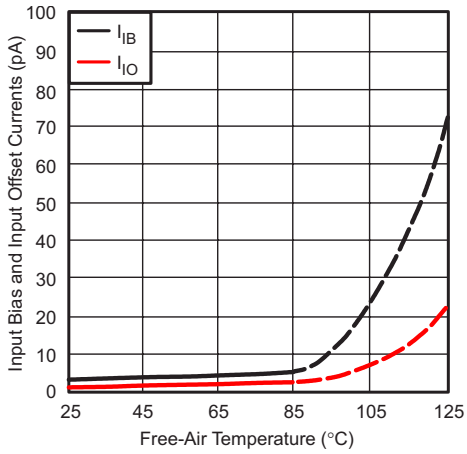


Figure 2. Input Offset Voltage vs Common-Mode Input Voltage



V_S = ±5 V_{DC} T_A = 25°C

Figure 3. Input Offset Voltage vs Common-Mode Input Voltage



V_S = 5 V V_{IC} = 2.5 V V_O = 2.5 V

Figure 4. Input Bias And Input Offset Current vs Free-Air Temperature

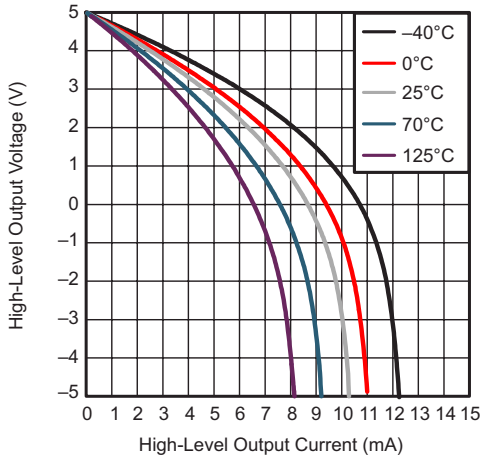
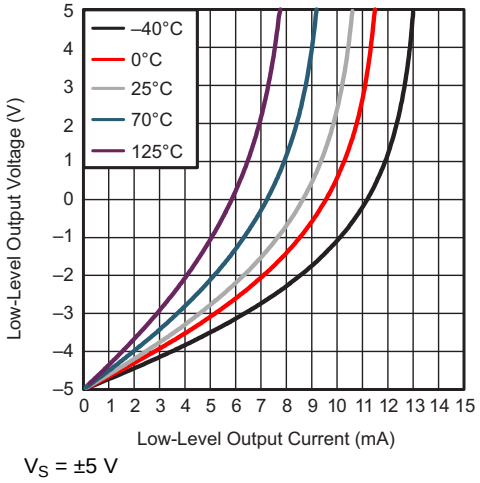
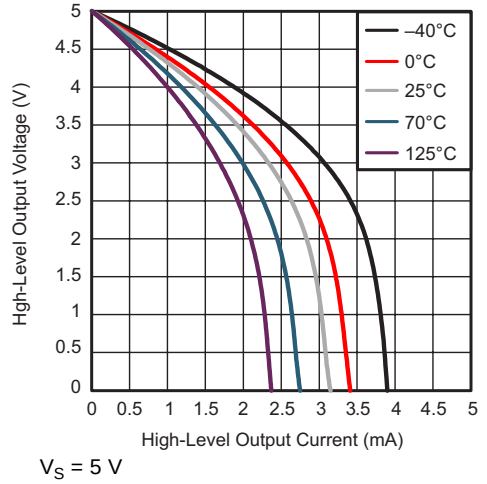


Figure 5. High-Level Output Voltage vs High-Level Output Current



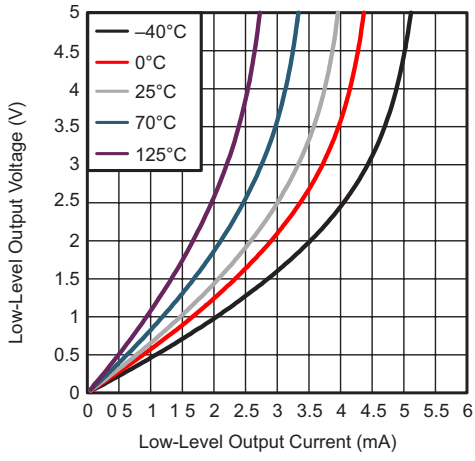
V_S = ±5 V

Figure 6. Low-Level Output Voltage vs Low-Level Output Current



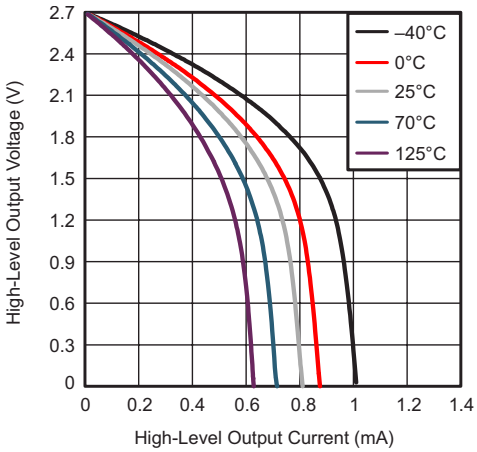
V_S = 5 V

Figure 7. High-Level Output Voltage vs High-Level Output Current



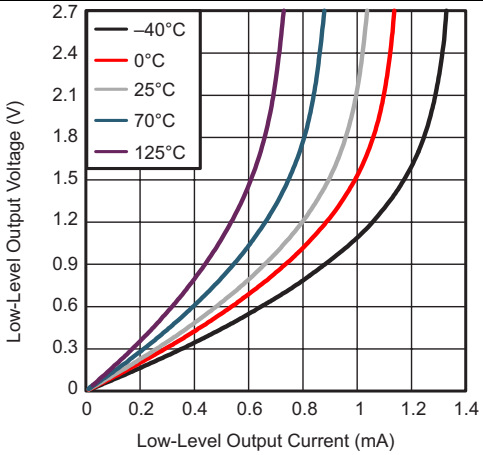
V_S = 5 V

Figure 8. Low-Level Output Voltage vs Low-Level Output Current



V_S = 2.7 V

Figure 9. High-Level Output Voltage vs High-Level Output Current



V_S = 2.7 V

Figure 10. Low-Level Output Voltage vs Low-Level Output Current

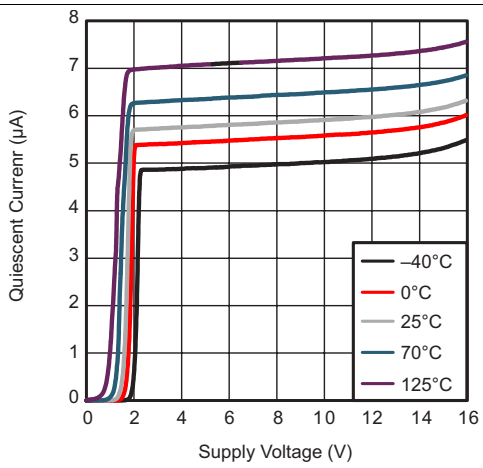


Figure 11. Quiescent Current vs Supply Voltage

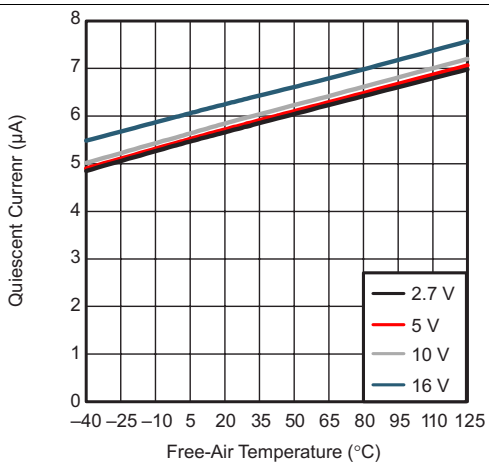
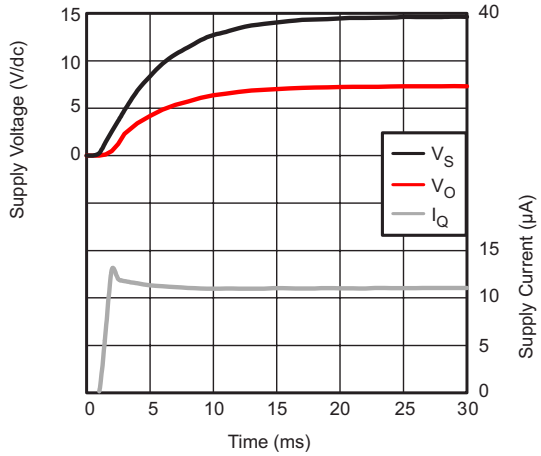
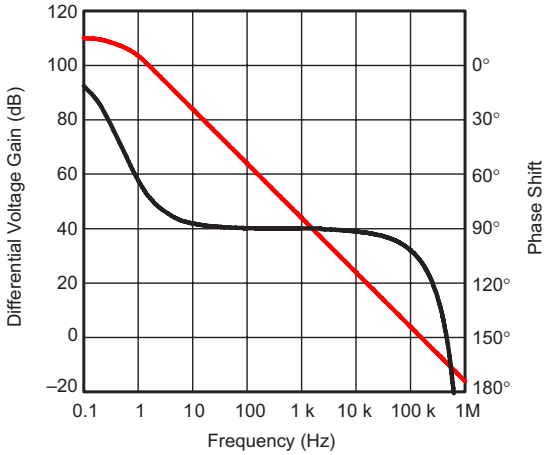


Figure 12. Quiescent Current vs Free-Air Temperature



V_S = 0 to 15 V R_L = 100 Ω C_L = 10 pF
T_A = 25°C

Figure 13. Supply Voltage and Supply Current Ramp Up



V_S = 5 V R_L = 100 Ω C_L = 10 pF
T_A = 25°C

Figure 14. Differential Voltage Gain and Phase Shift vs Frequency

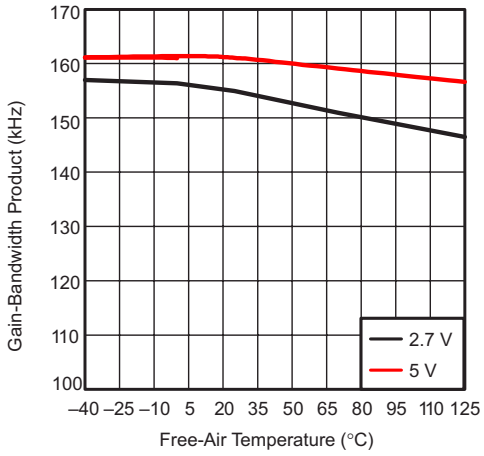
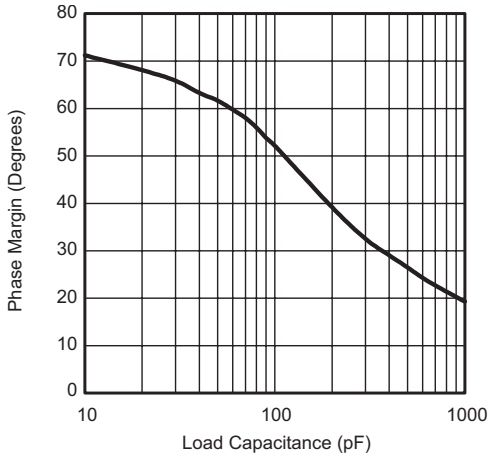
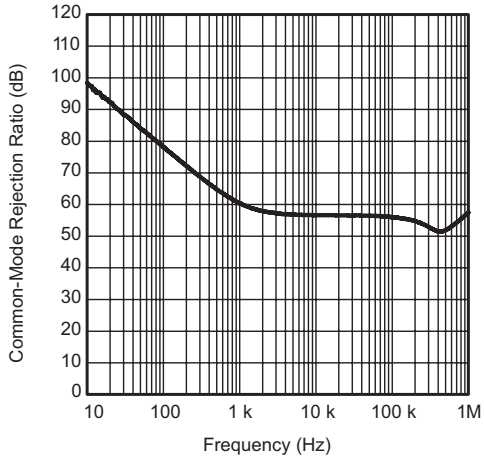


Figure 15. Gain-Bandwidth Product vs Free-Air Temperature



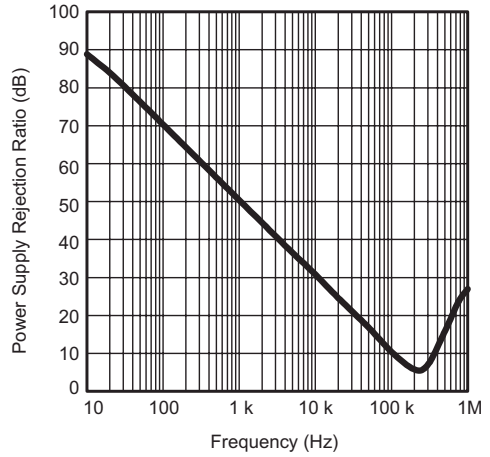
V_S = 5 V R_L = 100 kΩ T_A = 25°C

Figure 16. Phase Margin vs Load Capacitance



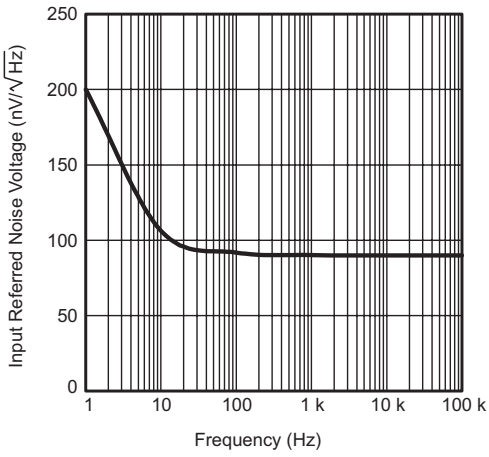
V_S = 5 V T_A = 25°C

Figure 17. Common-Mode Rejection Ratio vs Frequency



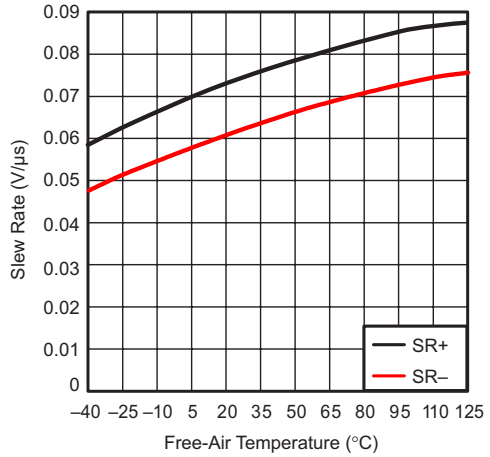
V_S = ±2.5 V T_A = 25°C

Figure 18. Power Supply Rejection Ratio vs Frequency



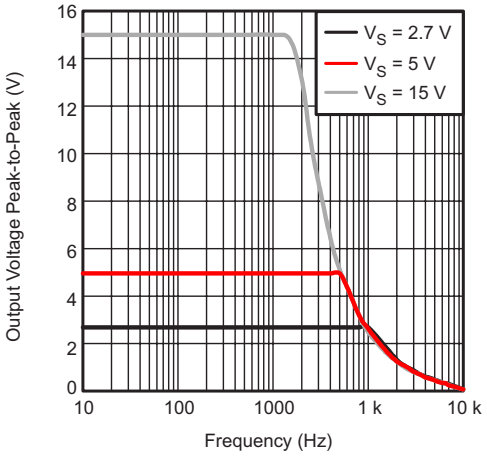
V_S = 5 V G = 2 R_F = 100 kΩ

Figure 19. Input Referred Noise Voltage vs Frequency



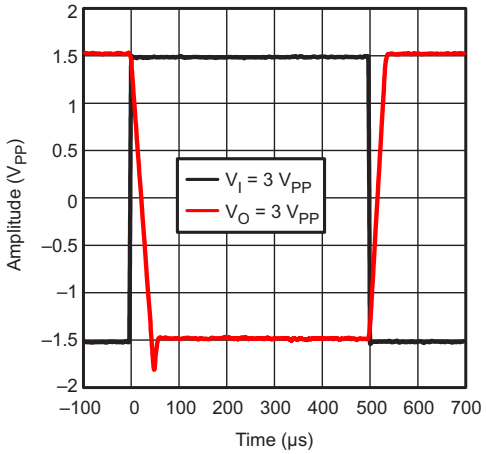
V_S = 5 V G = 1 V_O = 1 V
R_L = 100 kΩ C_L = 50 pF

Figure 20. Slew Rate vs Free-Air Temperature



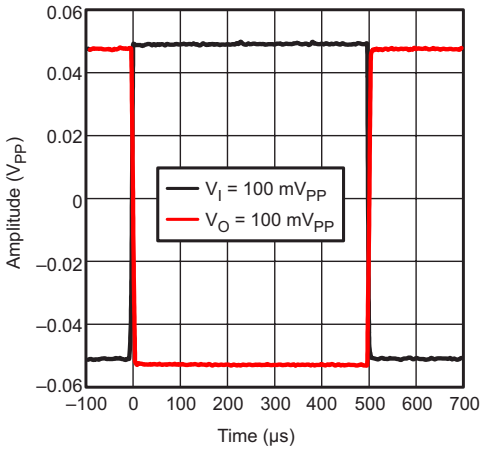
R_L = 100 kΩ C_L = 10 pF THD+N ≤ 5%

Figure 21. Peak-to-Peak Output Voltage vs Frequency



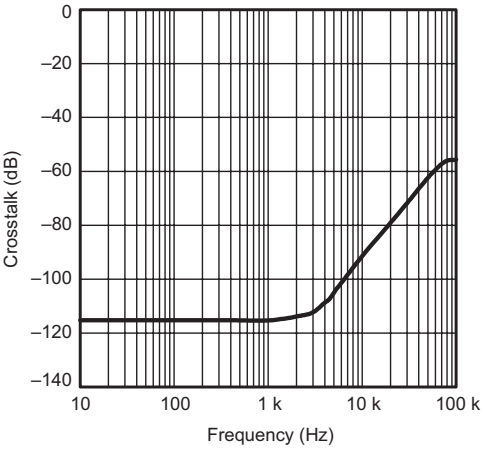
V_S = 5 V G = –1 V_O = 3 V_{PP}
R_L = 100 kΩ C_L = 10 pF f = 1 kHz

Figure 22. Inverting Small-Signal Response



V_S = 5 V G = –1 V_O = 100 mV_{PP}
R_L = 100 kΩ C_L = 10 pF f = 1 kHz

Figure 23. Inverting Large-Signal Response



V_S = 5 V G = –1 T_A = 25°C
R_L = 2 kΩ C_L = 10 pF Channel 1 to 2

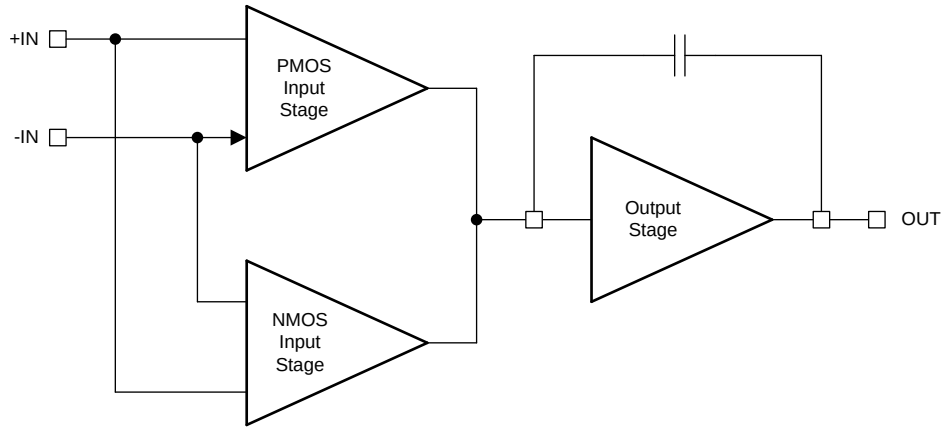
Figure 24. Crosstalk vs Frequency

8 Detailed Description

8.1 Overview

The TLV27L2-Q1 device is a micropower, rail-to-rail output, operational amplifier. This device operates from 2.7 V to 16 V, is unity-gain stable, and is suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes the negative rail and allows the TLV27L2-Q1 device to be used in virtually any single-supply application from 2.7 V to 16 V. The typical supply current of 7 µA makes the TLV27L2-Q1 device an excellent choice for battery operated systems.

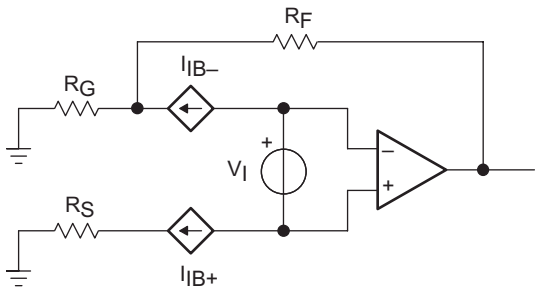
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Offset Voltage

The output offset voltage (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. Use the schematic and formula in Figure 25 to calculate the output offset voltage.



$$V_{OO} = V_{IO}\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB} + R_S\left(1 + \left(\frac{R_F}{R_G}\right)\right) \pm I_{IB-} R_F$$

Figure 25. Output Offset Voltage Model

8.4 Device Functional Modes

The TLV27L2-Q1 device is powered on when the supply is connected. The device can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application. The TLV27L2-Q1 device operates from power supplies as low as 2.7 V or as high as 16 V.

9 Application and Implementation

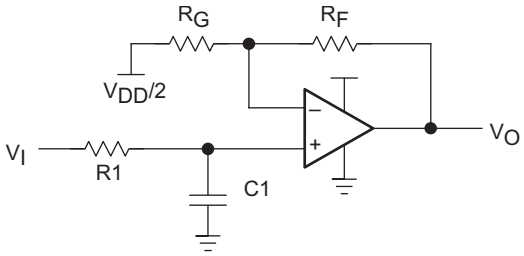
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way limit the bandwidth is to place an RC filter at the noninverting terminal of the amplifier as shown in Figure 26.

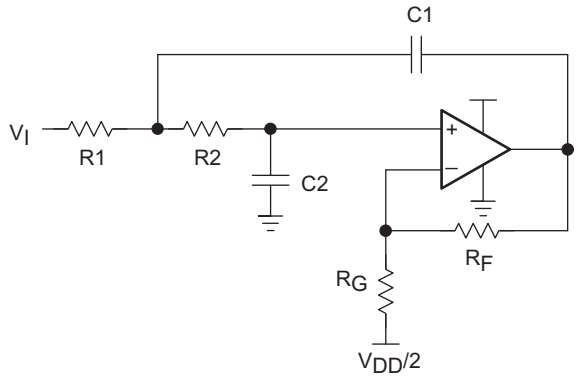


$$\frac{V_O}{V_I} = \left(1+\frac{R_F}{R_G}\right)\left(\frac{1}{1+sR1C1}\right)$$

$$f_{-3dB} = \frac{1}{2\pi R1C1}$$

Figure 26. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. The Sallen-Key filter can be used for this task. For best results, the amplifier should have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to do select an amplifier with an appropriate bandwidth can result in phase shift of the amplifier.



R1 = R2 = R
C1 = C2 = C
Q = Peaking Factor
(Butterworth Q = 0.707)

$$f_{-3dB} = \frac{1}{2\pi RC}$$
R

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

Figure 27. 2-Pole Low-Pass Sallen-Key Filter

9.2 Typical Application

This single-supply low-side, bi-directional current sensing solution can accurately detect load currents from –1 A to +1 A. The linear range of the output is from 110 mV to 3.19 V. The design uses the TLV27L2-Q1 device configured as a difference amplifier and reference voltage buffer.

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore the current sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, a reference voltage must be added to differentiate between positive and negative currents. Figure 28 shows a general circuit topology for a low-side, bidirectional current-sensing solution. This topology is particularly useful when cost is a priority at the expense of accuracy and printed circuit board (PCB) space. The shunt voltage (V_{SHUNT}) is created

Typical Application (continued)

by the load current (I_{LOAD}) flowing through the shunt resistor (R_{SHUNT}). The V_{SHUNT} voltage is amplified by an op amp (U1A) according to the gain set by the ratio of R4 to R3. To achieve the transfer function in Equation 1 and to minimize errors, set R4 equal to R2 and R3 equal to R1. To provide the reference voltage in this design, divide down the supply voltage (V_{CC}) using R5 and R6. The reference voltage is then buffered using an additional op amp (U1B).

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{ref} \quad (1)$$

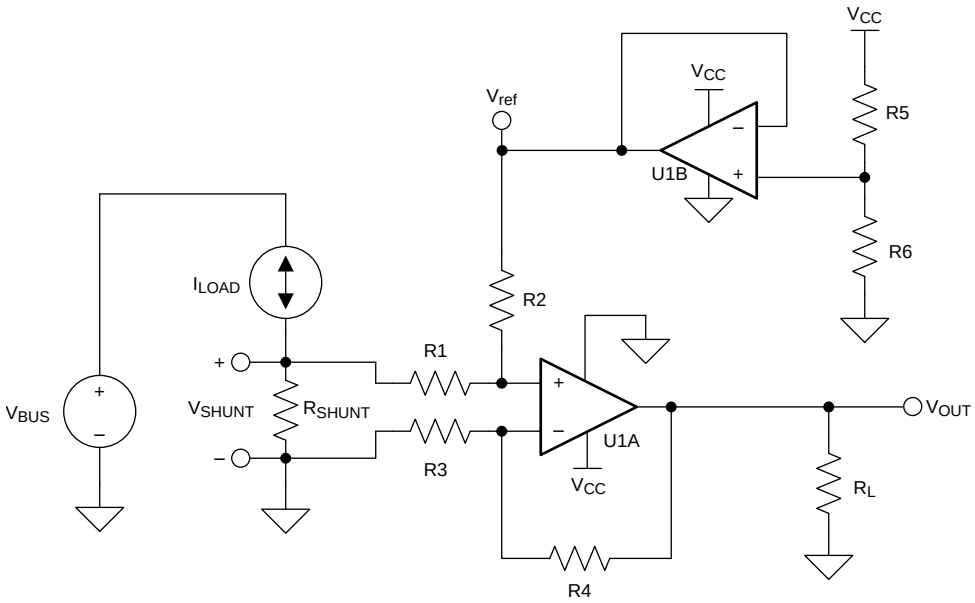


Figure 28. Application Schematic ±1-A Single-Supply Low-Side Current Sensing Solution

9.2.1 Design Requirements

The design requirements are as follows:

Supply voltage: 3.3 V

Input: –1 A to +1 A

Output: 110 mV to 3.19 V

Maximum shunt voltage: ±100 mV

9.2.2 Detailed Design Procedure

9.2.2.1 Shunt Resistor (R_{SHUNT})

As shown in Figure 28, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, it can cause issues when interfacing with systems with a true ground potential of 0 V. If the value of V_{SHUNT} is too negative, it can violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limit the voltage across the shunt resistor. Use Equation 2 to calculate the maximum value of R_{SHUNT} given a maximum shunt voltage of 100 mV.

$$R_{SHUNT(MAX)} = \frac{\left|V_{SHUNT(MAX)}\right|}{\left|I_{LOAD(MAX)}\right|} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

Because cost is a priority in this design, a shunt resistor with a 0.5% tolerance was selected.

Typical Application (continued)

9.2.2.2 Operational Amplifiers

The shunt voltage in this design can range from –100 mV to +100 mV. The shut voltage is divided down by the resistors, R1 and R2. The op amp configured as a difference amplifier (U1A) must have an input common-mode that includes this voltage range. Therefore an op amp with rail-to-rail input (RRI) that extends below V– is recommended. The output swing of the amplifier should also be rail-to-rail output (RRO) to maximize the dynamic range of the system. Use of a CMOS op amp is recommended because the supply voltage is 3.3 V. The supply-splitter op amp (U1B) should have low offset voltage. Because this design includes two op amps, a dual package minimizes the required area. This design uses the TLV27L2-Q1 device because it is a RRO CMOS device. In addition, the cost versus performance of the device is excellent.

9.2.2.3 Reference Voltage Resistors (R5-R6)

Because the load current range is symmetric (–1 A to +1 A), the resistors that divide down the supply voltage should be equal so that the reference voltage is the mid supply ([(V+) – (V–)] / 2 or, for this example, (3.3 V – 0 V) / 2 = 1.65 V). Because cost is a priority in this design, the tolerance should be consistent with the shunt resistor tolerance (0.5%). Finally, select resistors that are large enough to meet the power consumption requirement of the system. For this design, 10-kΩ resistors were selected.

9.2.2.4 Difference Amplifier Gain Setting Resistors (R1-R4)

Equation 3 and Equation 4 show the input common-mode (V_{CM}) and output voltage range (V_{OUT}) of the TLV27L2-Q1 device given a 3.3-V supply.

$$-200\ mV < V_{CM} < 2.1\ V \quad (3)$$

$$100\ mV < V_{OUT} < 3.2\ V \quad (4)$$

Use Equation 5 to calculate the gain.

$$Gain_{Diff\_Amp} = \frac{V_{OUT\_MAX} - V_{OUT\_MIN}}{R_{SHUNT} \times (I_{MAX} - I_{MIN})} = \frac{3.2\ V - 100\ mV}{100\ m\Omega \times (1\ A - (1\ A))} = 15.5\frac{V}{V} \quad (5)$$

The selected value for the R1 and R3 resistors was 1 kΩ. The selected value for the R2 and R4 resistors was 15.4 kΩ, which is the nearest 0.1% value to the ideal value of 15.5 kΩ. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

9.2.3 Application Curve

Figure 29 shows the measured transfer function of the design.

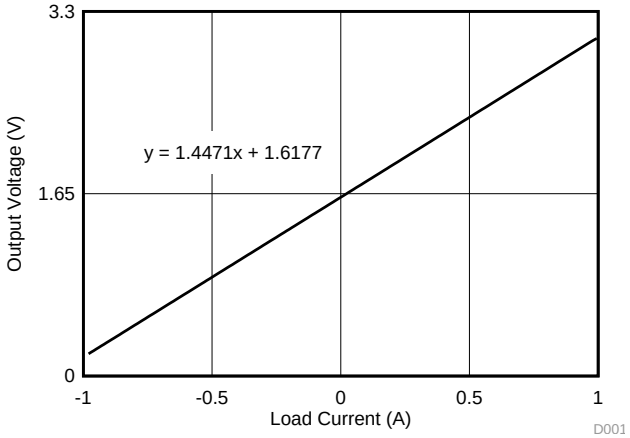


Figure 29. Measured Output Voltage vs Load Current (Board 1)

10 Power Supply Recommendations

The TLV27L2-Q1 device is specified for operation from 2.7 V to 16 V (±1.35 V to ±8 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 16.5 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

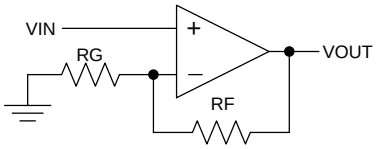
11 Layout

11.1 Layout Guidelines

To achieve the levels of high performance of the TLV27L2-Q1 device, follow proper printed-circuit board design techniques. The following list is a general set of guidelines:

- Ground planes—Using a ground plane on the board is highly recommended to provide all components with a low inductive-ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling—Use a 6.8-µF tantalum capacitor in parallel with a 0.1-µF ceramic capacitor on each supply terminal. Sharing the tantalum capacitor among several amplifiers is possible depending on the application, but a 0.1-µF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-µF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.
- Sockets—Sockets can be used but are not recommended. The additional lead inductance in the socket pins will often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board are the best implementation.
- Short trace runs and compact part placements—Optimum high performance is achieved when stray series inductance has been minimized. To achieve this performance, the circuit layout should be as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. The length should be kept as short as possible which helps minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components—Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, keep the lead lengths as short as possible.

11.2 Layout Example



(Schematic Representation)

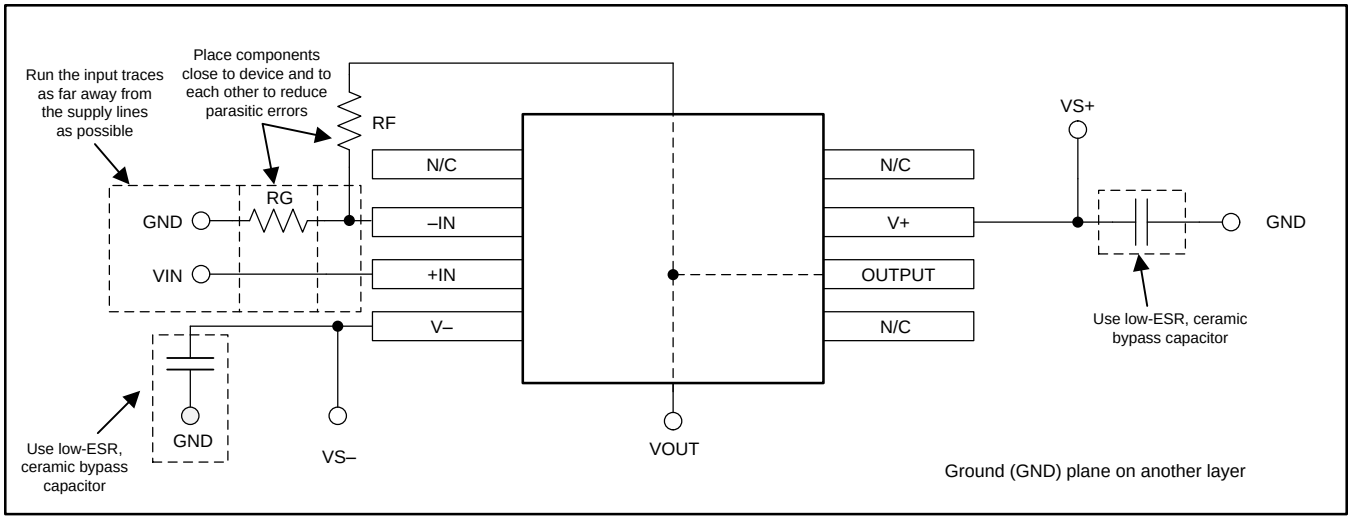


Figure 30. TLV27L2-Q1 Layout Example

11.3 General Power Dissipation Considerations

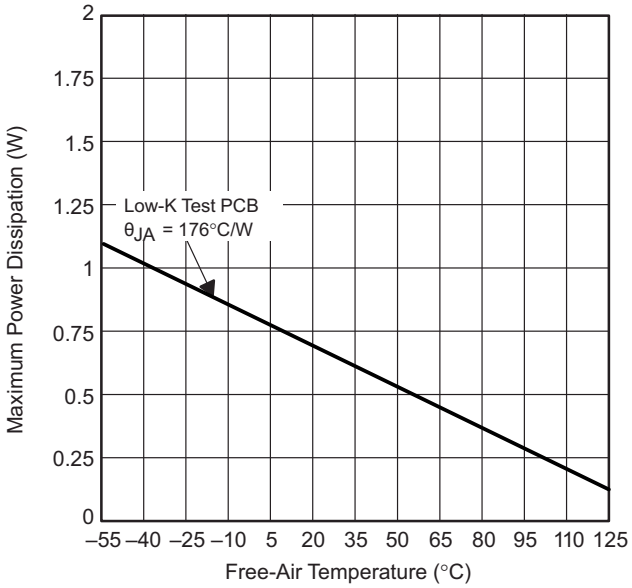
Use to calculate the maximum power dissipation for a given θ_{JA}.

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

where

- P_D = Maximum power dissipation of TLV27L2-Q1 IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
  - θ_{JC} = Thermal coefficient from junction to case
  - θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

General Power Dissipation Considerations (continued)



T_J = 150°C

Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 31. Maximum Power Dissipation vs Free-Air Temperature

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *OPAx348-Q1 1-MHz 45-µA CMOS Rail-to-Rail Operational Amplifier*, SBOS465
- *OPAx333-Q1 1.8-V microPower CMOS Operational Amplifier Zero-Drift Series*, SBOS522
- *OPA2314-Q1 3-MHz, Low-Power, Low-Noise, RRIO, 1.8-V CMOS Operational Amplifier*, SLOS896
- *OPAx376-Q1 Low-Noise, Low Quiescent Current, Precision Operational Amplifier e-trim™ Series*, SBOS549
- *TLV226x-Q1 Advanced LinCMOS™ CMOS Operational Amplifiers*, SGLS193

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV27L2QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	27L2Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV27L2-Q1 :

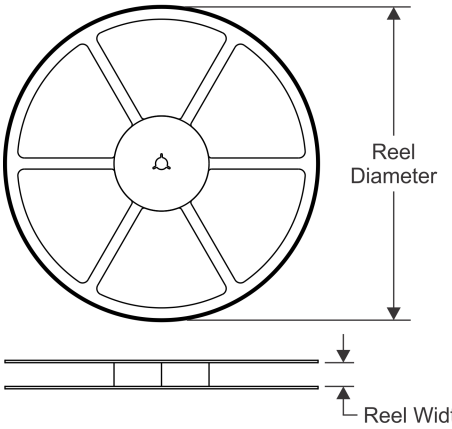
- Catalog: TLV27L2

NOTE: Qualified Version Definitions:

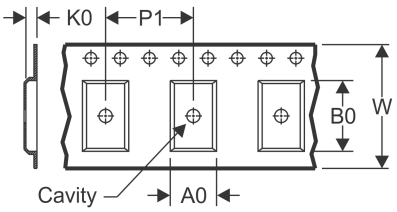
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

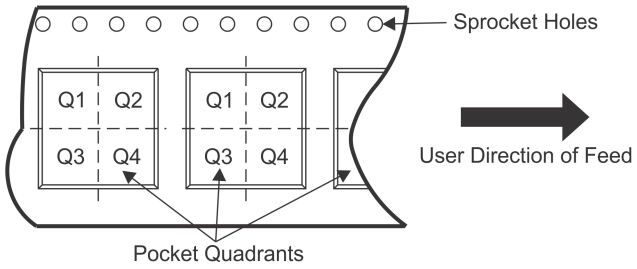


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

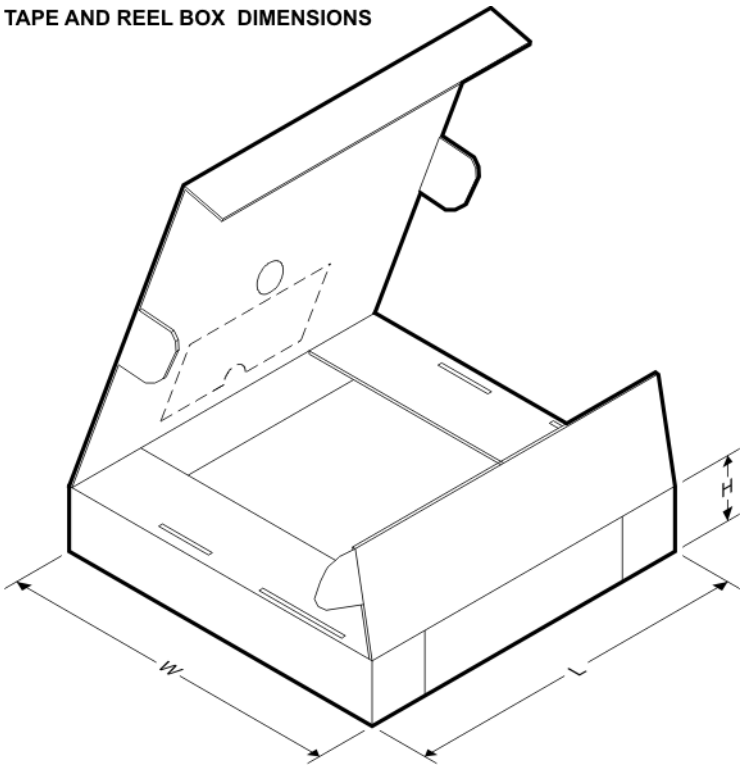
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV27L2QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

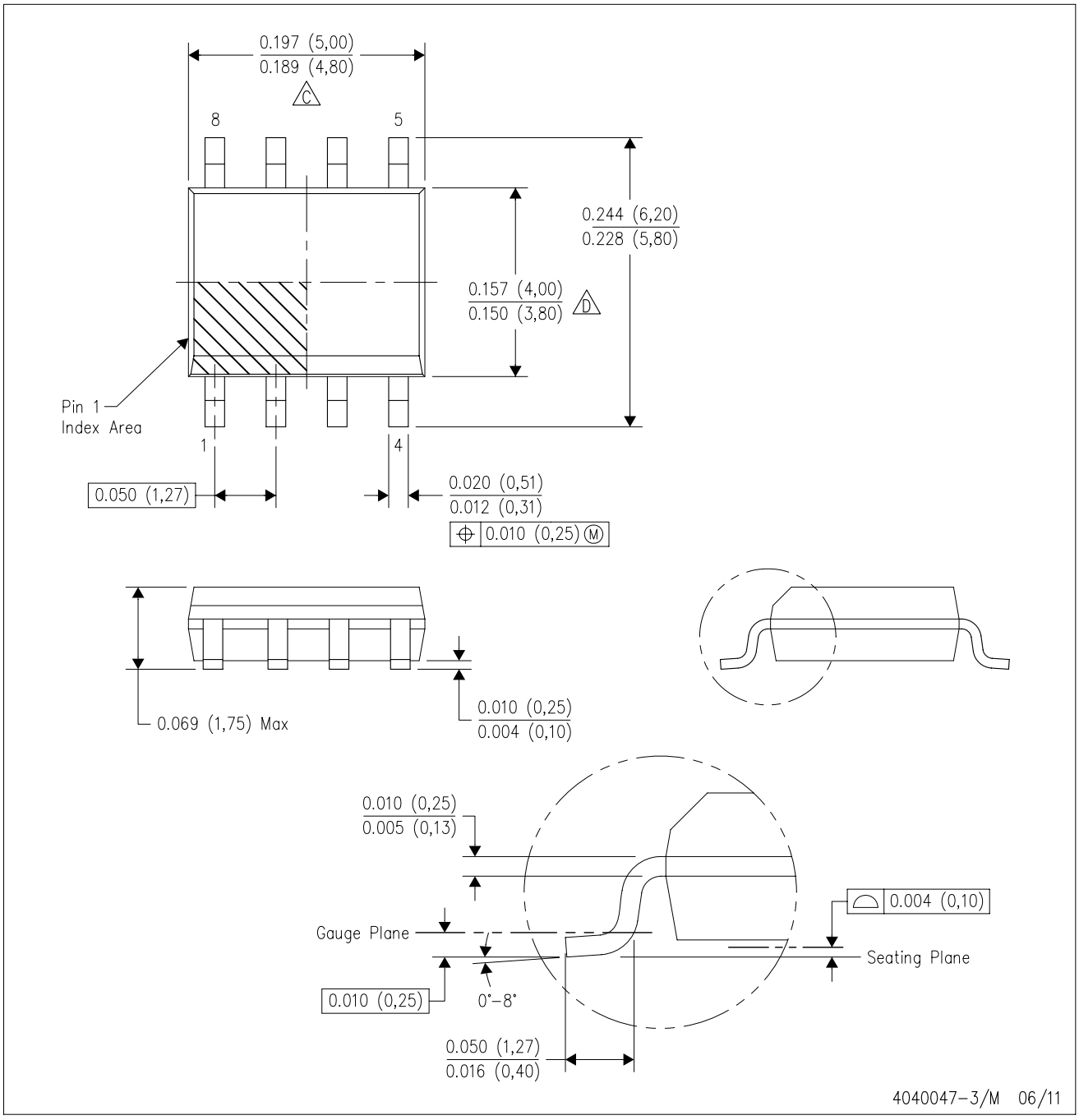
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

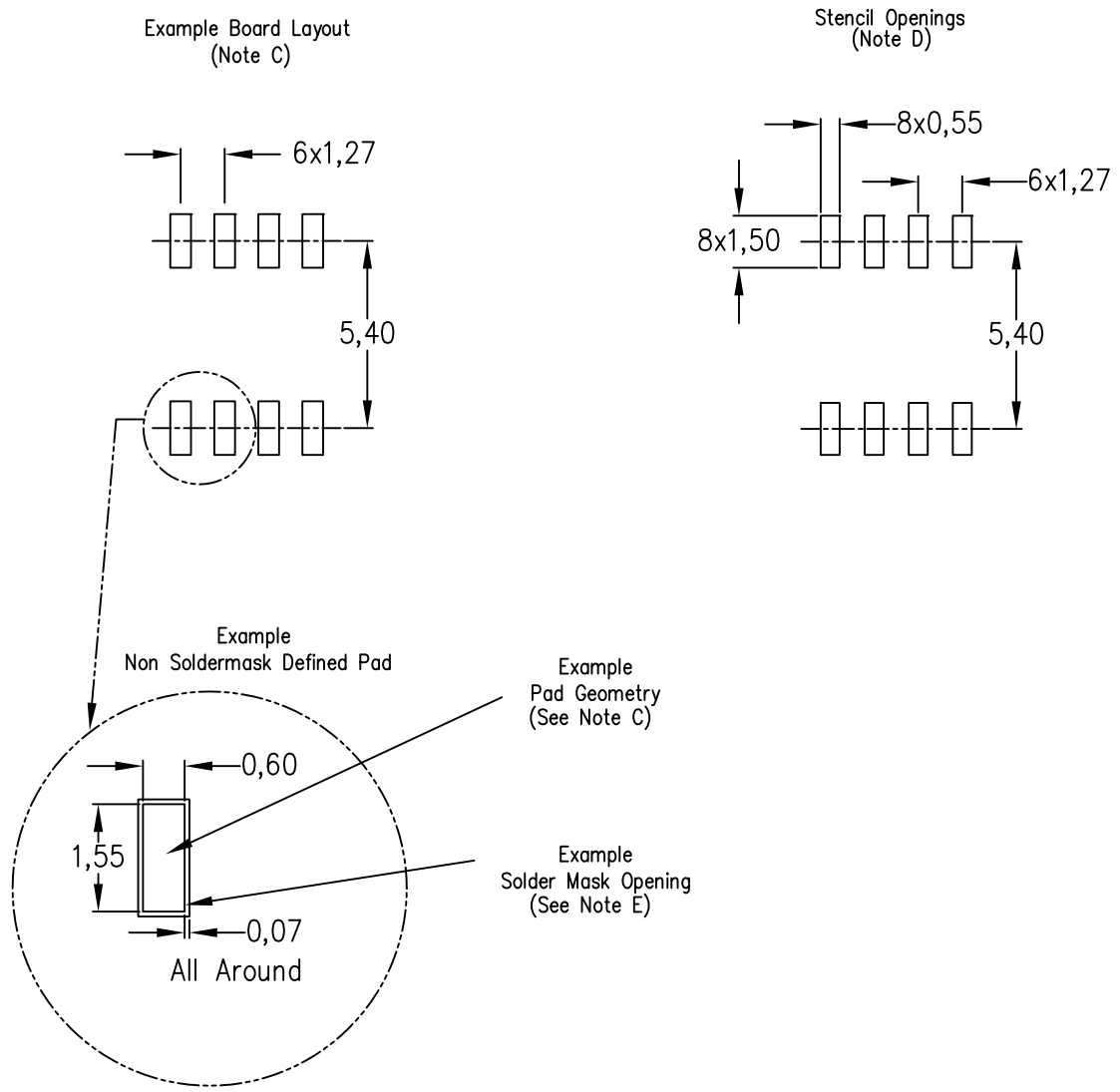
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV27L2QDRQ1	SOIC	D	8	2500	340.5	338.1	20.6

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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