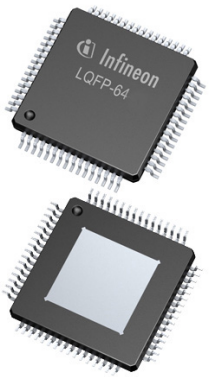
TLE9180D-21QK

Bridge Driver IC

Features



- High Power 3 Phase Bridge Driver for low RDSON N-channel FETs
- 0...100% duty cycle, adjustable without restrictions
- Specified supply voltage range of 5.5 V to 60 V
- Logic operation down to 3 V supply voltage
- High robustness of motor connection pins of -15 V to 90 V
- Extended protection and supervision functionality
- Serial Peripheral Interface (SPI), control of supervision
- Supervision read out by SPI
- Reverse diode measurement of external FET for temperature detection
- Limp-home functionality of diagnostic and failure behavior with SPI configurable content
- 2 current sense amplifiers for shunt signal conditioning
- 2 switch off paths by pins ENA and $\overline{\text{SOFF}}$
- Low quiescent current mode by pin $\overline{\text{INH}}$
- Compatible to 3.3 V µCs and TTL logic
- Phase voltage feedback with SPI programmable voltage thresholds
- Output for phase cut off circuit activation
- Green Product (RoHS compliant)

AEC Qualified

RoHS

Product validation

Qualified for Automotive Applications.
Product validation according to AEC-Q100/101.

Description

The TLE9180D-21QK is an advanced gate driver IC dedicated to control 6 external N-channel MOSFETs forming an inverter for high current 3 phase motor drives application in the automotive sector.

A sophisticated high voltage technology allows the TLE9180D-21QK to support applications for single and mixed battery systems with battery voltages of 12 V, 24 V and 48 V even within tough automotive environments in combination with high motor currents. Therefore bridge, motor and supply related pins can withstand voltages of up to 90 V. Motor related pins can even withstand negative voltage transients down to - 15 V without damage.

All low- and high-side output stages are based on a floating concept and its driver strength allows to drive lowest RDSON MOSFETs common on the market. In 12 V applications the gate driver IC is capable of driving 6 MOSFETs, each with a max. total gate charge of QgTOT = 300 nC, at a frequency of up to 20 kHz.

An integrated SPI interface is used to configure the TLE9180D-21QK for the application after power-up. After successful power-up parameters can be adjusted by SPI, monitoring data, configuration and error registers can be read. Cyclic redundancy check over data and address bits ensures safe communication and data integrity.

GND related bridge currents can be measured with 2 integrated current sense amplifiers. The outputs of the current sense amplifiers support 5 V ADCs and the robust inputs can withstand negative transients down to -10 V without damage. Gain and zero current voltage offset can be adjusted by SPI. The offset can be calibrated.

Diagnostic coverage and redundancy have increased steadily in recent years in automotive drive applications. Therefore the TLE9180D-21QK offers a wide range of diagnostic features, like monitoring of power supply voltages as well as system parameters. A testability of safety relevant supervision functions has been integrated. Failure behavior, threshold voltages and filter times of the supervisions of the device are adjustable via SPI.

The TLE9180D-21QK is integrated in a LQFP64 package with an exposed pad. Due to its exposed pad the gate driver IC provides an excellent thermal characteristic.

Table 1 Device Marking

Type	Package	Marking
TLE9180D-21QK	LQFP-64	TLE9180D-21QK

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1 Block Diagram

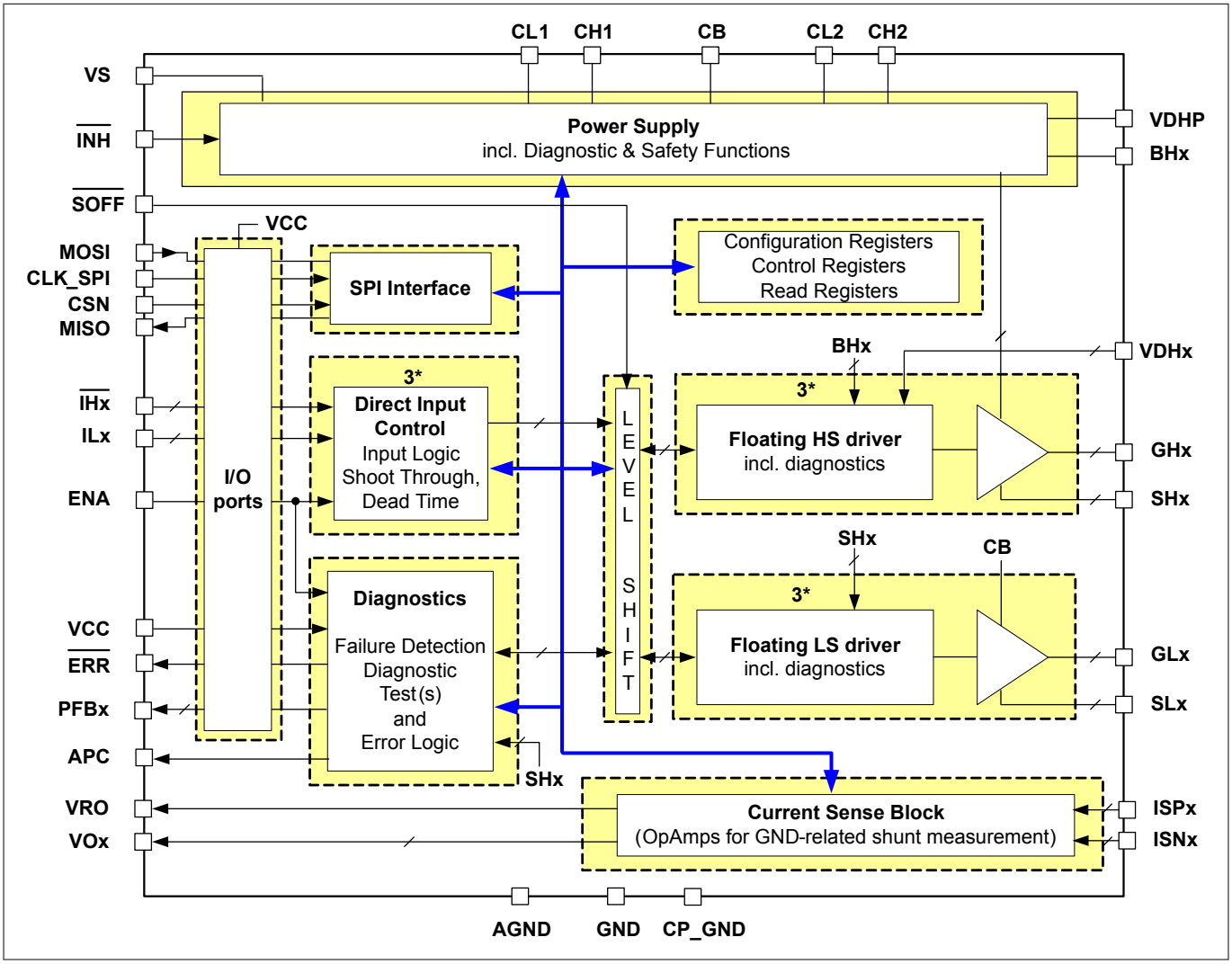


Figure 1 Block Diagram

2 Pin Configuration

2.1 Pin Assignment

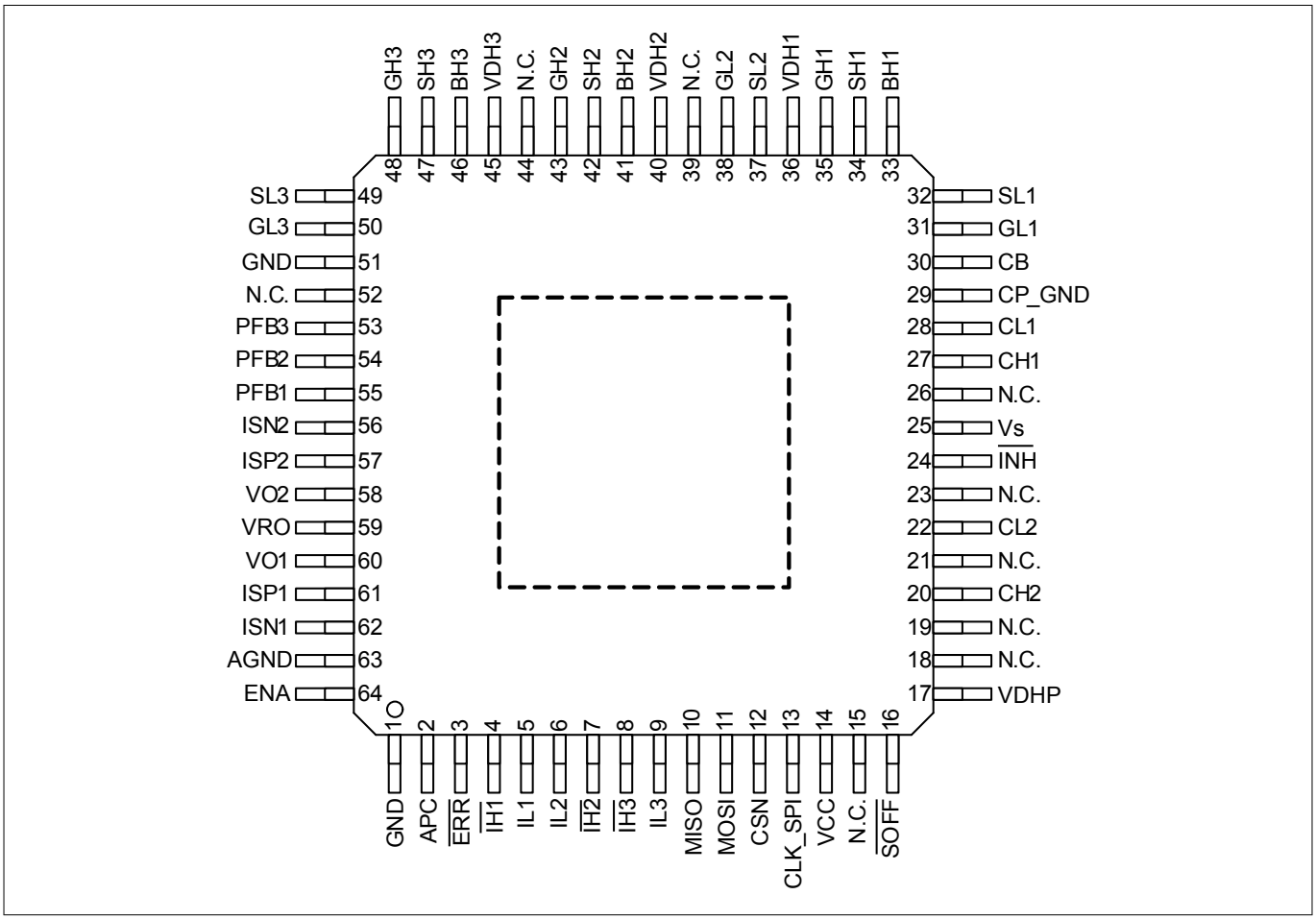


Figure 2 Pin Configuration

2.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	*Ground*
2	APC	*Activation Phase Cut off Circuit*
3	$\overline{\text{ERR}}$	*Error Not*
4	$\overline{\text{IH1}}$	*Input High-side 1 Not*
5	IL1	*Input Low-side 1*
6	IL2	*Input Low-side 2*
7	$\overline{\text{IH2}}$	*Input High-side 2 Not*
8	$\overline{\text{IH3}}$	*Input High-side 3 Not*
9	IL3	*Input Low-side 3*
10	MISO	*Master In Slave Out*

Pin Configuration

Pin	Symbol	Function
11	MOSI	*Master Out Slave In*
12	CSN	*Chip Select Not*
13	CLK_SPI	*Clock Serial Peripheral Interface*
14	VCC	*VCC Supply Voltage*
15	N.C.	*Not Connected*
16	$\overline{\text{SOFF}}$	*Safe Off Not*
17	VDHP	*Voltage Drain High-side Power*
18	N.C.	*Not Connected*
19	N.C.	*Not Connected*
20	CH2	*Charge Pump 2 High*
21	N.C.	*Not Connected*
22	CL2	*Charge Pump 2 Low*
23	N.C.	*Not Connected*
24	$\overline{\text{INH}}$	*Inhibit Not*
25	Vs	*Voltage Supply*
26	N.C.	*Not Connected*
27	CH1	*Charge Pump 1 High*
28	CL1	*Charge Pump 1 Low*
29	CP_GND	*Charge Pump Ground*
30	CB	*Charge Pump Buffer*
31	GL1	*Gate Low-side 1*
32	SL1	*Source Low-side 1*
33	BH1	*Bootstrap High-side 1*
34	SH1	*Source High-side 1*
35	GH1	*Gate High-side 1*
36	VDH1	*Voltage Drain High-side 1*
37	SL2	*Source Low-side 2*
38	GL2	*Gate Low-side 2*
39	N.C.	*Not Connected*
40	VDH2	*Voltage Drain High-side 2*
41	BH2	*Bootstrap High-side 2*
42	SH2	*Source High-side 2*
43	GH2	*Gate High-side 2*
44	N.C.	*Not Connected*
45	VDH3	*Voltage Drain High-side 3*

Pin Configuration

Pin	Symbol	Function
46	BH3	*Bootstrap High-side 3*
47	SH3	*Source High-side 3*
48	GH3	*Gate High-side 3*
49	SL3	*Source Low-side 3*
50	GL3	*Gate Low-side 3*
51	GND	*Ground*
52	N.C.	*Not Connected*
53	PFB3	*Phase Voltage Feedback 3*
54	PFB2	*Phase Voltage Feedback 2*
55	PFB1	*Phase Voltage Feedback 1*
56	ISN2	*Input Shunt Negative of CSA 2*
57	ISP2	*Input Shunt Positive of CSA 2*
58	VO2	*Voltage Output of CSA 2*
59	VRO	*Voltage Reference Output*
60	VO1	*Voltage Output of CSA 1*
61	ISP1	*Input Shunt Positive of CSA 1*
62	ISN1	*Input Shunt Negative of CSA 1*
63	AGND	*Analog Ground*
64	ENA	*Enable*
Cooling Tab	GND	*Cooling Tab*

3 General Product Characteristics

3.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power Supply							
Supply Voltage	V_{Vs1}	-0.3	–	60	V	–	P_4.1.1
Supply Voltage for Power-up	V_{Vs6}	–	–	40	V	–	P_4.1.7
Supply Voltage	V_{Vs2}	-5	–	–	V	Reverse polarity $R_{VS} \geq 10\ \Omega$ [1)]	P_4.1.2
Voltage Range VDHP	V_{VDHP1}	-5	–	85	V	[2)]	P_4.1.3
Voltage Difference Vs-VDHP	$V_{dVsVDHP}$	-85	–	60	V	–	P_4.1.5
Voltage Range VDH1, VDH2, VDH3	V_{VDHx1}	-5	–	90	V	–	P_4.1.6
Voltage Difference Vs-VDH1, VDH2, VDH3	$V_{dVsVDHx}$	-90	–	60	V	–	P_4.1.8
Voltage Range CL1	V_{CL1}	-0.3	–	60	V	–	P_4.1.9
Voltage Range CH1	V_{CH1}	-0.3	–	28	V	–	P_4.1.10
Voltage Range CB	V_{CB}	-0.3	–	28	V	–	P_4.1.11
Voltage Range CL2, CH2	V_{CHL2}	-0.3	–	90	V	–	P_4.1.12
Voltage Difference CH2-CL2	$V_{dCH2CL2}$	-0.3	–	28	V	–	P_4.1.62
Maximum Peak Pulse Current CB to CH2	I_{CBCH2}	–	–	1	A	t = 5 µs	P_4.1.61
Maximum Peak Pulse Current CB to BHx	I_{CBBHx}	–	–	1	A	t = 0.8 µs	P_4.1.66
Floating Driver Stages							
Voltage Range SLx	V_{SLx1}	-7	–	10	V	–	P_4.1.13
Voltage Range SLx	V_{SLx2}	-10	–	–	V	[5)]	P_4.1.14
Voltage Range SLx	V_{SLx3}	-15	–	–	V	[3)]	P_4.1.15
Voltage Range GLx	V_{GLx1}	-7	–	28	V	–	P_4.1.16
Voltage Range GLx	V_{GLx2}	-10	–	–	V	[5)]	P_4.1.17
Voltage Range GLx	V_{GLx3}	-15	–	–	V	[3)]	P_4.1.18

1 Voltage drop via resistor has be to taken into account for applications operating at low battery voltage
2 Minimum limit of -5 V valid only for a limited time frame
5 For a duration of t_on = 500ns; t_on/t_off = 1% per 20 kHz PWM frequency
3 For a duration of t_on = 250ns; t_on/t_off = 0.5% per 20 kHz PWM frequency

Table 2 Absolute Maximum Ratings (continued)

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage Range SHx	V_{SHx1}	-7	–	90	V	–	P_4.1.19
Voltage Range SHx	V_{SHx2}	-10	–	–	V	5)	P_4.1.20
Voltage Range SHx	V_{SHx3}	-15	–	–	V	3)	P_4.1.21
Max. Voltage Transients at SHx	V_{fSH_tr1}	–	–	20	V	Slew rate ≤ 1 V/ns	P_4.3.31
Voltage Range GHx	V_{GHx1}	-7	–	90	V	–	P_4.1.22
Voltage Range GHx	V_{GHx2}	-10	–	–	V	5)	P_4.1.23
Voltage Range GHx	V_{GHx3}	-15	–	–	V	3)	P_4.1.24
Voltage Range BHx	V_{BH}	-0.3	–	90	V	–	P_4.1.25
Voltage Difference Gxx-Sxx	V_{GS2}	-0.3	–	28	V	4)	P_4.1.26
Voltage Difference BHx-SHx	V_{BS2}	-0.3	–	28	V	4)	P_4.1.27
Voltage Difference CB-SLx	V_{CBSLx}	-0.3	–	28	V	4)	P_4.1.28
Voltage Difference SHx-SLx	V_{SSx1}	-12	–	90	V	–	P_4.1.29
Voltage Difference VDHP-SHx	$V_{dVDHPSHx2}$	-90	–	90	V	–	P_4.1.32
Voltage Difference VDHx-SHx	$V_{dVDHxSHx}$	-90	–	90	V	–	P_4.1.33
Inputs and Outputs							
Voltage Range $\overline{IHx}$, ILx, ENA	V_{DIP1}	-0.3	–	60	V	–	P_4.1.34
Voltage Range VCC	V_{VCC1}	-0.3	–	60	V	–	P_4.1.35
Voltage Range $\overline{INH}$	V_{INH}	-0.3	–	90	V	–	P_4.1.36
Voltage Range $\overline{SOFF}$	V_{SOFF}	-0.3	–	90	V	–	P_4.1.37
Voltage Range PFBx, $\overline{ERR}$	V_{DOP1}	-0.3	–	60	V	–	P_4.1.38
Voltage Range APC	V_{AOP1}	-0.3	–	60	V	–	P_4.1.39
SPI Interface							
Voltage Range CLK_SPI, CSN, MOSI	V_{SPI1}	-0.3	–	60	V	–	P_4.1.40
Voltage Range MISO	V_{SPI2}	-0.3	–	60	V	–	P_4.1.41
Shunt Signal Conditioning							
Voltage Range ISPx, ISNx	V_{ISx1}	-3.0	–	3.0	V	–	P_4.1.42
Voltage Range ISPx, ISNx	V_{ISx2}	-10	–	10	V	R_{ISP} ≥ 18 Ω R_{ISN} ≥ 18 Ω 5)	P_4.1.43

5 For a duration of t_on = 500ns; t_on/t_off = 1% per 20 kHz PWM frequency
3 For a duration of t_on = 250ns; t_on/t_off = 0.5% per 20 kHz PWM frequency
4 For a duration of t = 50 µs with 400 mA

Table 2 Absolute Maximum Ratings (continued)

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage Difference ISPx-ISNx	V_{dISx}	-5.0	–	5.0	V	–	P_4.1.44
Voltage Range VOx	V_{VOx1}	-0.3	–	3.0	V	–	P_4.1.45
Voltage Range VOx	V_{VOx3}	-0.3	–	5.5	V	$\overline{INH}$ = High; Vs supplied	P_4.1.46
Voltage Range VOx	V_{VOx2}	-0.3	–	18	V	1 kΩ in series	P_4.1.47
Current Range VOx	I_{VOx}	-10	–	18	mA	–	P_4.1.48
Voltage Range VRO	V_{VRO1}	-0.3	–	3	V	–	P_4.1.49
Voltage Range VRO	V_{VRO3}	-0.3	–	5.5	V	$\overline{INH}$ = High; Vs supplied	P_4.1.50
Voltage Range VRO	V_{VRO2}	-0.3	–	18	V	1 kΩ in series	P_4.1.51
Current Range VRO	I_{VRO}	-10	–	18	mA	–	P_4.1.52
GND							
Voltage Range CP_GND, AGND, GND, EPAD	V_{ISx}	-0.3	–	0.3	V	–	P_4.1.53
Temperatures							
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.54
Junction Temperature	T_{J1}	-40	–	150	°C	–	P_4.1.55
Junction Temperature	T_{J2}	-40	–	175	°C	200 h over lifetime	P_4.1.56
ESD Susceptibility							
ESD Resistivity HBM all Pins excluded Pin SHx, BHx, GHx, CB, ISNx and ISPx[6]	$V_{ESDHBM1}$	-2	–	2	kV	–	P_4.1.57
ESD Resistivity HBM all Pins excluded Pin CB, ISNx and ISPx[6]	$V_{ESDHBM3}$	-1.5	–	1.5	kV	–	P_4.1.65
ESD Resistivity HBM all Pins[6]	$V_{ESDHBM2}$	-1	–	1	kV	–	P_4.1.58
ESD Resistivity all Pins (charged device model)[7]	V_{ESDCDM}	–	–	500	V	–	P_4.1.59
ESD Resistivity Corner Pins (charged device model)[7]	$V_{ESDCDMc}$	–	–	750	V	–	P_4.1.60

6 ESD robustness according to Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001
7 ESD robustness according to Charged Device Model (CDM) JESD22-C101

Notes:

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case[8)]	R_{thJC}	–	5	_	K/W	$V_{Vs} = V_{VDH}$ = 14 V; T_a = 85°C; 6 FETs toggling: Q_{gTOT} = 200 nC; f_{PWM} = 20 kHz; inhomogeneous power distribution	P_4.2.1
Junction to Top[8)]	R_{thJCT}	–	18	_	K/W	$V_{Vs} = V_{VDH}$ = 14 V; T_a = 85°C; 6 FETs toggling: Q_{gTOT} = 200 nC; f_{PWM} = 20 kHz; inhomogeneous power distribution	P_4.2.2
Junction to Ambient[8)]	R_{thJA}	–	28	_	K/W	$V_{Vs} = V_{VDH}$ = 14 V; T_a = 85°C; 6 FETs toggling: Q_{gTOT} = 200 nC; f_{PWM} = 20kHz; inhomogeneous power distribution[9)]	P_4.2.3

8 Not subject to production test, specified by design

9 Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip + package) was simulated on a 76.2 × 114.3 ×1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer

3.3 Functional Range

Table 4 Functional Range

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltage	V_{Vs3}	5.5	–	60	V	Thermally limited	P_4.3.1
Supply Voltage for Startup	V_{Vs4}	V_{VsWU}	–	–	V	Startup	P_4.3.2
Supply Voltage Reduced Operation Range Vs[10]	V_{Vs5}	3.0	–	V_{VsROP}	V	Logic operational; I/Os turned off	P_4.3.3
Voltage Range VCC	V_{VCC4}	V_{VCCROP}	–	$V_{VCCxOVx}$	V	–	P_4.3.4
Supply Voltage Reduced Operation Range VCC	V_{VCC5}	-0.3	–	V_{VCCROP}	V	Logic operational; I/Os turned off	P_4.3.5
Voltage Range CB[11]	V_{fCB}	V_{CBUVSD}	–	15.0	V	–	P_4.3.6
Voltage Difference CH1-CL1[11]	V_{CP1}	V_{CBx} - V_s	–	V_{CBd}	V	$\overline{INH}$ = High; CP1 and CP2 operative	P_4.3.7
Voltage Difference CH2-CL2[11]	V_{CP2}	-0.3	–	V_{CBd}	V	$\overline{INH}$ = High; CP1 and CP2 operative	P_4.3.8
Voltage Difference CH1-CL1[11]	V_{CP1b}	-0.3	–	V_{CBd}	V	$\overline{INH}$ = Low or CP1 off	P_3.3.2
Voltage Difference CH2-CL2[11]	V_{CP2b}	-0.3	–	V_{CBd}	V	$\overline{INH}$ = Low or CP2 off	P_3.3.3
Voltage Range VDHP, VDH1, VDH2, VDH3	V_{VDH3}	4.0	–	$V_{VDHOVSD}$	V	PFBx- operational	P_4.3.27
Voltage Range VDHP, VDH1, VDH2, VDH3	V_{VDH4}	2.0	–	$V_{VDHOVSD}$	V	VDHP readout-operational	P_4.3.28
Voltage Range VDHP, VDH1, VDH2, VDH3	V_{VDH5}	0.0	–	$V_{VDHOVSD}$	V	CP2 and SCD-operational[12]	P_4.3.29
Voltage Range SHx	V_{fSHx}	-V_{BHSHxx}	–	90V-V_{BHSHxx}	V	–	P_4.3.9
Voltage Difference BHx-SHx	V_{fBS1}	V_{BSUV}	–	V_{fCB}	V	Bootstrap charging	P_4.3.10
Voltage Difference BHx-SHx	V_{fBS2}	V_{BSUV}	–	$V_{BHSHxlim}$	V	CP2 charging	P_4.3.30
Voltage Difference Gxx-Sxx	V_{fGS1}	-0.3	–	15.0	V	–	P_4.3.11
Duty Cycle Range Output Stages	*D.C.*	0	–	100	%	–	P_4.3.12
Voltage Range $\overline{INH}$	V_{AIP1}	-0.3	–	$V_{VCCxOVx}$	V	–	P_4.3.13
Voltage Range $\overline{SOFF}$	V_{AIP2}	-0.3	–	$V_{VCCxOVx}$	V	–	P_4.3.14

10 Power-up to be completed first

11 Max. value will not be exceeded under normal operation condition, voltage class of charge pump capacitor can be selected accordingly

12 At minimum limit charge pumps are operational even if freewheeling current flows via the reverse diode of the external high-side FET

Table 4 Functional Range (continued)

T_j = -40°C to +150°C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage Range $\overline{IHx}$, ILx, ENA, CLK_SPI, CSN, MOSI	V_{DIP2}	-0.3	–	$V_{VCCxOVx}$	V	–	P_4.3.15
Voltage Range PFBx, $\overline{ERR}$, MISO	V_{DOP2}	V_{ERRL} V_{SPIL}	–	V_{ERRHx} V_{SPIHx}	V	–	P_4.3.16
Output Impedance PFBx, $\overline{ERR}$	R_{DOP}	–	50	–	Ω	–	P_4.3.17
Output Impedance MISO	$R_{DOPMISO}$	–	130	–	Ω	–	P_3.3.1
Voltage Range APC	V_{AOP2}	-0.3	–	V_{AOPHx}	V	–	P_4.3.18
Current Range APC	I_{AOP2}	-1	–	1	mA	–	P_4.3.19
Input Voltage Range ISPx, ISNx	V_{fISx}	V_{SSC_CM}	–	V_{SSC_CM}	V	–	P_4.3.20
Differential Voltage Range ISPx, ISNx	$V_{fdiffISx}$	V_{SSC_Idiff}	–	V_{SSC_Idiff}	mV	–	P_4.3.21
Voltage Range VOx	V_{fVOx}	V_{SSC_OVR}	–	V_{SSC_OVR}	V	–	P_4.3.22
Voltage Range VRO	V_{fVRO}	V_{SSC_OVRO}	–	V_{SSC_OVRO}	V	–	P_4.3.24

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4 Input and Output Characteristics

The input and output pins of the TLE9180D-21QK drive the output stages and give feedback to the µC about the state of the gate driver IC, the µC and the state of the inverter stage. Digital in- and outputs are supplied out of VCC and refer to the VCC voltage, general in- and outputs have fixed input threshold and fixed output high levels. Every output stage driving an external FET has its own input pin. Additionally there are 3 different pins to activate or deactivate the output stages. The impact of the 3 pins ENA, $\overline{\text{INH}}$ and $\overline{\text{SOFF}}$ differs from each other regarding to the gate driver IC's reaction. With the SPI interface the TLE9180D-21QK can be configured and diagnostics can be read out by the µC. The $\overline{\text{ERR}}$ pin indicates a failure of the TLE9180D-21QK or the system.

Table 5 I/Os functionality

Name of I/O	Definition	Functionality	Default State
$\overline{\text{INH}}$	General Input	Sleep Mode	Internal pull-down, FETs off passive clamping, Power up/down of device
$\overline{\text{SOFF}}$	General Input	Safe switch off	Internal pull-down, FETs off without reset of error registers, SOFF mode
ILx	Digital Input	Driver input for LS FETs	Internal pull-down, Affected FET off
$\overline{\text{IHx}}$	Digital Input	Driver input for HS FETs	Internal pull-up to VCC, Affected FET off
ENA	Digital Input	Enable and Reset	Internal pull-down, All FETs off
CLK_SPI	Digital Input	SPI	Internal pull-down
MOSI	Digital Input	SPI	Internal pull-down
CSN	Digital Input	SPI	Internal pull-up to VCC
MISO	Digital Output	SPI	Push-pull stage to VCC, Tri-state (Hi-Z) in case of no supply or if deactivated
PFBx	Digital Output	Phase Feedback	Push-pull stage to VCC with internal pull-down
APC	General Output	Driving Phase Cut Off Circuit	Push-pull stage to 5 V with internal pull-down
$\overline{\text{ERR}}$	Digital Output	Diagnostic Output	Push-pull stage to VCC with internal pull-down

5 Serial Peripheral Interface - SPI

The 24-bit Serial Peripheral Interface (SPI) enables a communication link of the µC as SPI-master and the TLE9180D-21QK. The SPI interface is used to configure and to control the gate driver IC and to read out of the status registers.

The SPI interface in the TLE9180D-21QK is a SPI-Slave. It always requires a SPI-Master. This is usually a µC. The master generates the CLK_SPI and CSN signals used for data transfer and its synchronization.

The SPI interface can operate in bus application mode with additional SPI-Slave devices. Daisy Chain is not possible, as incoming data is not passed directly to the output port. The transmission format of incoming and outcoming SPI frames differ.

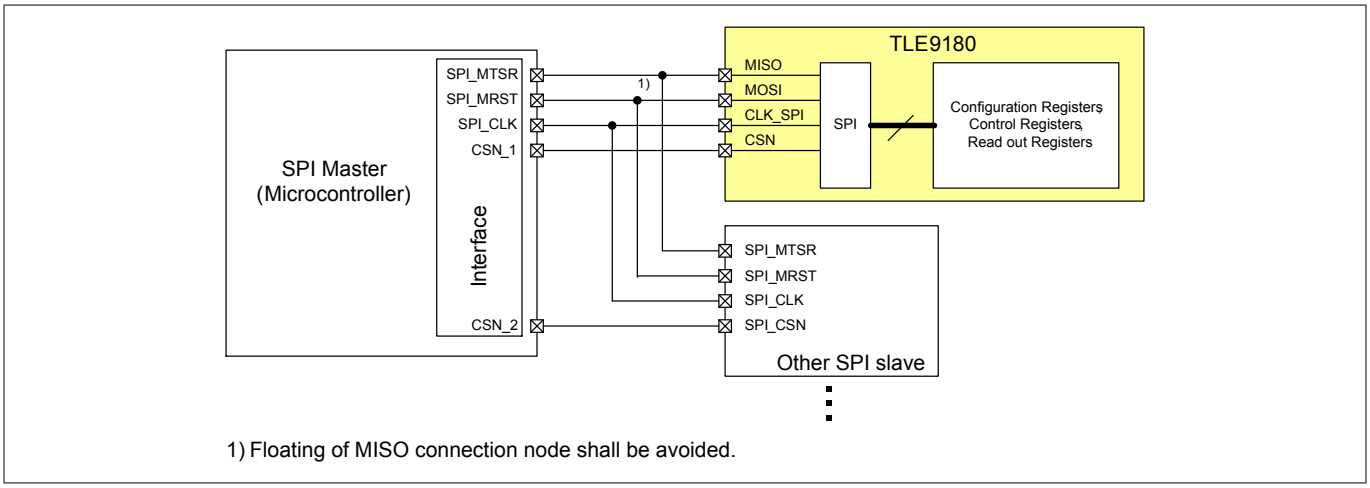


Figure 3 Principle for SPI-Bus Architecture

6 Power Supply

Power to the TLE9180D-21QK is supplied by pins Vs and VCC. The VCC supplies the digital I/O ports. All other supply voltages for the low- and high-side output stages, the digital and analog circuits and the gate voltage to drive the external MOSFETs are generated internally.

Additionally the TLE9180D-21QK is designed to operate with different supply voltages for the gate driver IC pin Vs and the power inverter stage at pin VDHP. Functional limitation of supply voltage differences between pin VDHP and the Vs supply is only their respective maximum ratings. Next to single supply systems typical environment is a boosted system for the power inverter while the gate driver is running with single battery supply voltage or a regulated supply voltage.

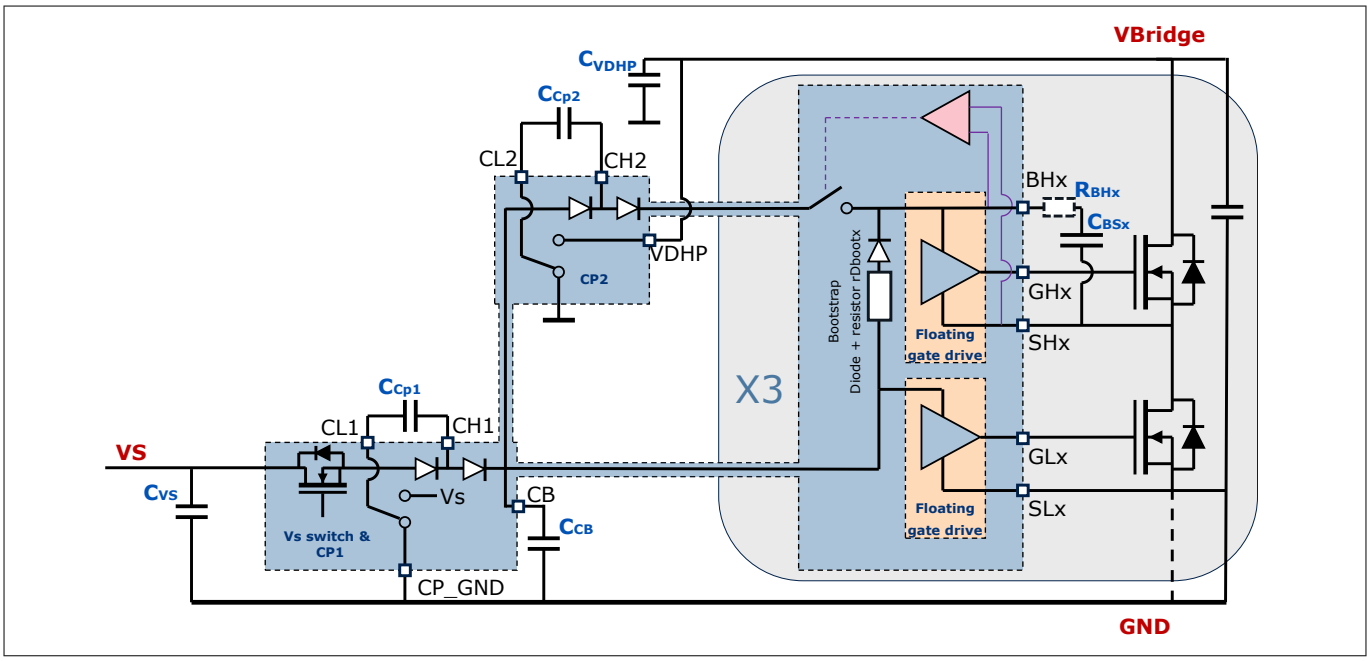


Figure 4 Simplified Block Diagram of Charge Pumps and Floating MOSFET Driver

7 Floating MOSFET Driver

The TLE9180D-21QK provides 6 identical output stages to drive external N-channel MOSFETs in a brushless DC motor configuration. The driving signal for each FET given by the µC will be referenced to the source of every single FET by the integrated level shifters. The pins SLx/SHx are the reference for the floating gate driver output stages. A shoot through protection and dead time control is integrated into the logic. Violation of the input patterns and the correct conversion of the GND related input signal into floating signal by the level shifter will be monitored. Additionally the design and layout of the 6 internal signal paths for gate driving are integrated similar to each other to minimize switching and propagation delay time differences.

8 Shunt Signal Conditioning

The shunt signal conditioning (SSC) incorporates 2 precise current sense amplifiers (CSAs) to amplify the voltage drop at the shunt resistors caused by the motor currents and a voltage reference output buffer (RB), see ***Figure 5***.

The signal conditioning refers to GND. Due to high common mode input voltage range it is robust against sense voltage ringing caused by stray inductances during fast PWM current switching. Due to high common mode functional input voltage range it is robust against high common mode shifts between the GNDs of the shunts and the common GND of the ECU.

High equivalent input resistances, low input offset voltages and low gain error provide an excellent DC performance of the CSAs and therefore minimizes the total error of the shunt signal conditioning.

Additionally, high common mode rejection ratio, high power supply rejection ratio and a low noise figure of the CSAs contribute to minimize the total error of the SSC.

In order to optimize the shunt signal conditioning - especially in systems designed for a wide motor current range with high accuracy requirements at high and low motor currents - different gains can be programmed.

The DC output voltage at the outputs of the CSAs (VOx) for zero differential input voltage is defined by the output of the reference buffer at pin VRO. Therefore, positive and negative currents through the shunt resistor can be amplified by the CSAs and thus measured by the ADC of µC. Three different VRO voltages can be set at the reference buffer RB. Each of the three VRO voltage settings can be fine tuned.

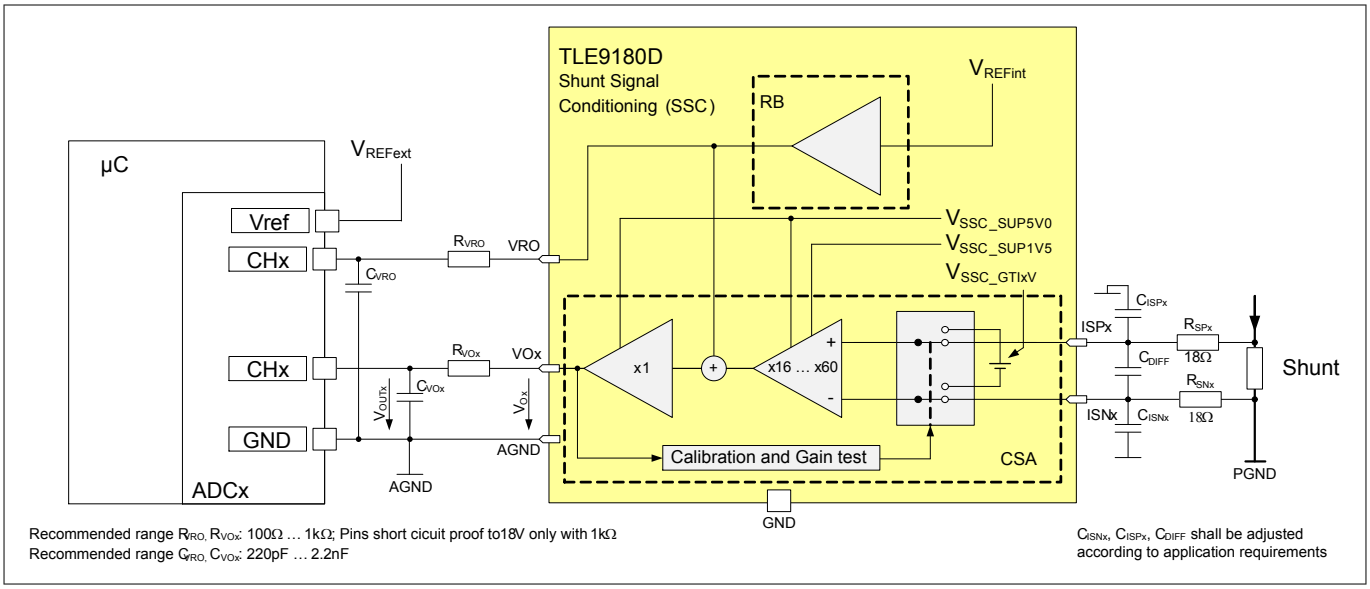


Figure 5 Simplified Block- and Application Diagram of the Shunt Signal Conditioning

9 Protection and Diagnostics

The TLE9180D-21QK provides extended protection and monitoring functions. All detected errors and warnings can be read by SPI, most of the thresholds are selectable by SPI configuration or SPI command. Safety relevant diagnostics can be tested during operation in a dedicated self-test mode.

9.1 Supervision Overview

The following diagnostics and read out functions are available.

Table 6 Diagnostic overview

Diagnostic	Availability in Configuration	Availability in reduced operation	Availability with SOFF=low	Test of Diagnosis Function
Power Supply Supervision and Diagnostics				
Overvoltage VS (Programmable Threshold)	yes (default value)	no	yes	no
Overvoltage VS shutdown	yes	no	yes	no
Undervoltage VS (Programmable Threshold)	yes (default value)	no	yes	no
VS Read Out	yes	no	yes	no
Overvoltage VDHP (Programmable Threshold)	yes (default value)	no	yes	no
Overvoltage LD VDHP	yes (default value)	no	yes	no
Overvoltage VDHP Shutdown	yes	no	yes	no
Undervoltage VDHP (Programmable Threshold)	yes (default value)	no	yes	no
VDHP Read Out	yes	no	yes	no
VCC Under- and Over Monitoring	yes	no	yes	yes
VCC Read Out	yes	no	yes	no
Output Stage Power Supply Supervision				
Undervoltage Charge Pump CB Shutdown	yes	no	yes	no
Undervoltage Charge Pump CB (prog. threshold)	yes (default value)	no	yes	no
CB Read Out	yes	no	yes	no
Overvoltage Charge Pump 1	yes	no	yes	no
Overvoltage Charge Pump 2 CH2-CL2	yes	no	yes	no
Overload Vs	yes	no	yes	no
Overload Charge Pump 1	yes	no	yes	no

Table 6 Diagnostic overview (continued)

Diagnostic	Availability in Configuration	Availability in reduced operation	Availability with SOFF=low	Test of Diagnosis Function
Overload Charge Pump 2	yes	no	yes	no
Undervoltage High-side Buffer Capacitor BHx-SHx	yes	no	yes	no
Overvoltage High-side Buffer Capacitor BHx-SHx	yes	no	yes	no
Gate Driver Internal Supervisions				
Internal Power Supply Monitoring	yes	no	yes	no
Clock Supervision (internal clock)	yes	no	yes	no
Overtemperature Shutdown	yes	no	yes	no
Overtemperature Detection (Programmable Threshold)	yes (default value)	no	yes	no
Temperature Read out	yes	no	yes	no
CSA Diagnostics	no	no	no	n.a.
Output Stage Status Feedback Information	no	no	yes	no
Digital Driving Path Monitoring	yes	no	yes	no
Latent Fault Warning Monitoring	yes	no	yes	no
Bridge and FET Diagnostics and Protection				
Shoot Through Protection	n.a.	n.a.	n.a.	n.a.
SCD Failure	no	no	no	yes
FET Drain Source Voltage Read out	n.a.	n.a.	n.a.	n.a.
FET Reverse Diode Forward Voltage Read out	n.a.	n.a.	n.a.	n.a.
Overcurrent Detection	yes	no	yes	no
Drain Source Measurement	no	no	no	n.a.
Interface to µC Supervision				
Input Pattern Violation Monitoring	n.a.	n.a.	n.a.	no
Overload Digital Output Pins	yes	no	yes	no
Configuration Signature Invalid	yes	yes	yes	no

Table 6 Diagnostic overview (continued)

Diagnostic	Availability in Configuration	Availability in reduced operation	Availability with SOFF=low	Test of Diagnosis Function
Configuration Time-out	yes	no		no
SPI Frame Error	yes	n.a.	yes	no
SPI Frame Time-out	yes	n.a.	yes	no
SPI Window Watchdog Time-out	no	no	yes	n.a.
CRC error (incoming data)	yes	n.a.	yes	no
Invalid Address Access	yes	n.a.	yes	no

10 Digital Phase Voltage Feedback

The TLE9180D-21QK incorporates a fast conversion of the phase voltages into logic level signals. Its threshold values are proportional to the voltage at pin VDHP as long as the VDHP voltage is below 60 V and stays above 4.0 V. The outputs are VCC push-pull stages with an internal pull down resistor. The phase voltage feedback is realized functional independent to the core logic. If the digital phase feedback is not used the output pins shall be open.

11 Operation Modes

This chapter describes the different operation modes.

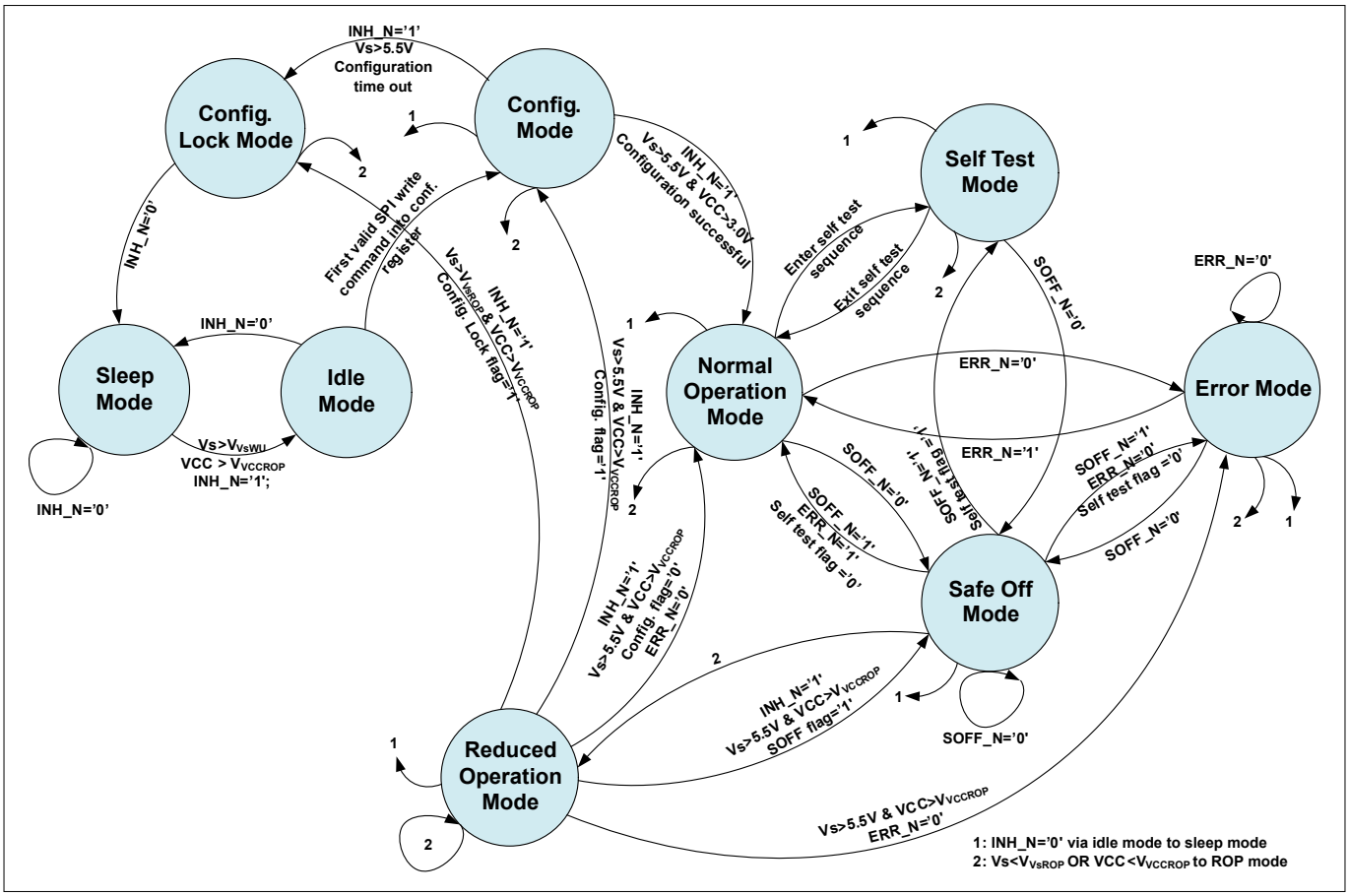


Figure 6 Overview of Digital Operation Modes

12 Application Information

In this application 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

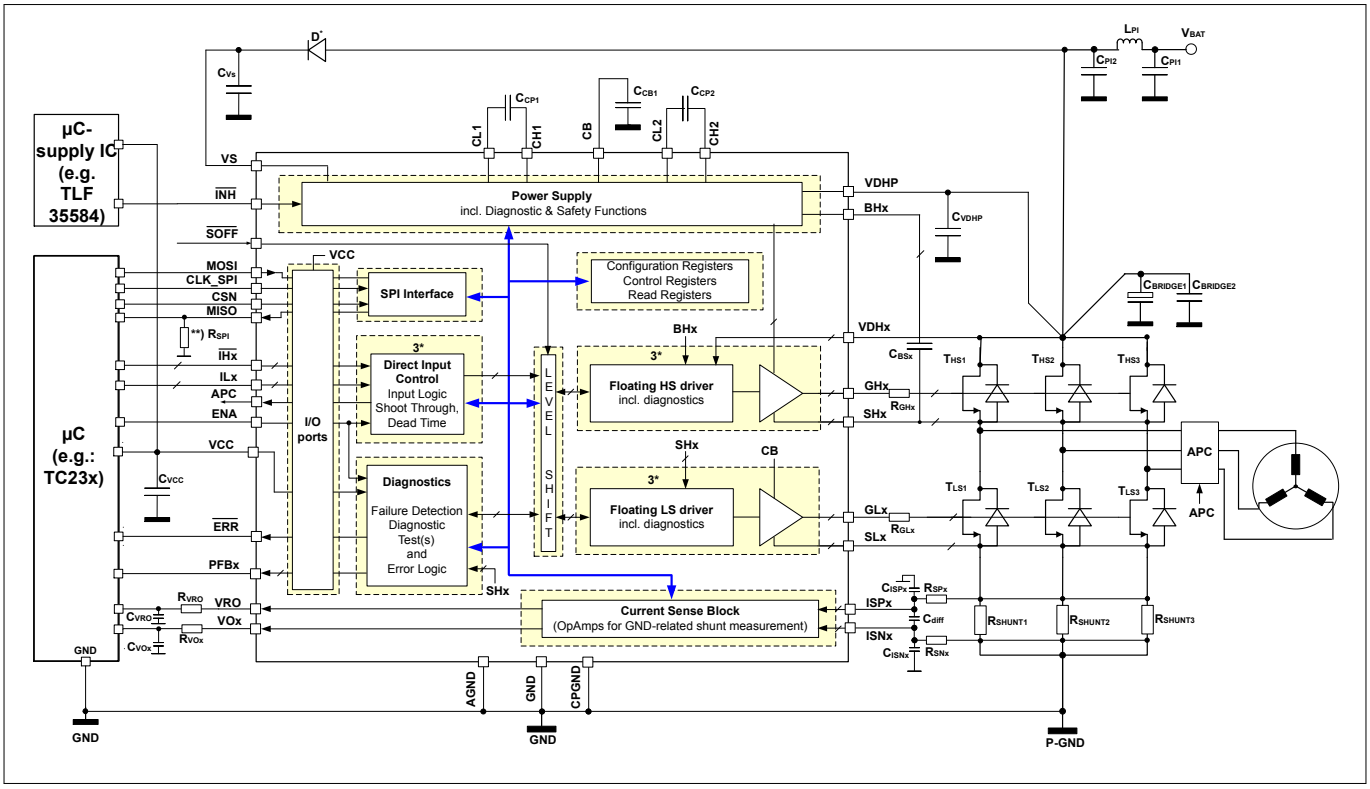
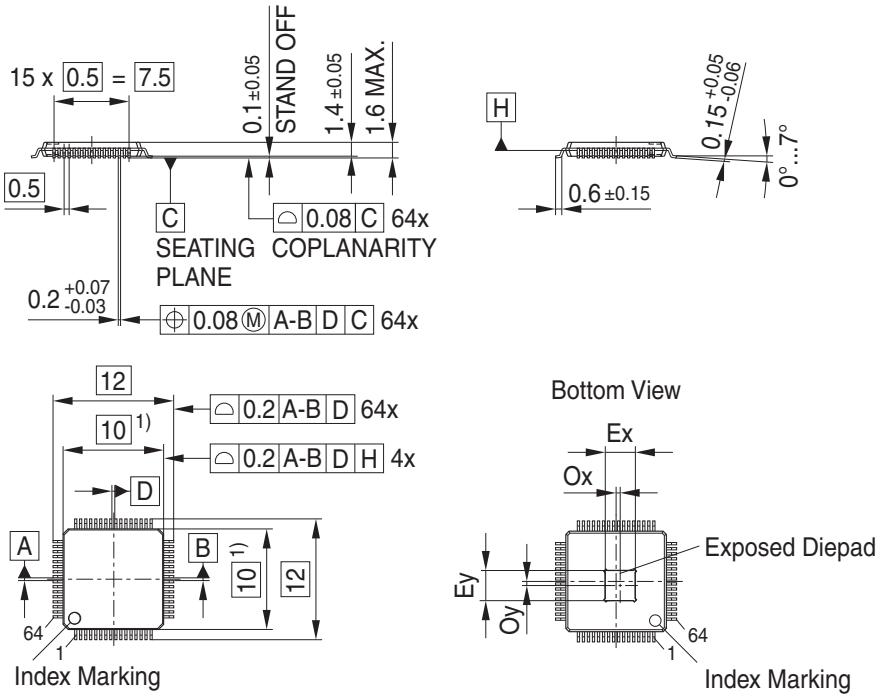


Figure 7 Simplified Application Circuit

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

13 Package Outlines



1) Does not include plastic or metal protrusion of 0.25 max. per side

EXPOSED DIEPAD DIMENSIONS				
PACKAGE	Ex	Ey	Ox	Oy
PG-LQFP-64	4.5	4.5	0.0	0.0

Figure 8 PG-LQFP-64

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

Revision History

Revision	Date	Changes
1.0	2019-03-15	Initial product summary

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