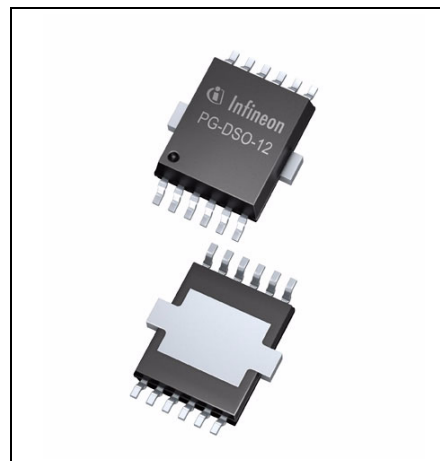




## Features

- Dual output  
5 V ( $\pm 2\%$ ), 215mA and 2.6 V<sup>1)</sup> ( $\pm 4\%$ ), 200mA or  
5 V ( $\pm 2\%$ ), 215mA and 3.3 V ( $\pm 3\%$ ), 200mA
- Ultra low quiescent current consumption  $< 55 \mu\text{A}$
- Inhibit function
- Very low dropout voltage
- Reset with power-on delay
- Early Warning comparator
- Window watchdog
- Power sequencing for dual voltage  $\mu\text{C}$
- Output protected against short circuit
- Wide operation range: up to 45 V
- Wide temperature range:  $-40^\circ\text{C}$  to  $150^\circ\text{C}$
- Overtemperature protection
- Overload protection
- Green Product (RoHS compliant)
- AEC Qualified



## Functional Description

The TLE 7469 is a monolithic integrated voltage regulator with two voltage outputs specially designed to supply microcontrollers with dual supply voltage: 2.6 V<sup>1)</sup> or 3.3 V core and 5 V I/O voltage like the Infineon XC164 and XC161.

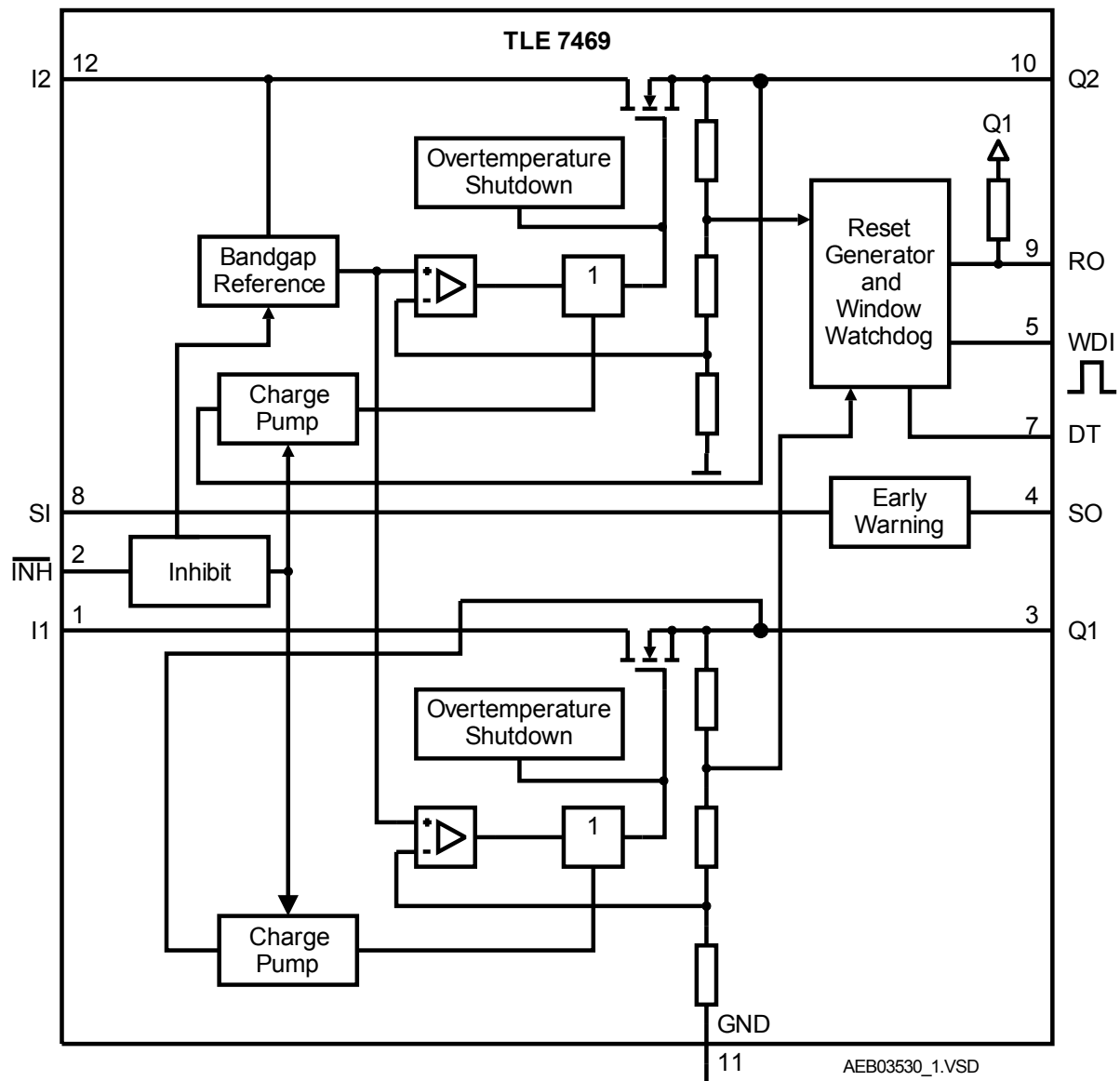
1) 2.5 V nominal specification range of most  $\mu\text{Cs}$  is compatible with the 2.6 V output voltage range of the TLE 7469.

Type	Package
TLE 7469 GV52	PG-DSO-12
TLE 7469 GV53	PG-DSO-12

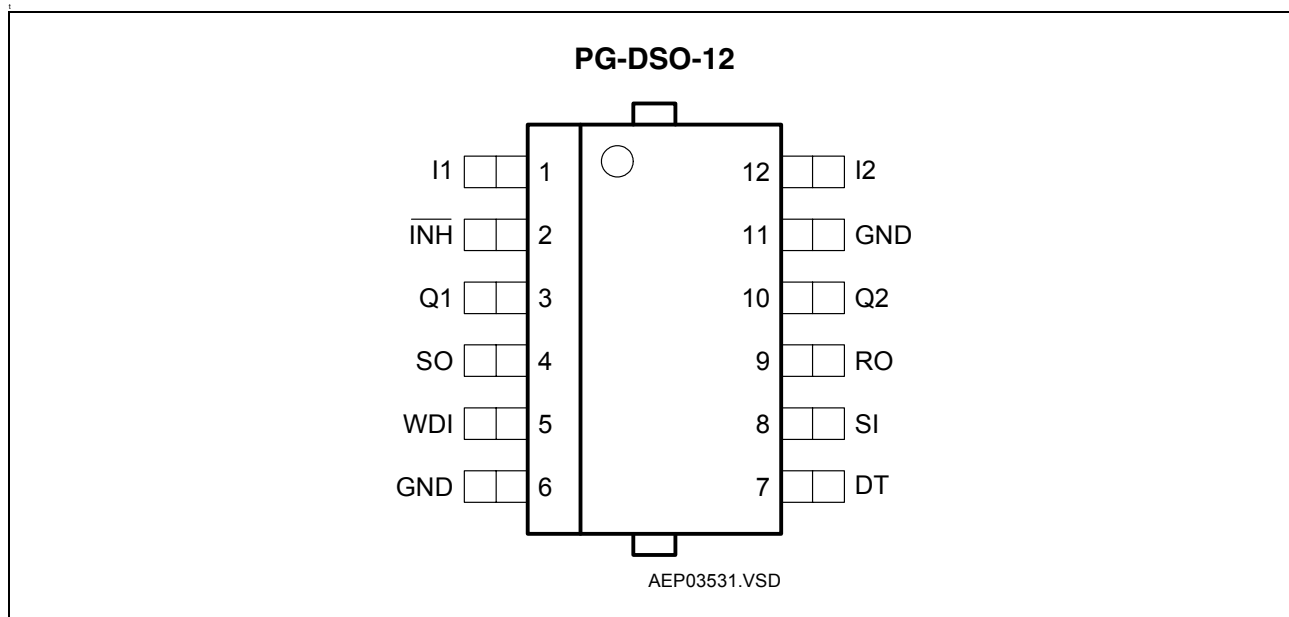
The voltage regulator features an integrated reset circuitry which monitors the 2.6 V/ 3.3 V supply voltage. At power on the reset checks both supply voltages and performs the power-on reset with an adjustable delay time. The voltage difference is kept in the range  $-0.5 \text{ V} < (V_{Q1} - V_{Q2}) < 3.0 \text{ V}$  even during power-on and power-down time enabling save  $\mu\text{C}$  operation without external clamping. Using the integrated early warning comparator an external voltage can be supervised. An integrated output sink current circuitry keeps the voltage at the Q1 pin below 5.5 V even when reverse currents are applied. Thus connected devices are protected from overvoltage damage. The regulator can be shut down via the Inhibit input causing the current consumption to drop below  $9 \mu\text{A}$ .

The TLE 7469 is designed for use under the severe conditions of automotive applications, and is therefore equipped with protection functions against overload, short circuit and overtemperature. It operates in the wide junction temperature range from  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  and offers the low quiescent current consumption required for body applications.

For applications requiring extremely low noise levels the Infineon voltage regulator family TLE 42XY and TLE 44XY is more suited than the TLE 7469. A mV-range output noise on the TLE 7469 caused by the charge pump operation is unavoidable due to the ultra low quiescent current concept.



**Figure 1** Block Diagram



**Figure 2** Pin Configuration (top view)

**Table 1** Pin Definitions and Functions

Pin No.	Symb.	Function
1	I1	<b>Input voltage 1</b> ; block to ground directly at the IC with a 100 nF ceramic capacitor
2	INH	<b>Inhibit Input</b> ; low level disables the IC. Integrated pull-down resistor
3	Q1	<b>Output voltage 1</b> ; 5.0 V, block to GND with a capacitor $C_{Q1} \geq 1 \mu\text{F}$ , ESR < 6 $\Omega$ at 10 kHz
4	SO	<b>Sense output</b> ; Output of Early Warning Comparator, open collector output
5	WDI	<b>Watchdog Input</b> ; Trigger Input for Watchdog pulses
6, 11	GND	<b>Ground</b> ; Pin 6, 11 and heat slug must be connected to GND
7	DT	<b>DT Delay timing</b> ; connect to GND, Q1 or Q2 to select Reset and Watchdog timing
8	SI	<b>Sense input</b> ; Input for Early Warning comparator
9	RO	<b>Reset output</b> ; open collector output with integrated 20 k $\Omega$ pull-up resistor
10	Q2	<b>Output voltage 2</b> ; 2.6 V (TLE 7469 GV52), 3.3 V (TLE 7469 GV53); block to GND with a capacitor $C_{Q2} \geq 1 \mu\text{F}$ , ESR < 6 $\Omega$ at 10 kHz
12	I2	<b>Input voltage 2</b> ; block to ground directly at the IC with a 100 nF ceramic capacitor

**Table 2 Absolute Maximum Ratings**
 $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ 

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input I1					
Voltage	$V_{I1}$	-0.3	45	V	–
Current	$I_{I1}$	–	–	mA	Internally limited
Input I2					
Voltage	$V_{I2}$	-0.3	45	V	–
Current	$I_{I2}$	–	–	mA	Internally limited
Output Q1					
Voltage	$V_{Q1}$	-0.3	5.5	V	Permanent
Voltage	$V_{Q1}$	-0.3	6.2	V	$t < 10\text{ s}^{1)}$
Current	$I_{Q1}$	–	2	mA	Internally limited
Output Q2					
Voltage	$V_{Q2}$	-0.3	5.5	V	Permanent
Voltage	$V_{Q2}$	-0.3	6.2	V	$t < 10\text{ s}^{1)}$
Current	$I_{Q2}$	–	–	mA	Internally limited
Inhibit Input $\overline{\text{INH}}$					
Voltage	$V_{\overline{\text{INH}}}$	-0.3	45	V	Observe current limit $I_{\overline{\text{INHmax}}}^{2)}$
Current	$I_{\overline{\text{INH}}}$	-1	1	mA	–
Reset Output RO					
Voltage	$V_{\text{RO}}$	-0.3	5.5	V	Permanent
Voltage	$V_{\text{RO}}$	-0.3	6.2	V	$t < 10\text{ s}^{1)}$
Current	$I_{\text{RO}}$	–	–	mA	internally limited
Delay Timing DT					
Voltage	$V_{\text{DT}}$	-0.3	5.5	V	Permanent
Voltage	$V_{\text{DT}}$	-0.3	6.2	V	$t < 10\text{ s}^{1)}$
Current	$I_{\text{DT}}$	-5	5	mA	–

**Table 2 Absolute Maximum Ratings (cont'd)**
 $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$ 

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Watchdog Input WDI					
Voltage	$V_{\text{WDI}}$	-0.3	5.5	V	Permanent
Voltage	$V_{\text{WDI}}$	-0.3	6.2	V	$t < 10 \text{ s}^{1)}$
Current	$I_{\text{WDI}}$	–	–	mA	internally limited
Sense Input SI					
Voltage	$V_{\text{SI}}$	-0.3	45	V	Observe current limit $I_{\text{SI} \max}^{2)}$
Current	$I_{\text{SI}}$	-1	1	mA	–
Sense Output SO					
Voltage	$V_{\text{SO}}$	-0.3	5.5	V	Permanent
Voltage	$V_{\text{SO}}$	-0.3	6.2	V	$t < 10 \text{ s}^{1)}$
Current	$I_{\text{SO}}$	–	–	mA	internally limited
Temperatures					
Junction temperature	$T_{\text{j}}$	–	150	°C	–
Storage temperature	$T_{\text{stg}}$	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods ( $t > 10\text{ s}$ ) may affect device reliability.

2) External resistor required to keep current below absolute maximum rating when voltages  $\geq 5.5\text{ V}$  are applied.

*Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.*

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	$V_{I1}$	5.6	45	V	–
Input voltage	$V_{I2}$	6.0	45	V	$V_{I1} > 8V$
Input voltage	$V_{I2}$	4.2	45	V	$V_{I1} < 8V$
Junction temperature	$T_j$	-40	150	°C	–

**Thermal Resistances PG-DSO-12**

Junction case	$R_{thjc}$	–	4.4	K/W	–
Junction ambient	$R_{thj-a}$	–	107	K/W	PCB, only Footprint <sup>1)</sup>
Junction ambient	$R_{thj-a}$	–	58	K/W	PCB Heat Sink Area 300 mm <sup>2</sup> <sup>1)</sup>
Junction ambient	$R_{thj-a}$	–	48	K/W	PCB Heat Sink Area 600 mm <sup>2</sup> <sup>1)</sup>

1) Package mounted on PCB 80 × 80 × 1.5 mm<sup>3</sup>; 35μ Cu; 5μ Sn; zero airflow; 85 °C ambient temperature.

*Note: In the operating range the functions given in the circuit description are fulfilled.*

**Table 4 Electrical Characteristics**
 $V_{I1} = 13.5 \text{ V}; V_{I2} = 13.5 \text{ V}; -40 \text{ }^{\circ}\text{C} < T_j < 150 \text{ }^{\circ}\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output Q1						
Output voltage	$V_{Q1}$	4.90	5.0	5.10	V	$1\text{ mA} < I_{Q1} < 215\text{ mA}$ , $6\text{ V} < V_{I1} < 16\text{ V}$
Output current limitation	$I_{Q1}$	320	–	700	mA	$V_{Q1} = 4.0\text{ V}$
Output drop voltage; $V_{DRQ1} = V_{I1} - V_{Q1}$	$V_{DRQ1}$	–	300	600	mV	$I_{Q1} = 215\text{ mA}^{1)}$
Load regulation	$\Delta V_{Q1,Lo}$	–	25	60	mV	$1\text{ mA} < I_{Q1} < 215\text{ mA}$
Line regulation	$\Delta V_{Q1,Li}$	–	20	50	mV	$I_{Q1} = 1\text{ mA}$ , $10\text{ V} < V_I < 28\text{ V}$
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	$f_r = 100\text{ Hz}$ , $V_r = 1\text{ Vpp}$
Reverse Output Current Protection	$V_{Q,REV}$	–	–	5.5	V	$I_{Q,REV} = 1\text{ mA}$ , $V_{INH} = 0\text{ V}$
Output Q2						
Output voltage	$V_{Q2}$	2.50	2.60	2.70	V	$1\text{ mA} < I_{Q2} < 200\text{ mA}$ , $6\text{ V} < V_{I2} < 16\text{ V}$ , TLE 7469 GV52
Output voltage	$V_{Q2}$	3.20	3.30	3.40	V	$1\text{ mA} < I_{Q2} < 200\text{ mA}$ , $6\text{ V} < V_{I2} < 16\text{ V}$ , TLE 7469 GV53
Absolute differential voltage	$V_{Q1} - V_{Q2}$	-0.5	–	3.0	V	$V_{Q1}, V_{Q2} > 1\text{ V}$
Output current limitation	$I_{Q2}$	300	–	550	mA	$V_{Q2} = 2.0\text{ V}$
Load regulation	$\Delta V_{Q2,Lo}$	–	25	60	mV	$1\text{ mA} < I_{Q2} < 200\text{ mA}$
Line regulation	$\Delta V_{Q22,Li}$	–	20	50	mV	$I_{Q2} = 1\text{ mA}$ , $10\text{ V} < V_I < 28\text{ V}$
Power Supply Ripple Rejection	$PSRR$	–	60	–	dB	$f_r = 100\text{ Hz}$ , $V_r = 1\text{ Vpp}$



**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{I2} = 13.5 \text{ V}; -40 \text{ }^{\circ}\text{C} < T_j < 150 \text{ }^{\circ}\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Current Consumption						
Quiescent current; $I_q = I_{I1} + I_{I2} - I_{Q1} - I_{Q2}$	$I_q$	—	—	55	μA	$I_{Q2} = I_{Q1} = 100\text{ }\mu\text{A}$ , $T_j < 80\text{ }^{\circ}\text{C}$
Quiescent current; inhibited	$I_q$	—	5	9	μA	$V_{\overline{\text{INH}}} = 0\text{ V}$ , $T_j < 80\text{ }^{\circ}\text{C}$
Inhibit Input $\overline{\text{INH}}$						
Turn-on Voltage	$V_{\overline{\text{INH}}\text{ ON}}$	—	—	3.1	V	$V_{Q1}$ & $V_{Q2}$ on
Turn-off Voltage	$V_{\overline{\text{INH}}\text{ OFF}}$	0.8	—	—	V	$V_{Q1}$ & $V_{Q2}$ off
H-input current	$I_{\overline{\text{INH}}\text{ ON}}$	—	3	4	μA	$V_{\overline{\text{INH}}} = 5\text{ V}$
L-input current	$I_{\overline{\text{INH}}\text{ OFF}}$	—	0.5	1	μA	$V_{\overline{\text{INH}}} = 0\text{ V}$ , $T_j < 80\text{ }^{\circ}\text{C}$
Delay Timing DT						
Threshold Fast Timing Select	$V_{\text{DT,FAST}}$	4.5	—	—	V	—
Threshold Slow Timing Select	$V_{\text{DT,SLOW}}$	2.3	—	3.3	V	TLE 7469 GV52
Threshold Slow Timing Select	$V_{\text{DT,SLOW}}$	2.3	—	3.6	V	TLE 7469 GV53
Threshold Watchdog Turn Off <sup>2)</sup>	$V_{\text{DT,OFF}}$	—	—	0.8	V	—
Watchdog Input WDI						
H-input voltage threshold	$V_{\text{WDIH}}$	—	—	3.0	V	—
L-input voltage threshold	$V_{\text{WDIL}}$	—	—	0.8	V	—
Watchdog sampling time	$t_{\text{sam}}$	0.20	0.25	0.30	ms	Fast Timing
		0.80	1.00	1.20	ms	Slow Timing
Ignore window time	$t_{\text{OW}}$	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing
Open window time	$t_{\text{OW}}$	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing

**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{I2} = 13.5 \text{ V}; -40 \text{ }^{\circ}\text{C} < T_j < 150 \text{ }^{\circ}\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Closed window time	$t_{CW}$	25.6	32.0	38.4	ms	Fast Timing
		102	128	154	ms	Slow Timing
Window watchdog trigger time	$t_{WD}$	39.0	44.8	50.6	ms	Fast Timing
		156	179	202	ms	Slow Timing

**Reset Output RO**

Reset switching threshold 2	$V_{RT2}$	2.35	2.38	2.48	V	TLE 7469 GV52, $V_{Q2}$ decreasing
Reset Headroom 2	$V_{RH2}$	130	190		mV	TLE 7469 GV52
Reset switching threshold 2	$V_{RT2}$	3.00	3.07	3.15	V	TLE 7469 GV53, $V_{Q2}$ decreasing
Reset Headroom 2	$V_{RH2}$	165	240		mV	TLE 7469 GV53
Reset hysteresis 2	$V_{RH2}$	–	45	–	mV	TLE 7469 GV52 <sup>3)</sup>
		–	60	–	mV	TLE 7469 GV53 <sup>4)</sup>
Reset switching threshold 1	$V_{RT1}$	4.50	4.65	4.80	V	$V_{Q1}$ decreasing
Reset hysteresis 1	$V_{RH1}$	–	90	–	mV	–
Reset sink current	$I_{RO}$	–	–	1	mA	$V_Q = 5 \text{ V}, V_{RO} = 0.5 \text{ V}$
Reset output low voltage	$V_{ROL}$	–	0.15	0.25	V	$V_{Q2} \geq 1 \text{ V}$
Reset high voltage	$V_{ROH}$	4.5	–	–	V	–
Integrated reset pull-up resistor	$R_{RO}$	10	20	40	k $\Omega$	Internally connected to Q1
Power-up Reset delay time	$T_{RD}$	6.0	8.0	10.0	ms	Fast Timing ( $V_{DT} \geq 4.5 \text{ V}$ )
		24.0	32.0	40	ms	Slow Timing ( $V_{DT} \leq 3.3 \text{ V}$ )
Reset Reaction Time	$T_{RR}$	–	10	26	$\mu\text{s}$	–

**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{I2} = 13.5 \text{ V}; -40 \text{ }^{\circ}\text{C} < T_j < 150 \text{ }^{\circ}\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage Sense						
Sense threshold high	$V_{SIH}$	1.10	1.16	1.22	V	$V_{SI}$ increasing (see <a href="#">Figure 4</a> )
Sense threshold low	$V_{SIL}$	1.06	1.12	1.18	V	$V_{SI}$ decreasing (see <a href="#">Figure 4</a> )
Sense output low voltage	$V_{SOL}$	–	0.1	0.4	V	$V_{SI} < 1.01 \text{ V};$ $V_{I1} > 4.20 \text{ V};$ $I_{SO} = 0.5 \text{ mA}$
External SO pull-up resistor	$R_{SO \text{ ext}}$	9.2	–	–	kΩ	$V_{Q1} = 5\text{V}$
Sense input current	$I_{SI}$	-1	0.1	1	μA	$V_{SI} = 5 \text{ V}$
Sense high reaction time	$t_{pd \text{ SO LH}}$	–	4.0	–	μs	–
Sense low reaction time	$t_{pd \text{ SO HL}}$	–	4.0	–	μs	–

1) Measured when the output voltage has dropped 100 mV from the nominal Value obtained at  $V_{I1} = 13.5 \text{ V}$ ,  $V_{I2} = 13.5 \text{ V}$ .

2) Watchdog off, Reset in slow mode.

3) Specified by design, not subject of production test.

4) Specified by design, not subject of production test.

[illegible]

A typical application of the TLE 7469 is shown in [Figure 3](#). To prevent the regulation loop from oscillating a ceramic capacitor of  $C_{Q1/2} \geq 1 \mu F$  is required at each of the outputs Q1 and Q2. In contrast to most low drop voltage regulators the TLE 7469 only needs moderate capacitance at the outputs and tolerates ceramic capacitors to keep the stability. This offers more design flexibility to the circuit designer enabling the IC also to operate without tantalum capacitors.

A general recommendation is to keep the drop over the equivalent serial resistor (ESR) together with the discharge of the blocking capacitor below the Reset Headroom (e.g. min. 130mV for the 2.6V Output).

Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as follows:

$$dV_{C_B} = dI_Q \cdot dt / C_B$$

The drop across the ESR calculates as:

$$dV_{ESR} = dI \cdot ESR$$

To prevent a reset the following relationship must be fulfilled:

$$dV_C + dV_{ESR} < V_{RH2} = 130mV$$

Example: Assuming a load current step of  $dI_Q = 50mA$ , a blocking capacitor of  $C_Q = 22\mu F$  and a typical regulator reaction time under normal operating conditions of  $dt \sim 25\mu s$  and for special dynamic load conditions, such as load step from very low base load, a reaction time of  $dt \sim 75\mu s$ .

$$dV_C = dI_Q \cdot dt / C_B = 50mA \cdot 25\mu s / 22\mu F = 54mV$$

So for the ESR we can allow

$$dV_{ESR} = V_{RH2} - dV_C = 130mV - 54mV = 76mV$$

The permissible ESR becomes:

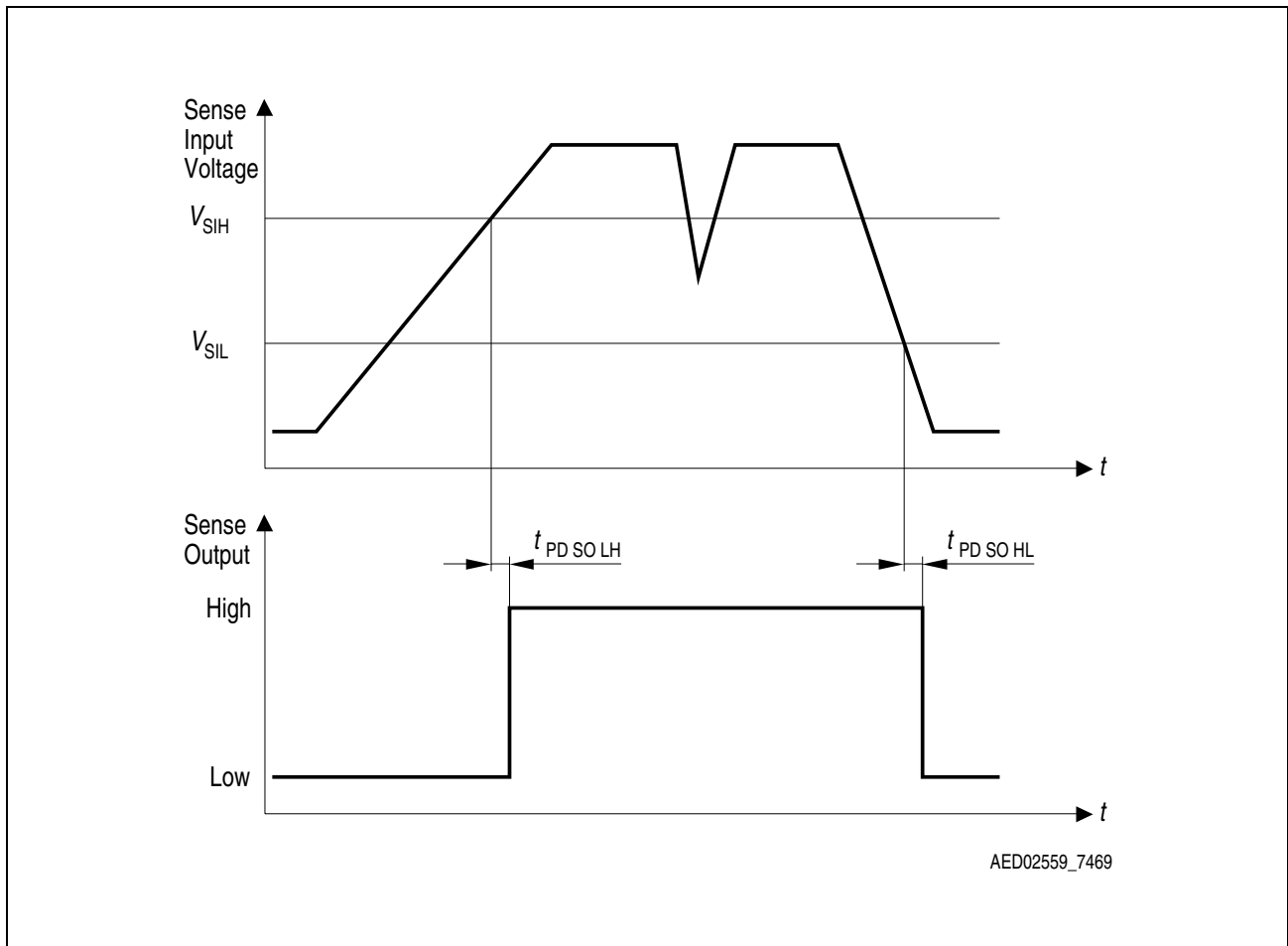
$$ESR = dV_{ESR} / dI_Q = 76mV / 50mA = 1.52\Omega$$

During design-in of the TLE7469 product family, special care needs to be taken with regards to the regulators reaction time to sudden load current changes starting from very low pre-load as well as cyclic load changes. The application note "*TLE7x Voltage Regulators - Application Note about Transient Response at ultra low quiescent current Voltage Regulators*" (see 3\_cip05405.pdf) gives important hints for successful design-in of the Voltage Regulators of the TLE7x family.

As a dual regulator the TLE 7469 for correct operation should be always supplied at both input pins I1 and I2 out of one voltage supply. The dual voltage regulator with both inputs accessible, offers the possibility to reduce the power dissipation in the package. This can be achieved by two different input voltages or a Drop Resistor\*  $R_{Vi}$  (see [Figure 3](#)) at the input pin I2 for the 2.6V output. If one of this options is chosen, care should be taken, to apply the device as described under "Table 3: Operating Range".

The reset output RO features an integrated pull-up resistor. Thus it can be directly coupled to the microcontroller reset input.

The sense comparator output SO is an open collector. An appropriate external pull-up resistor is typ. 5.6 k $\Omega$  ... 47 k $\Omega$ , the minimum value of 5.6 k $\Omega$  being defined by the max. sink current capability of the SO output transistor. If the sense comparator is not used the pull-up resistor can be spared. In this case the SI pin should be directly connected to Q1 in order to keep the comparator inactive.



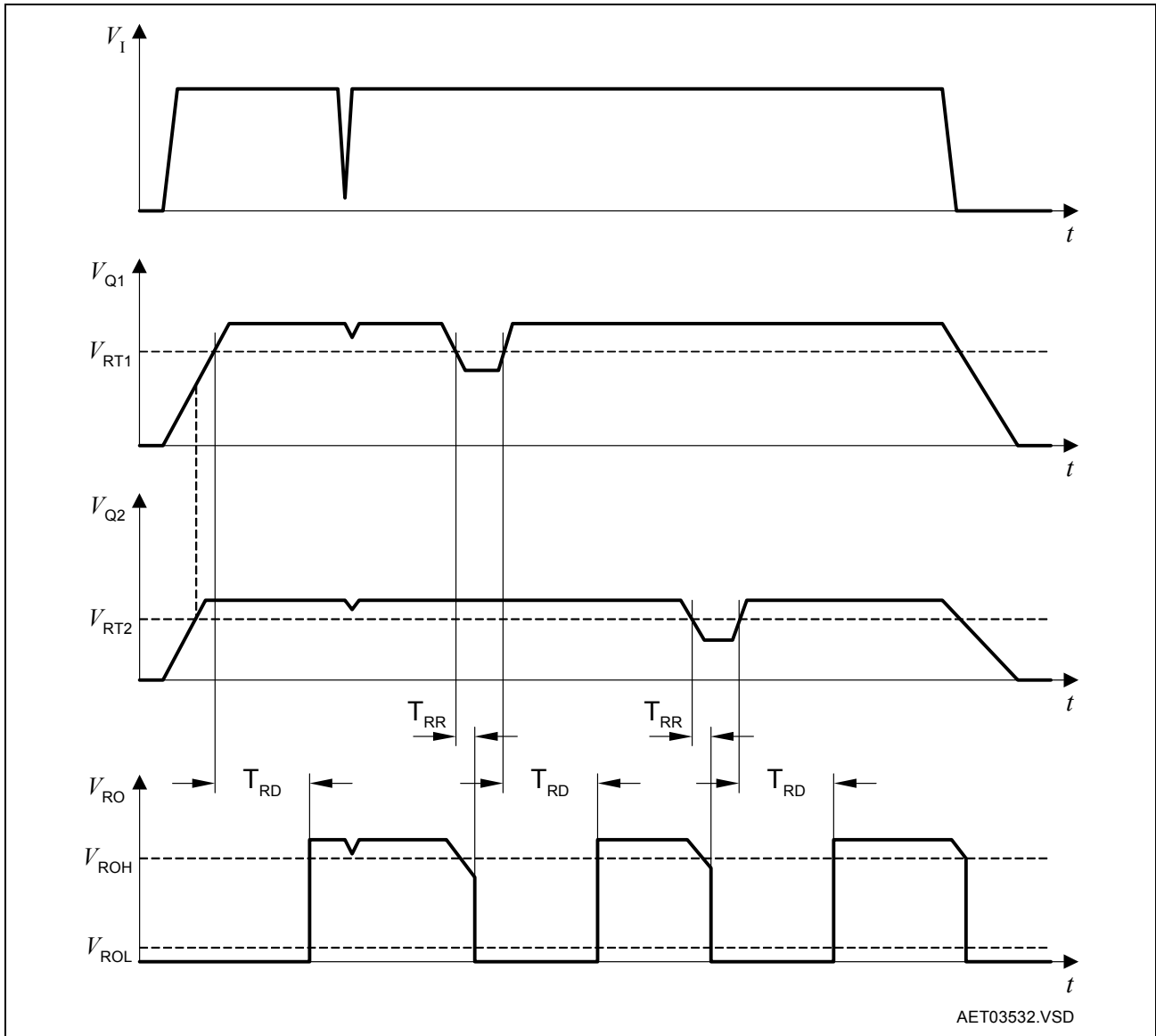
**Figure 4**      **Sense Timing Diagram**

## Circuit Description

### Power On Reset

In order to avoid any system failure, a sequence of several conditions has to be passed. When the level of  $V_{Q2}$  reaches the reset threshold  $V_{RT}$ , the signal at RO remains LOW for the Power-up reset delay time  $T_{RD}$ . Then a second comparator checks whether  $V_{Q1} \geq V_{RT1}$  and only if this test is passed the reset output is switched to HIGH. The Reset output is only released (set to High level) if both output voltages have passed their specific reset threshold  $V_{RT1/2}$ . The reset function and timing is illustrated in [Figure 5](#).

The reset reaction time  $T_{RR}$  avoids wrong triggering caused by short “glitches” on the  $V_{Q2}$ -line. For power-fail, in case of  $V_{Q2}$  or  $V_{Q1}$  power down ( $V_{Q2} < V_{RT2}$  or  $V_{Q1} < V_{RT1}$  for  $t > T_{RR}$ ) a logic LOW signal is generated at the pin RO to reset an external microcontroller.



**Figure 5 Reset Function and Timing Diagram**

### Watchdog Operation

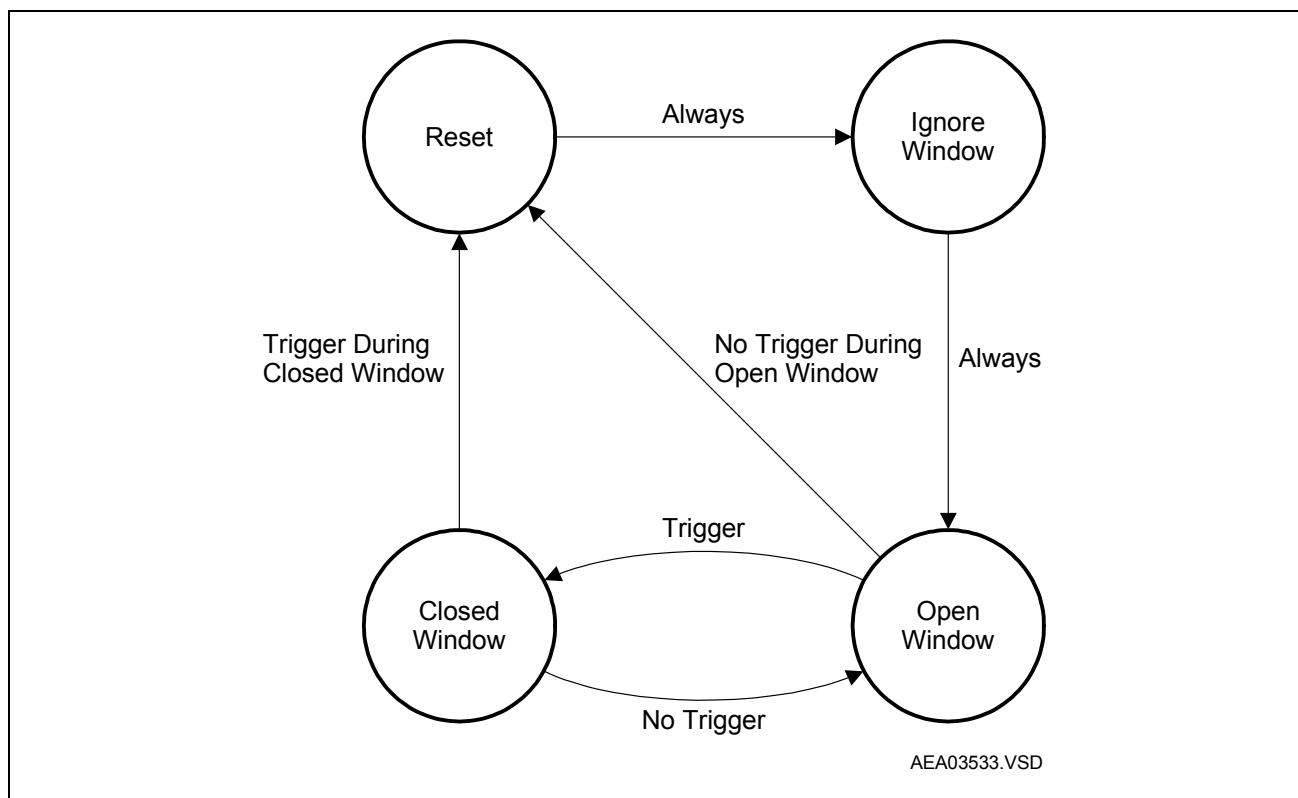
The watchdog uses a fraction of the charge pump oscillator's clock signal as timebase. Connecting the DT pin to Q1 or to Q2 the watchdog timebase can be adjusted. The watchdog can be turned off by a low level ( $V_{DT} \leq 0.8 \text{ V}$ ) applied to the DT pin. The timing values used in this text refer to typ. values with DT connected to Q1 (fast timing).

**Figure 6** shows the state diagram of the window watchdog (WWD). After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time  $T_{RD}$  of typ. 8 ms. With the LOW to HIGH transition of the signal at RO the device starts the ignore window time  $t_{CW}$  (32 ms). During this window the signal at the WDI pin is ignored. Next the WWD starts the open window. When a valid trigger signal is detected during the open window a closed window is initialized immediately. A trigger signal within

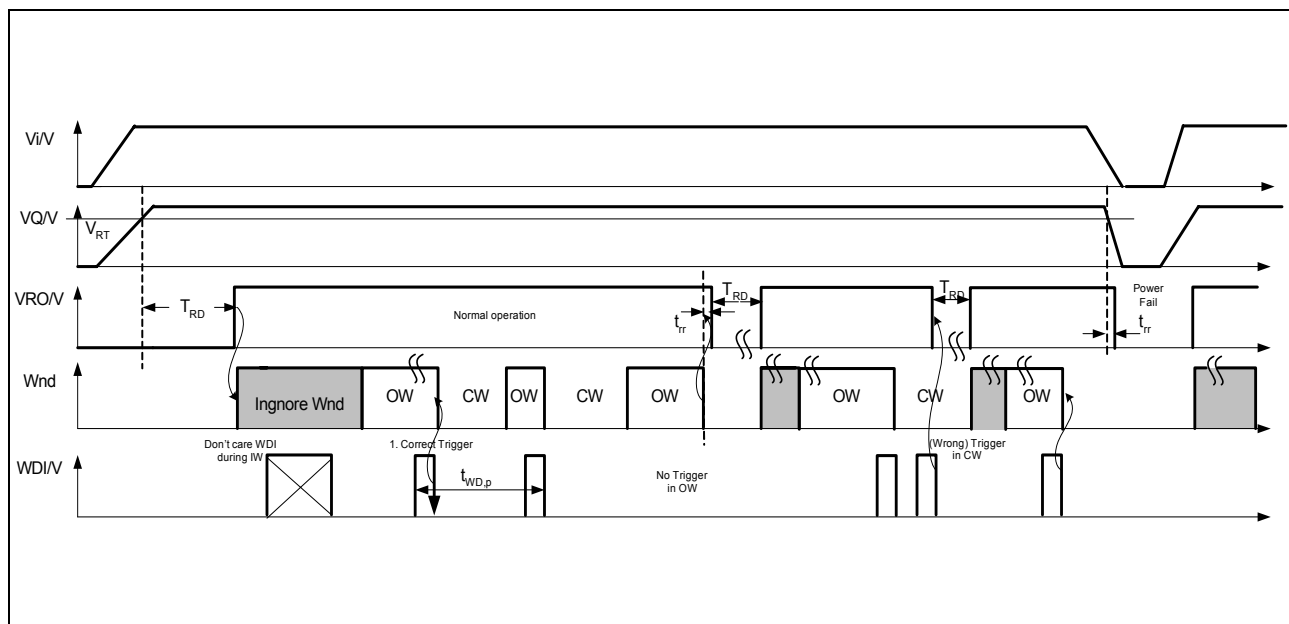


the closed window is interpreted as a pretrigger failure and results in a reset. After the closed window the open window with the duration  $t_{OW}$  is started again. The open window lasts at minimum until the trigger process has occurred, at maximum  $t_{OW}$  is 32 ms (typ. value with fast timing).

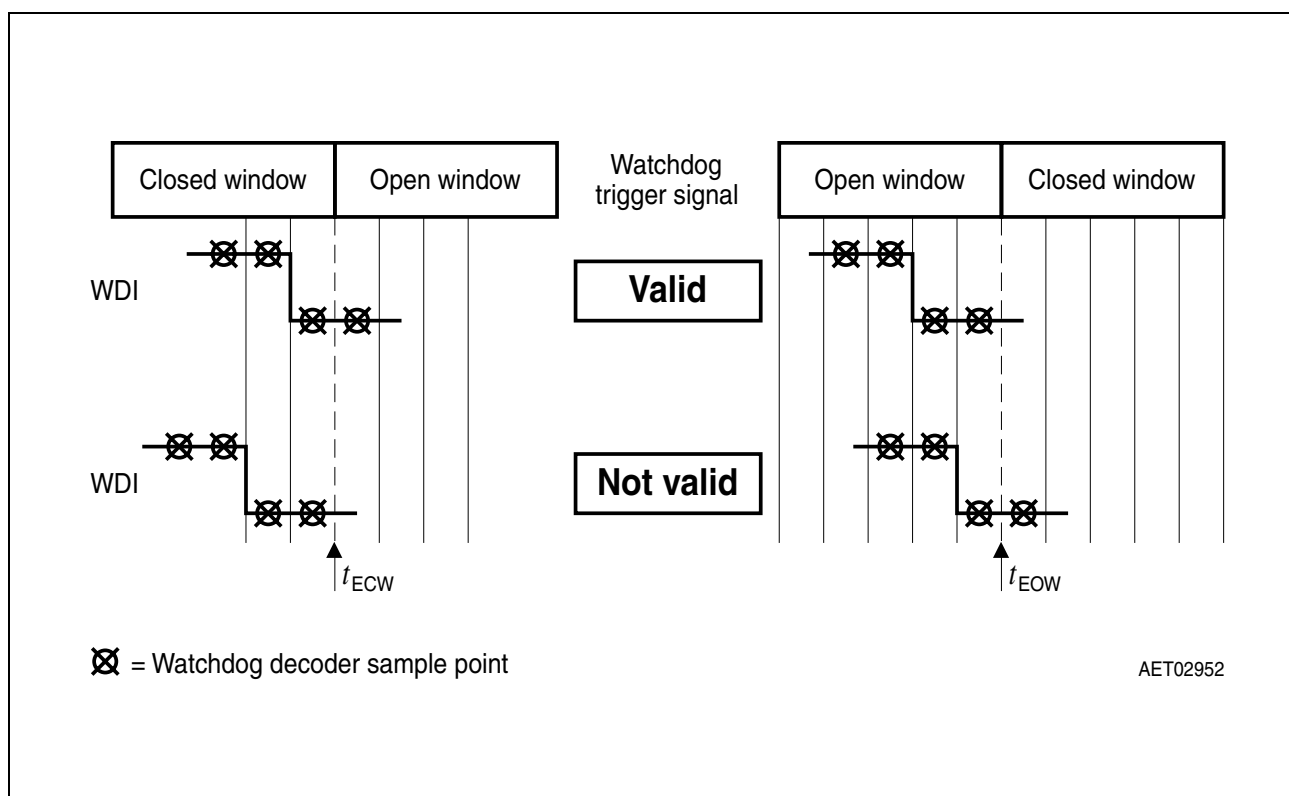
A HIGH to LOW transition of the watchdog trigger signal on pin WDI is taken as a trigger. To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period  $t_{sam}$  typ. 0.25 ms) are decoded as a valid trigger (see [Figure 8](#)). A reset is generated (RO goes LOW) if there is no trigger pulse during the open window or if a pretrigger occurs during the closed window. The triggering is correct also, if the first three samples (two HIGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window.



**Figure 6 Window Watchdog State Diagram**



**Figure 7** Window Watchdog Signal Flow



**Figure 8** Window Watchdog Definitions

Technical drawings of the GPS09628 component showing dimensions and tolerances:

- Top View:**
  - Overall width:  $7.8 \pm 0.1$  (Heatslug)
  - Overall height:  $2.6 \text{ MAX.}$
  - Body height:  $2.35 \pm 0.1$  (Body)
  - Standoff height:  $0 \pm 0.1$  (STANDOFF)
  - Heatslug height:  $0.8$
  - Radius:  $0.1$
- Side View:**
  - Overall height:  $10.3 \pm 0.3$
  - Heatslug height:  $0.7 \pm 0.15$
  - Standoff height:  $1.55$
  - Body height:  $7.5 \pm 0.1^{1)}$
  - Heatslug width:  $0.25 \pm 0.075 / -0.035$
  - Angle:  $5^\circ \pm 3^\circ$
  - Heatslug width:  $0.25 B$
- Bottom View:**
  - Overall width:  $7.6^{+0.13}_{-0.1}$
  - Overall height:  $6.4 \pm 0.1^{1)}$  (Mold)
  - Heatslug height:  $0.4^{+0.13}$
  - Heatslug width:  $5 \times 1 = 5$
  - Index Marking:  $12x$   $0.25 \text{ (M)} C A B$
  - Heatslug width:  $5.1 \pm 0.1$  (Metal)
  - Heatslug height:  $1.6 \pm 0.1$  (Metal)
  - Heatslug width:  $4.2 \pm 0.1$  (Metal)
  - Heatslug height:  $4.4 \text{ Mold}$
  - Heatslug width:  $1.8 \text{ Mold}$

1) Does not include plastic or metal protrusion of 0.15 max. per side

GPS09628

### Figure 9 PG-DSO-12 (Plastic Green Dual Small Outline)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Dimensions in mm

## Revision History

Version	Date	Changes
Rev. 1.6	2008-01-22	Initial version of RoHS-compliant derivate of TLE 7469 <b>Page 1</b> : AEC certified statement added. <b>Page 1</b> and <b>Page 19</b> : RoHS compliance statement and Green product feature added. <b>Page 1</b> and <b>Page 19</b> : Package changed to RoHS compliant version.
Rev. 1.5	2007-05-07	Modifications according to PCN No. 2007-070-A <ul style="list-style-type: none"><li>• Page 8: Parameter “Output current limitation <math>I_{Q2}</math>” : Max. Value modified from 500mA to 550mA.</li><li>• Page 3, Fig. 1 modified: RO pullup to Q1 instead to Q2.</li><li>• Legal disclaimer updated.</li></ul>
Rev. 1.4	2005-07-15	Final Datasheet

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