

Infineon[®] Basic LED Driver

TLD1125EL

1 Channel High Side Current Source

Data Sheet

Rev. 1.0, 2013-08-08

Automotive

1	Overview	3
2	Block Diagram	5
3	Pin Configuration	6
3.1	Pin Assignment	6
3.2	Pin Definitions and Functions	7
4	General Product Characteristics	8
4.1	Absolute Maximum Ratings	8
4.2	Functional Range	9
4.3	Thermal Resistance	9
5	EN Pin	10
5.1	EN Function	10
5.2	Internal Supply Pin	11
5.3	EN Unused	12
5.3.1	EN - Pull Up to VS	12
5.3.2	EN - Direct Connection to VS	12
6	PWMI Pin	13
6.1	PWM Dimming	13
6.2	Internal PWM Unit	14
6.3	Electrical Characteristics Internal Supply / EN / PWMI Pin	15
7	IN_SET Pin	18
7.1	Output Current Adjustment via RSET	18
7.2	Smart Input Pin	18
8	ST Pin	21
8.1	Diagnosis Selector	21
8.2	Diagnosis Output	21
8.3	Disable Input	21
9	D Pin	23
10	Load Diagnosis	24
10.1	Open Load	24
10.2	Short Circuit to GND detection	26
10.3	Electrical Characteristics IN_SET Pin and Load Diagnosis	27
11	Power Stage	30
11.1	Protection	30
11.1.1	Over Load Behavior	30
11.1.2	Reverse Battery Protection	30
11.2	Electrical Characteristics Power Stage	31
12	Application Information	33
12.1	Further Application Information	33
13	Package Outlines	34
14	Revision History	35

1 Channel High Side Current Source Basic LED Driver

TLD1125EL



1 Overview

Features

- 1 Channel device with integrated output stage (current source), optimized to drive LEDs
- Output current up to 360mA
- Low current consumption in sleep mode
- PWM-operation supported via VS- and EN-pin
- Integrated PWM dimming engine to provide two LED brightness levels without external logic (e.g. μC)
- Output current adjustable via external low power resistor and possibility to connect PTC resistor for LED protection during over temperature conditions
- Reverse polarity protection
- Overload protection
- Undervoltage detection
- Open load and short circuit to GND diagnosis
- Wide temperature range: $-40\text{ }^{\circ}\text{C} < T_j < 150\text{ }^{\circ}\text{C}$
- PG-SSOP14 package with exposed heatslug
- Green Product (RoHS compliant)
- AEC Qualified



PG-SSOP14

Description

The Basic LED Driver TLD1125EL is a one channel high side driver IC with integrated output stage. It is designed to control LEDs with a current up to 360 mA. In typical automotive applications the device is capable to drive i.e. 3 red LEDs with a current up to 180 mA, which is limited by thermal cooling aspects. The output current is controlled practically independent of load and supply voltage changes.

Table 1 Product Summary

Operating voltage	$V_{S(\text{nom})}$	5.5 V... 40 V
Maximum voltage	$V_{S(\text{max})}$ $V_{OUT(\text{max})}$	40 V
Nominal output (load) current	$I_{OUT(\text{nom})}$	180 mA when using a supply voltage range of 8V - 18V (e.g. Automotive car battery). Currents up to $I_{OUT(\text{max})}$ possible in applications with low thermal resistance R_{thJA}
Maximum output (load) current	$I_{OUT(\text{max})}$	360 mA; depending on thermal resistance R_{thJA}

Type	Package	Marking
TLD1125EL	PG-SSOP14	TLD1125EL

Table 1 Product Summary

Output current accuracy at $R_{SET} = 12\text{ k}\Omega$	k_{LT}	$2250 \pm 7\%$
Current consumption in sleep mode	$I_{S(sleep,typ)}$	$0.1\text{ }\mu\text{A}$

Protective functions

- ESD protection
- Under voltage lock out
- Over Load protection
- Over Temperature protection
- Reverse Polarity protection

Diagnostic functions

- OL detection
- SC to Vs (indicated by OL diagnosis)
- SC to GND detection

Applications

Designed for exterior LED lighting applications such as tail/brake light, turn indicator, position light, side marker,...
The device is also well suited for interior LED lighting applications such as ambient lighting, interior illumination and dash board lighting.

2 Block Diagram

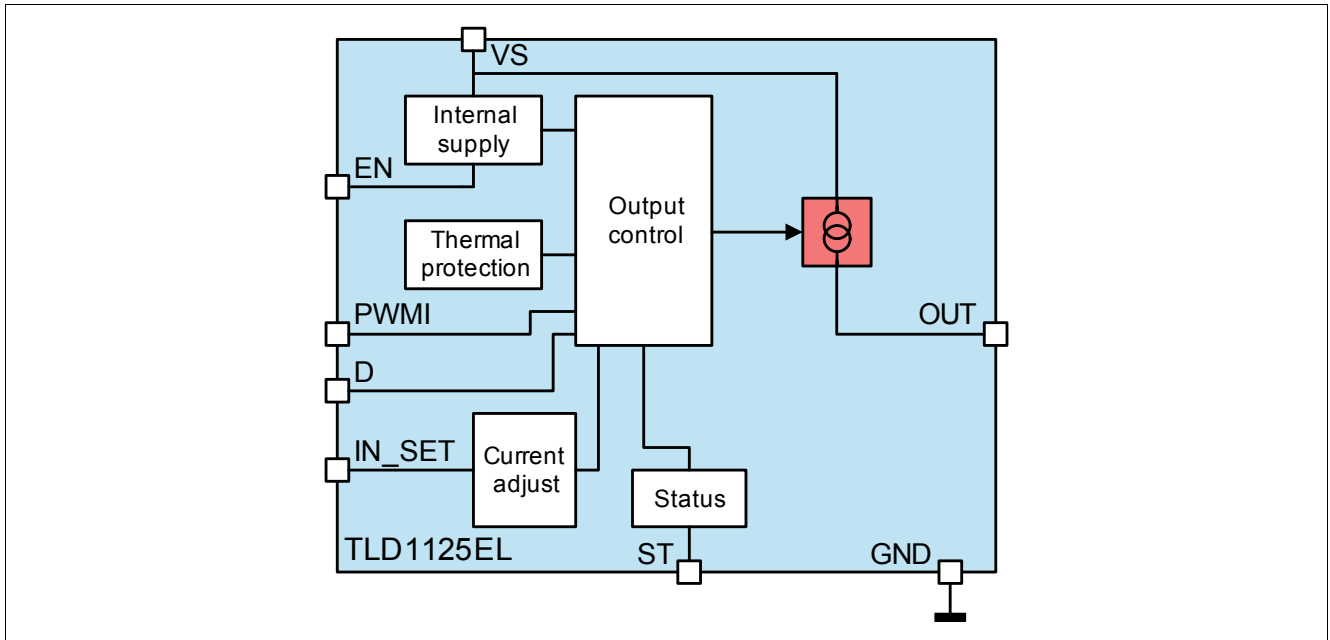


Figure 1 Basic Block Diagram

3 Pin Configuration

3.1 Pin Assignment

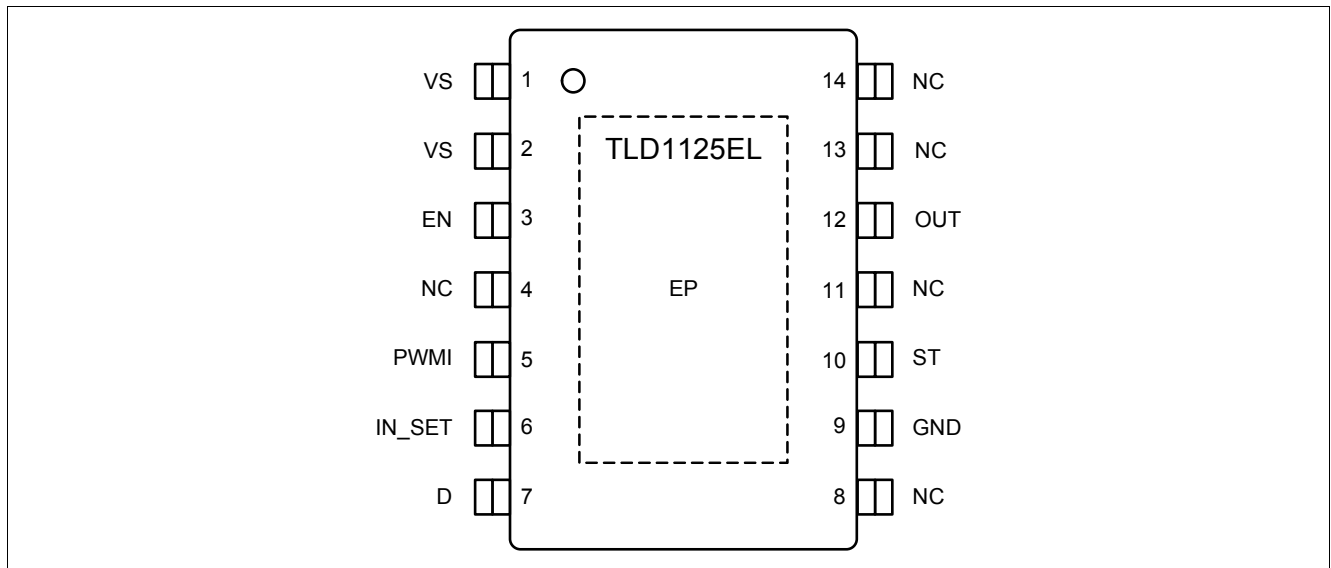


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Input/ Output	Function
1, 2	VS	–	Supply Voltage ; battery supply, connect a decoupling capacitor (100 nF - 1 μ F) to GND
3	EN	I	Enable pin
4	NC	–	Pin not connected
5	PWMI	I/O	PWM Input
6	IN_SET	I/O	Input / SET pin ; Connect a low power resistor to adjust the output current
7	D	I/O	Delay for open load detection
8	NC	–	Pin not connected
9	GND	–	¹⁾ Ground
10	ST	I/O	Status pin
11	NC	–	Pin not connected
12	OUT	O	Output
13	NC	–	Pin not connected
14	NC	–	Pin not connected
Exposed Pad	GND	–	¹⁾ Exposed Pad ; connect to GND in application

1) Connect all GND-pins together.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings ¹⁾

$T_j = -40\text{ °C to }+150\text{ °C}$; all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-16	40	V	–
4.1.2	Input voltage EN	V_{EN}	-16	40	V	–
4.1.3	Input voltage EN related to V_S	$V_{EN(VS)}$	$V_S - 40$	$V_S + 16$	V	–
4.1.4	Input voltage EN related to V_{OUT} $V_{EN} - V_{OUT}$	$V_{EN} - V_{OUT}$	-16	40	V	–
4.1.5	Output voltage	V_{OUT}	-1	40	V	–
4.1.6	Power stage voltage $V_{PS} = V_S - V_{OUT}$	V_{PS}	-16	40	V	–
4.1.7	Input voltage PWMI	V_{PWMI}	-0.3	6	V	–
4.1.8	IN_SET voltage	V_{IN_SET}	-0.3	6	V	–
4.1.9	D voltage	V_D	-0.3	6	V	–
4.1.10	Status voltage	V_{ST}	-0.3	6	V	–
Currents						
4.1.11	IN_SET current	I_{IN_SET}	– –	2 8	mA	– Diagnosis output
4.1.12	D current	I_D	-0.5	0.5	mA	–
4.1.13	Output current	I_{OUT}	–	390	mA	–
Temperatures						
4.1.14	Junction temperature	T_j	-40	150	°C	–
4.1.15	Storage temperature	T_{stg}	-55	150	°C	–
ESD Susceptibility						
4.1.16	ESD resistivity to GND	V_{ESD}	-2	2	kV	Human Body Model (100 pF via 1.5 kΩ) ²⁾
4.1.17	ESD resistivity all pins to GND	V_{ESD}	-500	500	V	CDM ³⁾
4.1.18	ESD resistivity corner pins to GND	V_{ESD}	-750	750	V	CDM ³⁾

1) Not subject to production test, specified by design

2) ESD susceptibility, Human Body Model "HBM" according to ANSI/ESDA/JEDEC JS-001-2011

3) ESD susceptibility, Charged Device Model "CDM" according to JESD22-C101E

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.19	Supply voltage range for normal operation	$V_{S(nom)}$	5.5	40	V	–
4.2.20	Power on reset threshold	$V_{S(POR)}$	–	5	V	$V_{EN} = V_S$ $R_{SET} = 12\text{ k}\Omega$ $I_{OUT} = 80\% I_{OUT(nom)}$ $V_{OUT} = 2.5\text{ V}$
4.2.21	Junction temperature	T_j	–40	150	°C	–

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case	R_{thJC}	–	8	10	K/W	1) 2)
4.3.2	Junction to Ambient 1s0p board	R_{thJA1}	–	61	–	K/W	1) 3) $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	56	–		
4.3.3	Junction to Ambient 2s2p board	R_{thJA2}	–	45	–	K/W	1) 4) $T_a = 85\text{ °C}$ $T_a = 135\text{ °C}$
			–	43	–		

- 1) Not subject to production test, specified by design. Based on simulation results.
- 2) Specified R_{thJC} value is simulated at natural convection on a cold plate setup (all pins and the exposed Pad are fixed to ambient temperature). $T_a = 85\text{ °C}$, Total power dissipation 1.5 W.
- 3) The R_{thJA} values are according to Jedec JESD51-3 at natural convection on 1s0p FR4 board. The product (chip + package) was simulated on a $76.2 \times 114.3 \times 1.5\text{ mm}^3$ board with $70\text{ }\mu\text{m}$ Cu, 300 mm^2 cooling area. Total power dissipation 1.5 W distributed statically and homogenously over power stage.
- 4) The R_{thJA} values are according to Jedec JESD51-5,-7 at natural convection on 2s2p FR4 board. The product (chip + package) was simulated on a $76.2 \times 114.3 \times 1.5\text{ mm}^3$ board with 2 inner copper layers (outside $2 \times 70\text{ }\mu\text{m}$ Cu, inner $2 \times 35\text{ }\mu\text{m}$ Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer. Total power dissipation 1.5 W distributed statically and homogenously over power stage.

5 EN Pin

The EN pin is a dual function pin:

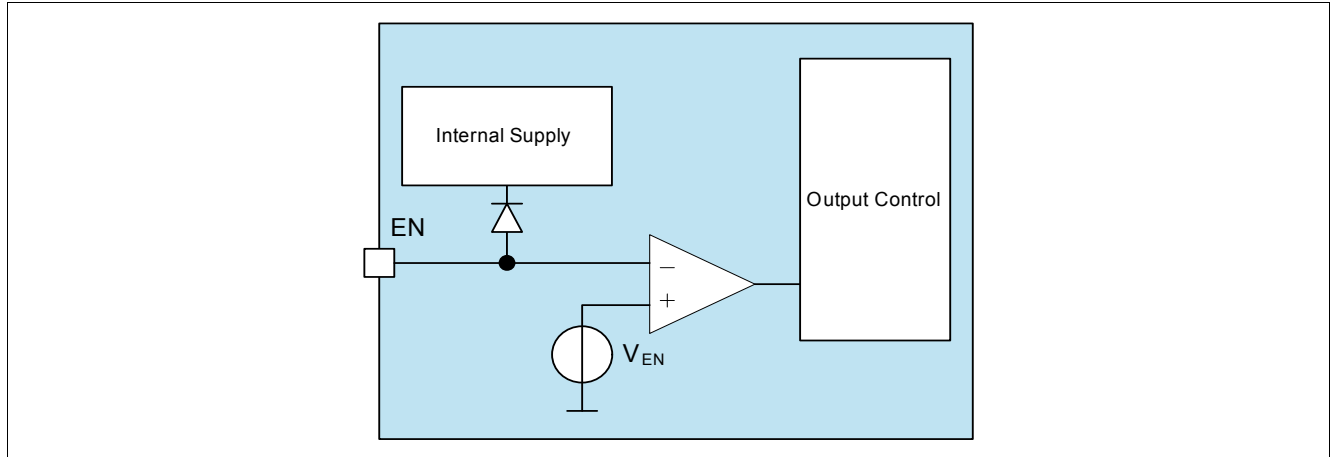


Figure 3 Block Diagram EN pin

Note: The current consumption at the EN-pin I_{EN} needs to be added to the total device current consumption. The total current consumption is the sum of the currents at the VS-pin I_S and the EN-pin I_{EN} .

5.1 EN Function

If the voltage at the pin EN is below a threshold of $V_{EN(off)}$ the Basic LED Driver IC will enter Sleep mode. In this state all internal functions are switched off, the current consumption is reduced to $I_{S(sleep)}$. A voltage above $V_{EN(on)}$ at this pin enables the device after the Power on reset time t_{POR} .

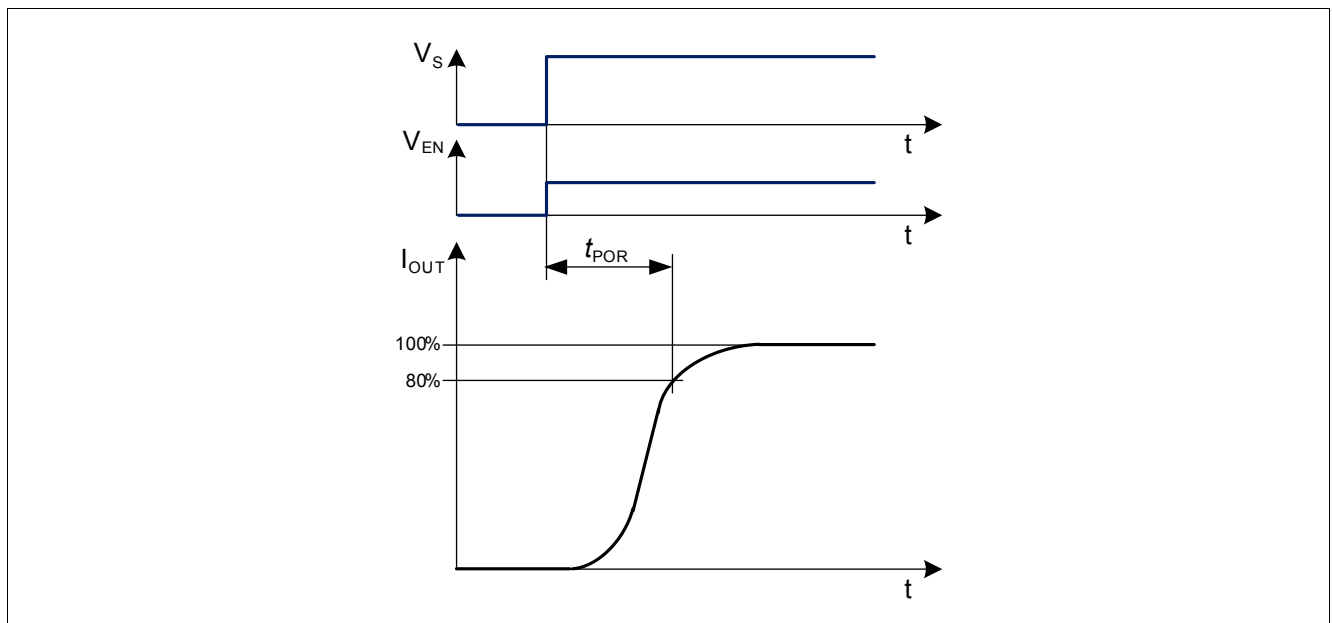


Figure 4 Power on reset

5.2 Internal Supply Pin

The EN pin can be used to supply the internal logic. There are two typical application conditions, where this feature can be used:

- 1) In “DC/DC control Buck” configurations, where the voltage V_s can be below 5.5V.
- 2) In configurations, where a PWM signal is applied at the Vbatt pin of a light module. The buffer capacitor C_{BUF} is used to supply the Basic LED Driver IC during Vbatt low (V_s low) periods. This feature can be used to minimize the turn-on time to the values specified in [Pos. 11.2.15](#). Otherwise, the power-on reset delay time t_{POR} ([Pos. 6.3.8](#)) has to be considered.

The capacitor can be calculated using the following formula:

$$C_{BUF} = t_{LOW(max)} \cdot \frac{I_{EN(ES)}}{V_s - V_{D1} - V_{S(POR)}} \quad (1)$$

See also a typical application drawing in [Chapter 12](#).

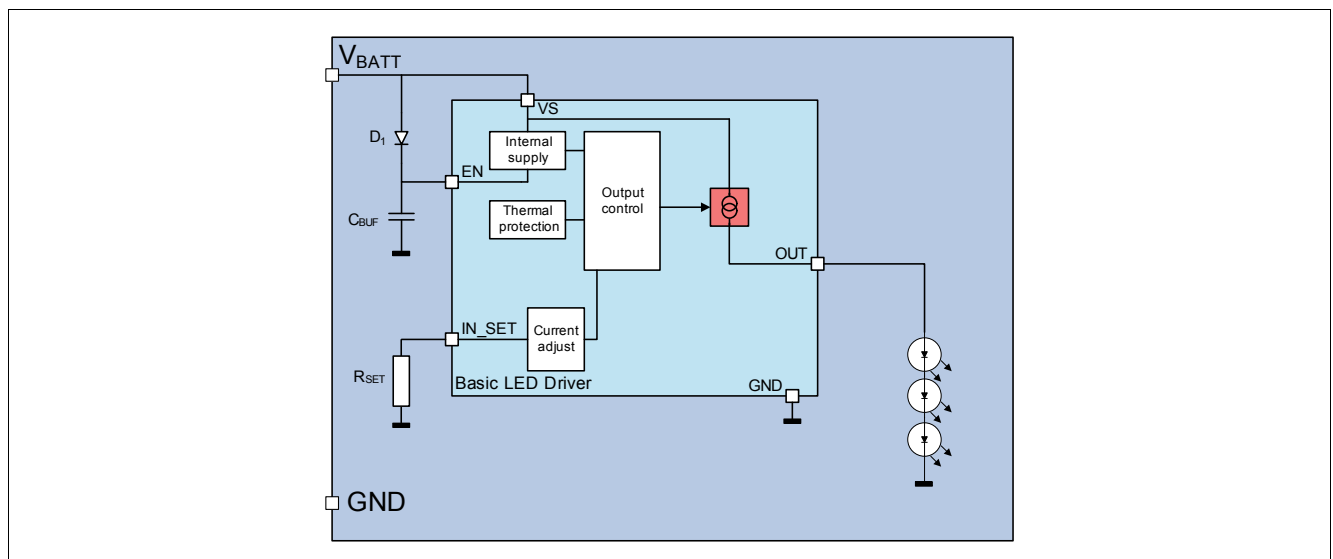


Figure 5 External circuit when applying a fast PWM signal on V_{BATT}

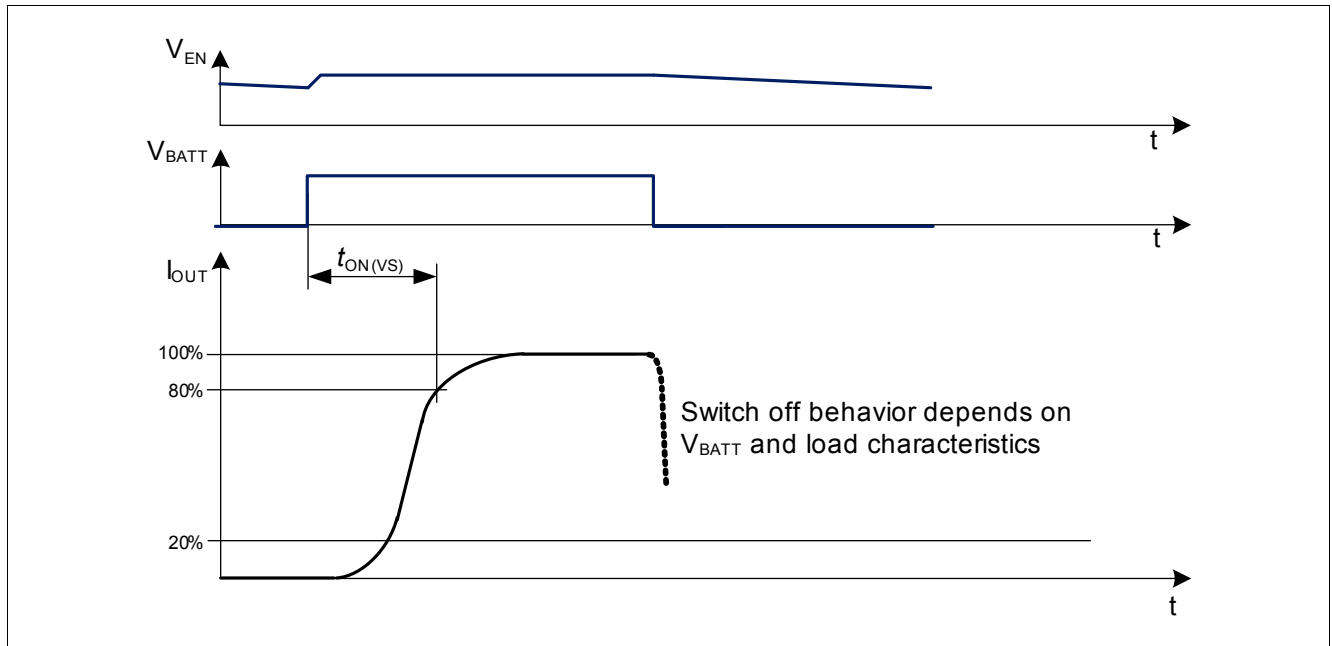


Figure 6 Typical waveforms when applying a fast PWM signal on V_{BATT}

The parameter $t_{ON(VS)}$ is defined at [Pos. 11.2.15](#). The parameter $t_{OFF(VS)}$ depends on the load and supply voltage V_{BATT} characteristics.

5.3 EN Unused

In case of an unused EN pin, there are two different ways to connect it:

5.3.1 EN - Pull Up to VS

The EN pin can be connected with a pull up resistor (e.g. 10 k Ω) to V_s potential. In this configuration the Basic LED Driver IC is always enabled.

5.3.2 EN - Direct Connection to VS

The EN pin can be connected directly to the VS pin (IC always enabled). This configuration has the advantage (compared to the configuration described in [Chapter 5.3.1](#)) that no additional external component is required.

6 PWMI Pin

The PWMI pin is designed as a dual function pin.

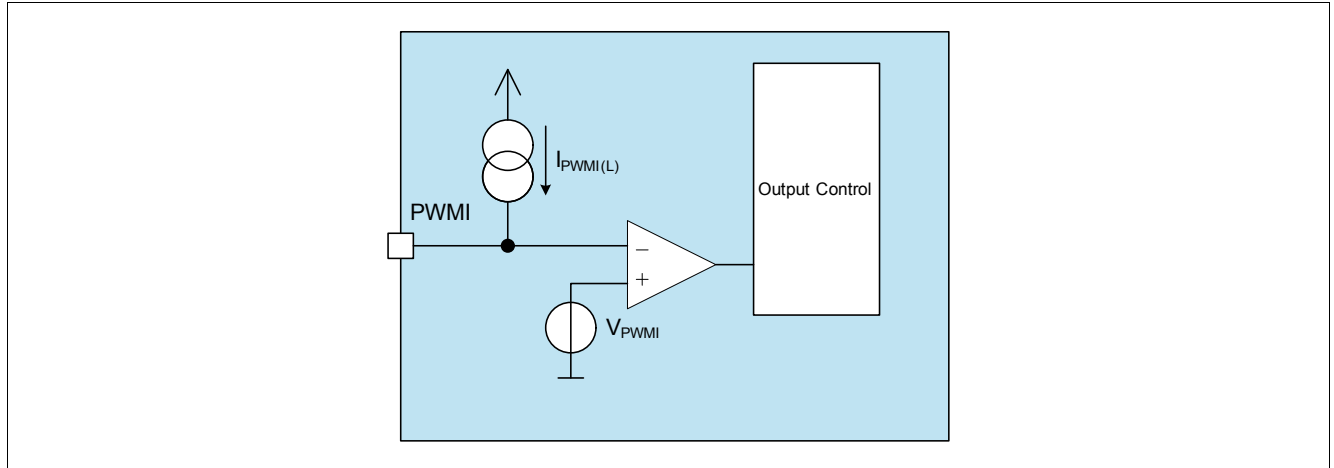


Figure 7 Block Diagram PWMI pin

The pin can be used for PWM-dimming via a push-pull stage of a micro controller, which is connecting the PWMI-pin to a low or high potential.

Note: The micro controller's push-pull stage has to be able to sink currents according to [Pos. 6.3.18](#) to activate the device.

Furthermore, the device offers also an internal PWM unit by connecting an external-RC network according to [Figure 10](#).

6.1 PWM Dimming

A PWM signal can be applied at the PWMI pin for LED brightness regulation. The dimming frequency can be adjusted in a very wide range (e.g. 400 Hz). The PWMI pin is low active. Turn on/off thresholds $V_{PWMI(L)}$ and $V_{PWMI(H)}$ are specified in parameters [Pos. 6.3.15](#) and [Pos. 6.3.16](#).

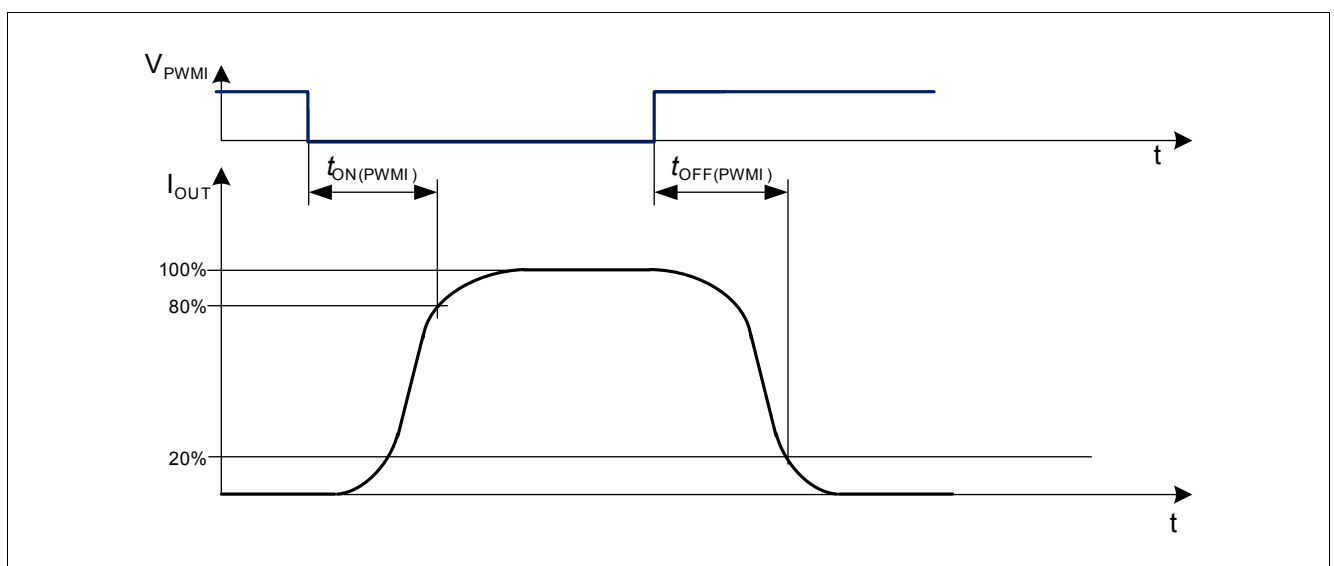


Figure 8 Turn on and Turn off time for PWMI pin usage

6.2 Internal PWM Unit

Connecting a resistor and a capacitor in parallel on the PWMI pin enables the internal pulse width modulation unit. The following figure shows the charging and discharging defined by the RC-network according to [Figure 10](#) and the internal PWM unit.

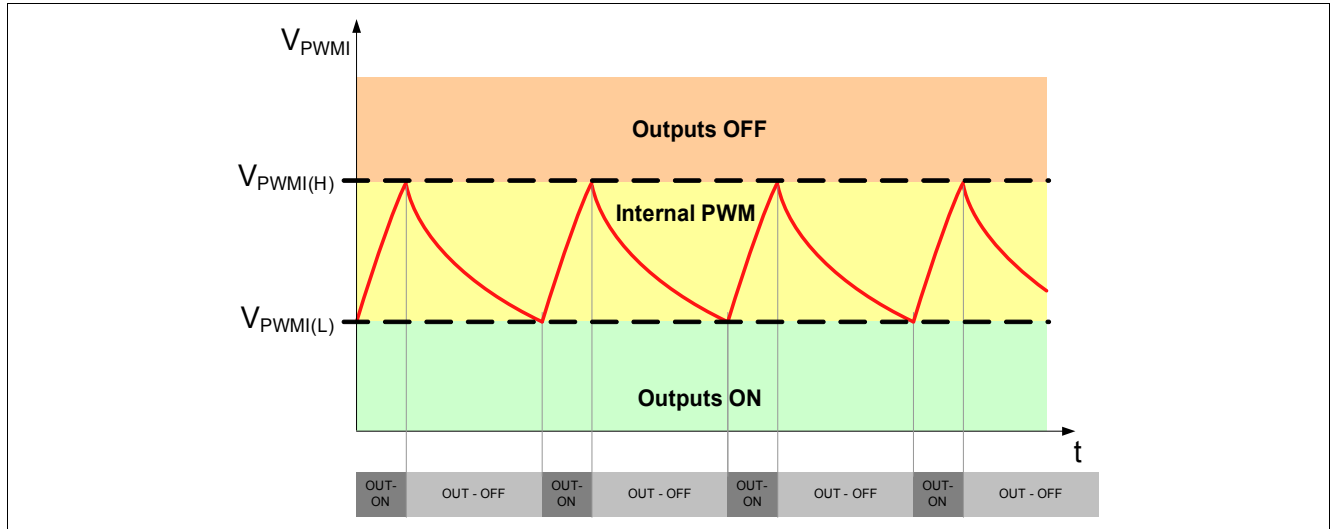


Figure 9 PWMI operating voltages

The PWM Duty cycle (DC) and the PWM frequency can be adjusted using the formulas below. Please use only typical values of $V_{PWMI(L)}$, $V_{PWMI(H)}$ and $I_{PWMI(on)}$ for the calculation of $t_{PWMI(on)}$ and $t_{PWMI(off)}$ (as described in [Pos. 6.3.15](#) to [Pos. 6.3.18](#)).

$$t_{PWMI(on)} = -R_{PWMI} \cdot C_{PWMI} \cdot \ln\left(\frac{V_{PWMI(H)} - I_{PWMI(on)} \cdot R_{PWMI}}{V_{PWMI(L)} - I_{PWMI(on)} \cdot R_{PWMI}}\right) \quad (2)$$

$$t_{PWMI(off)} = R_{PWMI} \cdot C_{PWMI} \cdot \ln\left(\frac{V_{PWMI(H)}}{V_{PWMI(L)}}\right) \quad (3)$$

$$f_{PWMI} = \frac{1}{t_{PWMI(on)} + t_{PWMI(off)}} \quad (4)$$

$$DC = t_{PWMI(on)} \cdot f_{PWMI} \quad (5)$$

Out of this equations the required C_{PWMI} and R_{PWMI} can be calculated:

$$C_{PWMI} = \frac{-I_{PWMI(on)} \cdot t_{PWMI(off)} \cdot \left[\left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}} \right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - 1 \right]}{\ln\left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}}\right) \cdot \left[V_{PWMI(L)} \cdot \left(\frac{V_{PWMI(L)}}{V_{PWMI(H)}} \right)^{\frac{t_{PWMI(on)}}{t_{PWMI(off)}}} - V_{PWMI(H)} \right]} \quad (6)$$

$$R_{PWMI} = \frac{t_{PWMI(off)}}{C_{PWMI} \cdot \ln\left(\frac{V_{PWMI(H)}}{V_{PWMI(L)}}\right)} \quad (7)$$

See [Figure 10](#) for a typical external circuitry.

Note: In case of junction temperatures above $T_{j(CRT)}$ ([Pos. 11.2.16](#)) the device provides a temperature dependent current reduction feature as described in [Chapter 11.1.1](#). In case of output current reduction I_{IN_SET} is reduced as well, which leads to increased turn on-times $t_{PWMI(on)}$, because the C_{PWMI} is charged slower. The turn off-time $t_{PWMI(off)}$ remains the same.

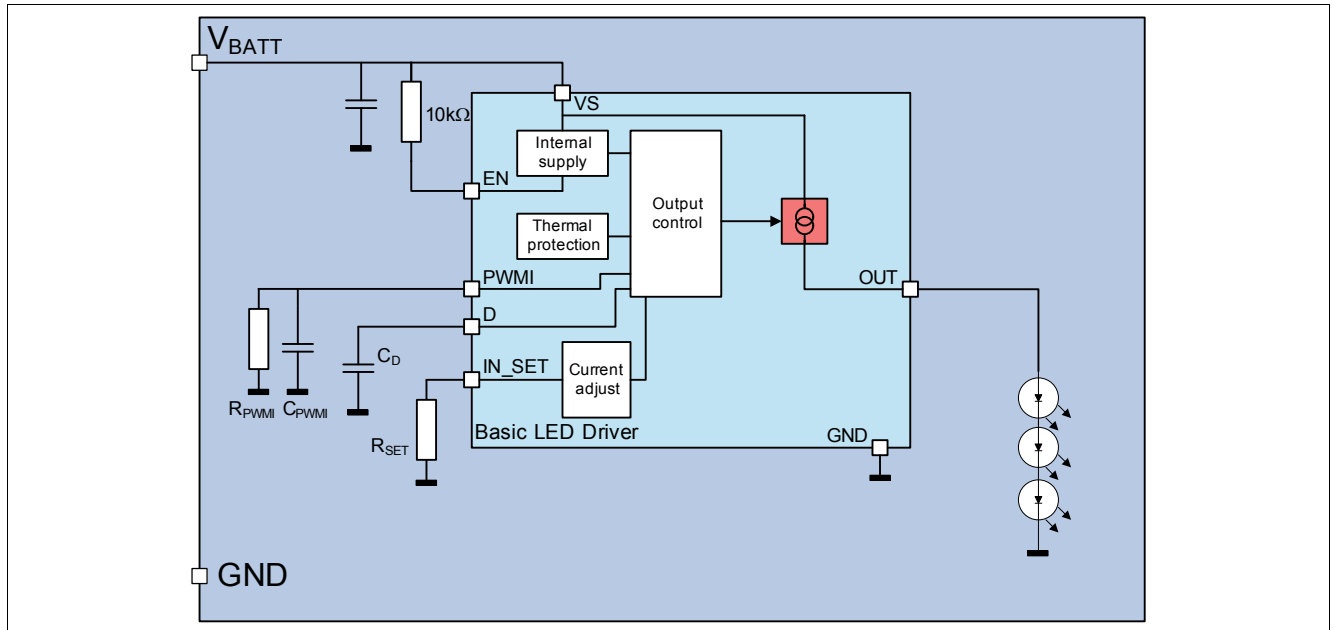


Figure 10 Typical circuit using internal PWM unit

6.3 Electrical Characteristics Internal Supply / EN / PWMI Pin

Electrical Characteristics Internal Supply / EN / PWMI pin

Unless otherwise specified: $V_S = 5.5 \text{ V to } 40 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.1	Current consumption, sleep mode	$I_{S(sleep)}$	—	0.1	2	μA	¹⁾ $V_{EN} = 0.5 \text{ V}$ $T_j < 85 \text{ }^\circ\text{C}$ $V_S = 18 \text{ V}$ $V_{OUT} = 3.6 \text{ V}$
6.3.2	Current consumption, active mode	$I_{S(on)}$	—	—	—	mA	²⁾ $V_{PWMI} = 0.5 \text{ V}$ $I_{IN_SET} = 0 \text{ }\mu\text{A}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_S = 18 \text{ V}$ $V_{OUT} = 3.6 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			—	—	1.4		
			—	—	0.75		
			—	—	1.5		

Electrical Characteristics Internal Supply / EN / PWMI pin (cont'd)

Unless otherwise specified: $V_S = 5.5 \text{ V to } 40 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.3	Current consumption, device disabled via ST	$I_{S(dis,ST)}$	–	–	1.4	mA	²⁾ $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{ST} = 5 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			–	–	0.65		
			–	–	1.4		
6.3.4	Current consumption, device disabled via IN_SET	$I_{S(dis,IN_SET)}$	–	–	1.4	mA	²⁾ $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{IN_SET} = 5 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			–	–	0.7		
			–	–	1.4		
6.3.5	Current consumption, device disabled via PWMI	$I_{S(dis,PWMI)}$	–	–	1.6	mA	²⁾ $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{PWMI} = 3.4 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			–	–	0.75		
			–	–	1.6		
6.3.6	Current consumption, active mode in fault detection condition with ST-pin unconnected	$I_{S(fault,STu)}$	–	–	1.7	mA	²⁾ $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $R_{SET} = 12 \text{ k}\Omega$ $V_{PWMI} = 0.5 \text{ V}$ $V_{OUT} = 18 \text{ V or } 0 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			–	–	1.1		
			–	–	1.8		
6.3.7	Current consumption, active mode in fault detection condition with ST-pin connected to GND	$I_{S(fault,STG)}$	–	–	6.0	mA	²⁾ $V_S = 18 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $R_{SET} = 12 \text{ k}\Omega$ $V_{PWMI} = 0.5 \text{ V}$ $V_{OUT} = 18 \text{ V or } 0 \text{ V}$ $V_{ST} = 0 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_{EN} = 18 \text{ V}$ ¹⁾ $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
			–	–	4.9		
			–	–	5.9		
6.3.8	Power-on reset delay time ³⁾	t_{POR}	–	–	25	μs	¹⁾ $V_S = V_{EN} = 0 \rightarrow 13.5 \text{ V}$ $V_{OUT(nom)} = 3.6 \pm 0.3 \text{ V}$ $I_{OUT} = 80\% I_{OUT(nom)}$

Electrical Characteristics Internal Supply / EN / PWMI pin (cont'd)

Unless otherwise specified: $V_S = 5.5 \text{ V}$ to 40 V , $T_j = -40 \text{ }^\circ\text{C}$ to $+150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$ all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.9	Required supply voltage for output activation	$V_{S(on)}$	–	–	4	V	$V_{EN} = 5.5 \text{ V}$ $V_{OUT} = 3 \text{ V}$ $I_{OUT} = 50\% I_{OUT(nom)}$
6.3.10	Required supply voltage for current control	$V_{S(CC)}$	–	–	5.2	V	$V_{EN} = 5.5 \text{ V}$ $V_{OUT} = 3.6 \text{ V}$ $I_{OUT} \geq 90\% I_{OUT(nom)}$
6.3.11	EN turn on threshold	$V_{EN(on)}$	–	–	2.5	V	–
6.3.12	EN turn off threshold	$V_{EN(off)}$	0.8	–	–	V	–
6.3.13	EN input current during low supply voltage	$I_{EN(LS)}$	–	–	1.8	mA	¹⁾ $V_S = 4.5 \text{ V}$ $T_j < 105 \text{ }^\circ\text{C}$ $V_{EN} = 5.5 \text{ V}$
6.3.14	EN high input current	$I_{EN(H)}$	– – – –	– – – –	0.1 0.1 1.65 0.45	mA	$T_j < 105 \text{ }^\circ\text{C}$ $V_S = 13.5 \text{ V}$, $V_{EN} = 5.5 \text{ V}$ $V_S = 18 \text{ V}$, $V_{EN} = 5.5 \text{ V}$ $V_S = V_{EN} = 18 \text{ V}$ ¹⁾ $V_S = 18 \text{ V}$, $R_{EN} = 10 \text{ k}\Omega$ between VS and EN-pin
6.3.15	PWMI (active low) Switching low threshold (output on)	$V_{PWMI(L)}$	1.5	1.85	2.3	V	¹⁾⁴⁾ $V_S = 8 \dots 18 \text{ V}$
6.3.16	PWMI(active low) Switching high threshold (output off)	$V_{PWMI(H)}$	2.45	2.85	3.2	V	¹⁾⁴⁾⁵⁾ $V_S = 8 \dots 18 \text{ V}$
6.3.17	PWMI Switching threshold difference $V_{PWMI(H)} - V_{PWMI(L)}$	ΔV_{PWMI}	0.75	1	1.10	V	¹⁾⁴⁾⁵⁾ $V_S = 8 \dots 18 \text{ V}$
6.3.18	PWMI (active low) Low input current with active channels (voltage $< V_{PWMI(L)}$)	$I_{PWMI(on)}$	I_{IN_SET} *3.1	I_{IN_SET} *4	I_{IN_SET} *4.9	μA	¹⁾ $T_j = 25 \dots 115 \text{ }^\circ\text{C}$ $I_{IN_SET} = 100 \text{ } \mu\text{A}$ $V_{PWMI} = 1.7 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_S = 8 \dots 18 \text{ V}$
6.3.19	PWMI(active low) High input current	$I_{PWMI(off)}$	-5	–	5	μA	$V_{PWMI} = 5 \text{ V}$ $V_{EN} = 5.5 \text{ V}$ $V_S = 8 \dots 18 \text{ V}$

1) Not subject to production test, specified by design

2) The total device current consumption is the sum of the currents I_S and $I_{EN(H)}$, please refer to [Pos. 6.3.14](#)

3) See also [Figure 4](#)

4) Parameter valid if an external PWM signal is applied

5) If TTL level compatibility is required, use μC open drain output with pull up resistor

7 IN_SET Pin

The IN_SET pin is a multiple function pin for output current definition, input and diagnostics:

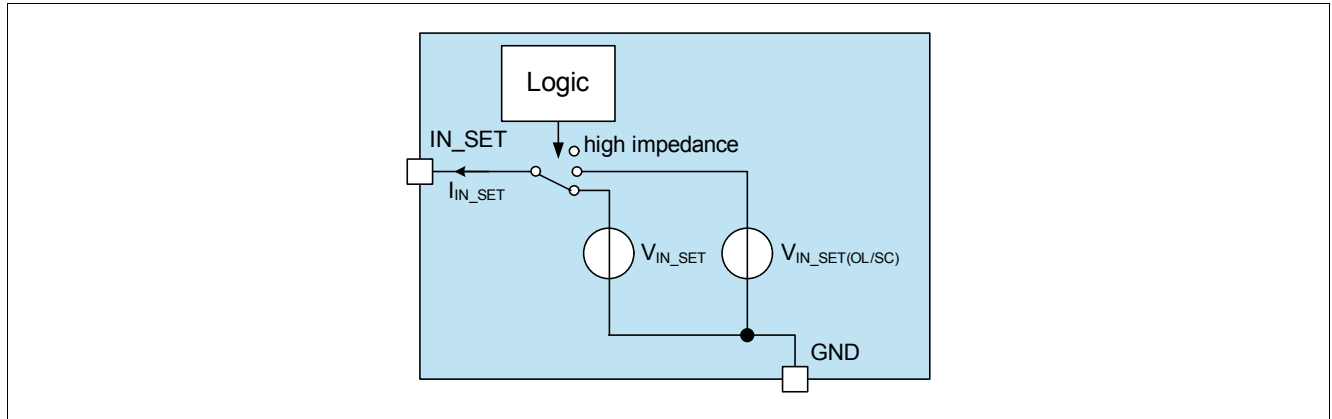


Figure 11 Block Diagram IN_SET pin

7.1 Output Current Adjustment via RSET

The current adjustment can be done by placing a low power resistor (R_{SET}) at the IN_SET pin to ground. The dimensioning of the resistor can be done using the formula below:

$$R_{SET} = \frac{k}{I_{OUT}} \quad (8)$$

The gain factor k ($R_{SET} \cdot$ output current) is specified in [Pos. 11.2.4](#) and [Pos. 11.2.5](#). The current through the R_{SET} is defined by the resistor itself and the reference voltage $V_{IN_SET(ref)}$, which is applied to the IN_SET during supplied device.

7.2 Smart Input Pin

The IN_SET pin can be connected via R_{SET} to the open-drain output of a μC or to an external NMOS transistor as described in [Figure 12](#). This signal can be used to turn off the output stage of the IC. A minimum IN_SET current of $I_{IN_SET(act)}$ is required to turn on the output stage. This feature is implemented to prevent glimming of LEDs caused by leakage currents on the IN_SET pin, see [Figure 15](#) for details. In addition, the IN_SET pin offers the diagnostic feedback information, if the status pin is connected to GND. Another diagnostic possibility is shown in [Figure 13](#), where the diagnosis information is provided via the ST pin (refer to [Chapter 8](#) and [Chapter 10](#)) to a micro controller. In case of a fault event with the ST pin connected to GND the IN_SET voltage is increased to $V_{IN_SET(OL/SC)}$ [Pos. 10.3.2](#). Therefore, the device has two voltage domains at the IN_SET-pin, which is shown in [Figure 16](#).

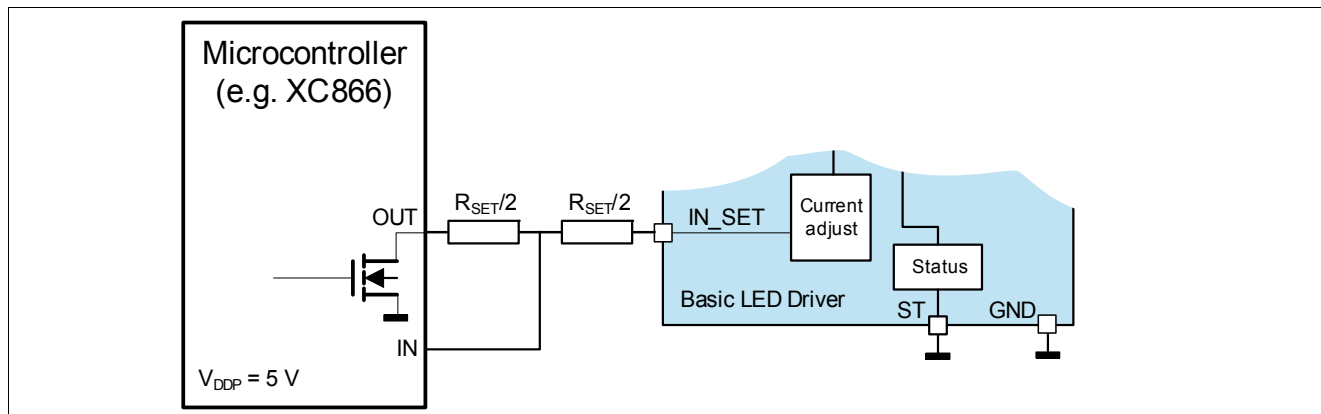


Figure 12 Schematics IN_SET interface to μ C, diagnosis via IN_SET pin

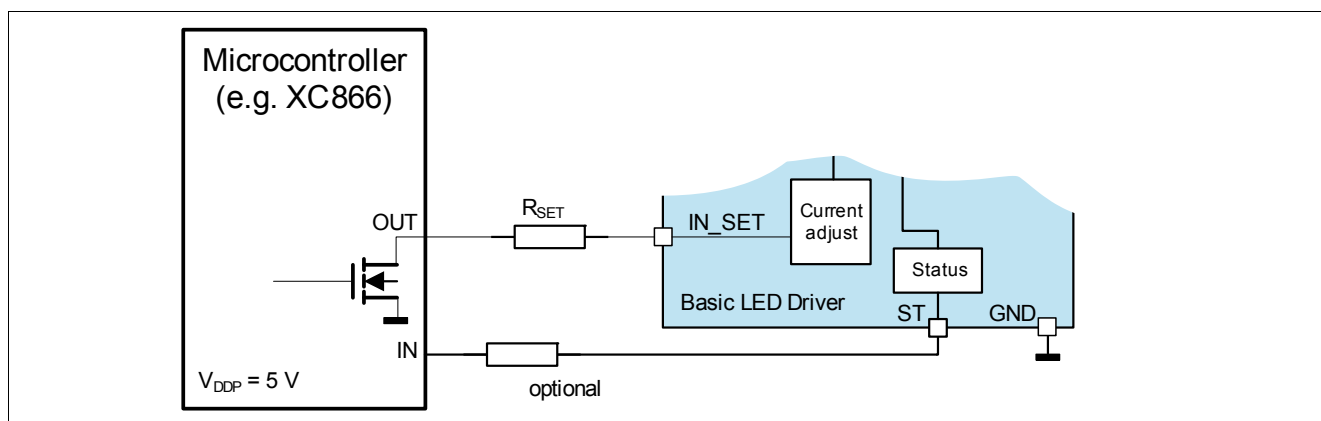


Figure 13 Schematics IN_SET interface to μ C, diagnosis via ST pin

The resulting switching times are shown in [Figure 14](#):

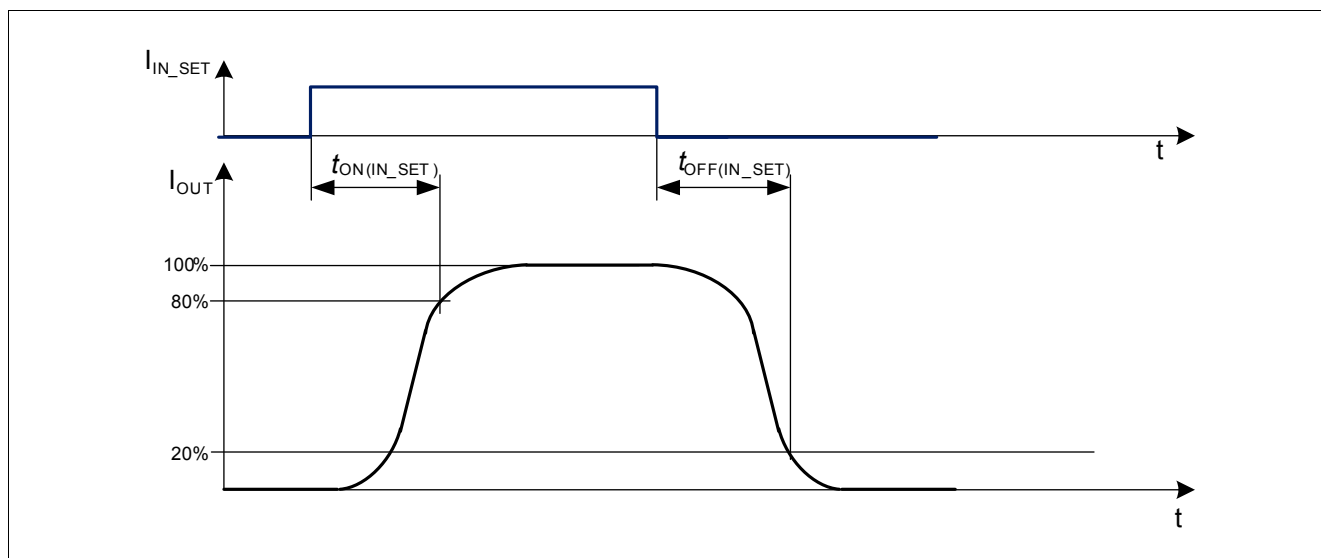


Figure 14 Switching times via IN_SET

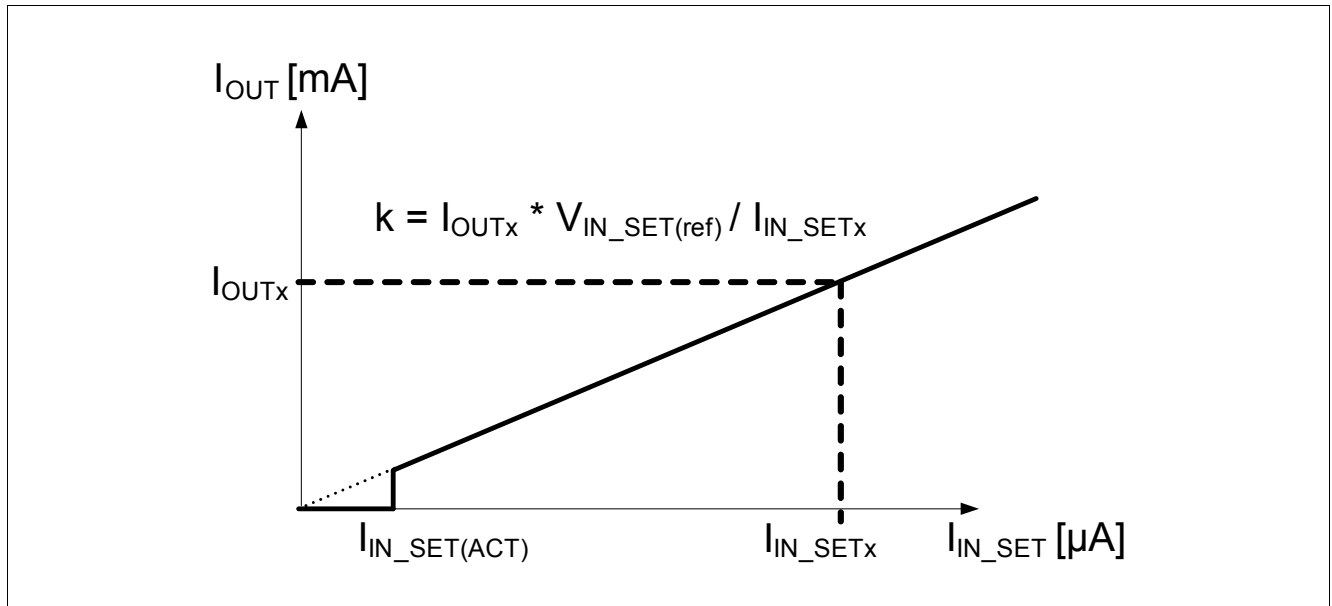


Figure 15 I_{OUT} versus I_{IN_SET}

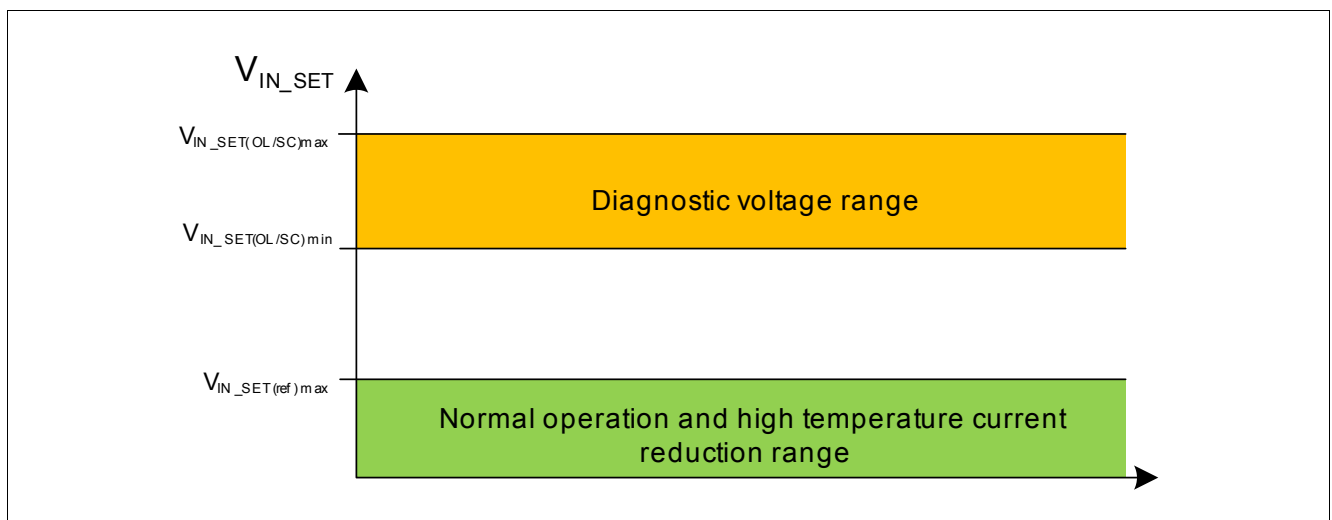


Figure 16 Voltage domains for IN_SET pin, if ST pin is connected to GND

8 ST Pin

The ST pin is a multiple function pin.

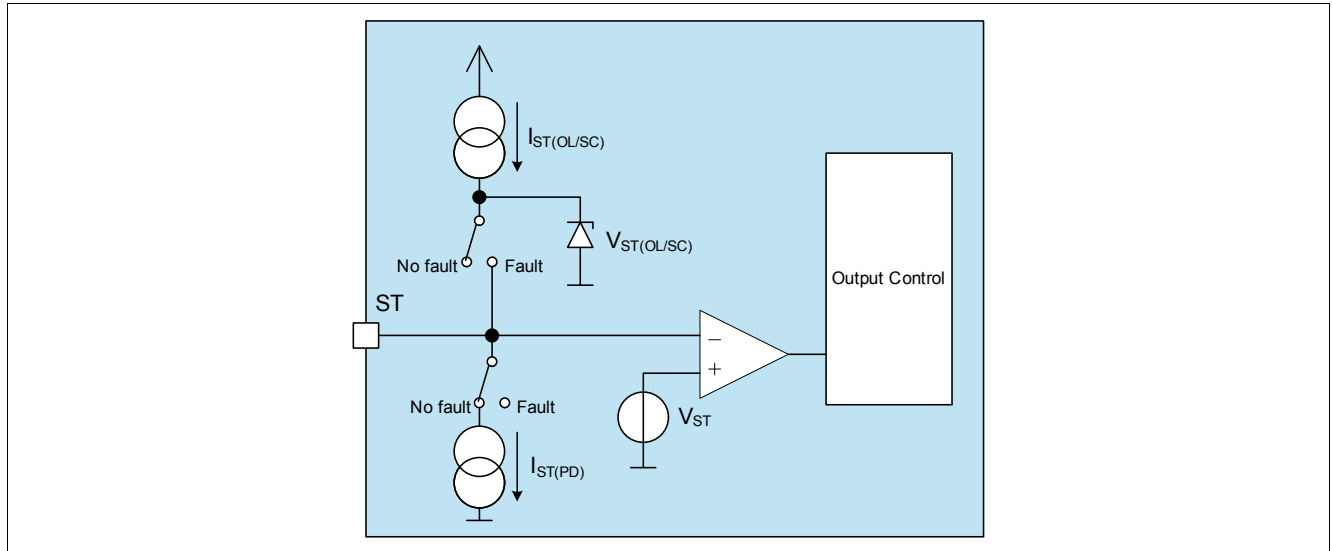


Figure 17 Block Diagram ST pin

8.1 Diagnosis Selector

If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), the ST pin acts as diagnosis output pin. In normal operation (device is activated) the ST pin is pulled to GND via the internal pull down current $I_{ST(PD)}$. In case of an open load or short circuit to GND condition the ST pin is switched to $V_{ST(OL/SC)}$ after the filter time t_D (see Equation (11)).

If the device is operated in PWM operation via the VS and/or EN pins the ST pin should be connected to GND via a high ohmic resistor (e.g. 470k Ω) to ensure proper device behavior during fast rising VS and/or EN slopes.

If the ST pin is shorted to GND the diagnostic feedback is performed via the IN_SET-pin, which is shown in Chapter 7.2 and Chapter 10.

8.2 Diagnosis Output

If the status pin is unconnected or connected to GND via a high ohmic resistor (V_{ST} to be below $V_{ST(L)}$), it acts as a diagnostic output. In case of a fault condition the ST pin rises its voltage to $V_{ST(OL/SC)}$ (Pos. 10.3.7). Details are shown in Chapter 10.

8.3 Disable Input

If an external voltage higher than $V_{ST(H)}$ (Pos. 10.3.5) is applied to the ST pin, the device is switched off. This function is used for applications, where multiple drivers should be used for one light function. It is possible to combine the drivers' fault diagnosis via the ST pins. If a single LED chain fails, the entire light function is switched off. In this scenario e.g. the diagnostic circuit on the body control module can easily distinguish between the two cases (normal load or load fault), because nearly no current is flowing into the LED module during the fault scenario - the drivers consume a current of $I_{S(fault,STu)}$ (Pos. 6.3.6) or $I_{S(dis,ST)}$ (Pos. 6.3.3).

As soon as one LED chain fails, the ST-pin of this device is switched to $V_{ST(OL/SC)}$. The other devices used for the same light function can be connected together via the ST pins. This leads to a switch off of all devices connected together. Application examples are shown in Chapter 12.

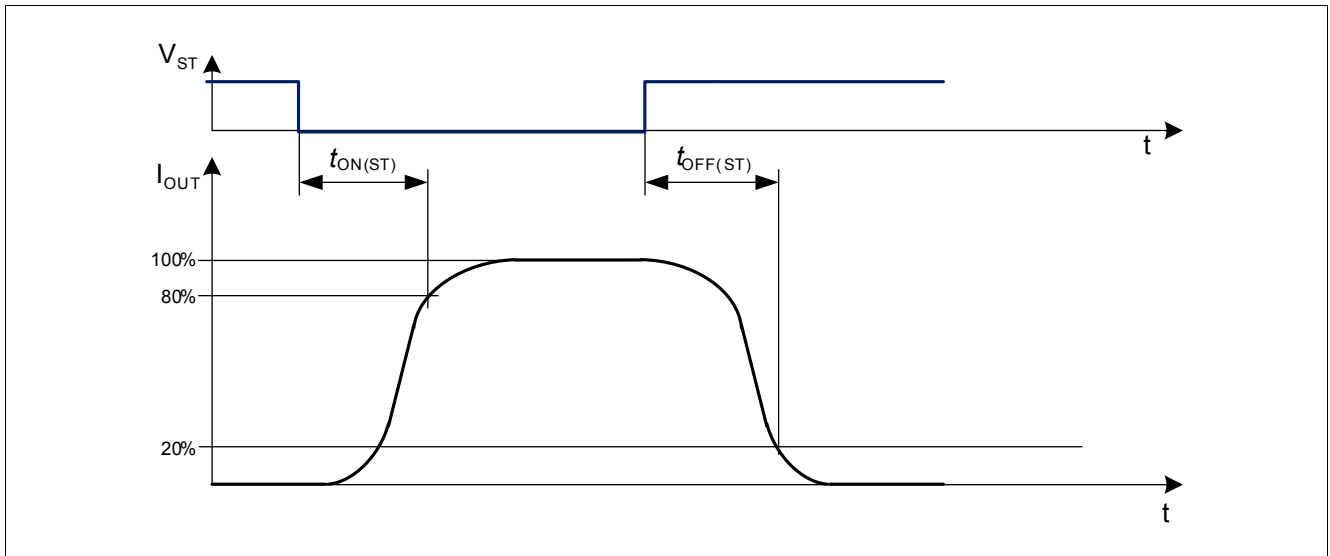


Figure 18 Switching times via ST Pin

9 D Pin

The D pin is designed as a single function pin.

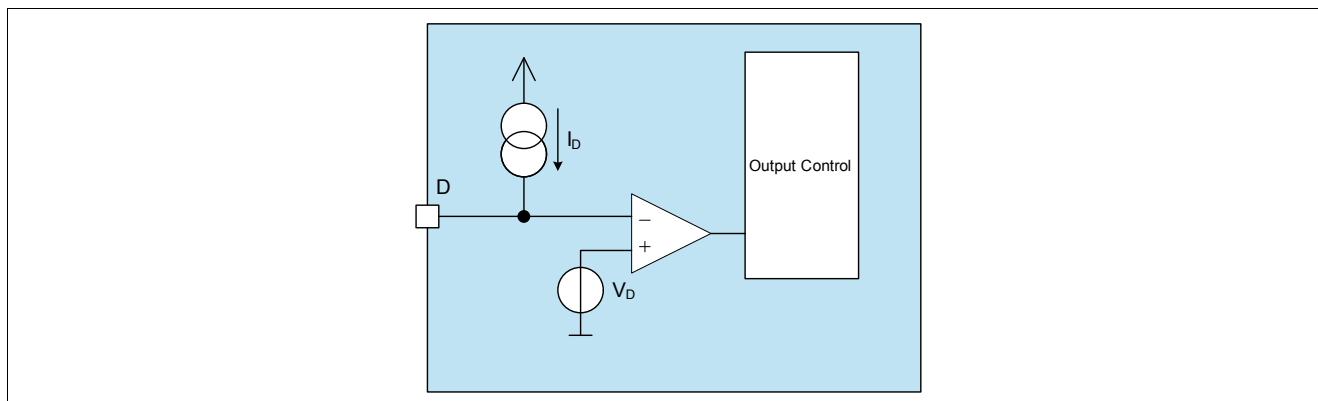


Figure 19 Block Diagram DIS pin

The D pin can be used to extend the open load detection filter time t_{OL} by adding a small signal capacitor to the D pin as shown in [Figure 26](#). The filter time t_D , which is defined by the charging current I_D ([Pos. 10.3.10](#)). The time is adjustable according to the following equation:

$$t_{typ} = \frac{C_D \cdot V_{D(th)}}{I_D} \quad (9)$$

10 Load Diagnosis

10.1 Open Load

An open load diagnosis feature is integrated in the TLD1125EL driver IC. If there is an open load on the output, the output is turned off. The potential on the IN_SET pin rises up to $V_{IN_SET(OL/SC)}$. This high voltage can be used as input signal for an μC as shown in [Figure 13](#). The open load status is not latched, as soon as the open load condition is no longer present, the output stage will be turned on again. An open load condition is detected, if the voltage drop over the output stage V_{PS} is below the threshold according [Pos. 10.3.11](#). The output is deactivated after a filter time t_D , which is defined by the charging current I_D [Pos. 10.3.10](#). The time is adjustable by the capacitor connected to the D pin according the following equation:

$$t_{D, typ} = \frac{C_D \cdot V_{D(th)}}{I_D} \quad (10)$$

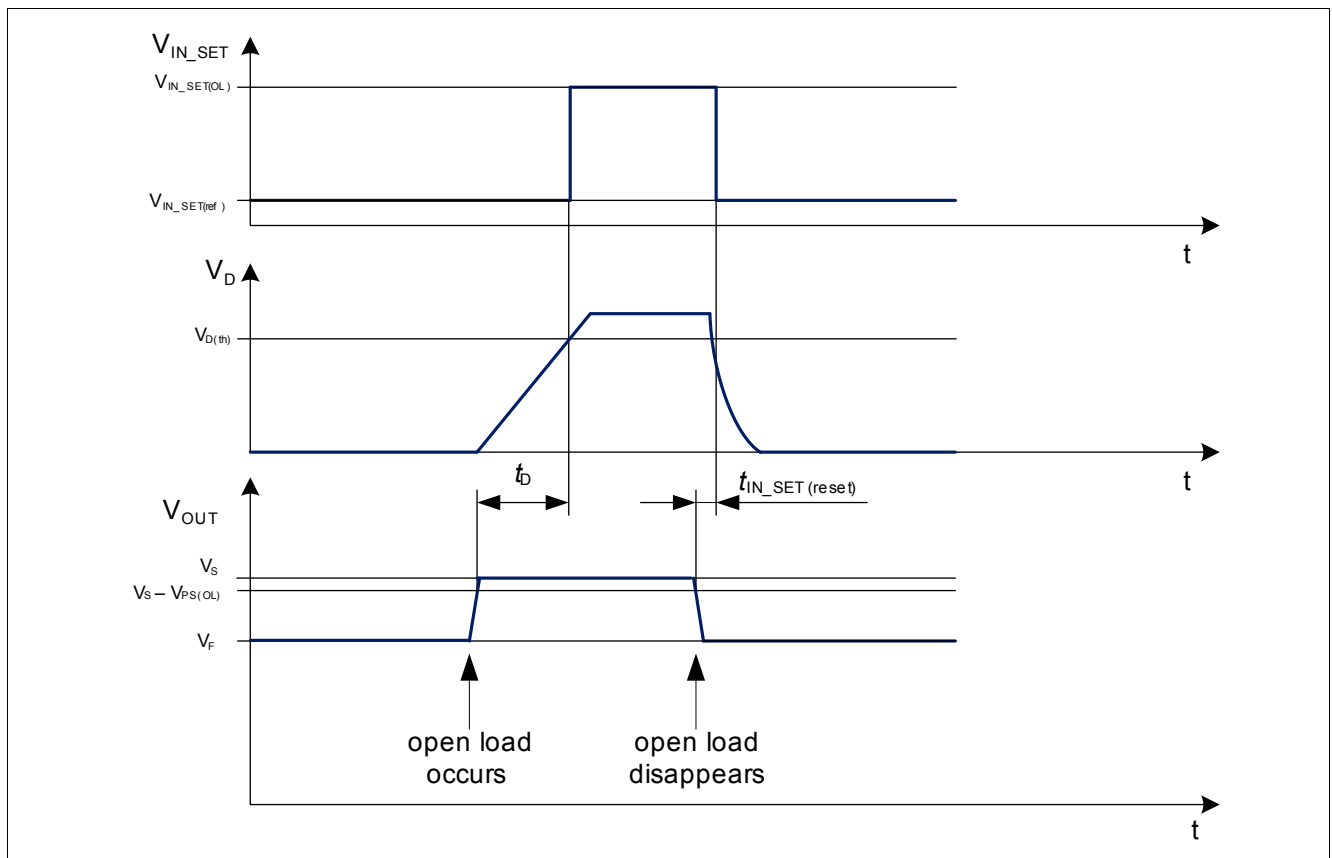


Figure 20 IN_SET behavior during open load condition with ST pin connected to GND

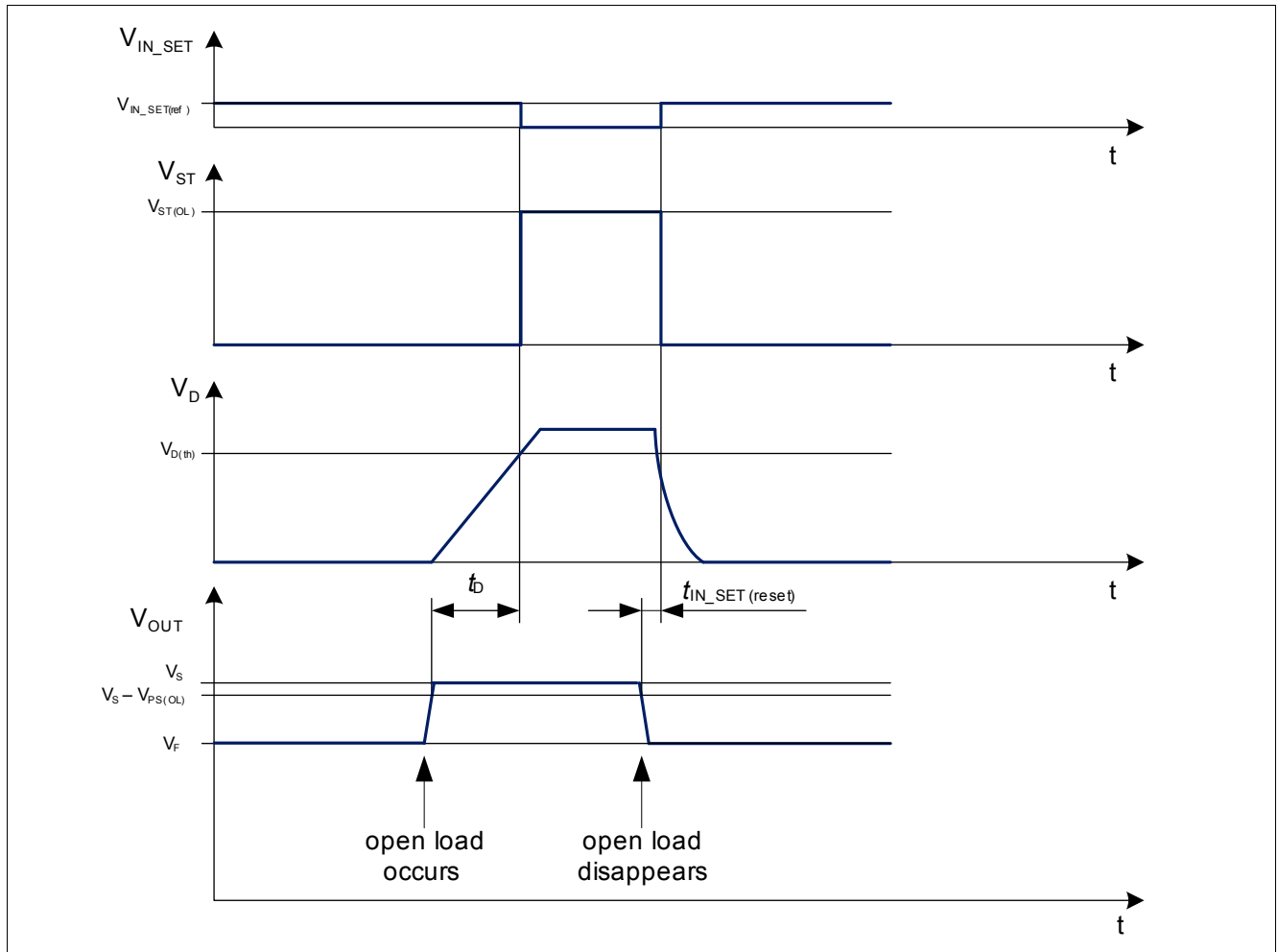


Figure 21 IN_SET and ST behavior during open load condition (ST unconnected)

To provide a Limp Home functionality (reactivation in case of open load instead of complete deactivation) the filter time t_D can be used. If a PWM signal with a frequency higher than $1/t_D$ is applied to the V_S line and EN signal, the OL detection feature will not be activated. The implementation of the D-pin is shown in the following figure:

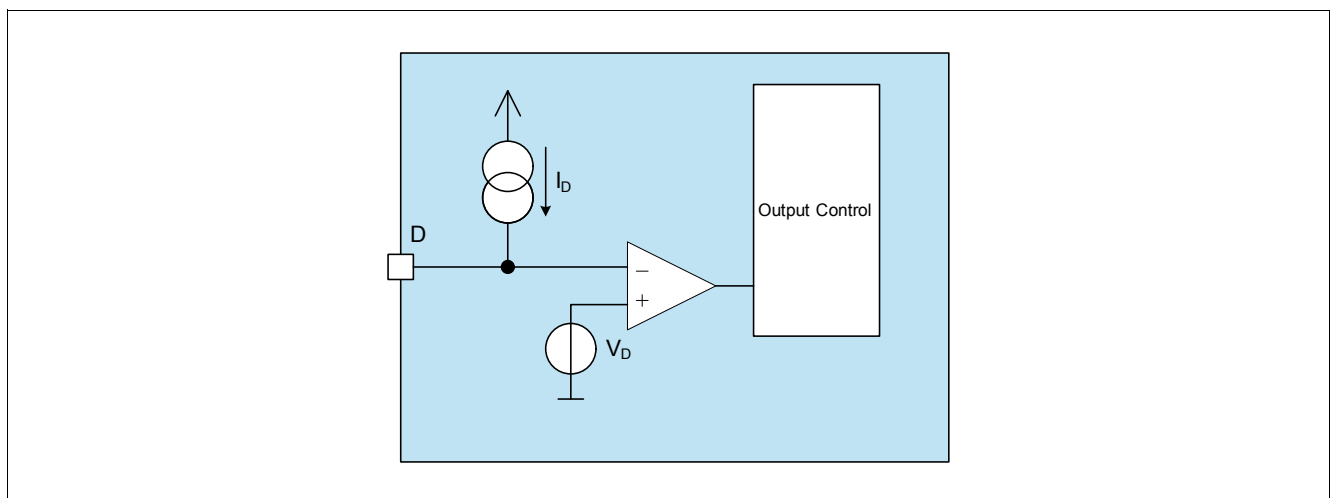


Figure 22 Block Diagram D pin

10.2 Short Circuit to GND detection

The TLD1125EL has an integrated SC to GND detection. If the output stage is turned on and the voltage at the output falls below $V_{OUT(SC)}$ the potential on the IN_SET pin is increased up to $V_{IN_SET(OL/SC)}$ after t_{SC} if the ST pin is connected to GND. If the ST is open or connected to GND via a high ohmic resistor the fault is indicated on the ST pin according to [Chapter 8](#) after t_D . More details are shown in [Figure 24](#). This condition is not latched. For detecting a normal condition after a short circuit detection an output current according to $I_{OUT(SC)}$ is driven by the channel.

The filter time t_D is defined by the charging current I_D [Pos. 10.3.10](#). The time is adjustable by the capacitor connected to the D pin according the following equation:

$$t_{D, typ} = \frac{C_D \cdot V_{D(th)}}{I_D} \quad (11)$$

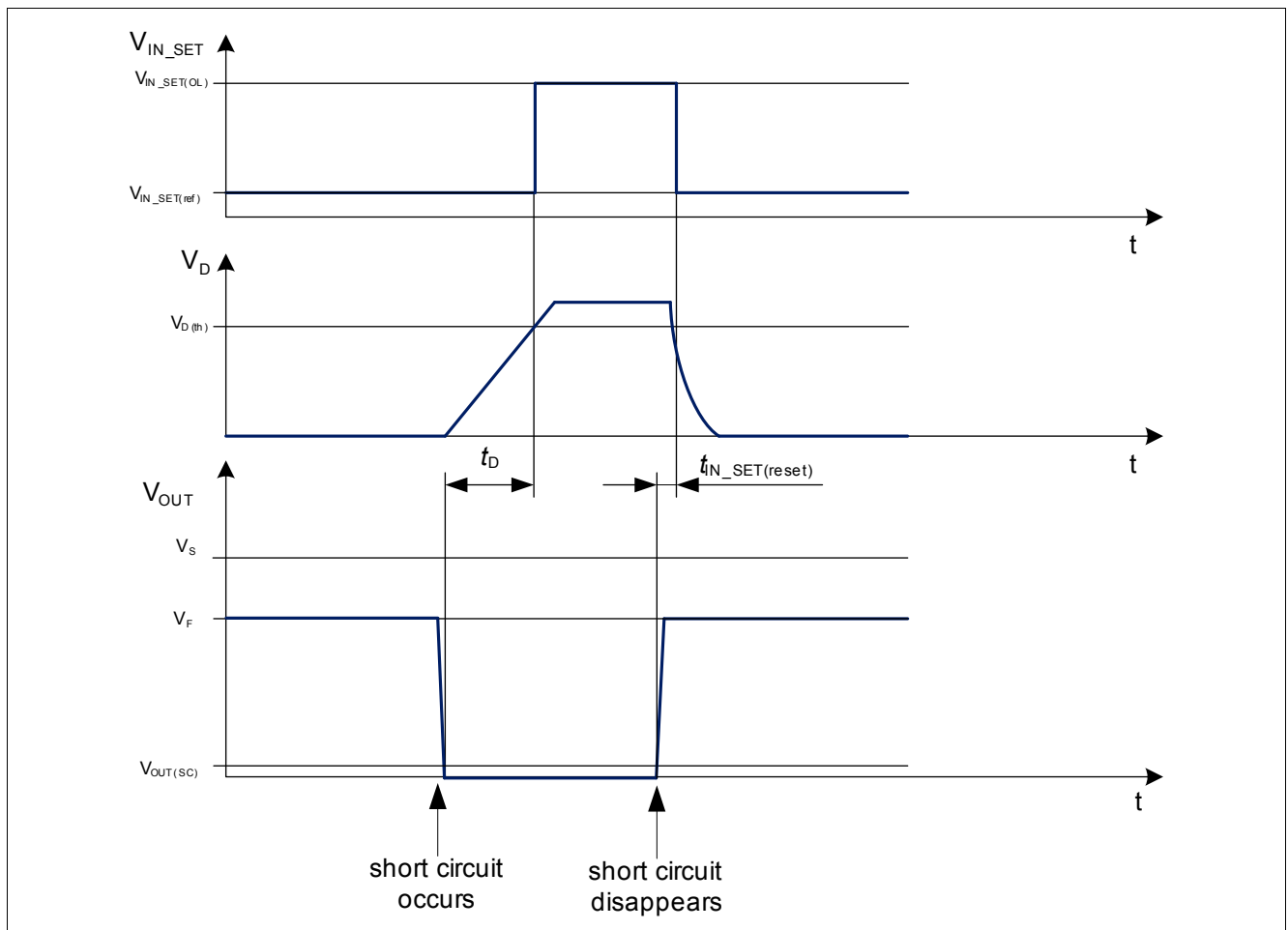


Figure 23 IN_SET behavior during short circuit to GND condition with ST connected to GND

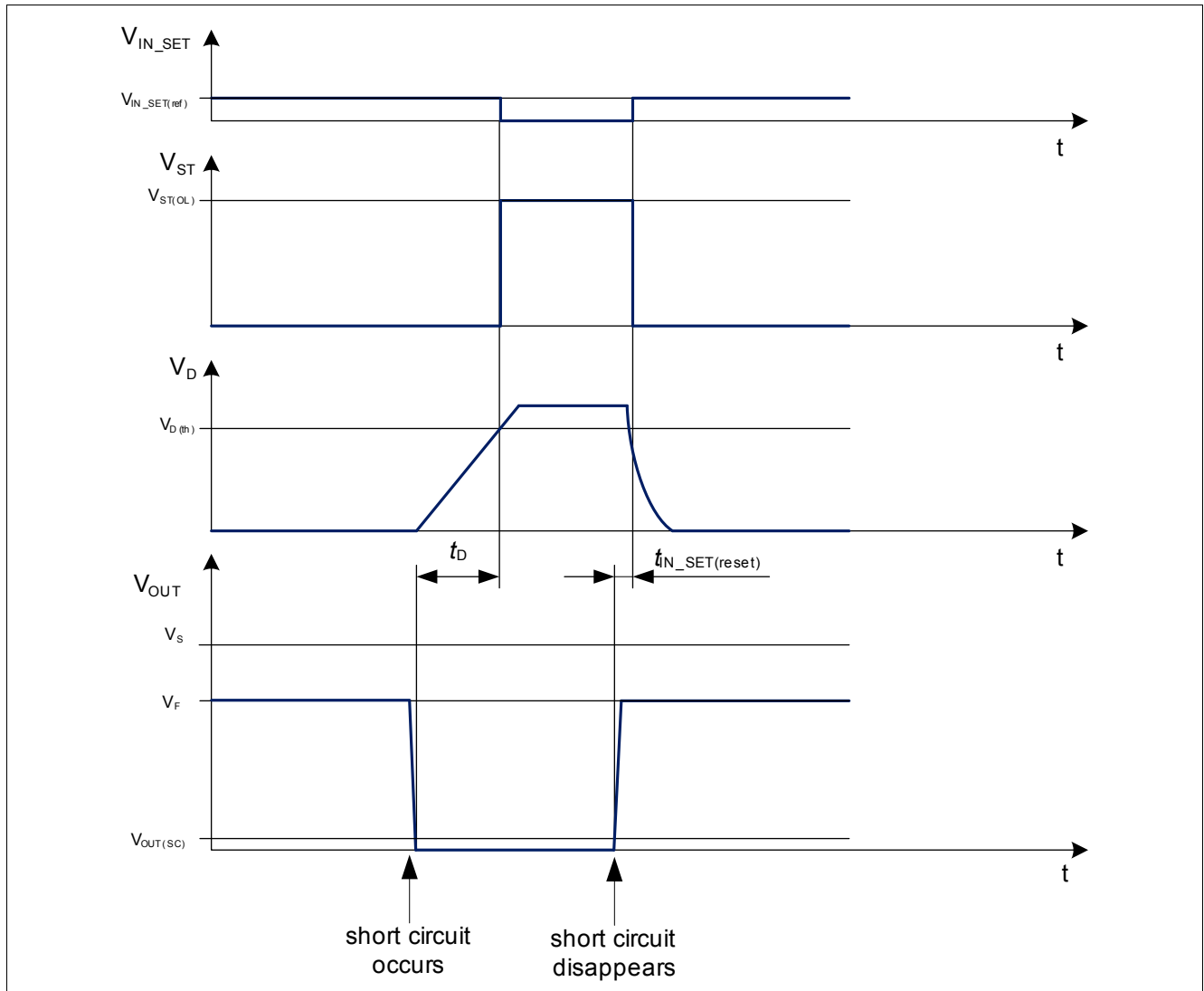


Figure 24 IN_SET and ST behavior during short circuit to GND condition (ST unconnected)

10.3 Electrical Characteristics IN_SET Pin and Load Diagnosis

Electrical Characteristics IN_SET pin and Load Diagnosis

Unless otherwise specified: $V_S = 5.5 \text{ V to } 40 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
10.3.1	IN_SET reference voltage	$V_{IN_SET(ref)}$	1.19	1.23	1.27	V	¹⁾ $V_{OUT} = 3.6 \text{ V}$ $T_j = 25 \dots 115 \text{ }^\circ\text{C}$
10.3.2	IN_SET open load/short circuit voltage	$V_{IN_SET(OL/SC)}$	4	—	5.5	V	¹⁾ $V_S > 8 \text{ V}$ $T_j = 25 \dots 150 \text{ }^\circ\text{C}$ $V_S = V_{OUT(OL)} \text{ or } V_{OUTx} = 0 \text{ V (SC)}$

Electrical Characteristics IN_SET pin and Load Diagnosis (cont'd)

Unless otherwise specified: $V_S = 5.5 \text{ V to } 40 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
10.3.3	IN_SET open load/short circuit current	$I_{IN_SET(OL/SC)}$	1.5	–	7.4	mA	¹⁾ $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $V_{IN_SET} = 4 \text{ V}$ $V_S = V_{OUT} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
10.3.4	ST device turn on threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(L)}$	0.8	–	–	V	–
10.3.5	ST device turn off threshold (active low) in case of voltage applied from external (ST-pin acting as input)	$V_{ST(H)}$	–	–	2.5	V	–
10.3.6	ST pull down current	$I_{ST(PD)}$	–	–	15	μA	$V_{EN} = 5.5 \text{ V}$ $V_{ST} = 0.8 \text{ V}$
10.3.7	ST open load/short circuit voltage (ST-pin acting as diagnosis output)	$V_{ST(OL/SC)}$	4	–	5.5	V	¹⁾ $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $R_{ST} = 470 \text{ k}\Omega$ $V_S = V_{OUT} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
10.3.8	ST open load/short circuit current (ST-pin acting as diagnosis output)	$I_{ST(OL/SC)}$	100	–	220	μA	¹⁾ $V_S > 8 \text{ V}$ $T_j = 25...150 \text{ }^\circ\text{C}$ $V_{ST} = 2.5 \text{ V}$ $V_S = V_{OUT} \text{ (OL) or } V_{OUT} = 0 \text{ V (SC)}$
10.3.9	D high threshold	$V_{D(th)}$	2.45	2.85	3.2	V	$V_S > 8 \text{ V}$
10.3.10	D output current	I_D	1	2	3	μA	$V_S > 8 \text{ V}$ $V_D = 2 \text{ V}$
10.3.11	OL detection voltage $V_{PS(OL)} = V_S - V_{OUT}$	$V_{PS(OL)}$	0.2	–	0.4	V	$V_S > 8 \text{ V}$
10.3.12	Short circuit to GND detection threshold	$V_{OUT(SC)}$	0.8	–	1.4	V	$V_S > 8 \text{ V}$
10.3.13	IN_SET diagnosis reset time	$t_{IN_SET(reset)}$	–	5	20	μs	¹⁾ $V_S > 8 \text{ V}$
10.3.14	SC detection current in case of unconnected ST-pin	$I_{OUT(SC,STu)}$	100	200	300	μA	$V_S > 8 \text{ V}$ $V_{OUT} = 0 \text{ V}$

Electrical Characteristics IN_SET pin and Load Diagnosis (cont'd)

Unless otherwise specified: $V_S = 5.5 \text{ V to } 40 \text{ V}$, $T_j = -40 \text{ }^\circ\text{C to } +150 \text{ }^\circ\text{C}$, $R_{SET} = 12 \text{ k}\Omega$, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
10.3.15	SC detection current in case of ST-pin shorted to GND	$I_{OUT(SC,STG)}$	0.1	2	4.75	mA	$V_S > 8 \text{ V}$ $V_{OUT} = 0 \text{ V}$ $V_{ST} = 0 \text{ V}$
10.3.16	IN_SET activation current without turn on of output stage	$I_{IN_SET(act)}$	2	–	15	μA	See Figure 15

1) Not subject to production test, specified by design

11 Power Stage

The output stage is realized as high side current source with a current of 360 mA. During off state the leakage current at the output stage is minimized in order to prevent a slightly glowing LED.

The maximum current of the channel is limited by the power dissipation and used PCB cooling areas (which results in the applications R_{thJA}).

For an operating current control loop the supply and output voltages according to the following parameters have to be considered:

- Required supply voltage for current control $V_{S(CC)}$, [Pos. 6.3.10](#)
- Voltage drop over output stage during current control $V_{PS(CC)}$, [Pos. 11.2.6](#)
- Required output voltage for current control $V_{OUT(CC)}$, [Pos. 11.2.7](#)

11.1 Protection

The device provides embedded protective functions, which are designed to prevent IC destruction under fault conditions described in this data sheet. Fault conditions are considered as “outside” normal operating range. Protective functions are neither designed for continuous nor for repetitive operation.

11.1.1 Over Load Behavior

An over load detection circuit is integrated in the Basic LED Driver IC. It is realized by a temperature monitoring of the output stage (OUT).

As soon as the junction temperature exceeds the current reduction temperature threshold $T_{j(CRT)}$ the output current will be reduced by the device by reducing the IN_SET reference voltage $V_{IN_SET(ref)}$. This feature avoids LED's flickering during static output overload conditions. Furthermore, it protects LEDs against over temperature, which are mounted thermally close to the device. If the device temperature still increases, the output current decreases close to 0 A. As soon as the device cools down the output current rises again.

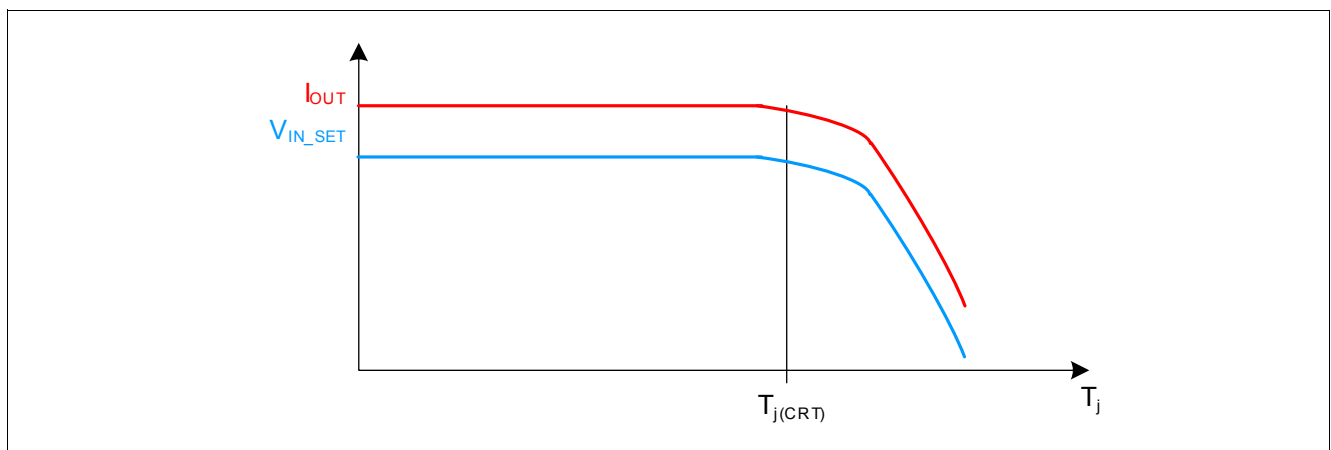


Figure 25 Output current reduction at high temperature

Note: This high temperature output current reduction is realized by reducing the IN_SET reference voltage voltage ([Pos. 10.3.1](#)). In case of very high power loss applied to the device and very high junction temperature the output current may drop down to $I_{OUT} = 0$ mA, after a slight cooling down the current increases again.

11.1.2 Reverse Battery Protection

The TLD1125EL has an integrated reverse battery protection feature. This feature protects the driver IC itself, but also connected LEDs. The output reverse current is limited to $I_{OUTx(rev)}$ by the reverse battery protection.

Note: Due to the reverse battery protection a reverse protection diode for the light module may be obsolete. In case of high ISO-pulse requirements and only minor protecting components like capacitors a reverse protection diode may be reasonable. The external protection circuit needs to be verified in the application.

11.2 Electrical Characteristics Power Stage

Electrical Characteristics Power Stage

Unless otherwise specified: $V_S = 5.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^\circ\text{C}$ to $+150 \text{ }^\circ\text{C}$, $V_{OUT} = 3.6 \text{ V}$, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
11.2.1	Output leakage current	$I_{OUT(leak)}$	–	–	21 9	μA	$V_{EN} = 5.5 \text{ V}$ $I_{IN_SET} = 0 \mu\text{A}$ $V_{OUT} = 2.5 \text{ V}$ $T_j = 150 \text{ }^\circ\text{C}$ ¹⁾ $T_j = 85 \text{ }^\circ\text{C}$
11.2.2	Output leakage current in boost over battery setup	$-I_{OUT(leak,B2B)}$	–	–	150	μA	¹⁾ $V_{EN} = 5.5 \text{ V}$ $I_{IN_SET} = 0 \mu\text{A}$ $V_{OUT} = V_S = 40 \text{ V}$
11.2.3	Reverse output current	$-I_{OUT(rev)}$	–	–	3	μA	¹⁾ $V_S = -16 \text{ V}$ Output load: LED with break down voltage $< -0.6 \text{ V}$
11.2.4	Output current accuracy limited temperature range	k_{LT}	2092 1800	2250 2250	2408 2700		¹⁾ $T_j = 25...115 \text{ }^\circ\text{C}$ $V_S = 8...18 \text{ V}$ $V_{PS} = 2 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ $R_{SET} = 30 \text{ k}\Omega$
11.2.5	Output current accuracy over temperature	k_{ALL}	1980 1710	2250 2250	2520 2790		¹⁾ $T_j = -40...115 \text{ }^\circ\text{C}$ $V_S = 8...18 \text{ V}$ $V_{PS} = 2 \text{ V}$ $R_{SET} = 6...12 \text{ k}\Omega$ $R_{SET} = 30 \text{ k}\Omega$
11.2.6	Voltage drop over power stage during current control $V_{PS(CC)} = V_S - V_{OUT}$	$V_{PS(CC)}$	0.75	–	–	V	¹⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ $I_{OUT} \geq 90\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.7	Required output voltage for current control	$V_{OUT(CC)}$	2.3	–	–	V	¹⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ $I_{OUT} \geq 90\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.8	Maximum output current	$I_{OUT(max)}$	360	–	–	mA	$R_{SET} = 4.7 \text{ k}\Omega$ The maximum output current is limited by the thermal conditions. Please refer to Pos. 4.3.1 - Pos. 4.3.3

Electrical Characteristics Power Stage (cont'd)

Unless otherwise specified: $V_S = 5.5 \text{ V}$ to 18 V , $T_j = -40 \text{ }^\circ\text{C}$ to $+150 \text{ }^\circ\text{C}$, $V_{OUT} = 3.6 \text{ V}$, all voltages with respect to ground, positive current flowing into pin for input pins (I), positive currents flowing out of the I/O and output pins (O) (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
11.2.9	PWMI turn on time	$t_{ON(PWMI)}$	—	—	15	μs	²⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ PWMI \rightarrow L $I_{OUT} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.10	PWMI turn off time	$t_{OFF(PWMI)}$	—	—	10	μs	²⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ PWMI \rightarrow H $I_{OUT} = 20\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.11	ST turn on time	$t_{ON(ST)}$	—	—	15	μs	³⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ ST \rightarrow L $I_{OUT} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.12	ST turn off time	$t_{OFF(ST)}$	—	—	10	μs	³⁾ $V_S = 13.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ ST \rightarrow H $I_{OUT} = 20\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.13	IN_SET turn on time	$t_{ON(IN_SET)}$	—	—	15	μs	$V_S = 13.5 \text{ V}$ $I_{IN_SET} = 0 \rightarrow 100 \mu\text{A}$ $I_{OUT} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.14	IN_SET turn off time	$t_{OFF(IN_SET)}$	—	—	10	μs	$V_S = 13.5 \text{ V}$ $I_{IN_SET} = 100 \rightarrow 0 \mu\text{A}$ $I_{OUT} = 20\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.15	VS turn on time	$t_{ON(VS)}$	—	—	20	μs	^{1) 4)} $V_{EN} = 5.5 \text{ V}$ $R_{SET} = 12 \text{ k}\Omega$ $V_S = 0 \rightarrow 13.5 \text{ V}$ $I_{OUT} = 80\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.16	Current reduction temperature threshold	$T_{j(CRT)}$	—	140	—	$^\circ\text{C}$	¹⁾ $I_{OUT} = 95\%$ of $(k_{LT(typ)}/R_{SET})$
11.2.17	Output current during current reduction at high temperature	$I_{OUT(CRT)}$	85% of $(k_{LT(typ)}/R_{SET})$	—	—	A	¹⁾ $R_{SET} = 12 \text{ k}\Omega$ $T_j = 150 \text{ }^\circ\text{C}$

1) Not subject to production test, specified by design

2) see also [Figure 8](#)

3) see also [Figure 18](#)

4) see also [Figure 6](#)

12 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

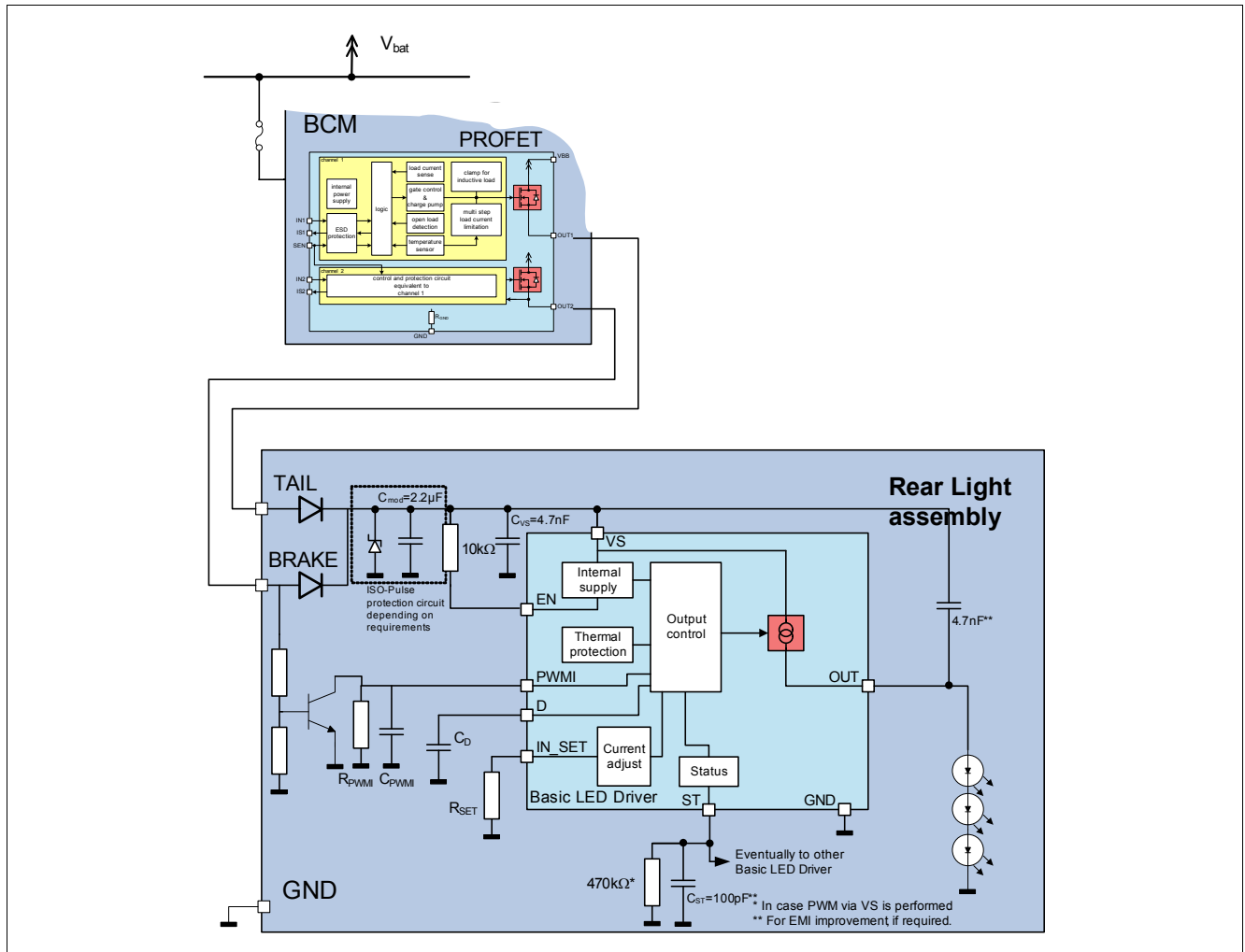


Figure 26 Application Diagram

Note: This is a very simplified example of an application circuit. In case of high ISO-pulse requirements a reverse protection diode may be used for LED protection. The function must be verified in the real application.

12.1 Further Application Information

- For further information you may contact <http://www.infineon.com/>

13 Package Outlines

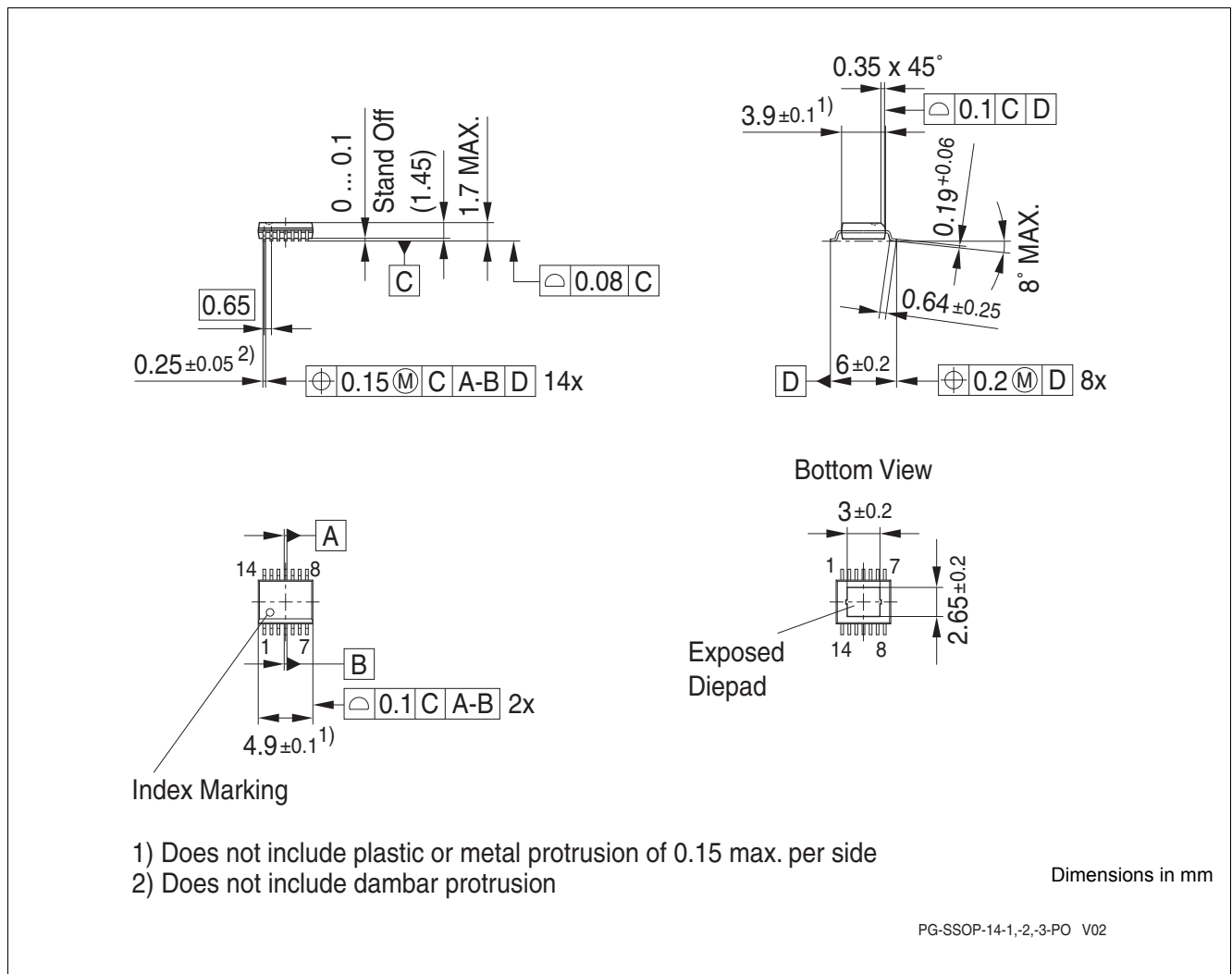


Figure 27 PG-SSOP14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:

<http://www.infineon.com/packages>.

14 Revision History

Revision	Date	Changes
1.0	2013-08-08	Initial revision of data sheet

Edition 2013-08-08

**Published by
Infineon Technologies AG
81726 Munich, Germany**

**© 2013 Infineon Technologies AG
All Rights Reserved.**

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.