

TLC7226C, TLC7226I, TLC7226M QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

features

- Four 8-Bit D/A Converters
- Microprocessor Compatible
- TTL/CMOS Compatible
- Single Supply Operation Possible
- CMOS Technology

applications

- Process Control
- Automatic Test Equipment
- Automatic Calibration of Large System Parameters, e.g. Gain/Offset

description

The TLC7226C, TLC7226I, and TLC7226M consist of four 8-bit voltage-output digital-to-analog converters (DACs) with output buffer amplifiers and interface logic on a single monolithic chip.

Separate on-chip latches are provided for each of the four DACs. Data is transferred into one of these data latches through a common 8-bit TTL/CMOS-compatible 5-V input port. Control inputs A0 and A1 determine which DAC is loaded when \overline{WR} goes low. The control logic is speed compatible with most 8-bit microprocessors.

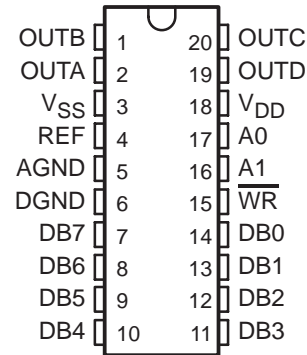
Each DAC includes an output buffer amplifier capable of sourcing up to 5 mA of output current.

The TLC7226 performance is specified for input reference voltages from 2 V to $V_{DD} - 4$ V with dual supplies. The voltage mode configuration of the DACs allows the TLC7226 to be operated from a single power supply rail at a reference of 10 V.

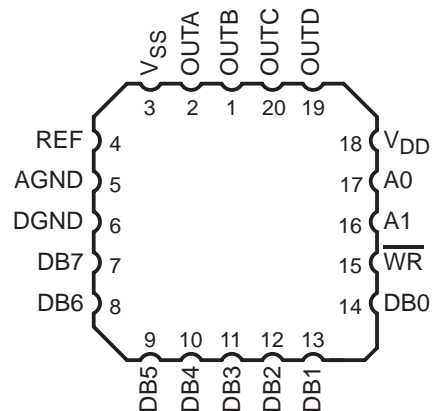
The TLC7226 is fabricated in a LinBiCMOS™ process that has been specifically developed to allow high-speed digital logic circuits and precision analog circuits to be integrated on the same chip. The TLC7226 has a common 8-bit data bus with individual DAC latches. This provides a versatile control architecture for simple interface to microprocessors. All latch-enable signals are level triggered.

Combining four DACs, four operational amplifiers, and interface logic into either a 0.3-inch wide, 20-terminal dual-in-line IC (DIP) or a small 20-terminal small-outline IC (SOIC) allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. The Leadless Ceramic Chip Carrier (LCCC) package provides for operation at military temperature range. The pinout is aimed at optimizing board layout with all of the analog inputs and outputs at one end of the package and all of the digital inputs at the other.

DW OR N PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinBiCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2009, Texas Instruments Incorporated

TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

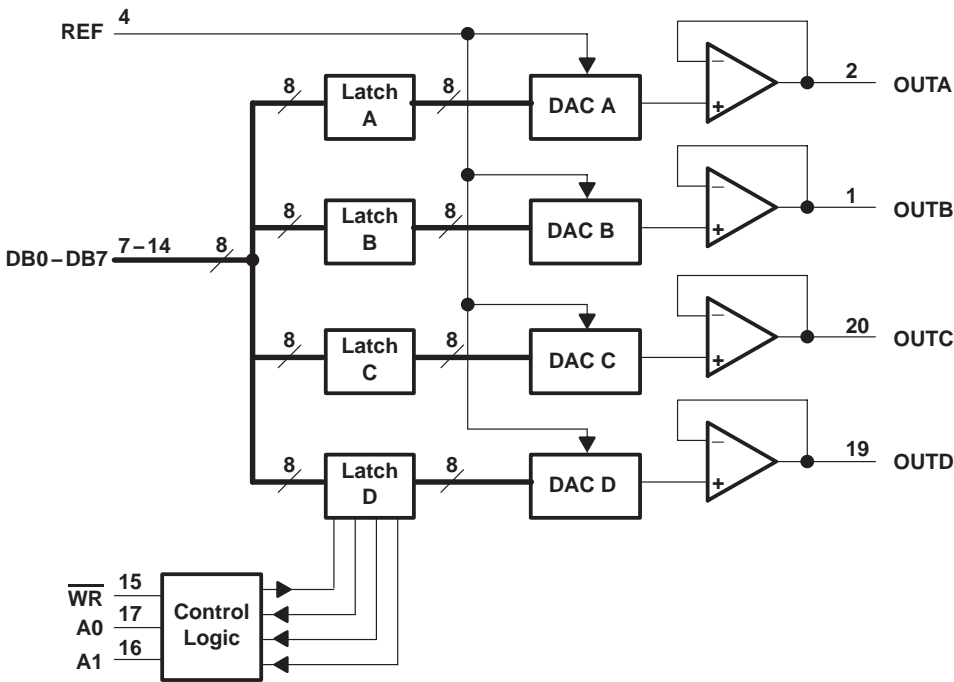
SLAS060F – JANUARY 1995 – REVISED APRIL 2009

description (continued)

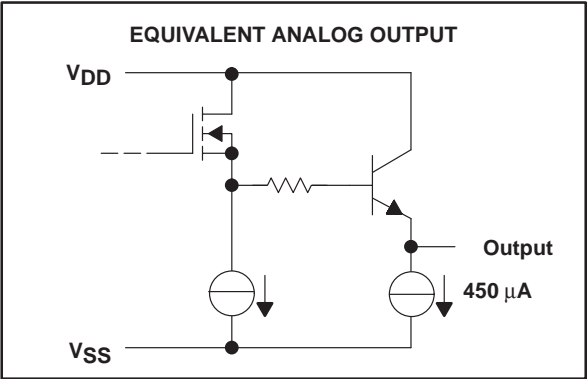
The TLC7226C is characterized for operation from 0°C to 70°C. The TLC7226I is characterized for operation from –30°C to 85°C. The TLC7226M is characterized for operation from –55°C to 125°C.

T _A	AVAILABLE OPTIONS		
	PACKAGE		
	SMALL OUTLINE (DW)	PLASTIC DIP (N)	LCCC (FK)
0°C to 70°C	TLC7226CDW	TLC7226CN	—
–30°C to 85°C	TLC7226IDW	TLC7226IN	—
–55°C to 125°C	—	—	TLC7226MFKB

functional block diagram



schematic of outputs



TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

Terminal Functions

TERMINAL NAME	NO.†	I/O	DESCRIPTION
AGND	5		Analog ground. AGND is the reference and return terminal for the analog signals and supply.
A0, A1	17, 16	I	DAC select inputs. The combination of high or low levels select either DACA, DACB, DACC, or DACD.
DGND	6		Digital ground. DGND is the reference and return terminal for the digital signals and supply.
DB0–DB7	14–7	I	Digital DAC data inputs. DB0–DB7 are the input digital data used for conversion.
OUTA	2	O	DACA output. OUTA is the analog output of DACA.
OUTB	1	O	DACB output. OUTB is the analog output of DACB.
OUTC	20	O	DACC output. OUTC is the analog output of DACC.
OUTD	19	O	DACD output. OUTD is the analog output of DACD.
REF	4	I	Voltage reference input. The voltage level on REF determines the full scale analog output.
V _{DD}	18		Positive supply voltage input terminal
V _{SS}	3		Negative supply voltage input terminal
WR	15	I	Write input. WR selects DAC transparency or latch mode. The selected input latch is transparent when $\overline{\text{WR}}$ is low.

† Terminal numbers shown are for the DW, N, and FK packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{DD} : AGND or DGND	–0.3 V to 17 V
V _{SS} ‡	–0.3 V to 24 V
Supply voltage range, V _{SS} : AGND or DGND	–7 V to 0.3 V
Voltage range between AGND and DGND	–17 V to 17 V
Input voltage range, V _I (to DGND)	–0.3 V to V _{DD} + 0.3 V
Reference voltage range: V _{ref} (to AGND)	–0.3 V to V _{DD}
V _{ref} (to V _{SS})	–0.3 V to 20 V
Output voltage range, V _O (to AGND) (see Note 1)	V _{SS} to V _{DD}
Continuous total power dissipation at (or below) T _A = 25°C (see Note 2)	500 mW
Operating free-air temperature range, T _A : C suffix	0°C to 70°C
E suffix	–30°C to 85°C
M suffix	–55°C to 125°C
Storage temperature range, T _{stg}	–65°C to 150°C
Case temperature for 10 seconds: FK package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The V_{SS} terminal is connected to the substrate and must be tied to the most negative supply voltage applied to the device.

- NOTES: 1. Output voltages may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.
2. For operation above T_A = 75°C, derate linearly at the rate of 2 mW/°C.



TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		11.4	16.5	V
Supply voltage, V_{SS}		-5.5	0	V
High-level input voltage, V_{IH}		2		V
Low-level input voltage, V_{IL}			0.8	V
Reference voltage, V_{ref}		0	$V_{DD}-4$	V
Load resistance, R_L		2		k Ω
Setup time, address valid before $\overline{WR}\downarrow$, $t_{su(AW)}$ (see Figure 1)	$V_{DD} = 11.4 \text{ V to } 16.5 \text{ V}$	*0		ns
Setup time, data valid before $\overline{WR}\uparrow$, $t_{su(DW)}$ (see Figure 1)	$V_{DD} = 11.4 \text{ V to } 16.5 \text{ V}$	*45		ns
Hold time, address valid after $\overline{WR}\uparrow$, $t_{h(AW)}$ (see Figure 1)	$V_{DD} = 11.4 \text{ V to } 16.5 \text{ V}$	*0		ns
Hold time, data valid after $\overline{WR}\uparrow$, $t_{h(DW)}$ (see Figure 1)	$V_{DD} = 11.4 \text{ V to } 16.5 \text{ V}$	*10		ns
Pulse duration, \overline{WR} low, t_w (see Figure 1)	$V_{DD} = 11.4 \text{ V to } 16.5 \text{ V}$	*50		ns
Operating free-air temperature, T_A	C suffix	0	70	$^{\circ}\text{C}$
	I suffix	-25	85	
	M suffix	-55	125	

* This parameter is not tested for M suffix devices.

electrical characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current, digital	$V_I = 0 \text{ V or } V_{DD}$				± 1	μA
$I_{(DD)}$	Supply current	$V_I = 0.8 \text{ V or } 2.4 \text{ V}, V_{DD} = 16.5 \text{ V}, V_{SS} = -5 \text{ V},$ No load			6	16	mA
$I_{(SS)}$	Supply current	$V_I = 0.8 \text{ V or } 2.4 \text{ V},$ No load			4	10	mA
$r_{i(ref)}$	Reference input resistance			2	4		k Ω
Power supply sensitivity		$\Delta V_{DD} = \pm 5\%$				0.01	%/%
C_i	REF input	All 0s loaded	C and I suffix	65			pF
			M suffix	*30			
		All 1s loaded			*300		
	Digital inputs		C and I suffix		8		
			M suffix		*12		

* This parameter is not tested for M suffix devices.

TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

operating characteristics over recommended operating free-air temperature range

dual power supply over recommended power supply and reference voltage ranges, AGND = DGND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Slew rate			*2.5			V•μs
Settling time to 1/2 LSB	Positive full scale	V _{ref} = 10 V	*5			μs
	Negative full scale		*7			
Resolution			8			bits
Total unadjusted error		V _{DD} = 15 V ±5%, V _{ref} = 10 V	±2			LSB
Linearity error	Differential/integral		±1			LSB
Full-scale error			±2			LSB
Gain error			±0.25			LSB
Temperature coefficient of gain	Full scale	V _{DD} = 14 V to 16.5 V, V _{ref} = 10 V	±20			ppm/°C
	Zero-code error		±50			μV/°C
Zero-code error			±20 ±80			mV
Digital crosstalk glitch impulse area		V _{ref} = 0	50			nV•s

* This parameter is not tested for M suffix devices.

single power supply, $V_{DD} = 14.25\text{ V to } 15.75\text{ V}$, $V_{SS} = \text{AGND} = \text{DGND} = 0\text{ V}$, $V_{ref} = 10\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current, I_{DD}		$V_I = 0.8\text{ V or } 2.4\text{ V}$, No load		5	13	mA
Slew rate			*2			V•μs
Settling time to 1/2 LSB	Positive full scale				*5	μs
	Negative full scale				*20	
Resolution				8		bits
Total unadjusted error					±2	LSB
Full-scale error					±2	LSB
Temperature coefficient of gain	Full scale	$V_{DD} = 14\text{ V to } 16.5\text{ V}$, $V_{ref} = 10\text{ V}$			±20	ppm/°C
	Zero-code error				±50	μV/°C
Linearity error					±1	LSB
Digital crosstalk-glitch impulse area				50		nV•s

* This parameter is not tested for M suffix devices.

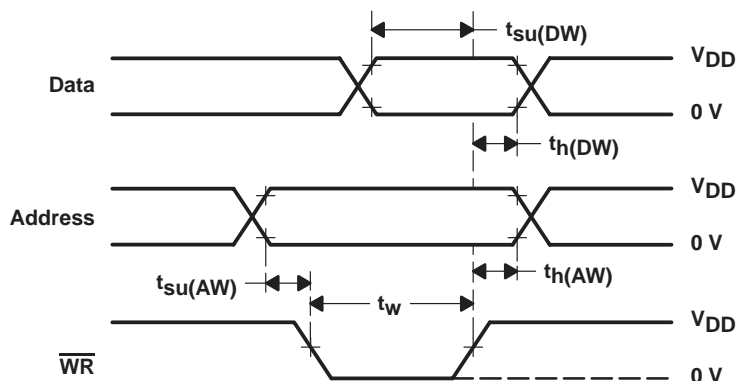


TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $t_r = t_f = 20$ ns over V_{DD} range.
 - The timing measurement reference level is equal to $V_{IH} + V_{IL}$ divided by 2.
 - The selected input latch is transparent while \overline{WR} is low. Invalid data during this time can cause erroneous outputs.

Figure 1. Write-Cycle Voltage Waveforms

TYPICAL CHARACTERISTICS

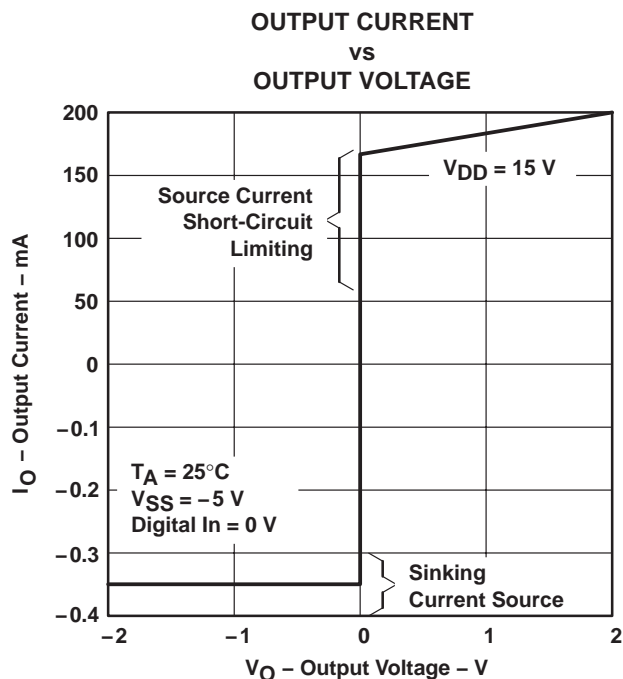


Figure 2

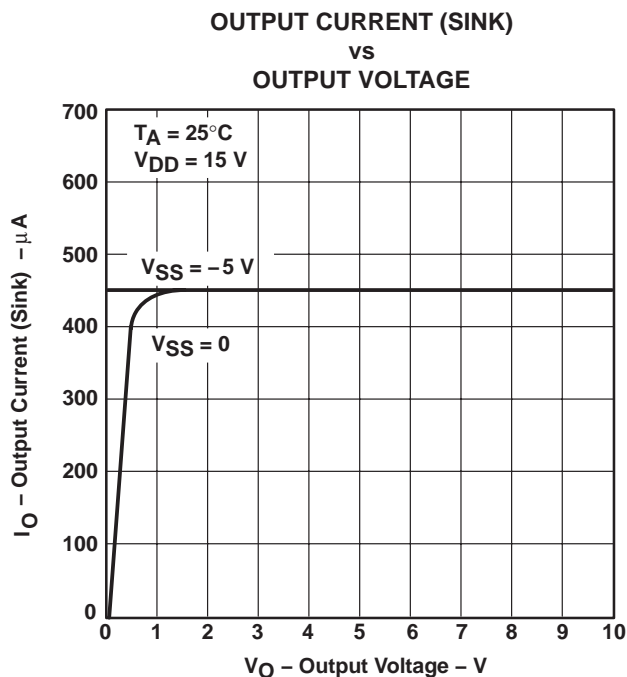
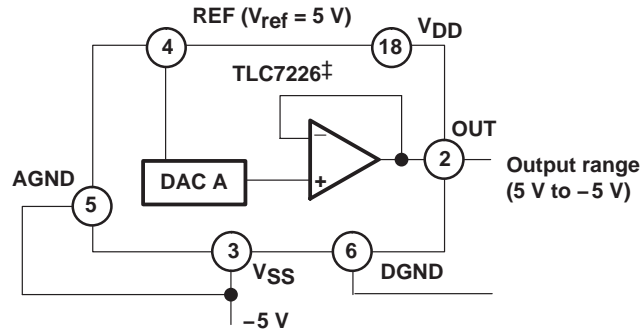


Figure 3

PRINCIPLES OF OPERATION

AGND bias for direct bipolar output operation

The TLC7226 can be used in bipolar operation without adding more external operational amplifiers as shown in Figure 4 by biasing AGND to V_{SS} . This configuration provides an excellent method for providing a direct bipolar output with no additional components. The transfer values are shown in Table 1.



‡ Digital inputs omitted for clarity.

Figure 4. AGND Bias for Direct Bipolar Operation

Table 1. Bipolar (Offset Binary) Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+V_{ref} \left(\frac{127}{128} \right)$
1000	0001	$+V_{ref} \left(\frac{1}{128} \right)$
1000	0000	0 V
0111	1111	$-V_{ref} \left(\frac{1}{128} \right)$
0000	0001	$-V_{ref} \left(\frac{127}{128} \right)$
0000	0000	$-V_{ref} \left(\frac{128}{128} \right) = -V_{ref}$

AGND bias for positive output offset

The TLC7226 AGND terminal can be biased above or below the system ground terminal, DGND, to provide an offset analog output voltage level. Figure 5 shows a circuit configuration to achieve this for channel A of the TLC7226. The output voltage, V_O , at OUTA can be expressed as:

$$V_O = V_{BIAS} + D_A (V_I) \quad (1)$$

where D_A is a fractional representation of the digital input word ($0 \leq D \leq 255/256$).

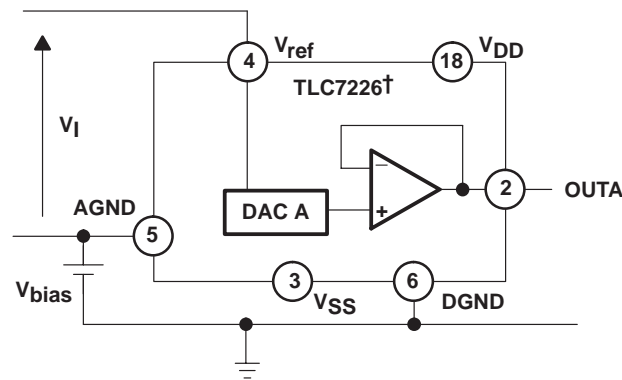
Increasing AGND above system GND reduces the output range. $V_{DD} - V_{ref}$ must be at least 4 V to ensure specified operation. Since the AGND terminal is common to all four DACs, this method biases up the output voltages of all the DACs in the TLC7226. Supply voltages V_{DD} and V_{SS} for the TLC7226 should be referenced to DGND.

TLC7226C, TLC7226I, TLC7226M
QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

PRINCIPLES OF OPERATION

AGND bias for positive output offset (continued)



† Digital inputs omitted for clarity.

Figure 5. AGND Bias Circuit

interface logic information

Address lines A0 and A1 select which DAC accepts data from the input port. Table 2 shows the operations of the four DACs. Figure 6 shows the input control logic. When the \overline{WR} signal is low, the input latches of the selected DAC are transparent and the output responds to activity on the data bus. The data is latched into the addressed DAC latch on the rising edge of \overline{WR} . While \overline{WR} is high, the analog outputs remain at the value corresponding to the data held in their respective latches.

Table 2. Function Table

CONTROL INPUTS			OPERATION
\overline{WR}	A1	A0	
H	X	X	No operation Device not selected
L	L	L	DAC A transparent
↑	L	L	DAC A latched
L	L	H	DAC B transparent
↑	L	H	DAC B latched
L	H	L	DAC C transparent
↑	H	L	DAC C latched
L	H	H	DAC D transparent
↑	H	H	DAC D latched

L = low, H = high, X = irrelevant

PRINCIPLES OF OPERATION

interface logic information (continued)

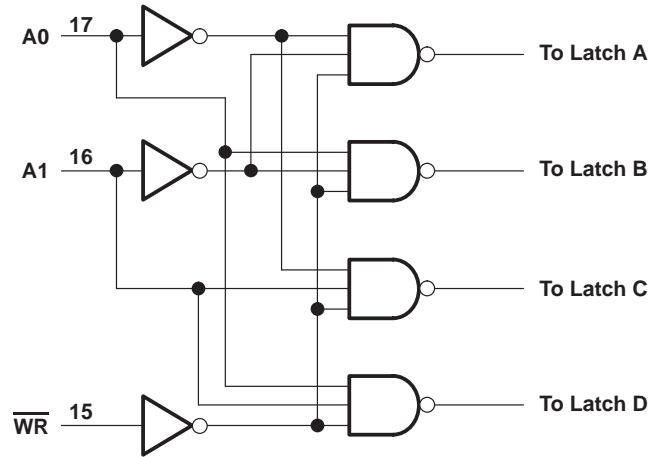


Figure 6. Input Control Logic

unipolar output operation

The unipolar output operation is the basic mode of operation for each channel of the TLC7226, with the output voltages having the same positive polarity as V_{ref} . The TLC7226 can be operated with a single power supply ($V_{SS} = AGND$) or with positive/negative power supplies. The voltage at V_{ref} must never be negative with respect to AGND to prevent parasitic transistor turnon. Connections for the unipolar output operation are shown in Figure 7. Transfer values are shown in Table 3.

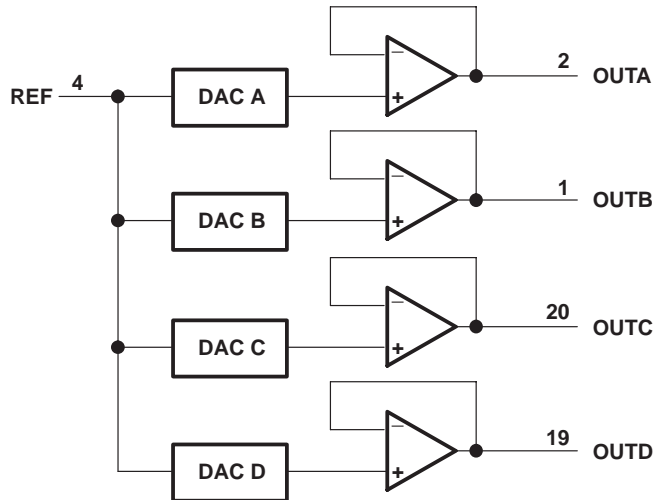


Figure 7. Unipolar Output Circuit

Table 3. Unipolar Code

DAC LATCH CONTENTS		ANALOG OUTPUT
MSB	LSB	
1111	1111	$+ V_{ref} \left(\frac{255}{256} \right)$
1000	0001	$+ V_{ref} \left(\frac{129}{256} \right)$
1000	0000	$+ V_{ref} \left(\frac{128}{256} \right) = + \frac{V_{ref}}{2}$
0111	1111	$+ V_{ref} \left(\frac{127}{256} \right)$
0000	0001	$+ V_{ref} \left(\frac{1}{256} \right)$
0000	0000	0 V

NOTE A. $1 \text{ LSB} = (V_{ref} 2^{-8}) = V_{ref} \left(\frac{1}{256} \right)$

TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

PRINCIPLES OF OPERATION

linearity, offset, and gain error using single-ended power supplies

When an amplifier is operated from a single power supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot be driven to a negative voltage.

So when the output offset voltage is negative, the output voltage remains at zero volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in a transfer function shown in Figure 8.

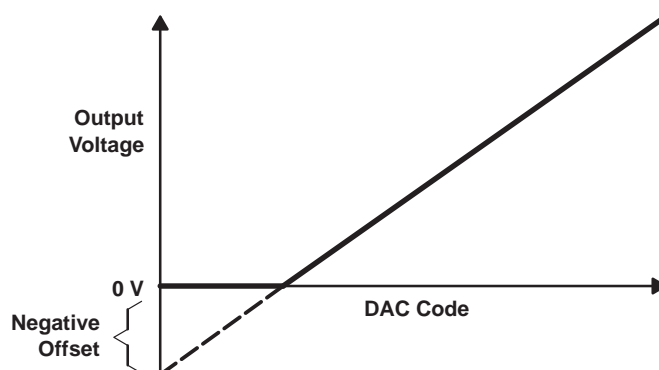


Figure 8. Effect of Negative Offset (Single Power Supply)

This negative offset error, not the linearity error, produces the breakpoint. The transfer function would have followed the dotted line if the output buffer could be driven to a negative voltage.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single power supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity in the unipolar mode is measured between full scale code and the lowest code which produces a positive output voltage.

The code is calculated from the maximum specification for the negative offset.

APPLICATION INFORMATION

bipolar output operation using external amplifier

Each of the DACs of the TLC7226 can also be individually configured to provide bipolar output operation, using an external amplifier and two resistors per channel. Figure 9 shows a circuit used to implement offset binary coding (bipolar operation) with DAC A of the TLC7226. In this case:

$$V_O = 1 + \frac{R_2}{R_1} \times (D_A \times V_{ref}) - \frac{R_2}{R_1} \times (V_{ref}) \quad (2)$$

with $R_1 = R_2$

$$V_O = (2D_A - 1) \times V_{ref}$$

where D_A is a fractional representation of the digital word in latch A.

Mismatch between R_1 and R_2 causes gain and offset errors. Therefore, these resistors must match and track over temperature. The TLC7226 can be operated with a single power supply or from positive and negative power supplies.

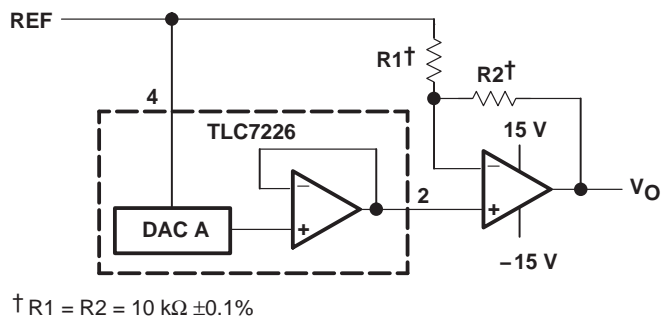


Figure 9. Bipolar Output Circuit

staircase window comparator

In many test systems, it is important to be able to determine whether some parameter lies within defined limits. The staircase window comparator shown in Figure 10 is a circuit that can be used to measure the V_{OH} and V_{OL} thresholds of a TTL device under test. Upper and lower limits on both V_{OH} and V_{OL} can be programmed using the TLC7226. Each adjacent pair of comparators forms a window of programmable size (see Figure 11). When the test voltage (V_{test}) is within a window, then the output for that window is higher. With a reference of 2.56 V applied to the REF input, the minimum window size is 10 mV.

TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

APPLICATION INFORMATION

staircase window comparator (continued)

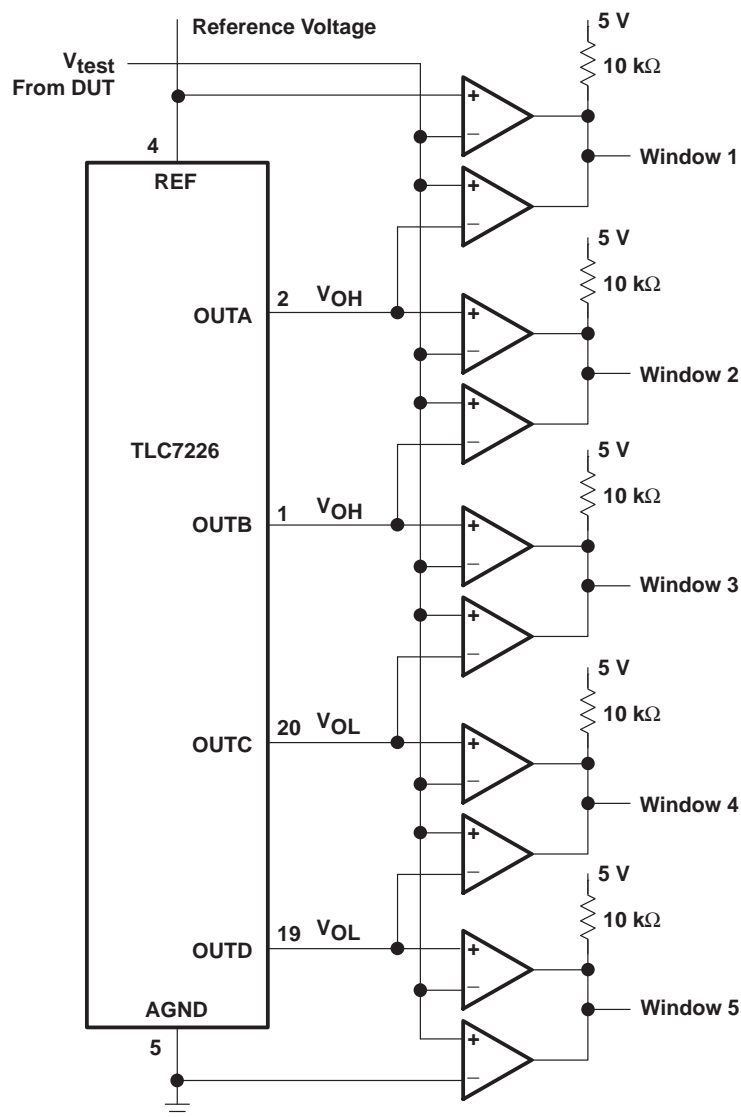


Figure 10. Logic Level Measurement

APPLICATION INFORMATION

staircase window comparator (continued)

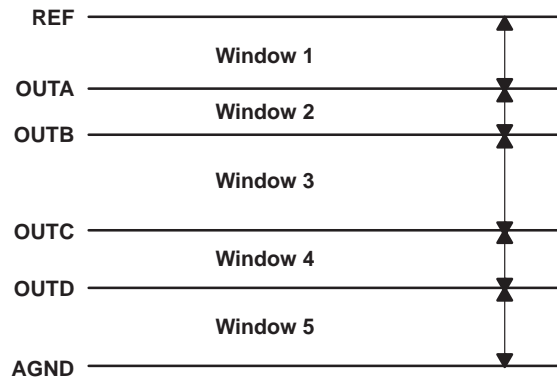


Figure 11. Adjacent Window Structure

The circuit can easily be adapted as shown in Figure 12 to allow for overlapping of windows. When the three outputs from this circuit are decoded, five different nonoverlapping programmable window possibilities can again be defined (see Figure 13).

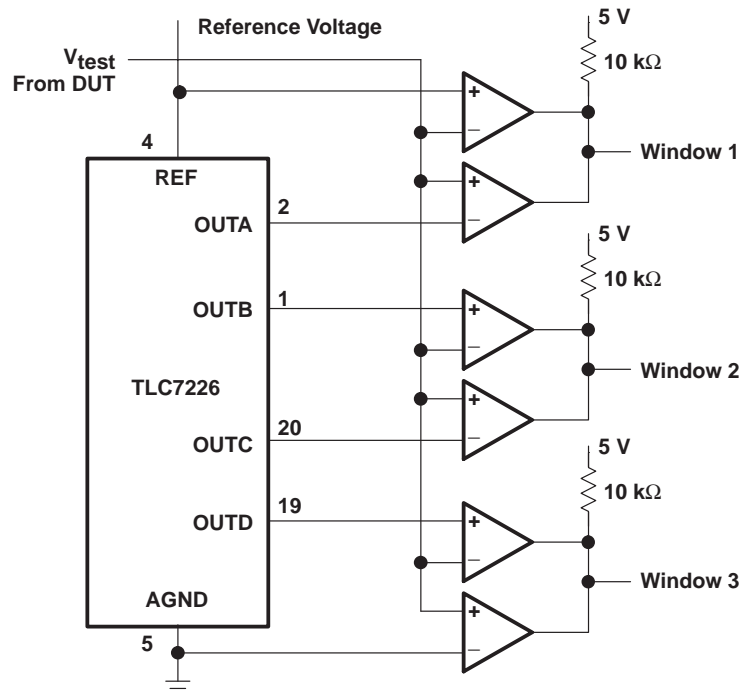


Figure 12. Overlapping Window Circuit

TLC7226C, TLC7226I, TLC7226M

QUADRUPLE 8-BIT DIGITAL-TO-ANALOG CONVERTERS

SLAS060F – JANUARY 1995 – REVISED APRIL 2009

APPLICATION INFORMATION

staircase window comparator (continued)

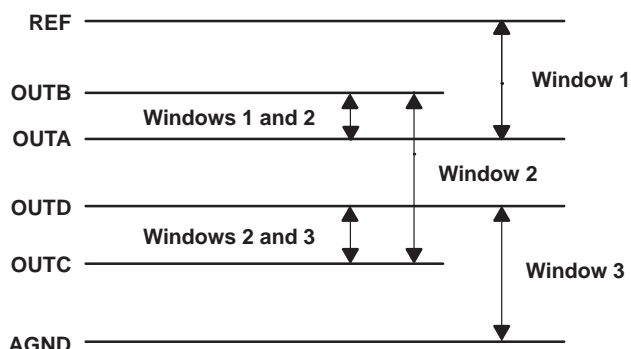


Figure 13. Overlapping Window Structure

output buffer amplifier

The unity-gain output amplifier is capable of sourcing 5 mA into a 2-k Ω load and can drive a 3300-pF capacitor. The output can be shorted to AGND indefinitely or it can be shorted to any voltage between V_{SS} and V_{DD} consistent with the maximum device power dissipation.

multiplying DAC

The TLC7226 can be used as a multiplying DAC when the reference signal is maintained between 2 V and $V_{DD} - 4$ V. When this configuration is used, V_{DD} should be 14.25 V to 15.75 V. A low output-impedance buffer should be used so that the input signal is not loaded by the resistor ladder. Figure 14 shows the general schematic.

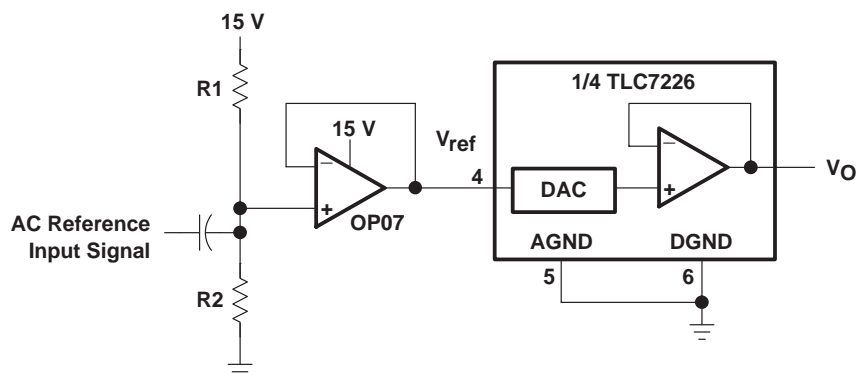


Figure 14. AC Signal Input Scheme

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-87802012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-87802012C	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
TLC7226CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226CDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226CDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226CN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7226CNE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7226IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226IDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TLC7226IN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7226INE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
TLC7226MFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC7226, TLC7226M :

- Catalog: [TLC7226](#)
- Military: [TLC7226M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

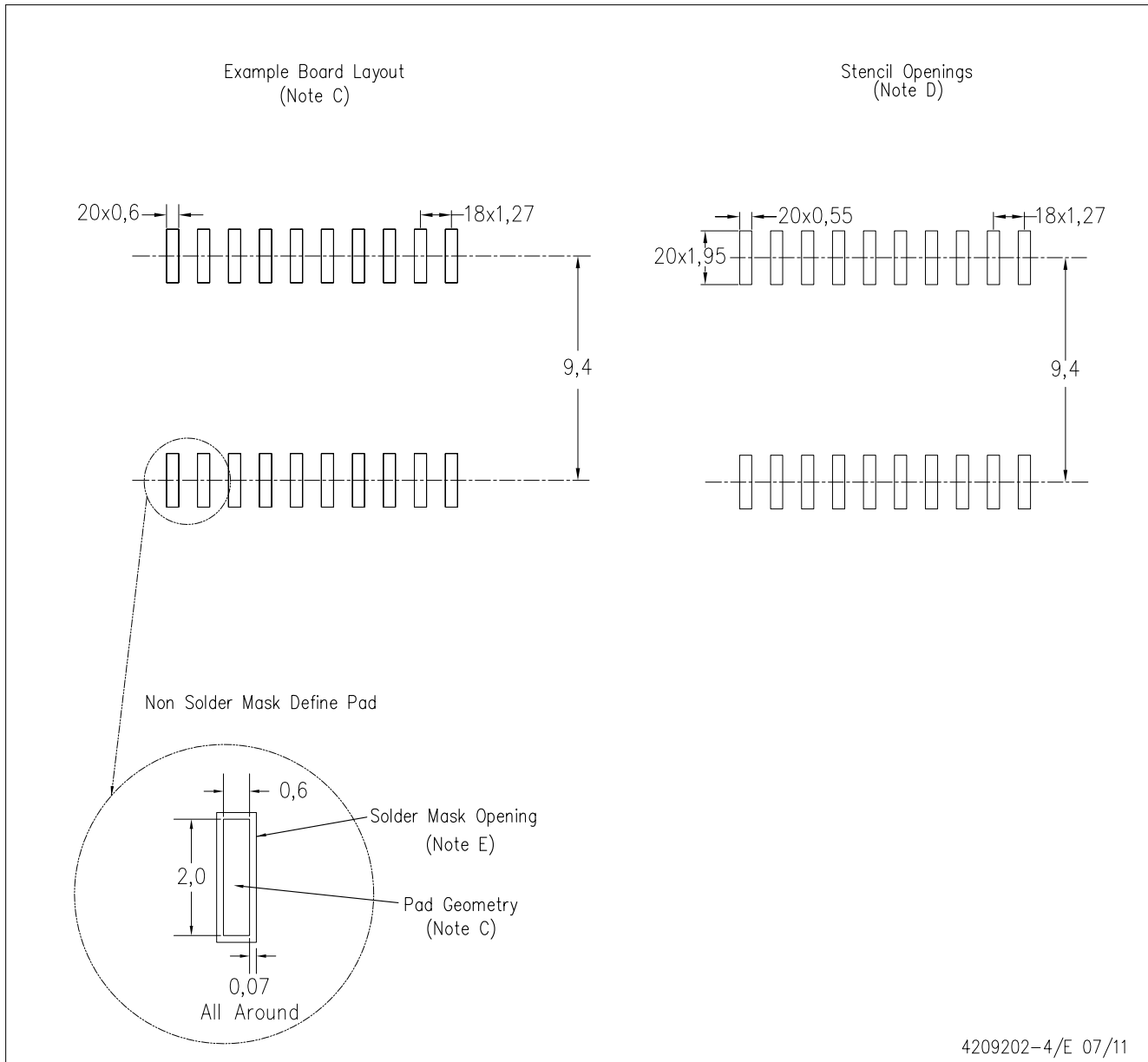
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated