TEXAS INSTRUMENTS

TLC5973

SBVS225B –MARCH 2013–REVISED MAY 2014

TLC5973 3-Channel, 12-Bit, PWM Constant-Current LED Driver with Single-Wire Interface (EasySet™)

1 Features

- Three Constant Sink Current Channels
- Current Capability:
  – 2 mA to 35 mA per Channel (VCC ≤ 4.0 V)
  – 2 mA to 50 mA per Channel (VCC > 4.0 V)
- Grayscale (GS) Control with PWM:
  – 12-Bit (4096 Steps)
- Single-Wire Interface (EasySet)
- Power-Supply (VCC) Voltage Range:
  – 3 V to 6 V
- OUT Pins Maximum Voltage: Up to 21 V
- Integrated Shunt Regulator
- Data Transfer Maximum Rate:
  – Bits per Second (bps): 3 Mbps
- Internal GS Clock Oscillator: 12 MHz (typ)
- Display Repeat Rate: 2.9 kHz (typ)
- Output Delay Switching to Prevent Inrush Current
- Unlimited Device Cascading
- Operating Temperature: –40°C to 85°C

2 Applications

This device is targeted towards one application. The primary application for this device is for RGB LED cluster lamp displays.

3 Description

The TLC5973 is an easy-to-use, 3-channel, 50-mA constant sink current LED driver. The single-wire, 3-Mbps serial interface (EasySet) provides a solution for minimizing wiring cost. The LED driver provides 12-bit pulse width modulation (PWM) resolution. The display repeat rate is achieved at 2.9 kHz (typ) with an integrated 12-MHz grayscale (GS) clock oscillator. The driver also provides unlimited cascading capability.

All output sink constant currents can be set by an external resistor. The TLC5973 has an internal shunt regulator that can be used for higher VCC power-supply voltage applications.

Device Information[1]

DEVICE NAME	PACKAGE	BODY SIZE
TLC5973	SOIC (8)	4.9 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
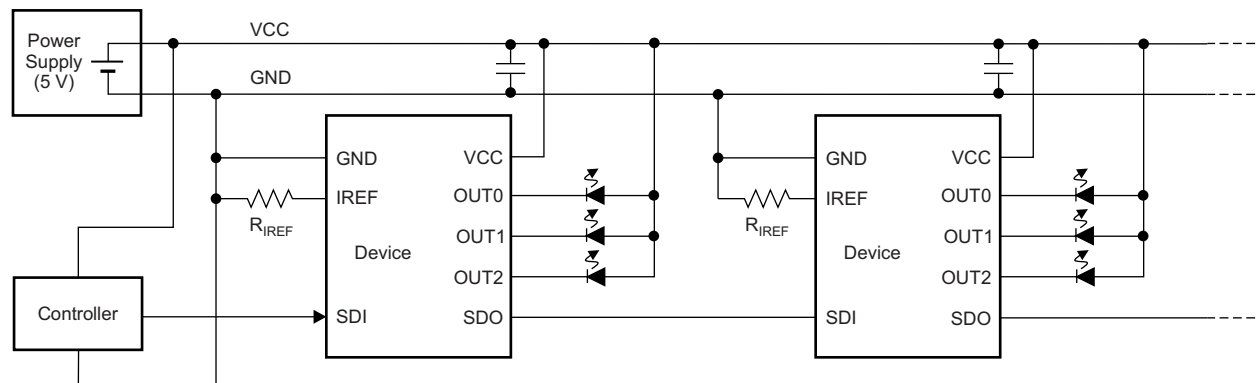
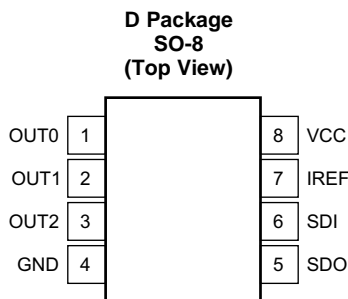**Typical Application Circuit Example**

Table of Contents

4 Revision History

Changes from Revision A (May 2013) to Revision B   **Page**

- Changed format to meet latest data sheet standards; added *Applications and Implementation*, *Power Supply Recommendations*, and *Layout* sections, moved existing sections 1
- Changed *8-bit pulse width modulation* to *12-bit pulse width modulation* in Description section 1
- Changed t_{H0} and t_{H1} parameter units from µs to ns in Recommended Operating Conditions table 4
- Changed Figure 8: deleted top SDO, changed bottom SDO to OUT*n* 7
- Changed Figure 11: deleted extraneous breaks in traces, extraneous data call-outs, and t_{H1} on GSLAT trace, changed data transfer trace note to *Internal to 1st Device* and 1st Data to 47th Data in 48-Bit Shift Register LSB trace.... 9
- Changed functional block diagram: changed Upper 8 Bits to Upper 12 Bits on 48-Bit Shift Register block 11
- Added *Grayscale (GS) Control*, *EasySet and Shunt Regulator*, and *No Limit Cascading* sections 11
- Changed *Connector Design* title 13
- Changed Figure 13: changed OUT*n* traces GSDATA = 4093 and GSDATA = 4094 15
- Changed description of the *Data '0' and Data '1' Write Sequence (Data Write Sequence)* section 16
- Changed title of *Controlling Devices Connected in Series* section 19
- Changed *Data 101* to *Data 1010* in Figure 18 19
- Changed *eight MSBs* to *12 MSBs* in third sentence of the *Register and Data Latch Configuration* section 21
- Changed Figure 21: corrected 3AAh bit set sequence 21
- Changed Figure 26: changed number of LEDs in optional dashed box 26
- Changed Table 7: changed all values in R_{VCC} column and first and last values in *Resistor Wattage* column 27

Changes from Original (March 2013) to Revision A   **Page**

- Changed second paragraph of *Grayscale (GS) Function (PWM Control)* section 13
- Changed t_{CYCLE} setting range in *Data Transfer Rate (t_{CYCLE}) Measurement Sequence* section 16
- Updated Figure 18 19
- Updated Figure 21 and Table 3 21

5 Pin Configuration and Functions

D Package
SO-8
(Top View)

```
        ┌──────────┐
OUT0  1 │          │ 8  VCC
OUT1  2 │          │ 7  IREF
OUT2  3 │          │ 6  SDI
GND   4 │          │ 5  SDO
        └──────────┘
```

Pin Functions

PIN			
NAME	NO.	I/O	DESCRIPTION
OUT0	1	O	Constant sink current driver outputs.
OUT1	2	O	Multiple outputs can be configured in parallel to increase the sink drive current capability.
OUT2	3	O	Different voltages can be applied to each output.
GND	4	—	Power ground
SDO	5	O	Serial data output
SDI	6	I	Serial data input. This pin is internally pulled down to GND with a 1-MΩ (typ) resistor.
IREF	7	I/O	Output current programming pin. A resistor connected between IREF and GND sets the current for each constant-current output. Place the external resistor close to the device.
VCC	8	—	Power-supply voltage

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Voltage[2]	Supply, V_{CC}	VCC	−0.3	7.0	V
	Input range, V_{IN}	SDI	−0.3	V_{CC} + 1.2	V
	Output range, V_{OUT}	OUT0 to OUT2	−0.3	21	V
		SDO	−0.3	7.0	V
Current	Output (dc), I_{OUT}	OUT0 to OUT2	0	60	mA
Operating junction temperature, T_J			−40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground pin.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		−55	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	−8000	8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	−2000	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
DC CHARACTERISTICS						
V_{CC}	Supply voltage	No internal shunt regulator mode	3.0	5.0	5.5	V
		Internal shunt regulator mode			6.0	V
V_O	Voltage applied to output	OUT0 to OUT2			21	V
V_{IH}	High-level input voltage	SDI	$0.7 \times V_{CC}$		V_{CC}	V
V_{IL}	Low-level input voltage	SDI	GND		$0.3 \times V_{CC}$	V
V_{IHYST}	Input voltage hysteresis	SDI		$0.2 \times V_{CC}$		V
I_{OH}	High-level output current	SDO			–2	mA
I_{OL}	Low-level output current	SDO			2	mA
		OUT0 to OUT2 (VCC ≤ 4.0 V)	2		35	mA
		OUT0 to OUT2 (VCC > 4.0 V)	2		50	mA
I_{REG}	Shunt regulator sink current	VCC			20	mA
T_A	Operating free-air temperature range		–40		85	°C
T_J	Operating junction temperature range		–40		125	°C
AC CHARACTERISTICS						
$f_{CLK (SDI)}$	Data transfer rate	SDI	100		3000	kHz
t_{SDI}	SDI input pulse duration	SDI	60		$0.5 / f_{CLK}$	ns
t_{WH}	Pulse duration, high	SDI	14			ns
t_{WL}	Pulse duration, low	SDI	14			ns
t_{H0}	Hold time: end of sequence (EOS)	SDI↑ to SDI↑	$3.5 / f_{CLK}$		$5.5 / f_{CLK}$	ns
t_{H1}	Hold time: data latch (GSLAT)	SDI↑ to SDI↑	$8 / f_{CLK}$			ns

6.4 Thermal Information

THERMAL METRIC[1]		TLC5973	UNIT
		D (SO)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	134.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	75.3	
ψ_{JT}	Junction-to-top characterization parameter	37.7	
ψ_{JB}	Junction-to-board characterization parameter	74.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1)   For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *TLC5973*

6.5 Electrical Characteristics

At T_A = –40°C to 85°C, V_{CC} = 3 V to 6.0 V, and C_{VCC} = 0.1 µF. Typical values at T_A = 25°C and V_{CC} = 5.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SDO)	I_{OH} = –2 mA		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage (SDO)	I_{OL} = 2 mA		0		0.4	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ		1.18	1.20	1.23	V
V_R	Shunt regulator output voltage (V_{CC})	I_{CC} = 1 mA, SDI = low			5.9		V
I_{CC0}	Supply current (V_{CC})	V_{CC} = 3.0 V to 5.5 V , SDI = low, all grayscale (GSn) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 27 kΩ (I_{OUTn} = 2-mA target)			3	6	mA
I_{CC1}		V_{CC} = 3.0 V to 5.5 V, SDI = low, all grayscale (GSn) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 3 kΩ (I_{OUTn} = 17-mA target)			4	7	mA
I_{CC2}		V_{CC} = 3.0 V to 5.5 V, SDI = 5 MHz, all grayscale (GSn) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 3 kΩ (I_{OUTn} = 17-mA target)			5	8	mA
I_{CC3}		V_{CC} = 3.0 V to 5.5 V, SDI = 5 MHz, all grayscale (GSn) = FFFh, V_{OUTn} = 1 V, SDO = 15 pF, R_{IREF} = 1.5 kΩ (I_{OUTn} = 34-mA target)			5.5	10	mA
I_{OLC}	Constant output current (OUT0 to OUT2)	All OUTn = on, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		31	34	37	mA
I_{OLKG}	Output leakage current (OUT0 to OUT2)	GSn = 000h, V_{OUTn} = 21 V	T_J = –40°C to 85°C			0.1	µA
			T_J = 85°C to 125°C			0.2	µA
ΔI_{OLC0}	Constant-current error (channel-to-channel)[1]	All OUTn = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5%	±3%	
ΔI_{OLC1}	Constant-current error (device-to-device)[2]	All OUTn = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5%	±6%	
ΔI_{OLC2}	Line regulation of constant-current output[3]	All OUTn = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5	±1	%/V
ΔI_{OLC3}	Load regulation of constant-current output[4]	All OUTn = on, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ			±0.5	±1	%/V
R_{PD}	Internal pull-down resistance (SDI)	At SDI			1		MΩ

(1) The deviation of each output (OUT0 to OUT2) from the constant-current average. Deviation is calculated by the formula:

$$\Delta \ (\%) = \left(\frac{I_{OUTn}}{\frac{I_{OUT0} + I_{OUT1} + I_{OUT2}}{3}} - 1 \right) \times 100$$

, where n = 0 to 2.

(2) Deviation of the constant-current average in each color group from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta \ (\%) = \left(\frac{\frac{I_{OUT0} + I_{OUT1} + I_{OUT2}}{3} - \text{Ideal Output Current}}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUTn(IDEAL)} \ (mA) = 43.4 \times \left(\frac{1.20}{R_{IREF} \ (\Omega)} \right)$$

, where n = 0 to 2.

(3) Line regulation is calculated by the formula:

$$\Delta \ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5 \text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})}{I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V}} \right) \times \frac{100}{5.5 \text{ V} - 3.0 \text{ V}}$$

, where n = 0 to 2.

(4) Load regulation is calculated by the equation:

$$\Delta \ (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3.0 \text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1.0 \text{ V})}{I_{OUTn} \text{ at } V_{OUTn} = 1.0 \text{ V}} \right) \times \frac{100}{3.0 \text{ V} - 1.0 \text{ V}}$$
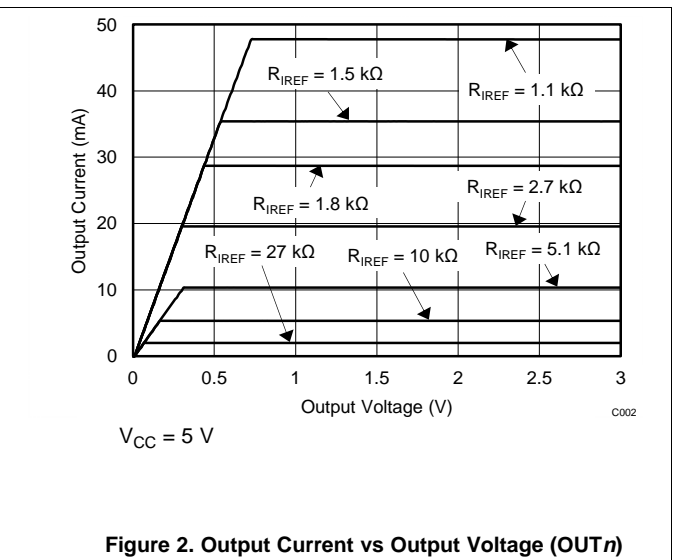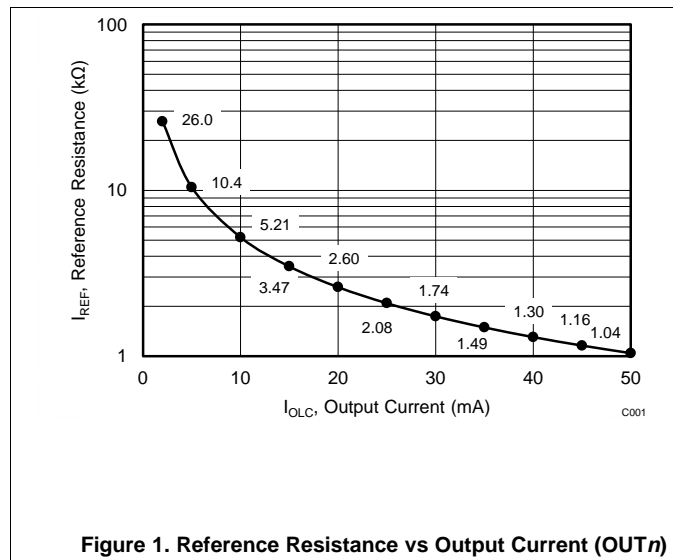
, where n = 0 to 2.

6.6 Switching Characteristics

At T_A = –40°C to 85°C, V_{CC} = 3.0 V to 5.5 V, C_L = 15 pF, R_L = 110 Ω, and V_{LED} = 5.0 V, unless otherwise noted.
Typical values are at T_A = 25°C and V_{CC} = 5.0 V.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{R0}	Rise time	SDO	2	6	12	ns
t_{R1}		OUTn (on → off)		200	400	ns
t_{F0}	Fall time	SDO	2	6	12	ns
t_{F1}		OUTn (off → on)		200	400	ns
t_{D0}	Propagation delay	SDI↑ to SDO↑		30	50	ns
t_{D1}		OUT0↓ to OUT1↓, OUT1↓to OUT2↓, OUT0↑ to OUT1↑, OUT1↑to OUT2↑		25		ns
t_{WO}	Shift data output one pulse duration	SDO↑ to SDO↓	15	25	45	ns
f_{OSC}	Internal GS oscillator frequency		8	12	16	MHz

6.7 Typical Characteristics

At T_A = 25°C and V_{CC} = 12 V, unless otherwise noted.

Figure 1. Reference Resistance vs Output Current (OUTn)

Figure 2. Output Current vs Output Voltage (OUTn)

Product Folder Links: *TLC5973*

7 Parameter Measurement Information

7.1 Pin-Equivalent Input and Output Schematic Diagrams
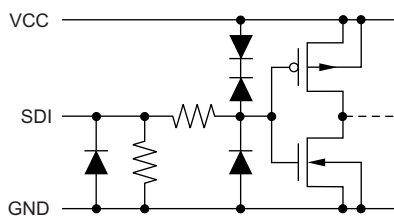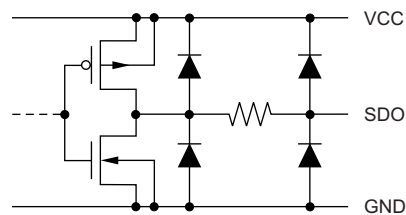

Figure 3. SDI

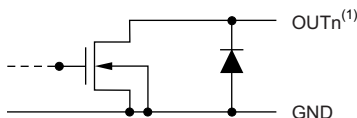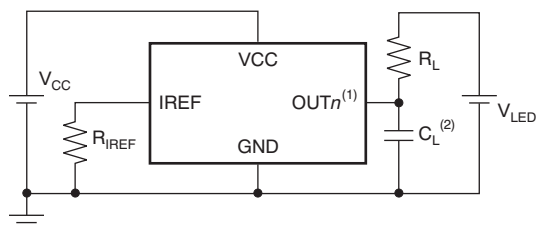**Figure 4. SDO**
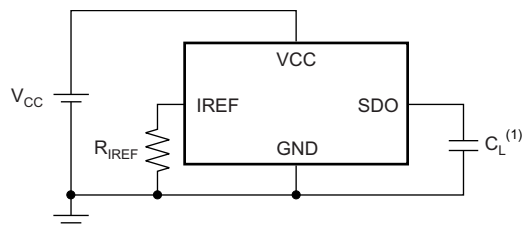

(1) n = 0 to 2.

Figure 5. OUT0 Through OUT2

7.2 Test Circuits
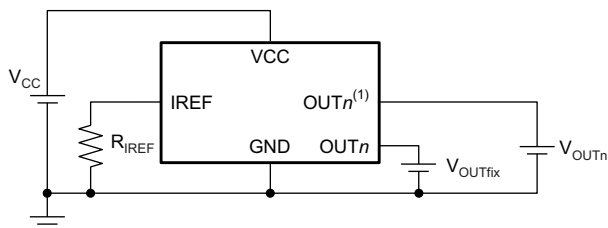

(1) n = 0 to 2.

(2) C_L includes measurement probe and jig capacitance.

**Figure 6. Rise and Fall Time Test Circuit for
OUT*n***

(1) C_L includes measurement probe and jig capacitance.
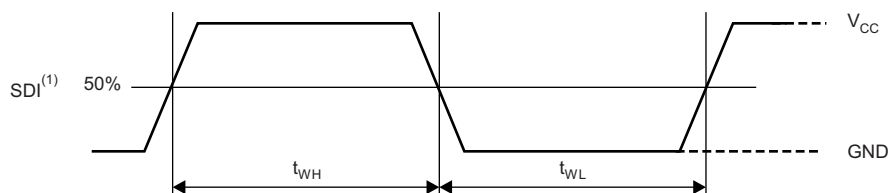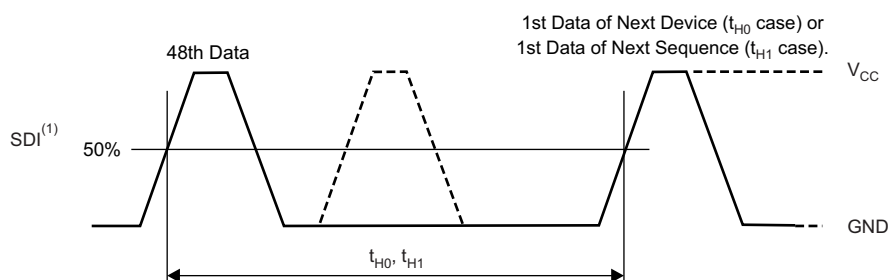
Figure 7. Rise and Fall Time Test Circuit for SDO
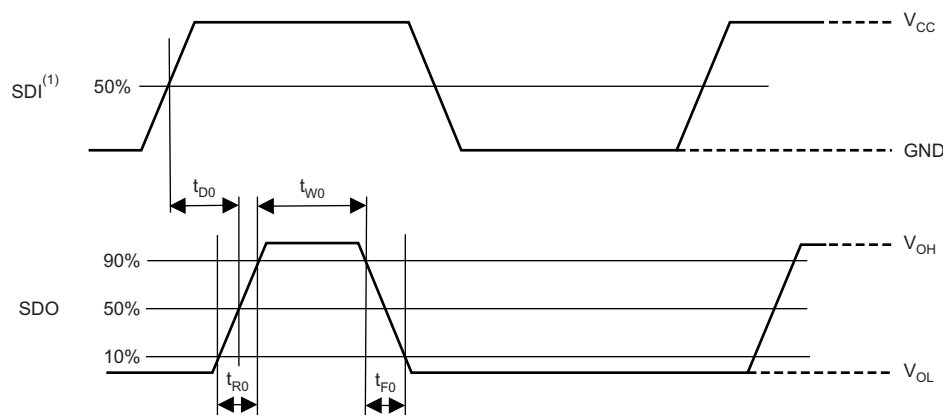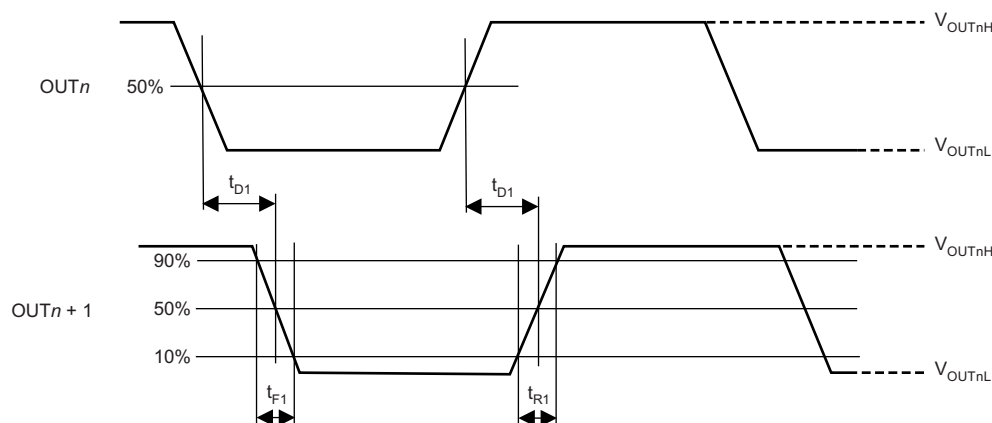

(1) n = 0 to 2.

Figure 8. Constant-Current Test Circuit for OUT*n*

Product Folder Links: *TLC5973*

7.3 Timing Diagrams

(1)   Input pulse rise and fall time is 1 ns to 3 ns.

Figure 9. Input Timing

(1)   Input pulse rise and fall time is 1 ns to 3 ns.

Figure 10. Output Timing

Timing Diagrams (continued)

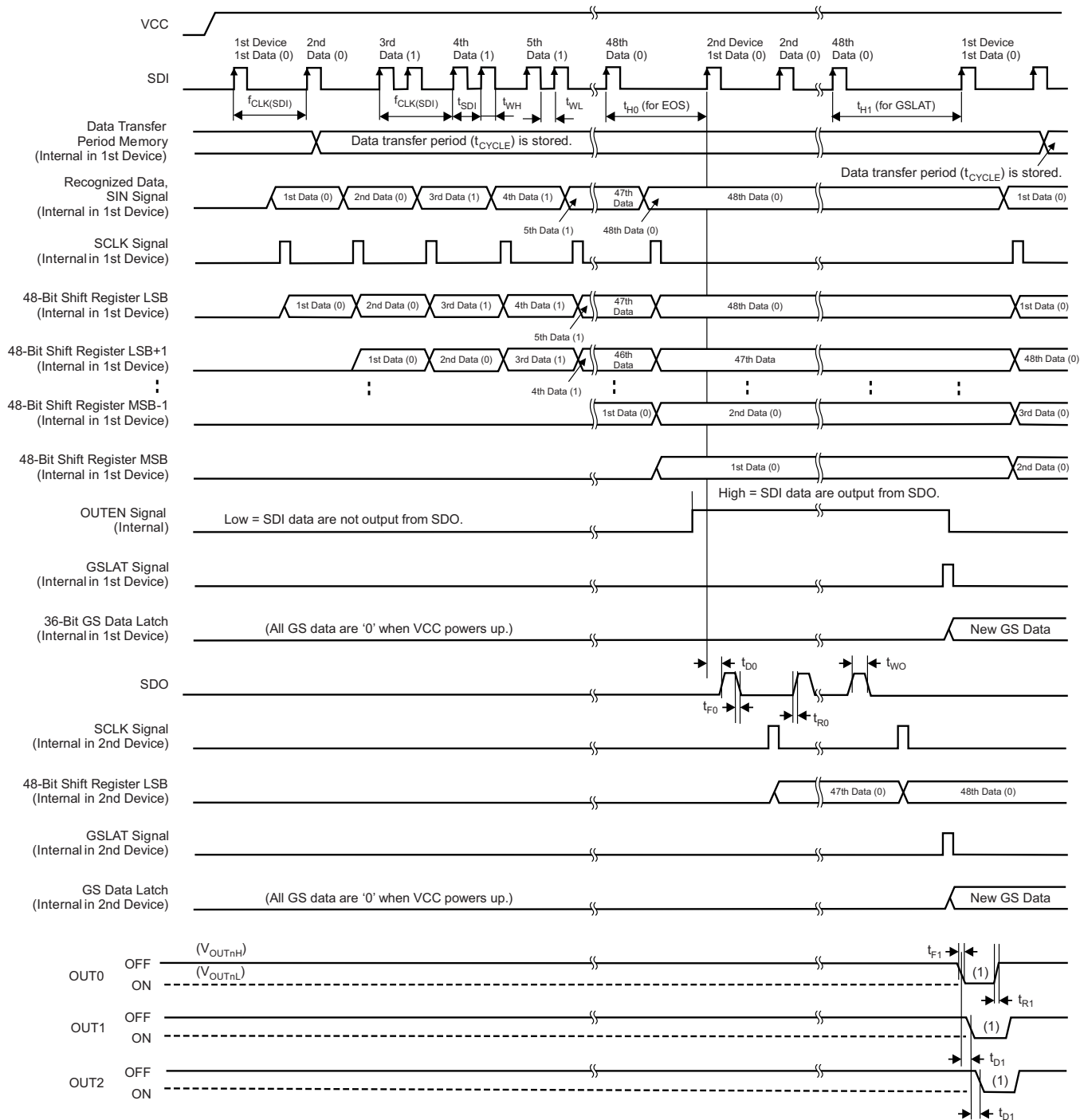(1) OUT*n* on-time changes, depending on the data in the 36-bit GS data latch.

Figure 11. Data Write and OUT*n* Switching Timing

8 Detailed Description

8.1 Overview

The TLC5973 is 3-channel, 50-mA, constant-current LED driver that can control LED on-time with pulse width modulation (PWM) in 4096 steps for grayscale (GS) control. A maximum of 68 billion colors can be generated with red, green, and blue LEDs connected to each constant-current output. Furthermore, a reference clock generator is implemented in the device, which means that the reference clock for PWM timing control is not required to be supplied from an external clock generator or controller.

The device adopts a single-wire input or output system. Therefore, communication wire cost and communication wire failure are reduced. Further wire cost reduction can be attained when supplying power to the device. One wire can be eliminated because the device power can be generated from the LED power line with the internal shunt regulator.

The device can reduce the amount of incorrect data writes because the one-write command is required to write GS data to the device. The maximum data transfer rate for the device is 3 Mbps. Therefore, GS data can be updated with a high refresh rate even if many devices are connected in series. The number of TLC5973 devices connected in series is not limited because the TLC5973 has an internal buffer that drives the output signal.

Product Folder Links: *TLC5973*

8.2 Functional Block Diagram
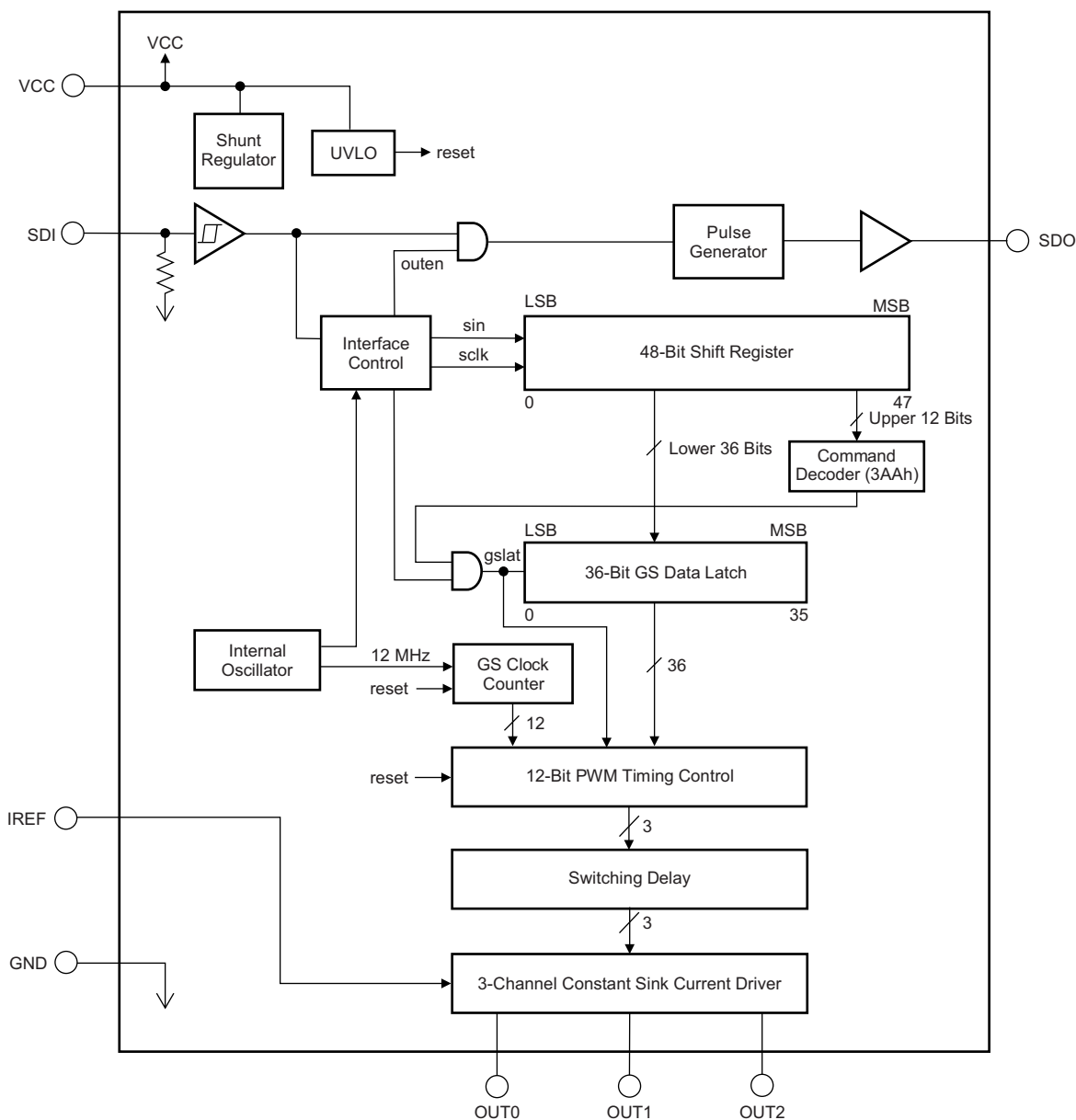
8.3 Feature Description

8.3.1 Grayscale (GS) Control

This control feature is a 12-bit (4096-step) grayscale (GS) control that provides a wide range of color generation. 68 billion colors can be generated with the red, green, and blue LEDs. Connect the LEDs to the device OUT*n* pins, as described in the *Applications and Implementation* section.

8.3.2 EasySet and Shunt Regulator

This device includes a single-wire serial interface (EasySet) and a shunt regulator. The total number of wires for power supply and data write operations can be reduced with the EasySet and shunt regulator included in the design.

Product Folder Links: *TLC5973*

Feature Description (continued)

8.3.3 No Limit Cascading

This feature results in no limitation on the number of total cascaded devices used in series in an application. This advantage is attained because a timing-adjusted pulse generator is implemented in the device.

8.3.4 Constant Sink Current Value

The output current value of each channel (I_{OLC}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by Equation 1:

$$R_{IREF} \ (k\Omega) = \frac{V_{IREF} \ (V)}{I_{OLC} \ (mA)} \times 43.4$$

where:

- V_{IREF} = the internal reference voltage on IREF (typically 1.20 V), and
- I_{OLC} = 2 mA to 50 mA   (1)

I_{OLC} is the current for each output. Each output sinks I_{OLC} current when it is turned on. R_{IREF} must be between 1 kΩ and 27 kΩ in order to hold I_{OLC} between 50 mA (typ) and 1.93 mA (typ). Otherwise, the output may be unstable. Refer to Figure 1 and Table 1 for the constant-current sink values for specific external resistor values.

**Table 1. Constant-Current Output versus
External Resistor Value**

I_{OLC} (mA)	R_{IREF} (kΩ, typ)
50	1.04
45	1.16
40	1.30
35	1.49
30	1.74
25	2.08
20	2.60
15	3.47
10	5.21
5	10.4
2	26.0

Product Folder Links: *TLC5973*

8.3.5 Connector Design

When the connector pin of the device application printed circuit board (PCB) is connected or disconnected to other PCBs, the power must be turned off to avoid device malfunction or failure. Furthermore, designing the connector GND pin to be longer than other pins (as shown in Figure 12) is preferable. This arrangement allows the GND line to either be connected first or disconnected last, which is imperative for proper device function.
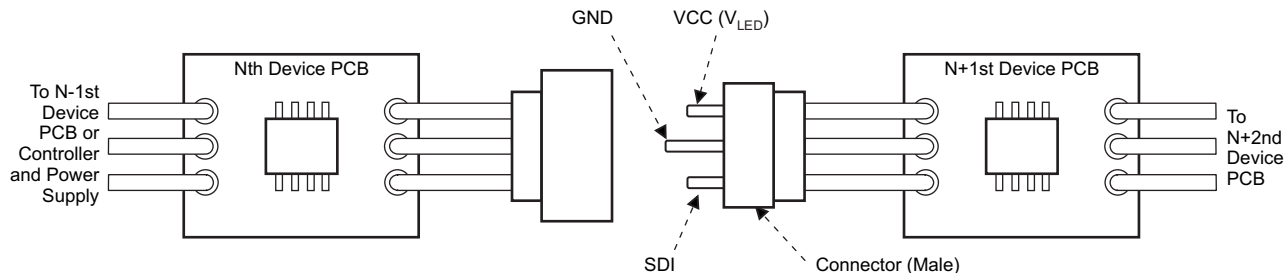

Figure 12. Connector Pin Design Application

8.4 Device Functional Modes

8.4.1 Grayscale (GS) Function (PWM Control)

The TLC5973 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The PWM data bit length for each output is 12 bits. The architecture of 12 bits per channel results in 4096 brightness steps, from 0% to 99.98% on-time duty cycle.

The PWM operation for OUTn is controlled by an 12-bit grayscale (GS) counter. The GS counter increments on each internal GS clock (GSCLK) rising edge. All OUTn are turned on when the GS counter is '1', except when OUTn are programed to GS data '0' in the 36-bit GS data latch. After turning on, each output is turns off when the GS counter value exceeds the programmed GS data for the output. The GS counter resets to 000h and all outputs are forced off when the GS data are written to the 36-bit GS data latch. Afterwards, the GS counter begins incrementing and PWM control is started from the next internal GS clock.

Product Folder Links: *TLC5973*

Device Functional Modes (continued)

Table 2 summarizes the GS data values versus the output ideal on-time duty cycle. Furthermore, actual on-time differs from the ideal on-time because the output drivers and control circuit have some timing delay. When the device is powered on, all outputs are forced off and remain off until the non-zero GS data are written to the 36-bit GS data latch.

Table 2. Output Duty Cycle and Total On-Time versus GS Data

GS DATA		NO. OF GSCLKs OUT*n* TURNS ON	NO. OF GSCLKs OUT*n* TURNS OFF	TOTAL IDEAL TIME (µs)	ON-TIME DUTY (%)
DECIMAL	HEX				
0	0	Off	Off	0	0
1	1	1	2	0.08	0.02
2	2	1	3	0.17	0.05
—	—	—	—	—	—
255	0FE	1	256	21.25	6.23
256	0FF	1	257	21.33	6.25
257	100	1	258	21.42	6.27
—	—	—	—	—	—
511	1FF	1	512	42.58	12.48
512	200	1	513	42.67	12.50
513	201	1	514	42.75	12.52
—	—	—	—	—	—
1023	3FF	1	1024	85.25	24.98
1024	400	1	1025	85.33	25.00
1025	401	1	1026	85.42	25.00
—	—	—	—	—	—
2047	7FF	1	2048	170.6	49.98
2048	800	1	2049	170.7	50.00
2049	801	1	2050	170.8	50.02
—	—	—	—	—	—
4093	FFD	1	4094	341.1	99.93
4094	FFE	1	4095	341.2	99.95
4095	FFF	1	4096	341.3	99.98

8.4.1.1 PWM Control

The GS counter keeps track of the number of grayscale reference clocks (GSCLKs) from the internal oscillator. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off when the GS counter is greater than the GS value in the 36-bit GS data latch. Figure 13 illustrates the PWM operation timing.
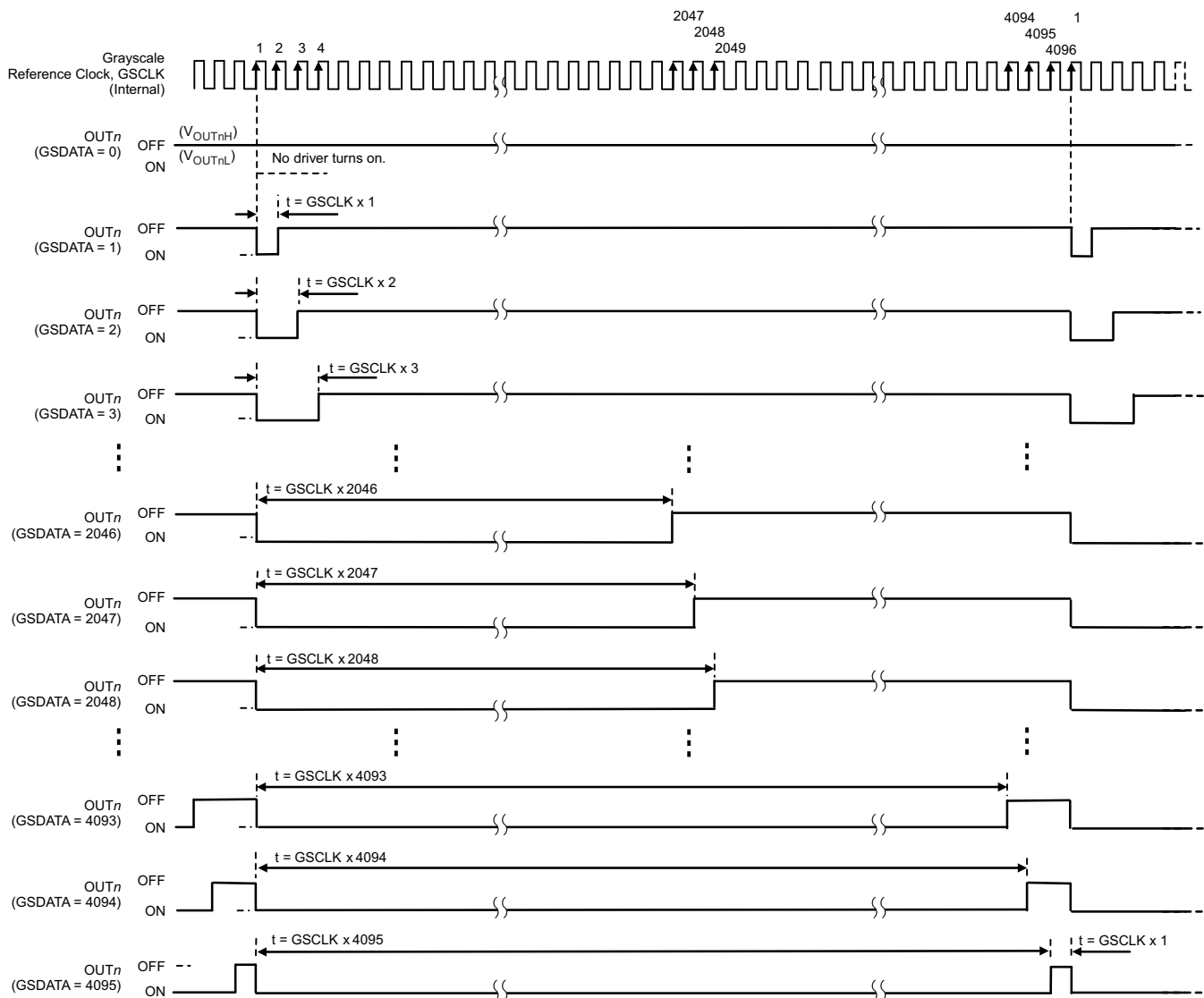
(1) Actual on-time differs from the ideal on-time.

Figure 13. PWM Operation

8.4.2 One-Wire Interface (EasySet) Data Writing Method

There are four sequences to write GS data into the TLC5973 via a single-wire interface. This section discusses each sequence in detail.

8.4.2.1 Data Transfer Rate (t_{CYCLE}) Measurement Sequence

The TLC5973 measures the time between the first and second SDI rising edges either after the device is powered up or when the GS data latch sequence is executed (as described in the *GS Data Latch Sequence (GSLAT)* section) and the time is internally stored as t_{CYCLE}. t_{CYCLE} serves as a base time used to recognize one complete data write operation, a 48-bit data write operation, and a GS data write operation to the GS data latch. t_{CYCLE} can be set between 0.33 µs and 10 µs ($f_{CLK(SDI)}$ = 100 kHz to 3000 kHz). In this sequence, two instances of data '0' are written to the LSB side of the 48-bit shift register. Figure 14 shows the t_{CYCLE} measurement timing.
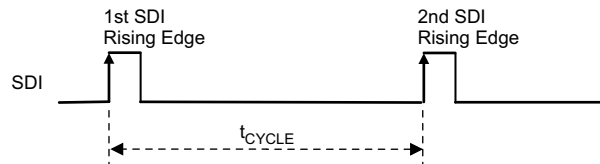

Figure 14. Data Transfer Rate (t_{CYCLE}) Measurement

8.4.2.2 Data '0' and Data '1' Write Sequence (Data Write Sequence)

When the second SDI rising edge is not input before 0.9 × t_{CYCLE} elapses from the first SDI rising edge input, the data are recognized as '0'. When the second SDI rising edge is input before 50% of t_{CYCLE} elapses from the first SDI rising edge input, the data are recognized as '1'. This write sequence must be repeated 46 times after the t_{CYCLE} measurement sequence in order to send the write command to the higher 10-bit (3AAh) and 36-bit GS data. Figure 15 shows the data '0' and '1' write timing.
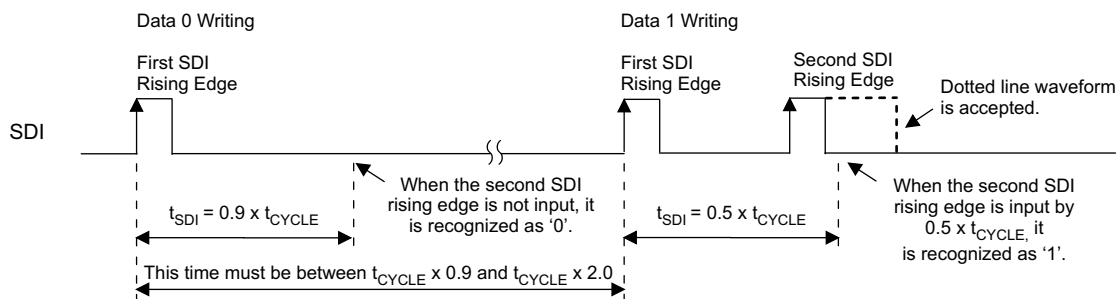

Figure 15. Data '0' and '1' Write Operation

Product Folder Links: *TLC5973*

8.4.2.3 *One Communication Cycle End of Sequence (EOS)*

One communication cycle end of sequence (EOS) must be input after the 48-bit data are written because the TLC5973 does not count the number of input data. When SDI is held low for the EOS hold time (t_{H0}), the 48-bit shift register values are locked and a buffered SDI signal is output from SDO to transfer GS data to the next device. Figure 16 shows the EOS timing.
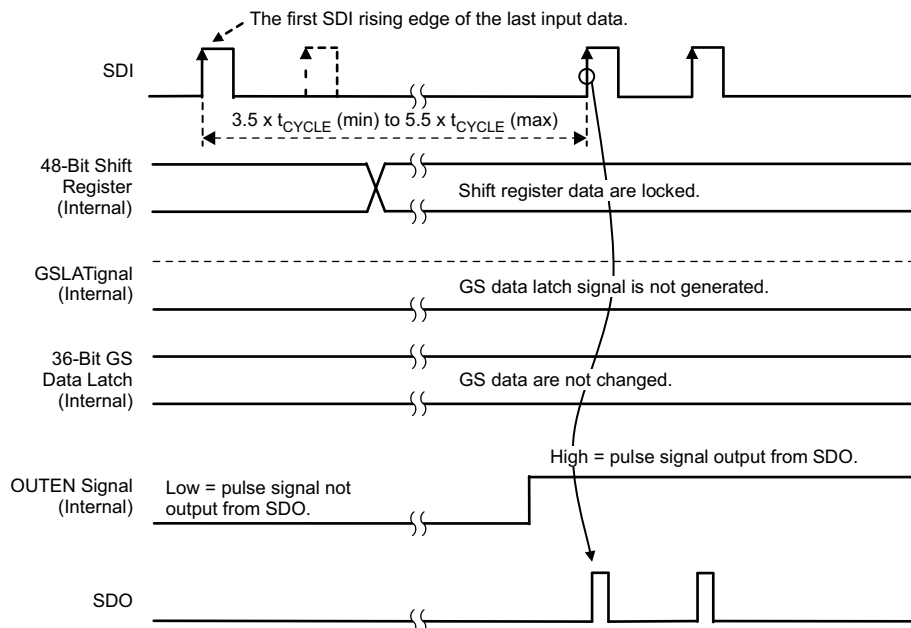

Figure 16. End of Sequence (EOS)

Product Folder Links: *TLC5973*

8.4.2.4 GS Data Latch (GSLAT) Sequence

A GS data latch (GSLAT) sequence must be input after the 48-bit data for all cascaded devices are written. When SDI is held low for the data latch hold time (t_{H1}), the 48-bit shift register data in all devices are copied to the GS data latch in each device. Furthermore, PWM control starts with the new GS data at the same time. Figure 17 shows the GSLAT timing.
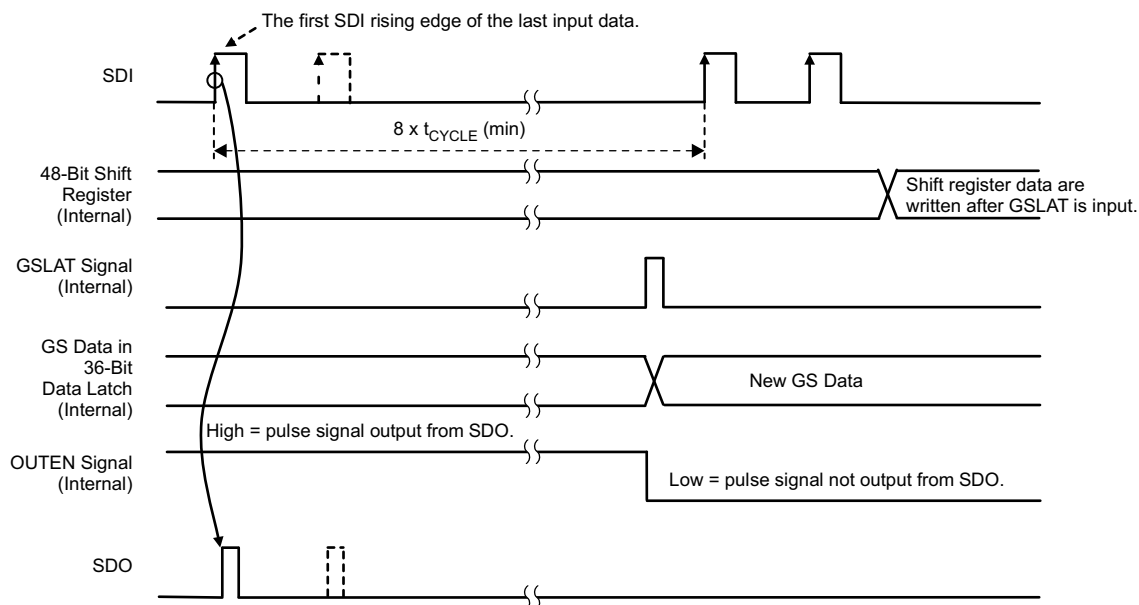

Figure 17. GS Data Latch Sequence (GSLAT)

Product Folder Links: *TLC5973*

8.5 Programming

8.5.1 Controlling Devices Connected in Series

The 12-bit write command and 36-bit grayscale (GS) data for OUT0 to OUT2 (for a total of 48 bits of data) must be written to the device. Figure 18 shows the 48-bit data packet configuration. When multiple devices are cascaded (as shown in Figure 19), N times the packet must be written into each TLC5973 in order to control all devices. There is no limit on how many devices can be cascaded, as long as proper VCC voltage is supplied. The packet for all devices must be written again whenever any GS data changes.
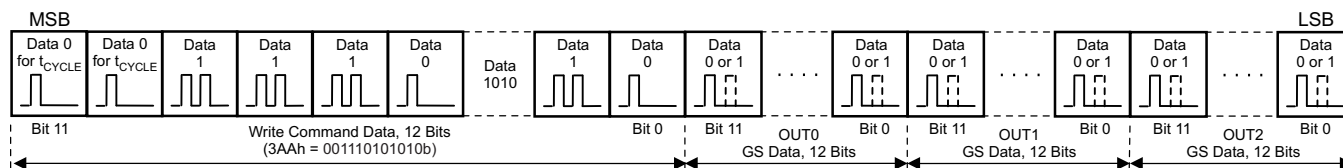

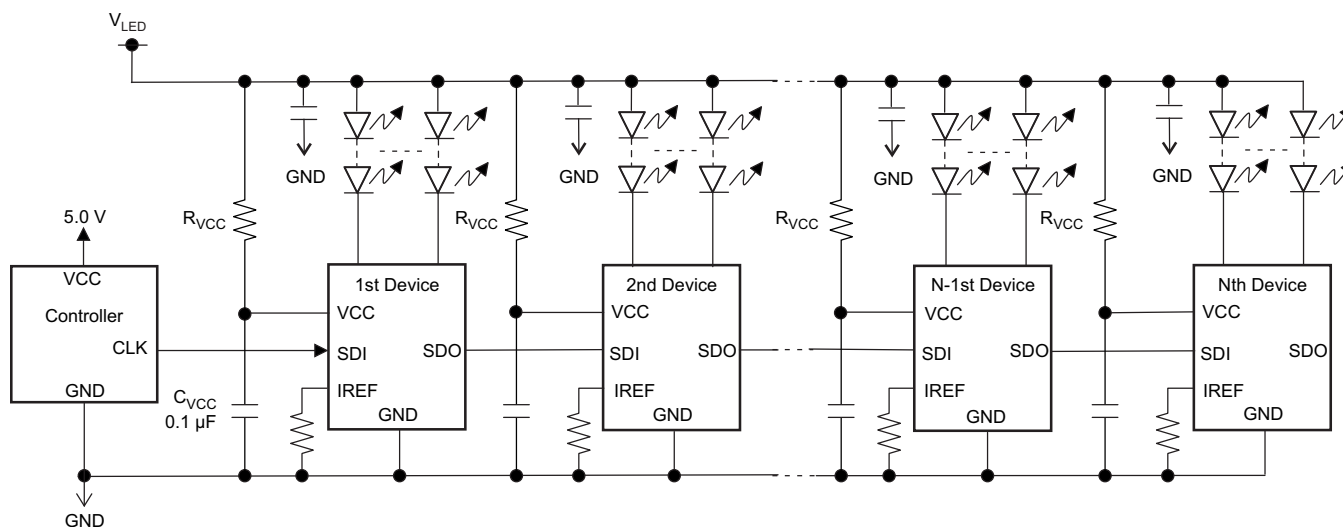**Figure 18. 48-Bit Data Packet Configuration for One TLC5973**

Figure 19. Cascade Connection of *N* TLC5973 Units (Internal Shunt Regulator Mode)

Programming (continued)

The function setting write procedure and display control is:

1. Power-up VCC (V_{LED}); all OUTn are off because GS data are not written yet.

2. Write the 48-bit data packet (MSB-first) for the first device using t_{CYCLE} and the data write sequences illustrated in Figure 14 and Figure 15. The first 12 bits of the 48-bit data packet are used as the write command. The write command must be 3AAh (001110101010b); otherwise, the 36-bit GS data in the 48-bit shift register are not copied to the 36-bit GS data latch.

3. Execute one communication cycle EOS (refer to Figure 16) for the first device.

4. Write the 48-bit data packet for the second TLC5973 as described step 2. However, t_{CYCLE} should be set to the same timing as the first device.

5. Execute one communication cycle EOS for the second device.

6. Repeat steps 4 and 5 until all devices have GS data.

7. The number of total bits is 48 × *N*. After all data are written, execute a GSLAT sequence as described in Figure 17 in order to copy the 36-bit LSBs in the 48-bit shift resister to the 36-bit GS data latch in each device; PWM control starts with the written GS data at the same time.
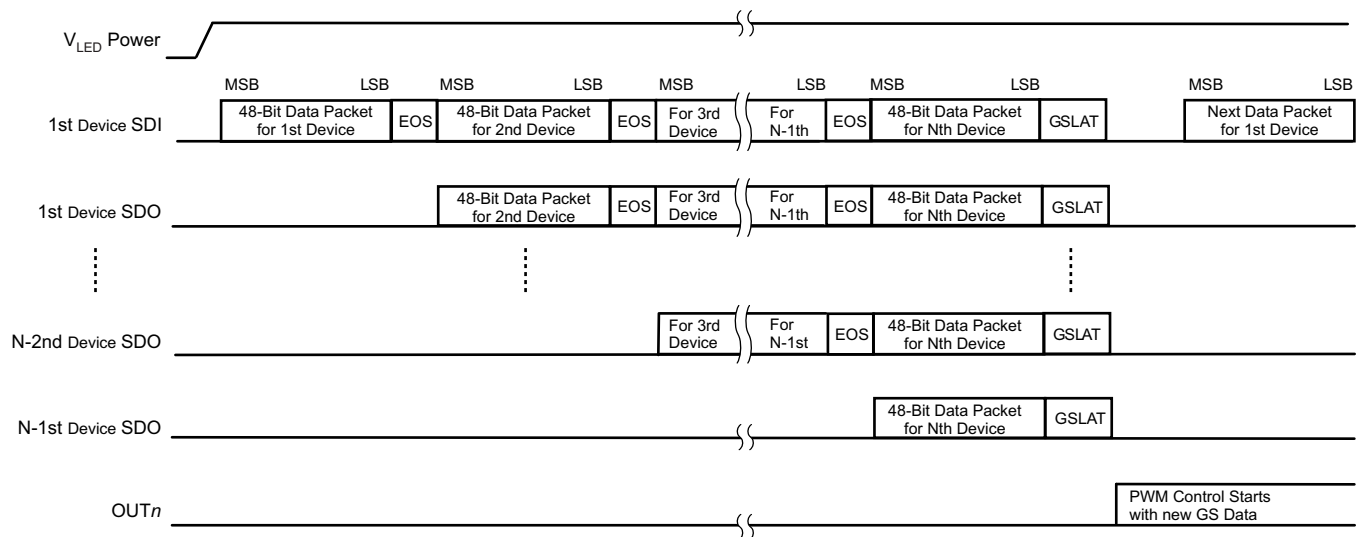

Figure 20. Data Packet Input Order for *N* TLC5973 Units

Product Folder Links: *TLC5973*

8.6 Register Maps

8.6.1 Register and Data Latch Configuration

The TLC5973 has a 48-bit shift register and a 36-bit data latch that stores GS data. When the internal GS data latch pulse is generated and the data of the 12 MSBs in the shift register are 3AAh, the lower 36-bit data in the 48-bit shift register are copied into the 36-bit GS data latch. If the data of the 12 MSBs is not 3AAh, the 36-bit data are not copied into the 36-bit GS data latch. Figure 21 shows the shift register and GS data latch configurations. Table 3 shows the 48-bit shift register bit assignment.
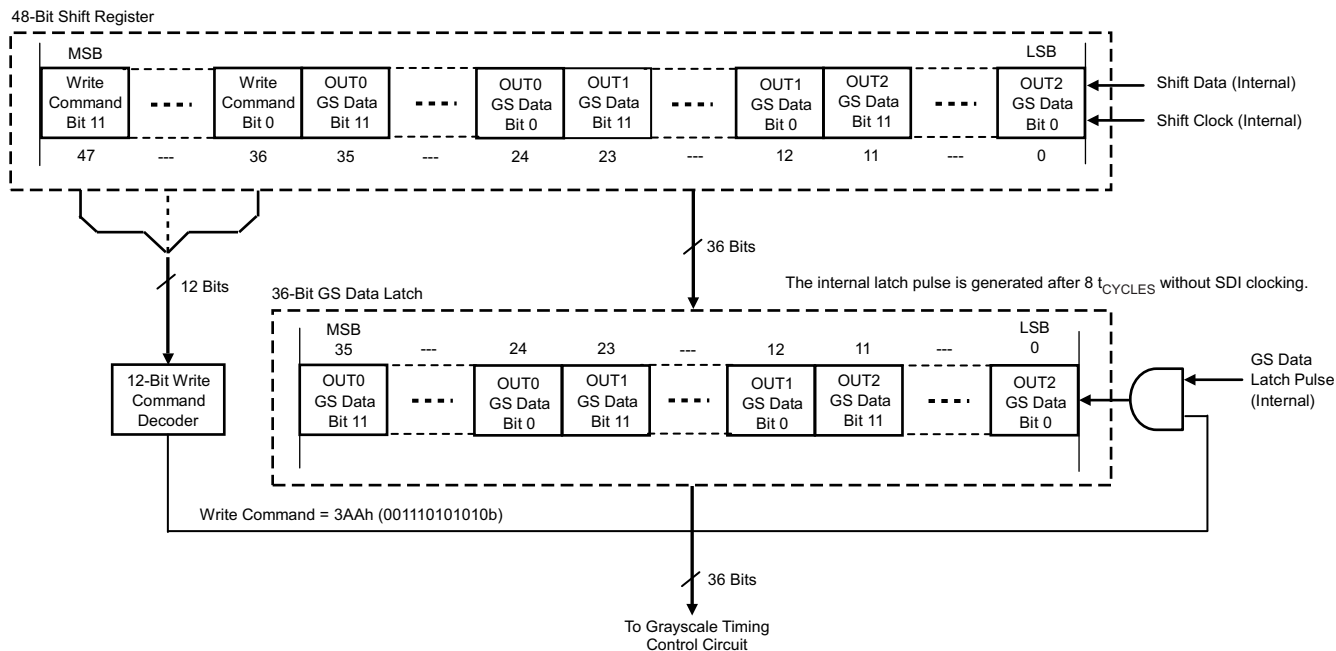
Figure 21. Common Shift Register and Control Data Latches Configuration

Table 3. 48-Bit Shift Register Data Bit Assignment

BITS	BIT NAME	CONTROLLED CHANNEL/FUNCTIONS
0 to 11	GSOUT2	GS data bits 0 to 11 for OUT2
12 to 23	GSOUT1	GS data bits 0 to 11 for OUT1
24 to 35	GSOUT0	GS data bits 0 to 11 for OUT0
36 to 47	WRTCMD	Data write command (3AAh) for GS data. The lower 36-bit GS data in the 48-bit shift register are copied to the GS data latch when the internal GS latch is generated (when these data bits are 3AAh, *001110101010b*).

9 Applications and Implementation

9.1 Application Information

The device is a constant sink current LED driver. This device is typically used to minimize wiring cost in applications and also provides no restrictions of cascading multiple devices in series. Furthermore, the device maximum data transfer rate is 3 Mbps and can contribute high-frequency display data change rates. The following design procedures can be used to maximize application design with minimal wiring cost. The device is also a good choice for higher VCC power-supply voltage applications because of the internal shunt regulator included in the device.

9.2 Typical Applications

9.2.1 No Internal Shunt Regulator Mode 1

This application does not use the shunt regulator. However, the device VCC and LED lamp anode voltage can be supplied from the same power supply because only one LED lamp is connected in series.

Figure 22. No Internal Shunt Regulator Mode 1 Typical Application Circuit

9.2.1.1 Design Requirements

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range for VCC	3.0 V or LED forward voltage (V_F) + 1 V to 5.5 V
SDI voltage range	Low level = GND, high level = VCC
SDI data transfer rate	100 kbps to 3 Mbps

9.2.1.2 Detailed Design Procedure

The OUTn (n = 0 to 2) constant output current is set by an external resistor connected between the device IREF and GND pins. Use Equation 1 to calculate the requirements for R_{IREF}.

9.2.1.3 Application Curve

One LED is connected to each output.
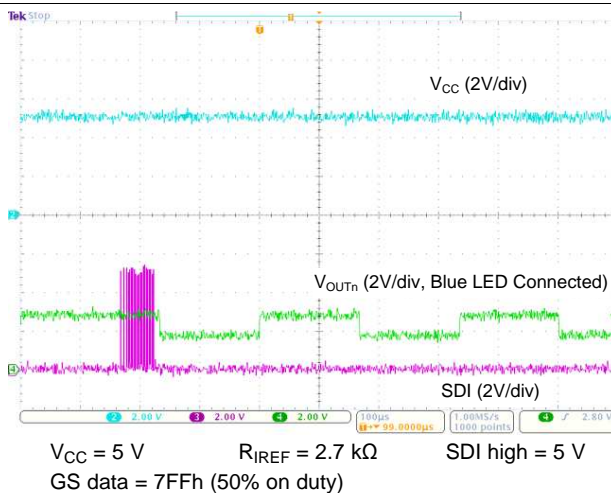
Figure 23. No Internal Shunt Regulator Mode 1 Waveform

9.2.2 No Internal Shunt Regulator Mode 2

This application does not use the shunt regulator. However, the device VCC and LED lamp anode voltage are supplied from different power supplies.
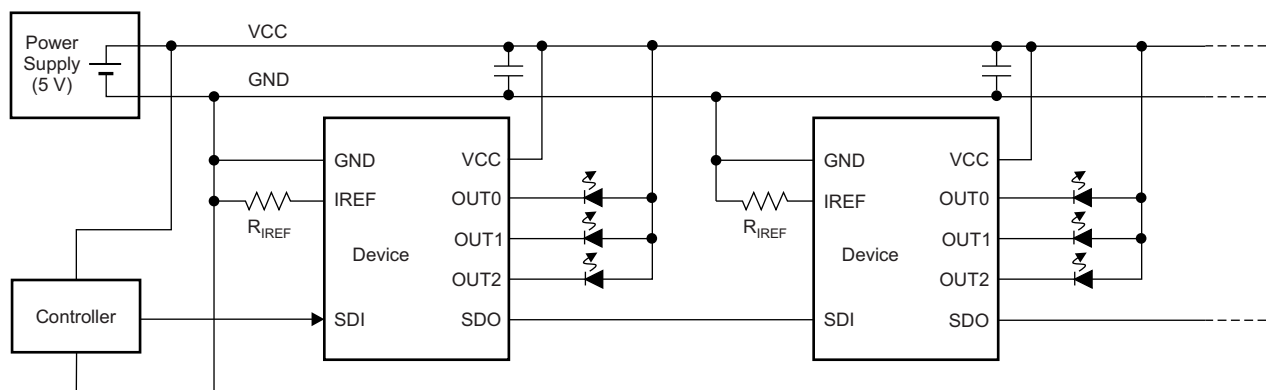
Figure 24. No Internal Shunt Regulator Mode 2 Typical Application Circuit

9.2.2.1 Design Requirements

Table 5. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range for VCC	3.0 V to 5.5 V
Input voltage range for LED lamp	LED forward voltage (V_F) × the number of LED lamps + 1 V; maximum voltage is 24 V
SDI voltage range	Low level = GND, high level = VCC
SDI data frequency	100 kbps to 3 Mbps

9.2.2.2 Detailed Design Procedure

The OUT*n* (n = 0 to 2) constant output current is set by an external resistor connected between the device IREF and GND pins. Use Equation 1 to calculate the requirements for R_{IREF}.

9.2.2.3 Application Curve

Six LEDs are connected in series to each output.

V_{CC} = 3.3 V V_{LED} = 21 V R_{IREF} = 2.7 kΩ
SDI high = 3.3 V   GS data = 7FFh (50% on duty)

Figure 25. No Internal Shunt Regulator Mode 2 Waveform

9.2.3 Internal Shunt Regulator Mode

This application uses the shunt regulator. The device VCC and LED lamp anode voltage are supplied from the same power supply. At least two LED lamps are connected in series.
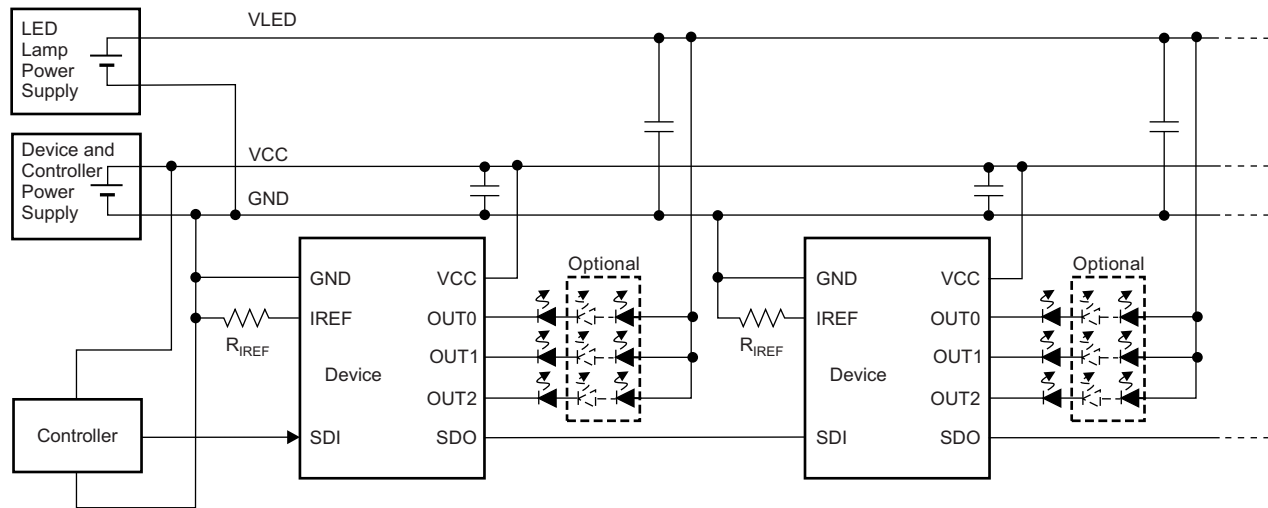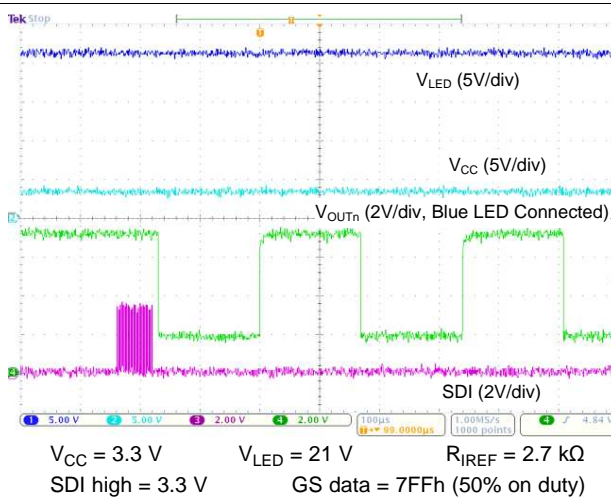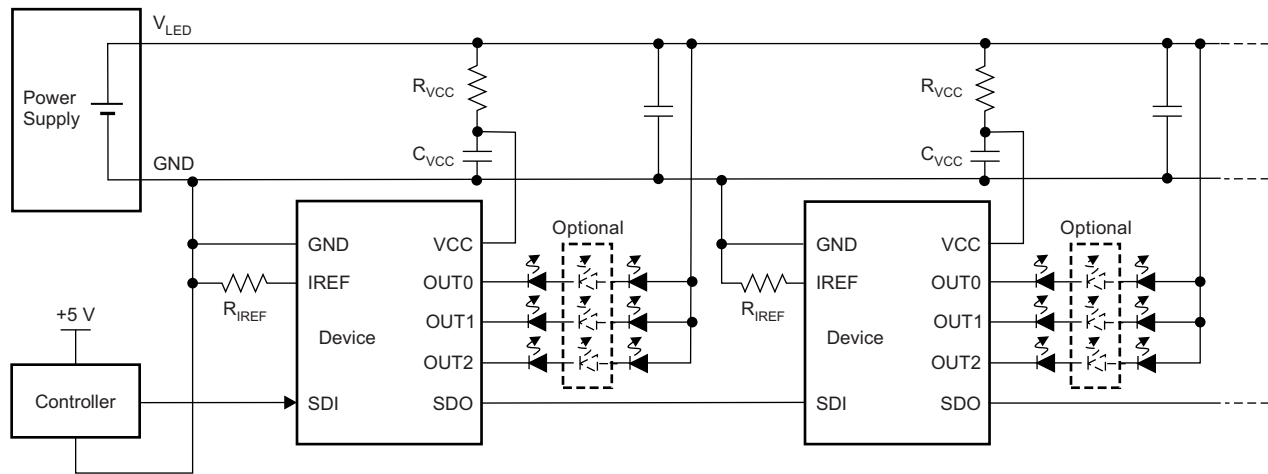

Figure 26. Internal Shunt Regulator Mode Typical Application Circuit

9.2.3.1 Design Requirements

Table 6. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range for V_{LED}	6 V to 24 V
SDI voltage range	Low level = GND, high level = 5.0 V to 6.0 V
SDI data transfer rate	100 kbps to 3 Mbps

9.2.3.2 Detailed Design Procedure

The TLC5973 internally integrates a shunt regulator to regulate V_{CC} voltage. Refer to Figure 27 for an application circuit that uses the internal shunt regulator through a resistor, R_{VCC}. The recommended R_{VCC} value can be calculated by Equation 2.

$$\frac{V_{LED} \ (V) - 5.9 \ V}{13 \ mA} < R_{VCC} < \frac{V_{LED} \ (V) - 5.9 \ V}{11 \ mA}$$

(2)
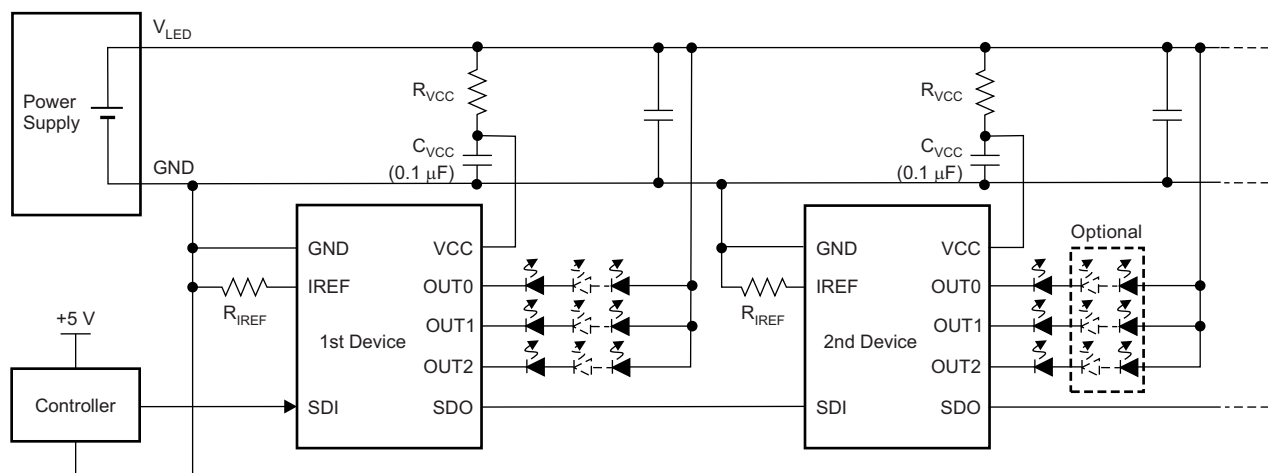
Figure 27. Internal Shunt Regulator Mode Application Circuit

Product Folder Links: *TLC5973*

Table 7 shows the typical resistor value for several V$_{LED}$ voltages. Note that the C$_{VCC}$ value should be 0.1 µF.

Table 7. Resistor Example for Shunt Resistor versus LED Voltage[1]

V$_{LED}$ (V)	R$_{VCC}$ (Ω)	RESISTOR WATTAGE (W)
9	270	0.04
12	510	0.07
18	1000	0.15
24	1500	0.22

(1)   R$_{IREF}$ is at 1.5 kΩ.

9.2.3.3 Application Curves

Six LEDs are connected in series to each output.

V$_{LED}$ = 21 V   R$_{IREF}$ = 2.7 kΩ   R$_{VCC}$ = 1.2 kΩ
SDI high = 6 V   GS data = 7FFh (50% on duty)

Figure 28. Internal Shunt Regulator Mode Waveform 1

V$_{LED}$ = 21 V   R$_{IREF}$ = 2.7 kΩ   R$_{VCC}$ = 1.2 kΩ
SDI high = 6 V   GS data = 7FFh (50% on duty)

Figure 29. Internal Shunt Regulator Mode Waveform 2
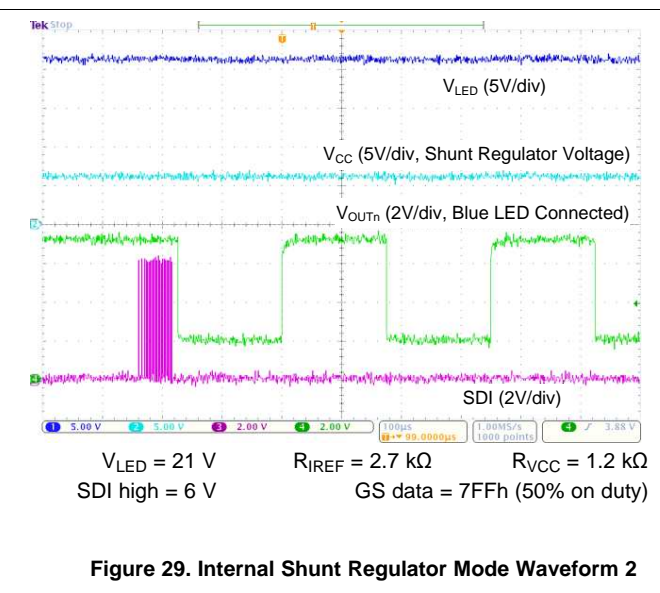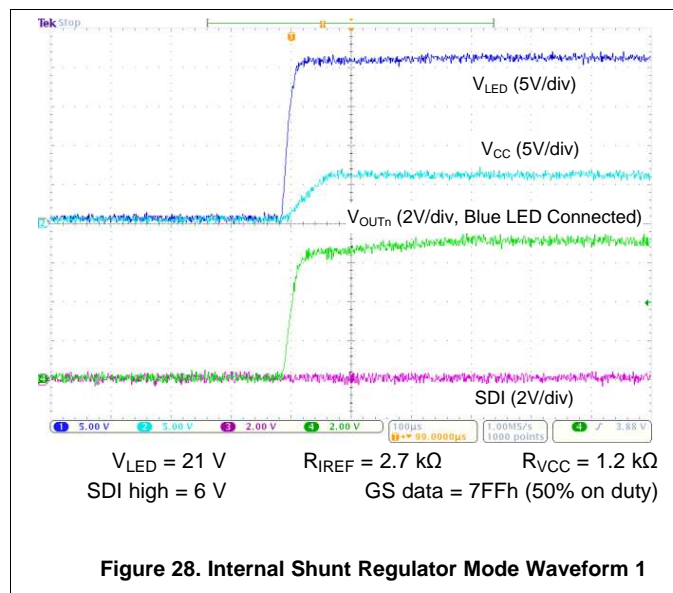
10   Power Supply Recommendations

The power supply voltage should be well regulated. An electrolytic capacitor must be used to reduce the voltage ripple to less than 5% of the input voltage.

11   Layout

11.1   Layout Guidelines

• The resistor used for the output current setting should be placed near the IREF and GND pins of the device.
• The decoupling capacitor and the shunt regulator resistor should be placed near the VCC pin of the device.

11.2   Layout Example
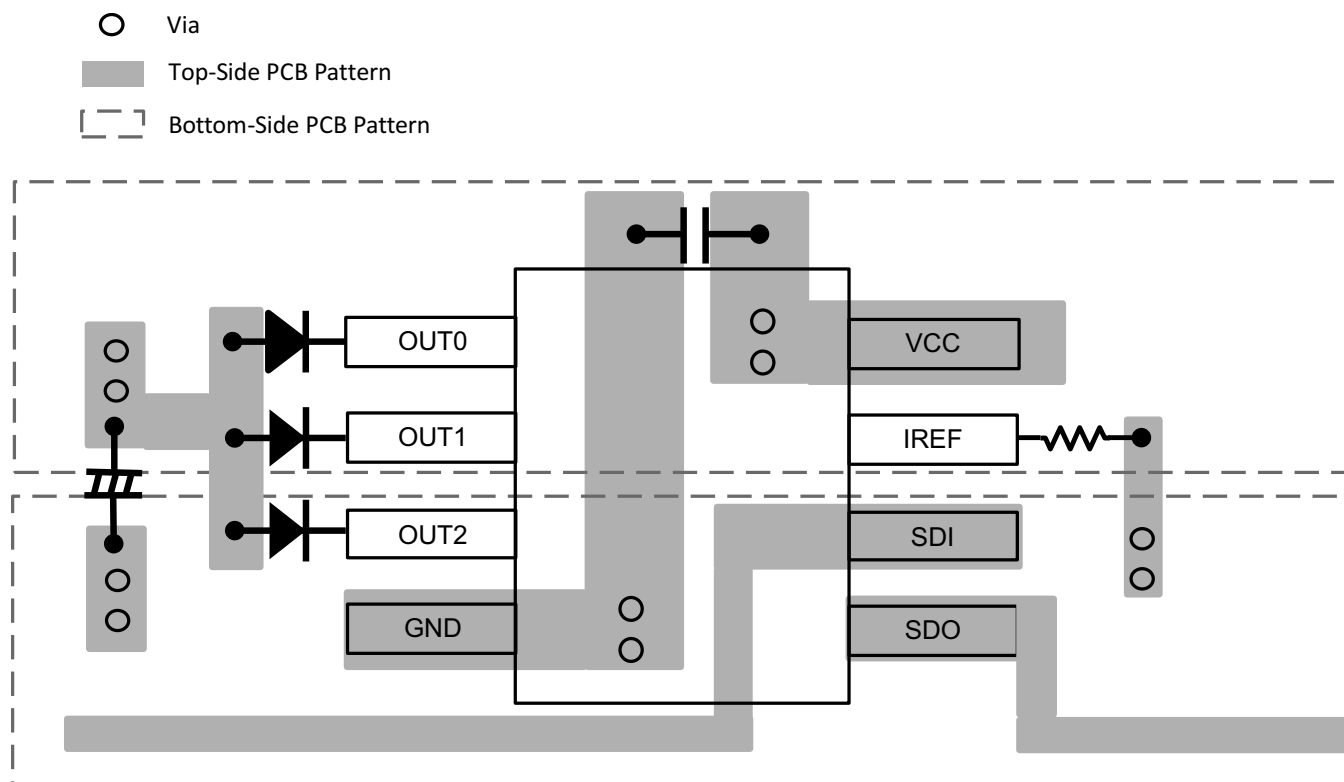
Figure 30. Layout Example

Product Folder Links: *TLC5973*

12 Device and Documentation Support

12.1 Trademarks

EasySet is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5973D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5973	Samples
TLC5973DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	5973	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80)
⟨C⟩

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00) ⟨D⟩
0.150 (3,80)

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         ⟨C⟩ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         ⟨D⟩ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AA.

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D (R−PDSO−G8)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

6x1,27

8x0,55

6x1,27

8x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0,07

All Around

4211283−2/E 08/12

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		