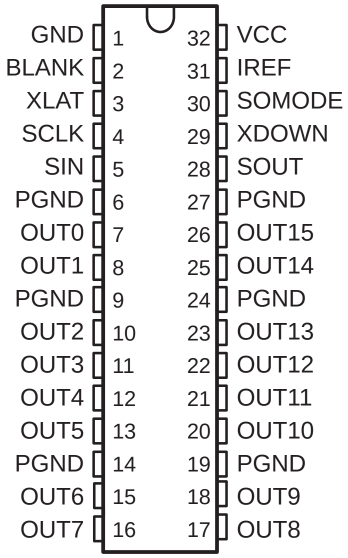
- **Drive Capability and Output Counts**
  - **80 mA (Current Sink) x 16 Bits**
- **Constant Current Output Range**
  - **1 to 80 mA (Current Value Setting for All Output Terminals Using External Resistor)**
- **Constant Current Accuracy**
  - **±1% (Typ)**
  - **±4% (Max) (Maximum Error Between Bits, All Bits On)**
- **Voltage Applied to Constant Current Output Terminal**
  - **Minimum 0.6 V (Output Current 40 mA)**
  - **Minimum 1 V (Output Current 80 mA)**
- **Data Input**
  - **Clock Synchronized 1 Bit Serial Input**
- **Data Output**
  - **Clock Synchronized 1 bit Serial Output (With Timing Selection)**
- **Input/Output Signal Level . . . CMOS Level**
- **Power Supply Voltage . . . 4.5 V to 5.5V**
- **Maximum Output Voltage . . . 17 V (Max)**
- **Data Transfer Rate . . . 20 MHz (Max)**
- **Operating Free-Air Temperature Range –20°C to 85°C**
- **Available in 32 Pin HTSSOP DAP Package (P_D=3.9 W, T_A = 25°C)**
- **LOD Function . . . LED Open Detection (Error Signal Output at LED Disconnection)**
- **TSD Function . . . Thermal Shutdown (Turn Output Off When Junction Temperature Exceeds Limit)**

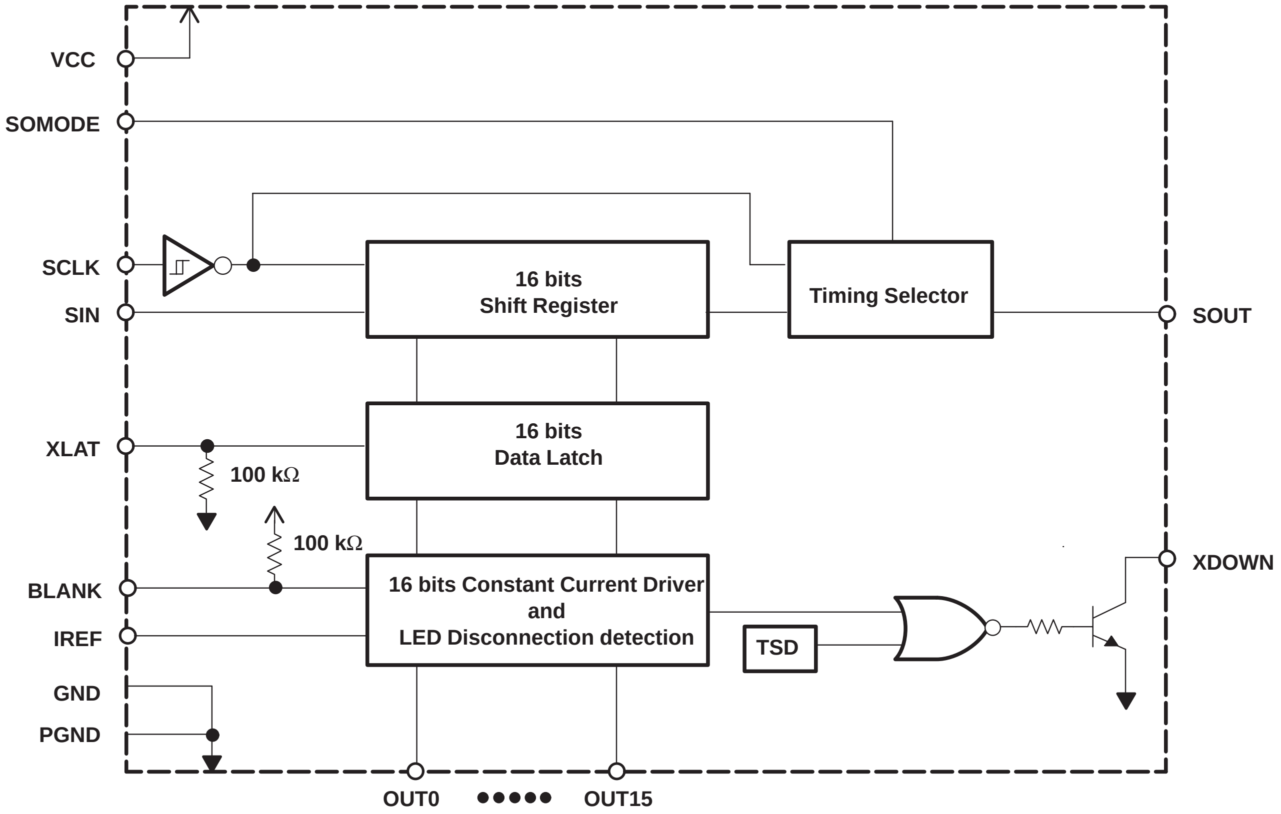
DAP PACKAGE
(TOP VIEW)



description

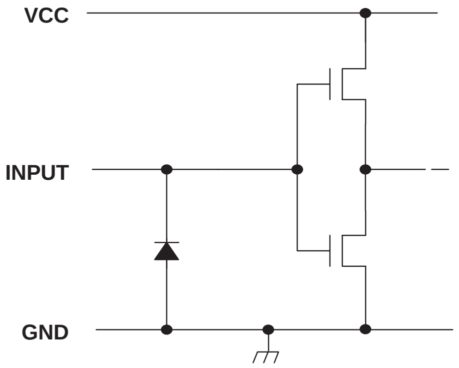
The TLC5921 is a current-sink constant current driver incorporating shift register and data latch. The current value at constant current output can be set by one external register. The device also incorporates thermal shutdown (TSD) circuitry which turns constant current output off when the junction temperature exceeds the limit, and LED open detection (LOD) circuitry to report the LED was disconnected.

functional block diagram

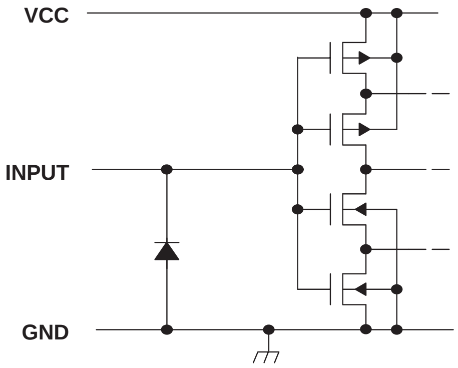


equivalent input and output schematic diagrams

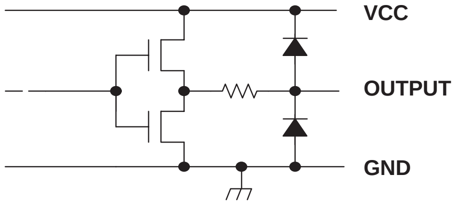
Input (except SCLK)



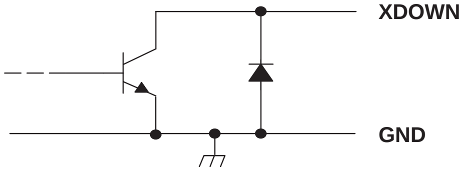
Input (SCLK)



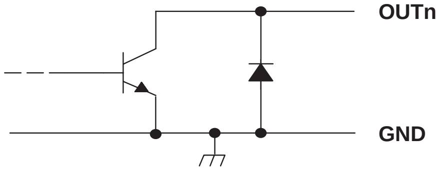
SOUT



XDOWN



OUTn



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
SIN	5	I	1 bit serial data input
SOUT	28	O	1 bit serial data output
SCLK	4	I	Clock input for data transfer. All the data in the shift register is shifted to MSB by 1 bit synchronizing to the rising edge of SCLK, and data at SIN is shifted to LSB at the same time. (Schmitt buffer input)
XLAT	3	I	Latch. When XLAT is high, data on shift register goes through latch. When XLAT is low, data is latched. Accordingly, if data on shift register is changed during XLAT high, this new value is latched (level latch). This terminal is internally pulled down with 100kΩ.
SOMODE	30	I	Timing select for serial data output. When SOMODE is low, output data on SOUT is changed synchronizing to the rising edge of SCLK. When SOMODE is high, output data on SOUT is changed synchronizing to the falling edge of SCLK.
OUT0 – OUT15	7,8,10,11,12,13, 15,16,17,18,20, 21,22,23,25,26	O	Constant current output.
BLANK	2	I	Blank(Light off). When BLANK is high, all the output of constant current driver is turned off. When BLANK is low and data written to latch is 1, the corresponding constant current output turns on (LED on). This terminal is internally pulled up with 100kΩ.
IREF	31	I	Constant current value setting. LED current is set to desired value by connecting external resistor between IREF and GND. The 38 times current compared to current across external resistor sink on output terminal.
XDOWN	29	O	Error output. XDOWN is configured as open collector. It goes low when TSD or LOD functions.
VCC	32		Power supply voltage
GND	1		Ground
PGND	6,9,14,19,24,27		Ground for LED driver. (Internally connected to GND)
THERMAL PAD	package bottom		Heat sink pad. This pad is connected to the lowest potential to IC or thermal layer.

absolute maximum ratings (see Note 1)†

Supply voltage, V_{CC}	– 0.3 V to 7 V
Output current (dc), $I_{O(LC)}$	90 mA
Input voltage range, V_I	– 0.3 V to V_{CC} + 0.3 V
Output voltage range, $V_{O(SOUT)}$, $V_{O(XDOWN)}$	– 0.3 V to V_{CC} + 0.3 V
Output voltage range, $V_{O(OUTn)}$	– 0.3 V to 18 V
Storage temperature range, T_{stg}	–40°C to 150°C
Continuous total power dissipation at (or below) $T_A = 25°C$	3.9 W
Power dissipation rating at (or above) $T_A = 25°C$	31.4 mW/°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

dc characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Voltage applied to constant current output, V_O	OUT0 to OUT15 off			17	V
High-level input voltage, V_{IH}		0.8 VCC		VCC	V
Low-level input voltage, V_{IL}		GND		0.2 VCC	V
High-level output current, I_{OH}	V_{CC} = 4.5 V, SOUT			– 1	mA
Low-level output current, I_{OL}	V_{CC} = 4.5 V, SOUT, XDOWN			1	
Constant output current, $I_{O(LC)}$	OUT0 to OUT15			80	mA
Operating free-air temperature range, T_A		– 20		85	°C

ac characteristics, MIN/MAX: V_{CC} = 4.5 V to 5.5 V, T_A = –20 to 85°C TYP: V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK clock frequency	At single operation			20	MHz
		At cascade operation (SOMODE = L)			15	
t_{wh}/t_{wl}	SCLK pulse duration		20			ns
t_{wh}	XLAT pulse duration		10			ns
t_r/t_f	Rise/fall time				100	ns
t_{su}	Setup time	SIN – SCLK	5			ns
		XLAT – SCLK	5			
t_h	Hold time	SIN – SCLK	20			ns
		XLAT – SCLK	20			

electrical characteristics, MIN/MAX: V_{CC} = 4.5 V to 5.5 V, T_A = – 20 to 85°C TYP: V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = – 1 mA	V_{CC} –0.5V			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA			0.5	V
I_I	Input current	V_I = V_{CC} or GND (except BLANK, XLAT)			± 1	µA
I_{CC}	Supply current	Input signal is static, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ, All output bits turn off		3	4.5	mA
		Input signal is static, V_O = 1 V R_{IREF} = 1300 Ω, All output bits turn off		7	9	
		Input signal is static, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, All output bits turn off		11	15	
		Data transfer, V_O = 1 V, $R_{(IREF)}$ = 1300 Ω, All output bits turn on		15	20	
		Data transfer, V_O = 1 V, $R_{(IREF)}$ = 640 Ω, All output bits turn on		35	50	
$I_{OL(C1)}$	Constant output current	V_O = 1 V, $R_{(IREF)}$ = 1300 Ω	35	40	45	mA
$I_{OL(C2)}$	Constant output current	V_O = 1 V $R_{(IREF)}$ = 640 Ω	70	80	90	mA
I_{lkg}	Constant output leakage current	OUT0 to OUT15 ($V_{(OUTn)}$ = 15 V)			0.1	µA
		XDOWN (5V pullup)			1	µA
$\Delta I_{O(LC)}$	Constant output current error between bit	V_O = 1 V, $R_{(IREF)}$ = 640 Ω, All output bits turn on		± 1	± 4	%
$I\Delta_{O(LC1)}$	Changes in constant output current depend on supply voltage	V_{ref} = 1.3 V		± 1	± 4	%/V
$I\Delta_{O(LC2)}$	Changes in constant output current depend on output voltage	V_O = 1 V to 3 V, $R_{(IREF)}$ = 1300 Ω, V_{ref} = 1.3 V, 1 bit output turn on		± 2	± 6	%/V
$T_{(tsd)}$	TSD detection temperature	Junction temperature	150	160	170	°C
V_{ref}	Reference voltage	$R_{(IREF)}$ = 640 Ω		1.3		V
$V_{(LEDDET)}$	LED disconnection detection voltage			0.3		V

switching characteristics, C_L = 15 pF

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time	SOUT		15	20	ns
		OUTn (see Figure 1)		300		
t_f	Fall time	SOUT		5	15	ns
		OUTn		300		
t_{pd}	Propagation delay time	BLANK↑ – OUTn		400	650	ns
		BLANK↓ – OUTn		300	400	
		BLANK↑ – XDOWN (see Note 2)		600	1000	
		BLANK↓ – XDOWN (see Note 2)		500	1000	
		SCLK – SOUT	10	20	35	

NOTE 2: At external resistor 5 kΩ

PARAMETER MEASUREMENT INFORMATION

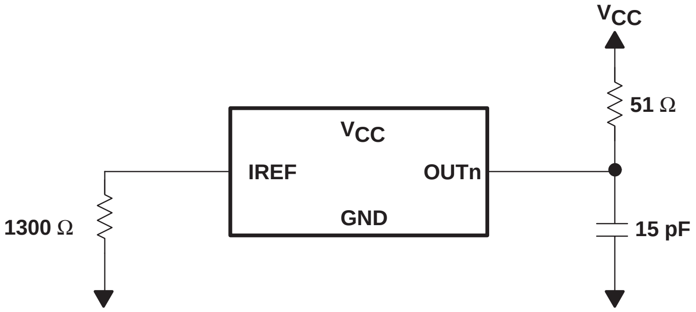


Figure 1. Rise Time and Fall Time Test Circuit for OUTn

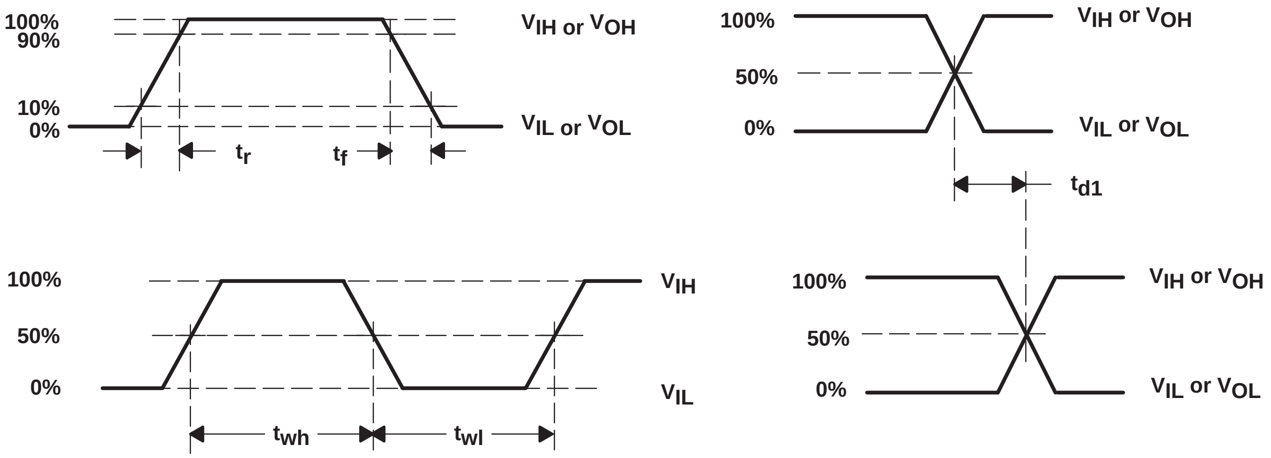


Figure 2. Timing Requirements

PRINCIPLES OF OPERATION

setting for constant output current value

The constant current value is determined by external resistor, $R_{(IREF)}$ between IREF and GND. Refer constant output current characteristics shown on Figure 5 for this external resistor value.

Note that more current flows if connect IREF to GND directly.

constant output current operation

When BLANK is low, the corresponding output is turned on if data latch value is 1, and turned off if data latch value is 0. When BLANK is high, all outputs are forced to turn off. If there is constant current output terminal left unconnected (includes LED disconnection), it should be lighted on after writing zero to corresponding data latch to its output. If this operation is not done, supply current through constant current driver will increase.

shift register latch

The shift register latch is configured with 16 × 1 bits. The 1 bit for constant current output data represents ON for constant current output if data is 1, or OFF if data is 0. The configuration of shift register latch is shown in below.

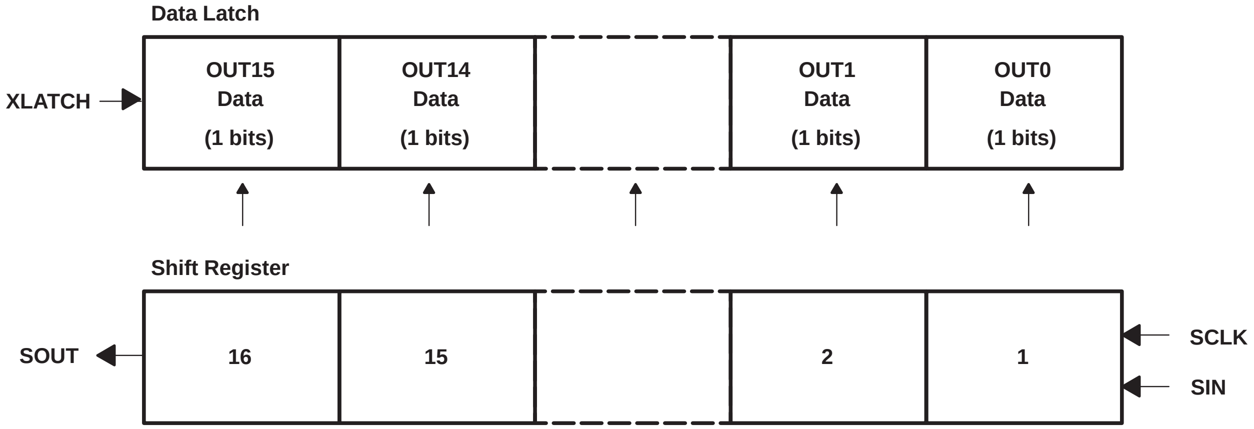


Figure 3. Relationship Between Shift Register and Latch

SOUT output timing selection

By setting level of SOMODE, the SOUT output timing can be changed. When SOMODE is set to low, data is clocked out to SOUT synchronized on the rising edge of SCLK, and when SOMODE is set to high, data is clocked out to SOUT synchronized on the falling edge of SCLK. When SOMODE is set to high and shift operation is done, the data shift error can be prevented even though SCLK signal is externally buffered in serial. Note that the maximum data transfer rate in cascade operation is slower than that when SMODE is set to low.

TSD (thermal shutdown)

When the junction temperature exceeds the limit, TSD starts to function and turn constant current output off and XDOWN goes low. Since XDOWN is configured with open-collector output, the outputs of multiple ICs can be concatenated. To recover from constant current output off-state to normal operation, power supply should be turned off and then turned on after several seconds.

PRINCIPLES OF OPERATION

LOD function (LED open detection)

If any terminal voltage of constant current output (OUT0 TO 15) to be turned on is approximately below 0.3 V, XDOWN output goes low during output on by knowing LED disconnection. This function is operational for sixteen OUTn individually. To know which constant current output is disconnected, the level of XDOWN is repeatedly checked 16 times from OUT0 to OUT15 turning one constant current output on. The power supply voltage for LED should be set to that the constant current output is applied to above 0.4 V to prevent from XDOWN low when LED is lighting on normally. Note that on-time should be minimum1µs after the constant current output is turned on since XDOWN output is required approximately 1 µs.

As discussed earlier, XDOWN is used for both TSD and LOD function. Therefore, BLANK is used to know which one of TSD or LOD worked when XDOWN went low at LED disconnection, that is, in this condition, when set BLANK to high, all the constant current outputs are turned off and LOD disconnection detection is disabled, then, if XDOWN was changed to high, LED disconnection must be occurred.

Table 1 is an example for XDOWN output status using four LEDs.

Table 1. XDOWN Output Example

LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	ON	ON	ON	ON
DETECTION RESULT	GOOD	NG	GOOD	NG
XDOWN	LOW (by case 2, 4)			
LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	ON	ON	OFF	OFF
DETECTION RESULT	GOOD	NG	GOOD	GOOD
XDOWN	LOW (by case 2)			
LED NUMBER	1	2	3	4
LED STATUS	GOOD	NG	GOOD	NG
OUTn	OFF	OFF	OFF	OFF
DETECTION RESULT	GOOD	GOOD	GOOD	GOOD
XDOWN2	HIGH–IMPEDANCE			

noise reduction : output slope

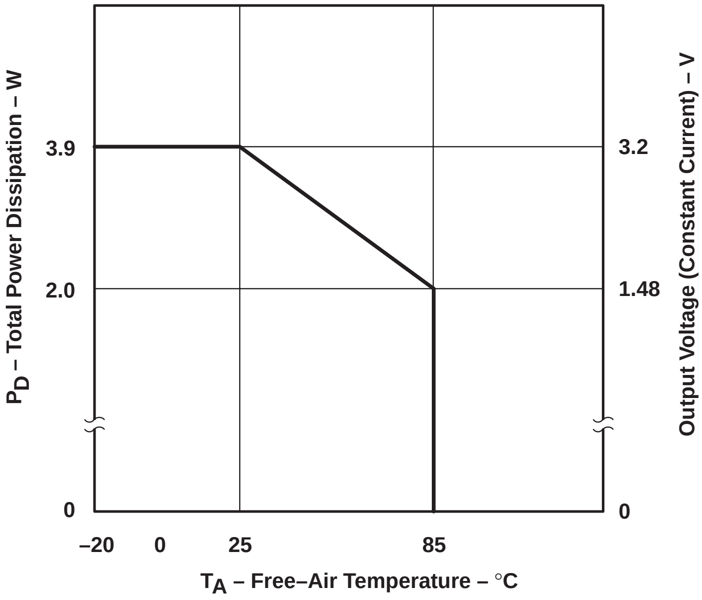
When output current is 80 mA, the time to change constant current output to turn-on and turn-off is approximately 150 ns and 250 ns respectively. This allows to reduce concurrent switching noise occurred when multiple outputs turn or off at the same time.

thermal pad

The thermal pad should be connected to GND to eliminate the noise influence since it is connected to the bottom side of IC chip. Also, desired thermal effect will be obtained by connecting this pad to the PCB pattern with better thermal conductivity.

PRINCIPLES OF OPERATION

power rating – free-air temperature



NOTES: A. The data is based on simulation result. When TI recommended print circuit board is used, derate linearly at the rate of 31.4 mW/°C for operation above 25°C free-air temperature. VCC=5 V, $I_{O(LC)}$ = 80 mA, I_{CC} is typical value.

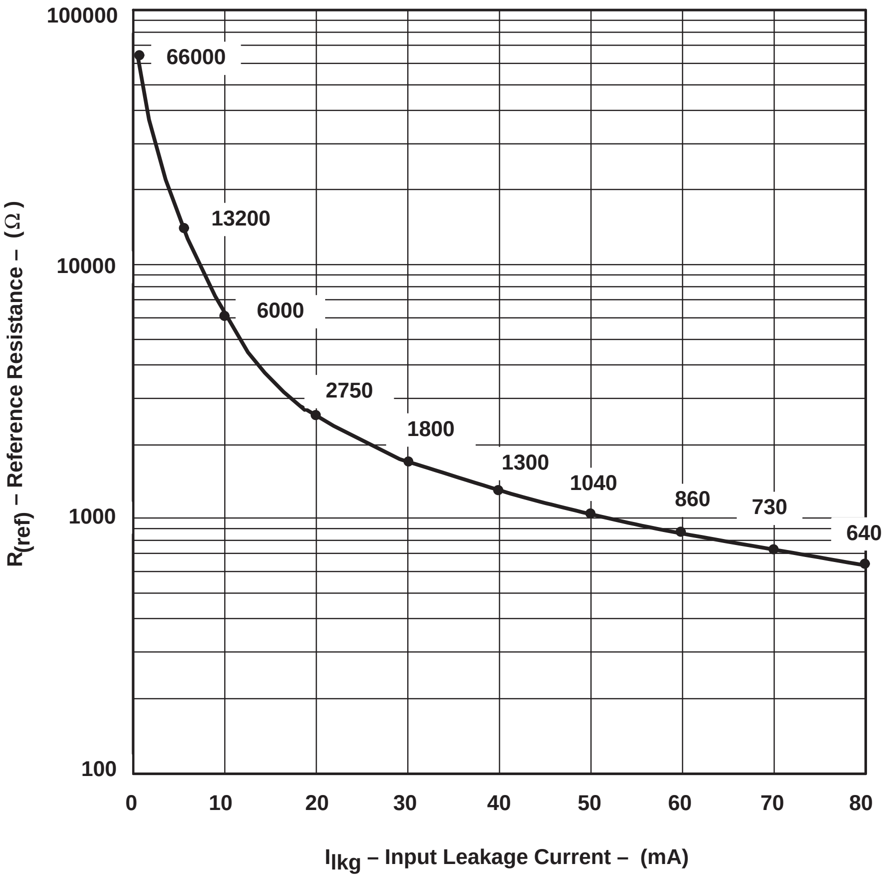
B. The thermal impedance will be varied depend on mounting conditions. Since PZP package established low thermal impedance by radiating heat from thermal pad, the thermal pad should be soldered to pattern with low thermal impedance.

C. The material for PCB should be selected considering the thermal characteristics since the temperature will rise around the thermal pad.

Figure 4. Power Rating

PRINCIPLES OF OPERATION

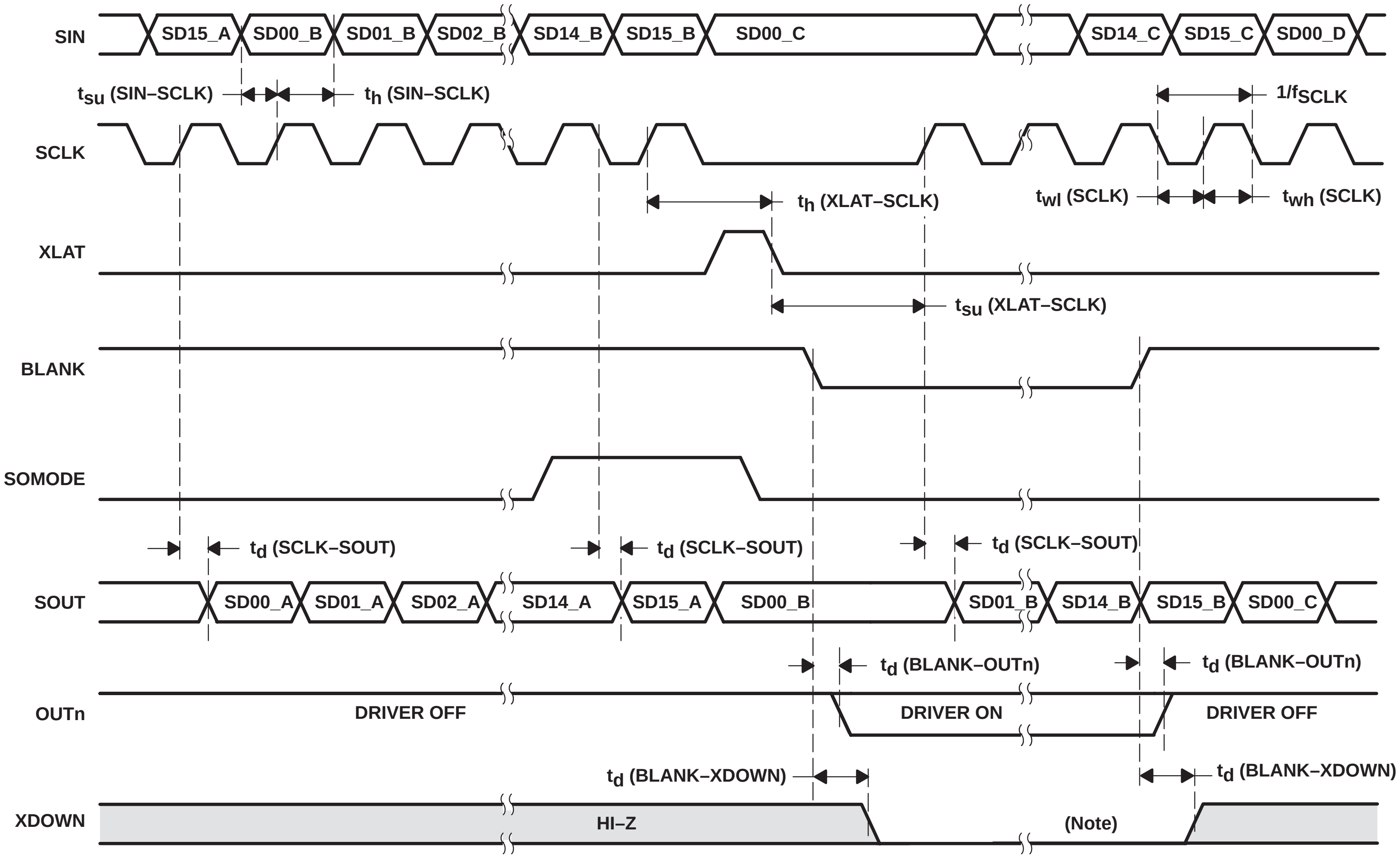
constant output current



Conditions : V_O = 1 V, V_{ref} = 1.3 V

NOTE: The resistor, $R_{(IREF)}$, should be located as close to IREF terminal as possible to avoid the noise influence.

Figure 5. Current on Constant Current Output vs External Resistor



NOTE : LED disconnected

Figure 6. Timing Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA00208DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples
HPA00209DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples
TLC5921DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples
TLC5921DAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples
TLC5921DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples
TLC5921DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5921	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

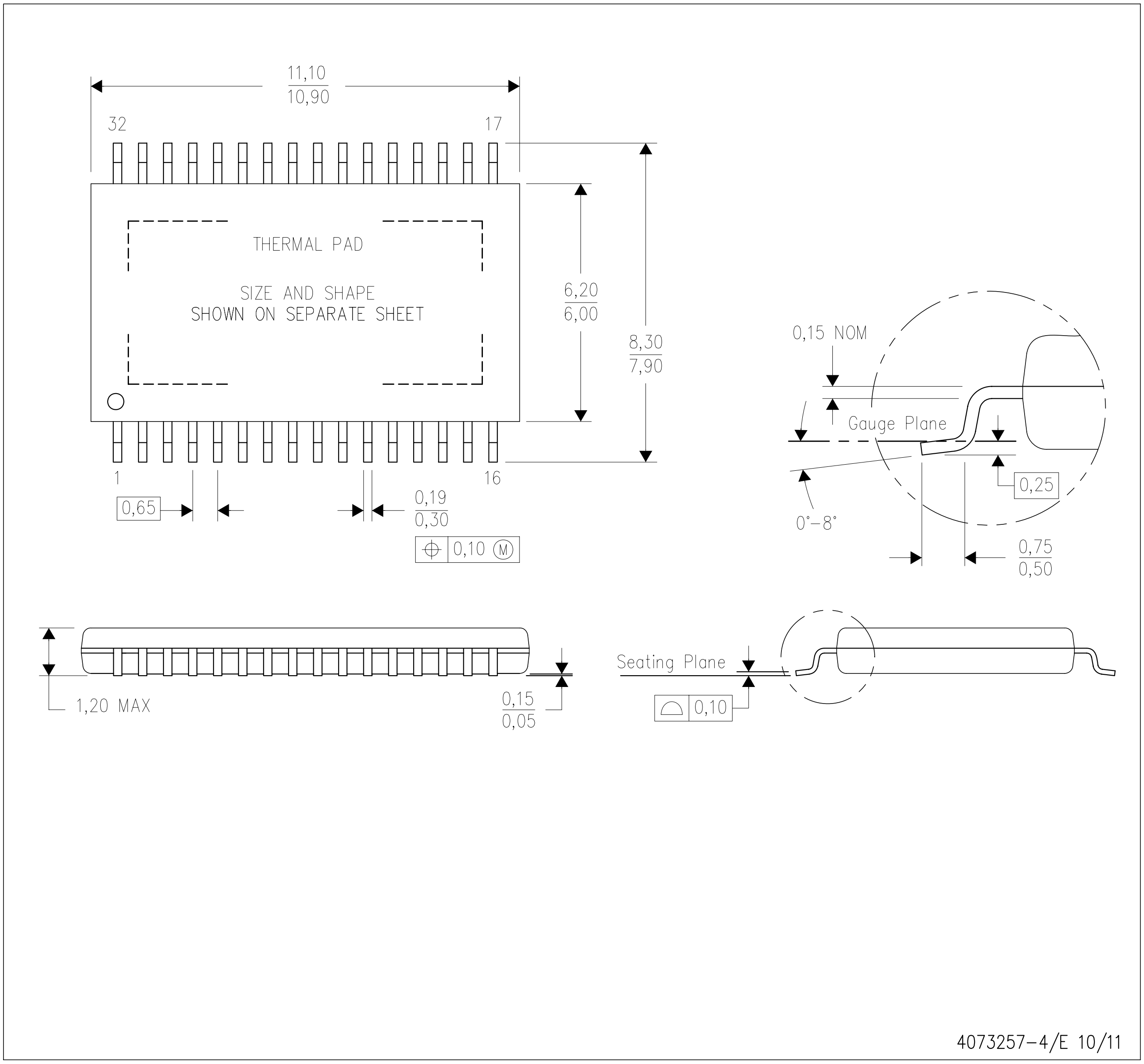
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- F Falls within JEDEC MO-153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

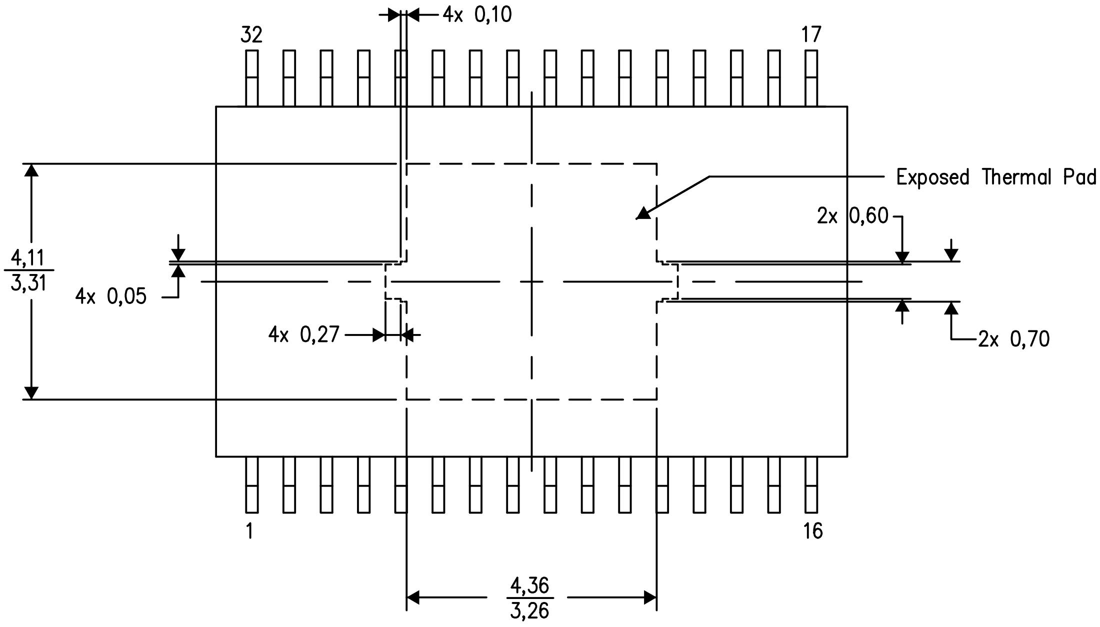
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

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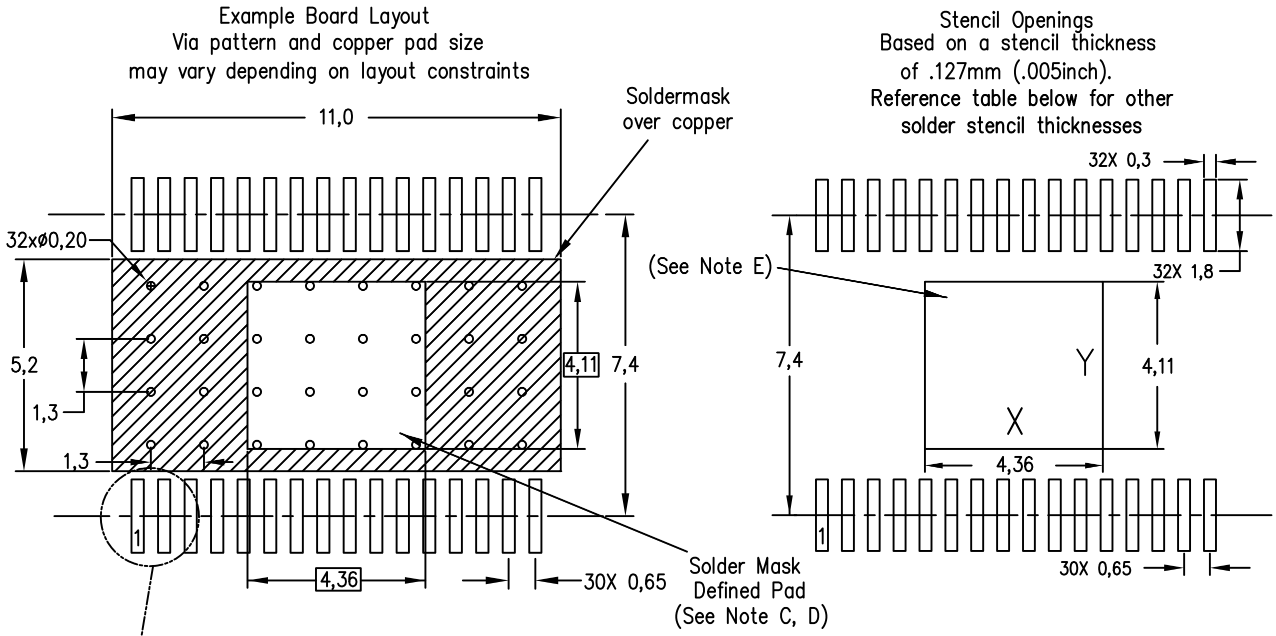
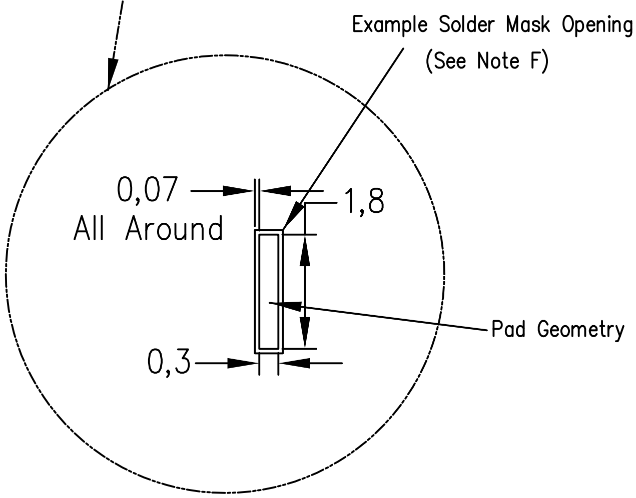
DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

4210213-2/E 01/14

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- F. Contact the board fabrication site for recommended soldermask tolerances.

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