TLA2518 Small, 8-Channel, 12-Bit ADC With SPI Interface and GPIOs

1 Features

- Small package size:
  - WQFN 3 mm × 3 mm
- 8 channels configurable as any combination of:
  - Up to 8 analog inputs, digital inputs, or digital outputs
- GPIOs for I/O expansion:
  - Open-drain, push-pull digital outputs
- Wide operating ranges:
  - AVDD: 2.35 V to 5.5 V
  - DVDD: 1.65 V to 5.5 V
  - –40°C to +85°C temperature range
- Enhanced-SPI digital interface:
  - High-speed, 60-MHz interface
  - Achieve full throughput with >13.5-MHz SPI
- Programmable averaging filters:
  - Programmable sample size for averaging
  - Averaging with internal conversions
  - 16-bit resolution

2 Applications

- Supervisory functions
- Portable instrumentation
- Telecommunication infrastructure
- Power-supply monitoring

3 Description

The TLA2518 is an easy-to-use, 8-channel, multiplexed, 12-bit, 1-MSPS, successive approximation register analog-to-digital converter (SAR ADC). The eight channels can be independently configured as either analog inputs, digital inputs, or digital outputs. The device has an internal oscillator for the ADC conversion process.

The TLA2518 communicates via an SPI compatible interface and supports averaging multiple data samples with a single start of conversion. The built-in programmable averaging filters help reduce noise from the analog inputs and reduce the number of data samples required to be read by the host.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLA2518	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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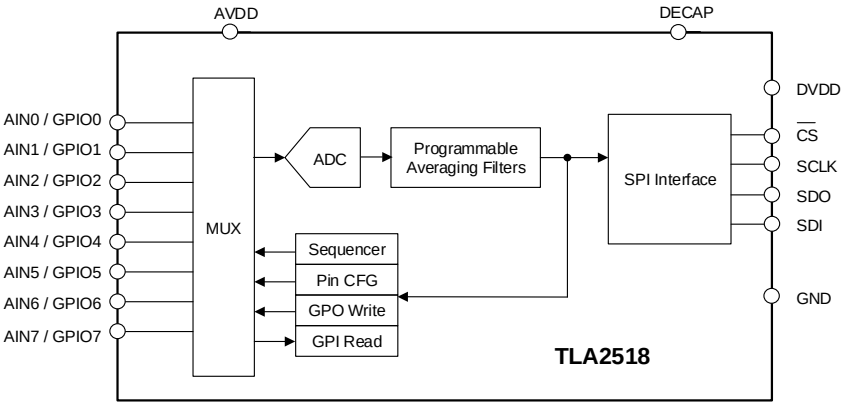
TLA2518 Block Diagram and Applications

Device Block Diagram



Example Applications

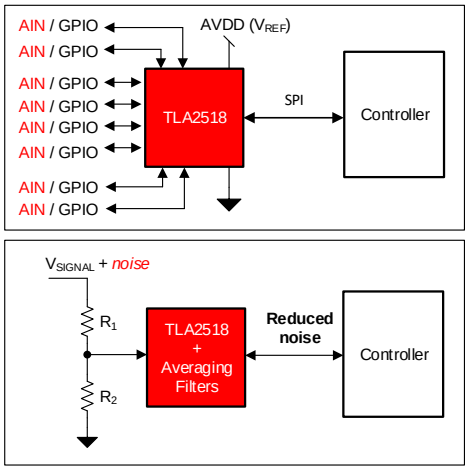


Table of Contents

ADVANCE INFORMATION

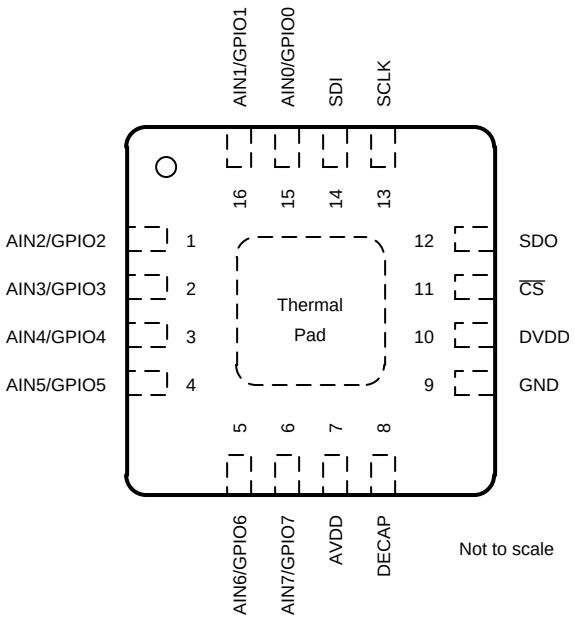
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2019	*	Initial release.

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NAME	NO.		
AIN0/GPIO0	15	AI, DI, DO	Channel 0; can be configured as either an analog input (default), digital input, or digital output.
AIN1/GPIO1	16	AI, DI, DO	Channel 1; can be configured as either an analog input (default), digital input, or digital output.
AIN2/GPIO2	1	AI, DI, DO	Channel 2; can be configured as either an analog input (default), digital input, or digital output.
AIN3/GPIO3	2	AI, DI, DO	Channel 3; can be configured as either an analog input (default), digital input, or digital output.
AIN4/GPIO4	3	AI, DI, DO	Channel 4; can be configured as either an analog input (default), digital input, or digital output.
AIN5/GPIO5	4	AI, DI, DO	Channel 5; can be configured as either an analog input (default), digital input, or digital output.
AIN6/GPIO6	5	AI, DI, DO	Channel 6; can be configured as either an analog input (default), digital input, or digital output.
AIN7/GPIO7	6	AI, DI, DO	Channel 7; can be configured as either an analog input (default), digital input, or digital output.
AVDD	7	Supply	Analog supply input, also used as the reference voltage to the ADC; connect a 1-µF decoupling capacitor to GND.
$\overline{CS}$	11	DI	Chip-select input pin; active low. The device takes control of the data bus when $\overline{CS}$ is low. The device starts converting the active input channel on the rising edge of $\overline{CS}$. SDO goes hi-Z when $\overline{CS}$ is high.
DECAP	8	Supply	Connect a decoupling capacitor to this pin for the internal power supply.
DVDD	10	Supply	Digital I/O supply voltage; connect a 1-µF decoupling capacitor to GND.
GND	9	Supply	Ground for the power supply; all analog and digital signals are referred to this pin voltage.
SCLK	13	DI	Serial clock for the SPI interface.
SDI	14	DI	Serial data in for the device.
SDO	12	DO	Serial data out for the device.

(1) AI = analog input, DI = digital input, and DO = digital output.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx / GPOx(2) to GND	GND – 0.3	AVDD + 0.3	V
Digital input to GND	GND – 0.3	5.5	V
Current through any pin except supply pins(3)	–10	10	mA
Junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx / GPIOx refers to pins 1, 2, 3, 4, 5, 6, 15, and 16.
(3) Pin current must be limited to 10mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog supply voltage		2.35	3.3	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
ANALOG INPUTS						
FSR	Full-scale input range	AIN_X - GND	0		AVDD	V
V_{IN}	Absolute input voltage	AIN_X - GND	–0.1		AVDD + 0.1	V
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	85	℃

(1) AINx refers to AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

6.4 Thermal Information

THERMAL METRIC(1)		TLA2518 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{SH}	Sampling capacitance			12		pF
DC PERFORMANCE						
	Resolution	No missing codes		12		bits
DNL	Differential nonlinearity			±0.3		LSB
INL	Integral nonlinearity			±0.5		LSB
$V_{(OS)}$	Input offset error	Post offset calibration		±0.5		LSB
	Input offset thermal drift	Post offset calibration		±5		ppm/°C
G_E	Gain error			±0.05		%FSR
	Gain error thermal drift			±5		ppm/°C
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	AVDD = 5 V, f_{IN} = 2 kHz		71.5		dB
		AVDD = 3 V, f_{IN} = 2 kHz		70.5		dB
DECAP Pin						
	Decoupling capacitor on DECAP pin		0.1	1		µF
SPI INTERFACE ($\overline{CS}$, SCLK, SDI, SDO)						
V_{IH}	Input high logic level		0.7 x DVDD		5.5	V
V_{IL}	Input low logic level		–0.3		0.3 x DVDD	V
V_{OH}	Output high logic level	Source current = 2 mA, DVDD > 2 V	0.8 x DVDD		DVDD	V
		Source current = 2 mA, DVDD ≤ 2 V	0.7 x DVDD		DVDD	
V_{OL}	Output low logic level	Sink current = 2 mA, DVDD > 2 V	0		0.4	V
		Sink current = 2 mA, DVDD ≤ 2 V	0		0.2 x DVDD	
GPIOs						
V_{IH}	Input high logic level		0.7 x AVDD		AVDD + 0.3	V
V_{IL}	Input low logic level		–0.3		0.3 x AVDD	V
V_{OH}	Output high logic level	GPO_DRIVE_CFG = push-pull, I_{SOURCE} = 2 mA	0.8 x AVDD		AVDD	V
V_{OL}	Output low logic level	I_{SINK} = 2 mA	0		0.2 x AVDD	V
I_{OH}	Output high source current	V_{OH} > 0.7 x AVDD			5	mA
I_{OL}	Output low sink current	V_{OL} < 0.3 x AVDD			5	mA
POWER-SUPPLY CURRENTS						
I_{AVDD}	Analog supply current	Full throughput, AVDD = 5 V		1.6		mA
		Full throughput, AVDD = 3 V		1.1		
		No conversion, AVDD = 5 V		0.03		

6.6 Timing Requirements

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C

		MIN	MAX	UNIT
CONVERSION CYCLE				
f_{CYCLE}	Sampling frequency		1000	kSPS
t_{CYCLE}	ADC cycle-time period	1 / f_{CYCLE}		s
t_{ACQ}	Acquisition time	300		ns
t_{QT_ACQ}	Quiet acquisition time	10		ns

ADVANCE INFORMATION

Timing Requirements (continued)

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C

		MIN	MAX	UNIT
t_{D_CNVCAP}	Quiet conversion time	10		ns
t_{WH_CSZ}	Pulse duration: $\overline{CS}$ high	10		ns
t_{WL_CSZ}	Pulse duration: $\overline{CS}$ low	10		ns
SPI INTERFACE TIMINGS				
f_{CLK}	Maximum SCLK frequency		60	MHz
t_{CLK}	Minimum SCLK time period	16.67		ns
t_{PH_CK}	SCLK high time	0.45	0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45	0.55	t_{CLK}
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	5		ns
t_{SU_CKDI}	Setup time: SDI data valid to the SCLK capture edge	1.2		ns
t_{HT_CKDI}	Hold time: SCLK capture edge to data valid on SDI	0.65		ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	5		ns

6.7 Switching Characteristics

at AVDD = 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +85°C; typical values at T_A = 25°C

PARAMETER		Test Conditions	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time			600	ns
t_{ACQ}	Acquisition time		400		ns
RESET					
t_{PU}	Power-up time for device	AVDD ≥ 2.35 V, C_{DECAP} = 1 µF		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete(1)			5	ms
SPI INTERFACE TIMINGS					
t_{DEN_CSDO}	Delay time: $\overline{CS}$ falling to data enable			15	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going Hi-Z			15	ns
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO			15	ns

(1) RST bit is automatically reset to 0b after t_{RST}.

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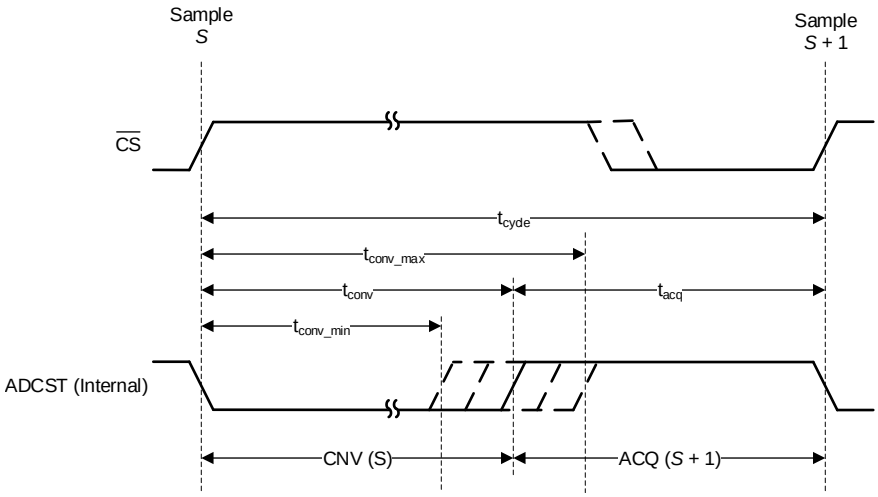
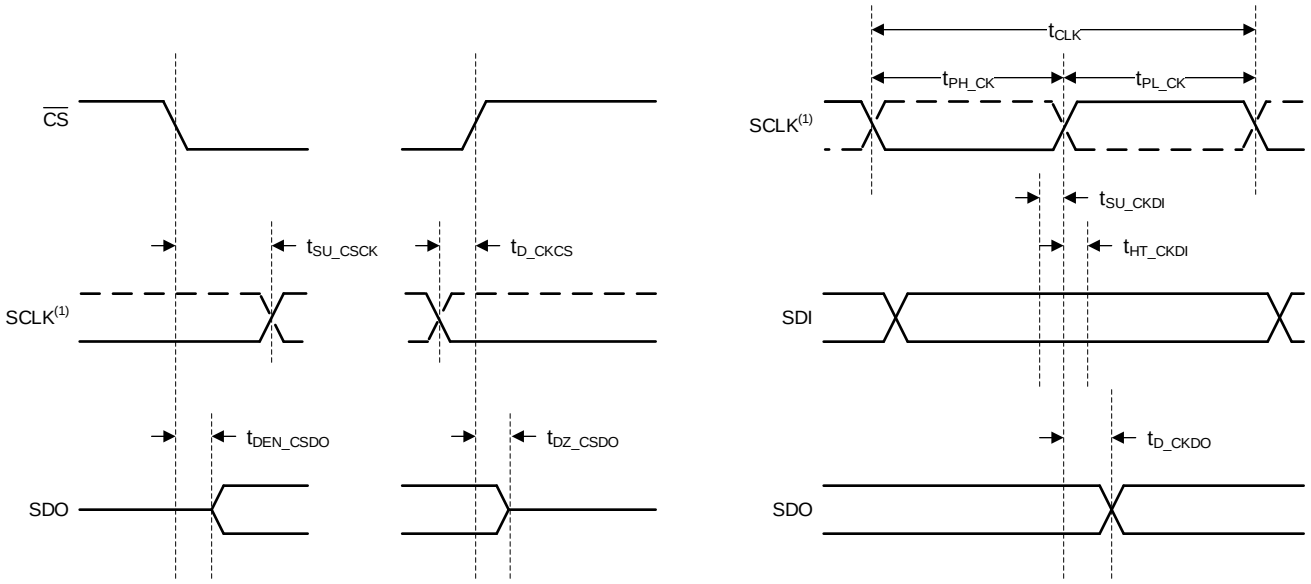


Figure 1. Conversion Cycle Timing



(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

Figure 2. SPI-Compatible Serial Interface Timing

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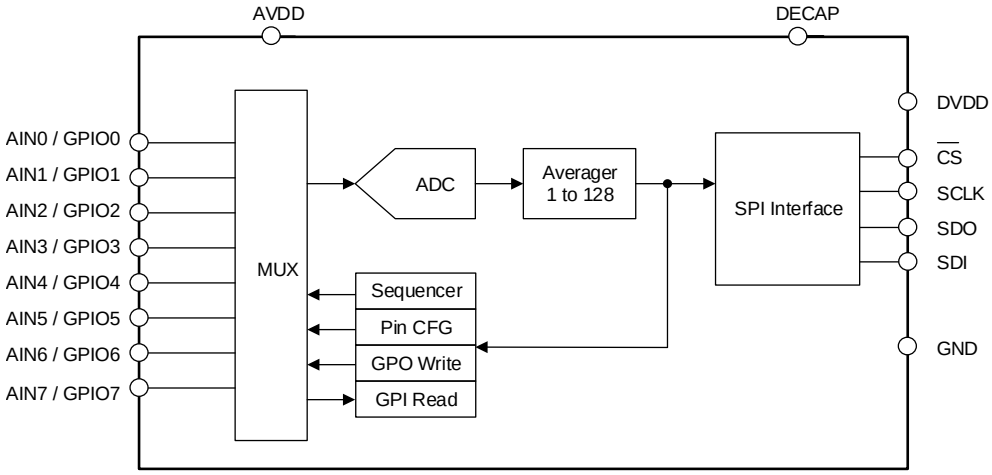
7 Detailed Description

7.1 Overview

The TLA2518 is a small, eight-channel, multiplexed, 12-bit, 1-MSPS, analog-to-digital converter (ADC) with an enhanced-SPI serial interface. The eight channels of the TLA2518 can be individually configured as either analog inputs, digital inputs, or digital outputs. The device uses an internal oscillator for conversion. The analog input channel selection can be auto-sequenced to simplify the digital interface with the host.

The device features a programmable averaging filter that outputs a 16-bit result for enhanced resolution.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Multiplexer and ADC

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). Figure 3 shows that each input pin has ESD protection diodes to AVDD and GND. On power-up or after device reset, all eight multiplexer channels are configured as analog inputs.

Figure 3 shows an equivalent circuit for pins configured as analog inputs. The ADC sampling switch is represented by ideal switch (SW) in series with the resistor R_{SW} (typically 150 Ω) and the sampling capacitor, C_{SH} (typically 12 pF).

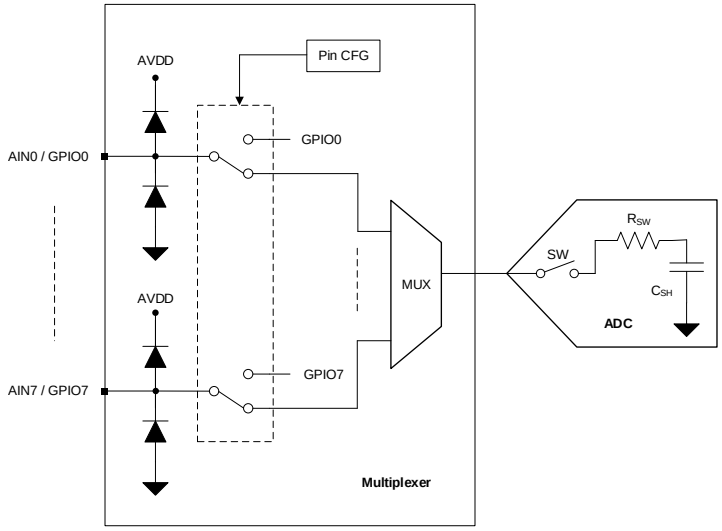


Figure 3. Analog Inputs, GPIOs, and ADC Connections

During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN_CFG register. The direction of a GPIO (either as an input or an output) can be set in the GPIO_CFG register. The logic level on the channels configured as digital inputs can be read from the GPI_VALUE register. The digital outputs can be accessed by writing to the GPO_OUTPUT_VALUE register. The digital outputs can be configured as either open-drain or push-pull in the GPO_DRIVE_CFG register.

7.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends connecting a 1-µF, low-equivalent series resistance (ESR) ceramic decoupling capacitor between the AVDD and GND pins.

7.3.3 ADC Transfer Function

The ADC output is in straight binary format. Equation 1 computes the ADC resolution:

$$1\ LSB = V_{REF} / 2^N \quad (1)$$

where:

- V_{REF} = AVDD
- N = 12

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Feature Description (continued)

Figure 4 and Table 1 detail the transfer characteristics for the device.

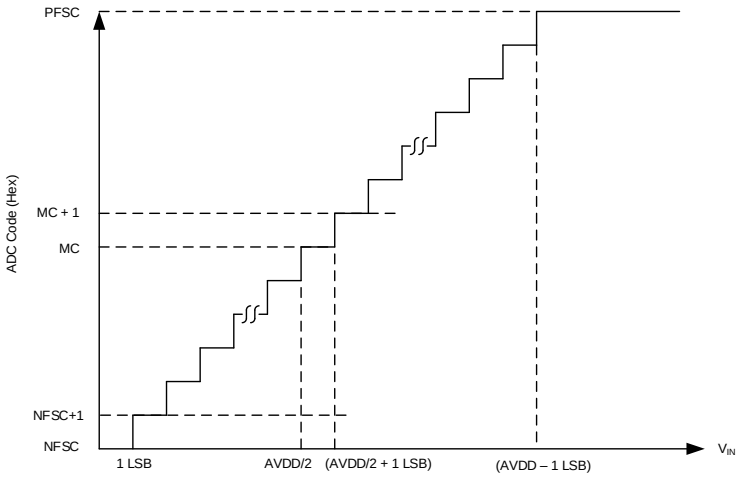

Figure 4. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE FOR SINGLE-ENDED INPUT	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
(AVDD / 2) to (AVDD / 2) + 1 LSB	MC	Mid code	800
(AVDD / 2) + 1 LSB to (AVDD / 2) + 2 LSB	MC + 1	—	801
≥ AVDD – 1 LSB	PFSC	Positive full-scale code	FFF

7.3.4 ADC Offset Calibration

The variation in ADC offset error resulting from changes in temperature or AVDD can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

ADVANCE INFORMATION

7.3.5 Programmable Averaging Filter

The TLA2518 features a built-in oversampling (OSR) function that can be used to average several samples. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register. The averaging filter configuration is common to all analog input channels. Figure 5 shows that the averaging filter module output is 16 bits long. In manual conversion mode and auto-sequence mode, only the first conversion for the selected analog input channel must be initiated by the host; see the *Manual Mode* and *Auto-Sequence Mode* sections. As shown in Figure 5, any remaining conversions for the selected averaging factor are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. As shown in Figure 5, the 16-bit result can be read out after the averaging operation completes.

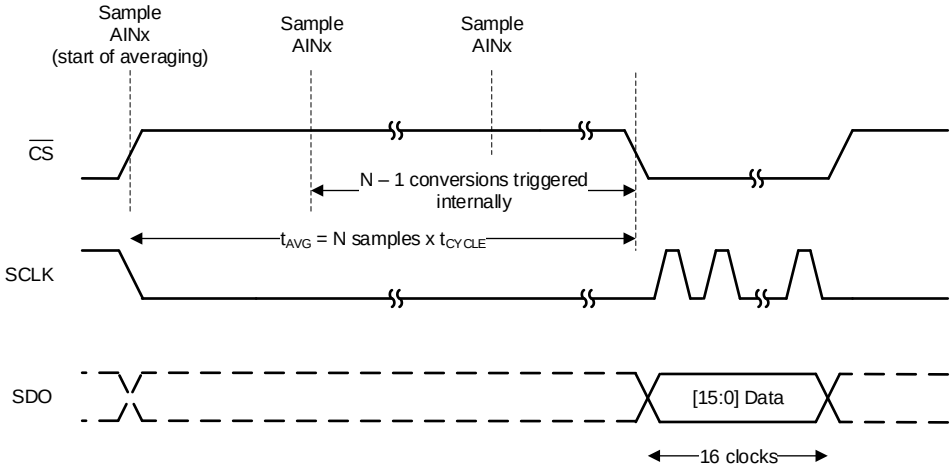

Figure 5. Averaging Example

Equation 2 provides the LSB value of the 16-bit average result.

$$1\ LSB = \frac{AVDD}{2^{16}} \quad (2)$$

7.3.6 General-Purpose I/Os

The eight channels of the TLA2518 can be independently configured as analog inputs, digital inputs, or digital outputs. Table 2 shows how the PIN_CFG and GPIO_CFG registers can be used to configure the device channels.

Table 2. Configuring Channels as Analog Inputs or GPIOs

PIN_CFG[7:0]	GPIO_CFG[7:0]	GPO_DRIVE_CFG[7:0]	CHANNEL CONFIGURATION
0	x	x	Analog input (default)
1	0	x	Digital input
1	1	0	Digital output; open-drain driver
1	1	1	Digital output; push-pull driver

Digital outputs can be configured to logic 1 or 0 by writing to the GPO_OUTPUT_VALUE register. Reading the GPI_VALUE register returns the logic level for all channels configured as digital inputs or digital outputs. The GPI_VALUE register can be read to detect a failure in external components, such as a floating pullup resistor or a low-impedance pulldown resistor, that prevents digital outputs being set to the desired logic level.

7.3.7 Oscillator and Timing Control

The device uses an internal oscillator for conversion. When using the averaging module, the host initiates the first conversion and subsequent conversions are generated internally by the device. Also, in autonomous mode of operation, the start of the conversion signal is generated by the device. Table 3 describes how the sampling rate can be controlled by the OSC_SEL and CLK_DIV[3:0] register fields when the device generates the start of the conversion.

ADVANCE INFORMATION

Table 3. Configuring Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)
0000b	1000	1	31.25	32
0001b	666.7	1.5	20.83	48
0010b	500	2	15.63	64
0011b	333.3	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072

The conversion time of the device, given by t_{CONV} in the *Switching Characteristics* table, is independent of the OSC_SEL and CLK_DIV[3:0] configuration.

7.3.8 Output Data Format

Figure 6 shows various SPI frames for reading data. The data output is MSB aligned. If averaging is enabled the output data from the ADC are 16 bits long, otherwise the output data are 12 bits long. Optionally, a 4-bit channel ID can be appended at the end of the output data by configuring the APPEND_STATUS[1:0] field.

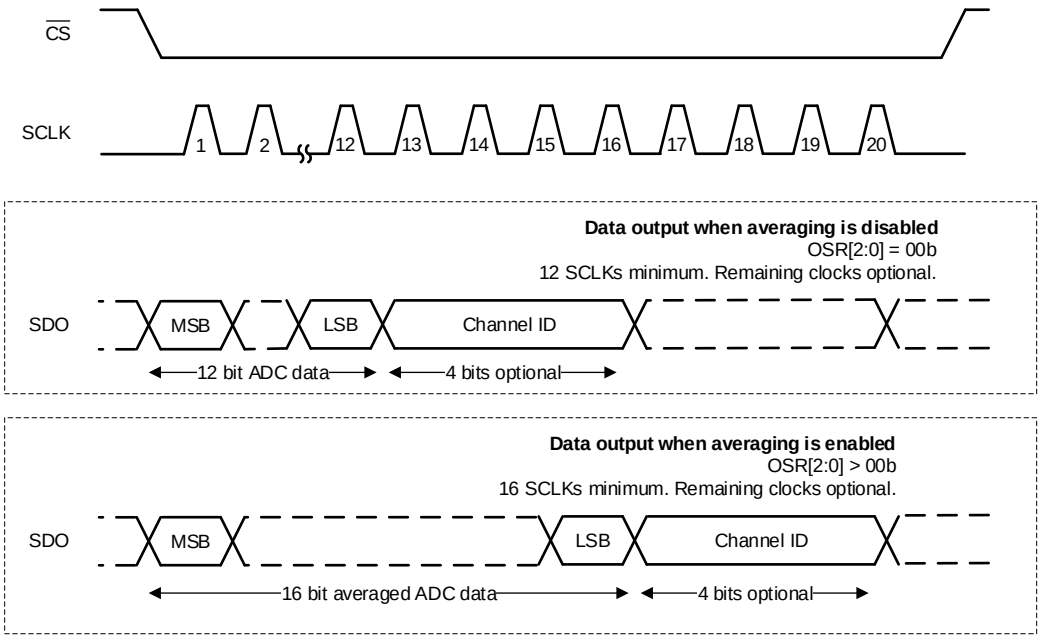

Figure 6. SPI Frames for Reading Data

7.3.9 Device Programming

7.3.9.1 Enhanced-SPI Interface

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve full throughput. As described in Table 4, the host controller can use any of the four SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to access the device.

Table 4. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	CPOL_CPHA[1:0]	DIAGRAM
SPI-00	Low	Rising	00b	Figure 7
SPI-01	Low	Falling	01b	Figure 8
SPI-10	High	Falling	10b	Figure 7
SPI-11	High	Rising	11b	Figure 8

On power-up or after coming out of any asynchronous reset, the device supports the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol, program the CPOL_CPHA[1:0] field. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.

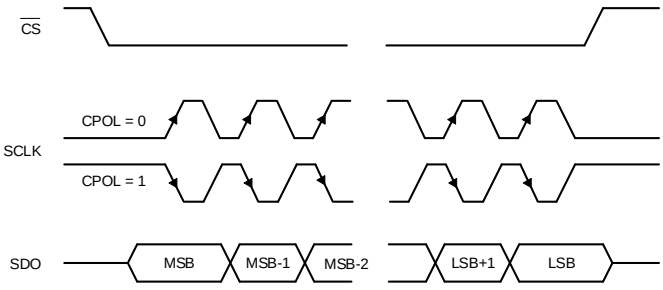

Figure 7. Standard SPI Timing Protocol (CPHA = 0)

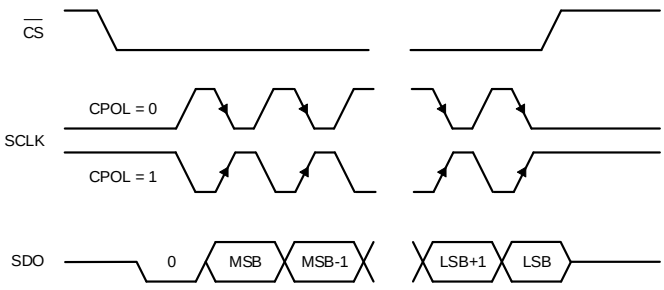

Figure 8. Standard SPI Timing Protocol (CPHA = 1)

7.3.9.2 Register Read/Write Operation

The device supports the commands listed in Table 5 to access the internal configuration registers.

Table 5. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0000 0000b	No operation
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit

ADVANCE INFORMATION

7.3.9.2.1 Register Write

A 24-bit SPI frame is required for writing data to configuration registers. The 24-bit data on SDI, as shown in Figure 9. consists of an 8-bit write command (0000 1000b), an 8-bit register address, and 8-bit data. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 8-bit data specified during the register write operation.

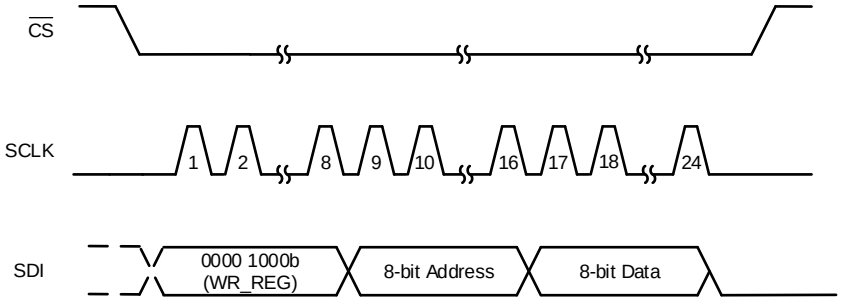

Figure 9. Register Write Operation

7.3.9.2.2 Register Read

Register read operation consists of two SPI frames: the first SPI frame initiates a register read and the second SPI frame reads data from the register address provided in the first frame. As shown in Figure 10, the 8-bit register address and the 8-bit dummy data are sent over the SDI pin during the first 24-bit frame with the read command (0001 0000b). On the rising edge of $\overline{CS}$, the read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO correspond to the requested register read. During the second frame, SDI can be used to initiate another operation or can be set to 0.

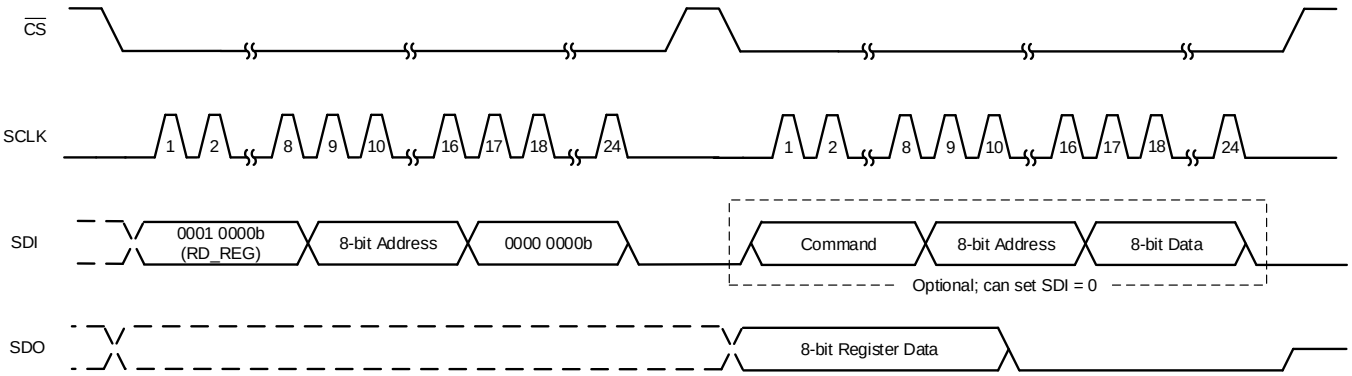

Figure 10. Register Read Operation

ADVANCE INFORMATION

7.4 Device Functional Modes

Table 6 lists the functional modes supported by the TLA2518.

Table 6. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	SEQ_MODE[1:0]
Manual	$\overline{CS}$ rising edge	Register write to MANUAL_CHID	00b
On-the-fly	$\overline{CS}$ rising edge	First 5 bits after the $\overline{CS}$ falling edge	10b
Auto-sequence	$\overline{CS}$ rising edge	Channel sequencer	01b

The device powers up in manual mode and can be configured into either of these modes by writing the configuration registers for the desired mode.

7.4.1 Device Power-Up and Reset

On power-up, the BOR bit is set indicating a power-cycle or reset event. The device can be reset by setting the RST bit or by recycling the power on the AVDD pin.

7.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. Figure 11 shows the steps for operating the device in manual mode.

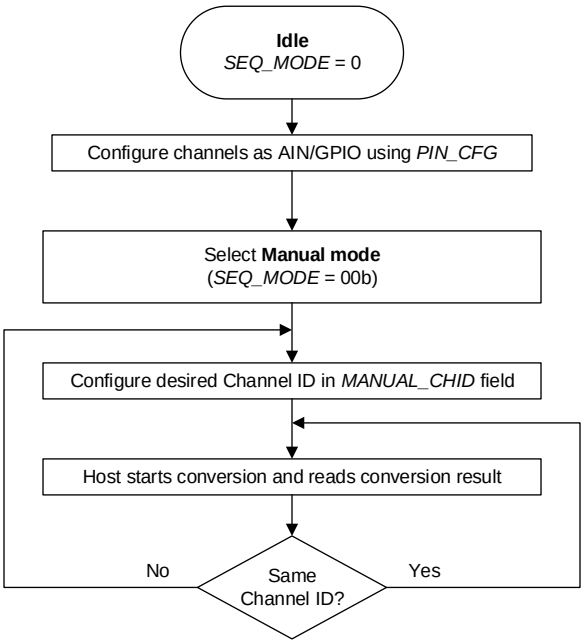

Figure 11. Device Operation in Manual Mode

In manual mode, the command to switch to a new channel (indicated by cycle N in Figure 12) is decoded by the device on the $\overline{CS}$ rising edge. The $\overline{CS}$ rising edge is also the start of the conversion signal, and therefore the device samples the previously selected MUX channel in cycle N+1. The newly selected analog input channel data are available in cycle N+2. For switching the analog input channel, a register write to the MANUAL_CHID field requires 24 clocks; see the *Register Write* section for more details. After a channel is selected, the number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

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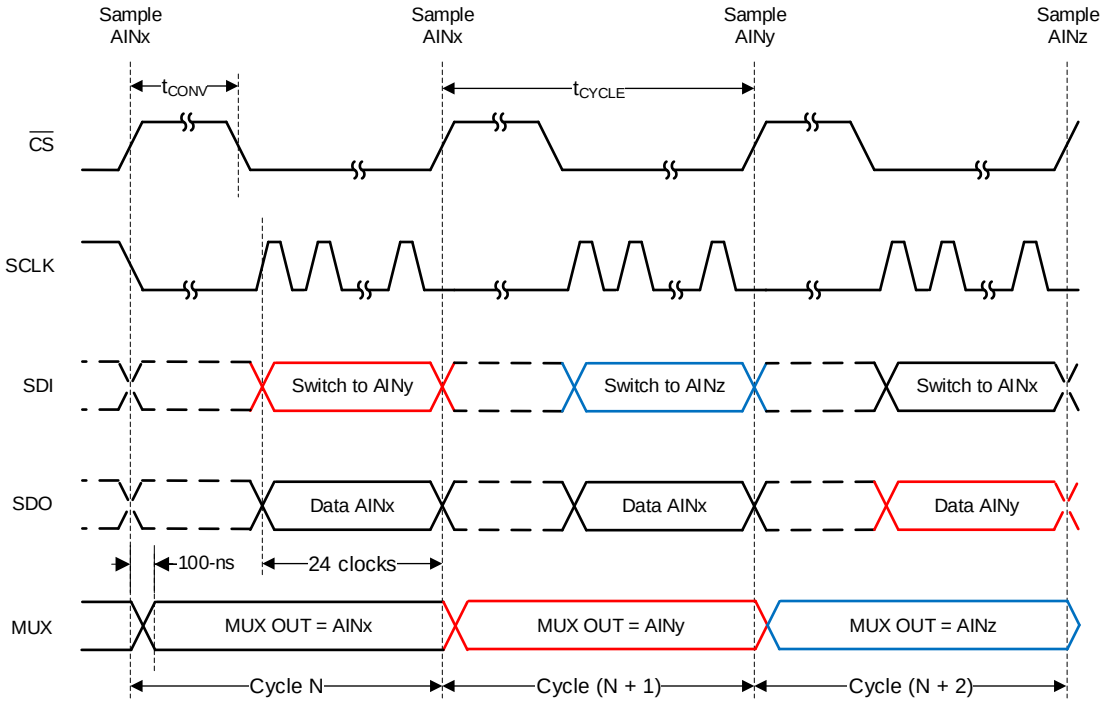

Figure 12. Starting Conversions and Reading Data in Manual Mode

7.4.3 On-the-Fly Mode

In the on-the-fly mode of operation, the analog input channel is selected, as shown in Figure 13, using the first five bits on SDI without waiting for the $\overline{CS}$ rising edge. Thus, the ADC samples the newly selected channel on the $\overline{CS}$ edge and there is no latency between the channel selection and the ADC output data.

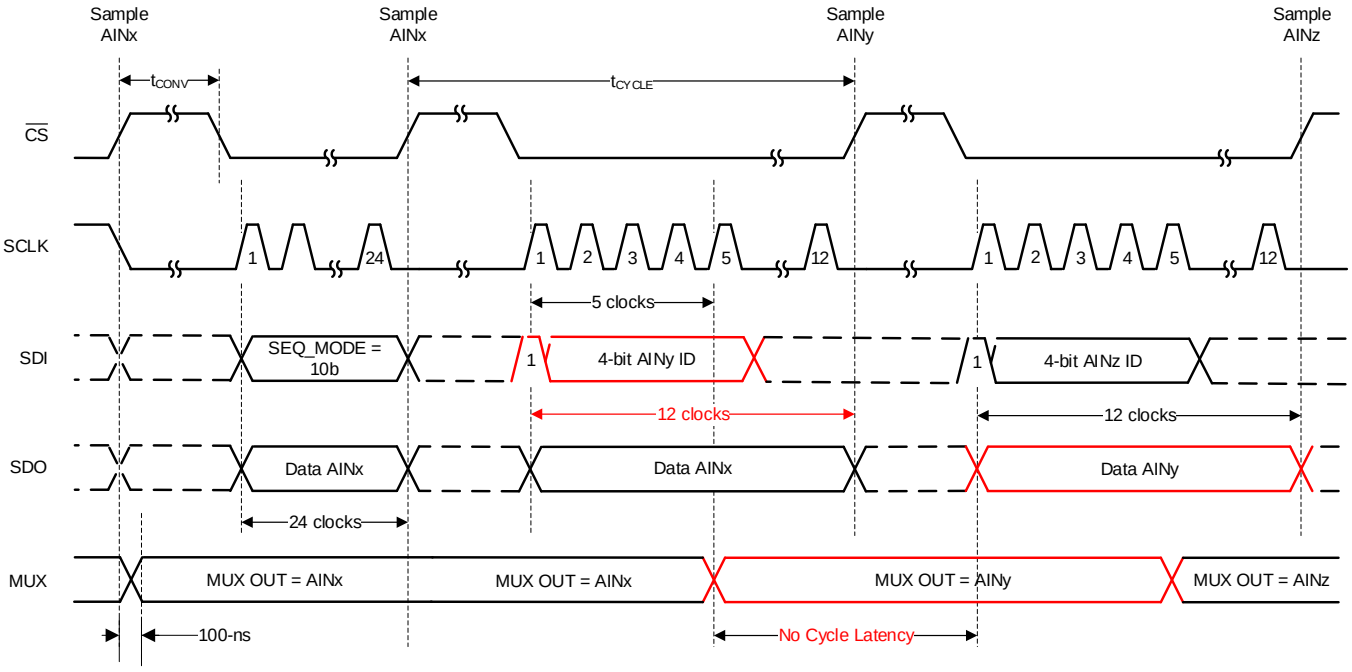

Figure 13. Starting Conversions and Reading Data in On-the-Fly Mode

ADVANCE INFORMATION

The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

7.4.4 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CHSEL register. To enable the channel sequencer, set SEQ_START = 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START = 0b.

In the example shown in Figure 14, AIN2 and AIN6 are enabled for sequencing in AUTO_SEQ_CHSEL. The channel sequencer loops through AIN2 and AIN6 and repeats until SEQ_START is set to 0b. The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

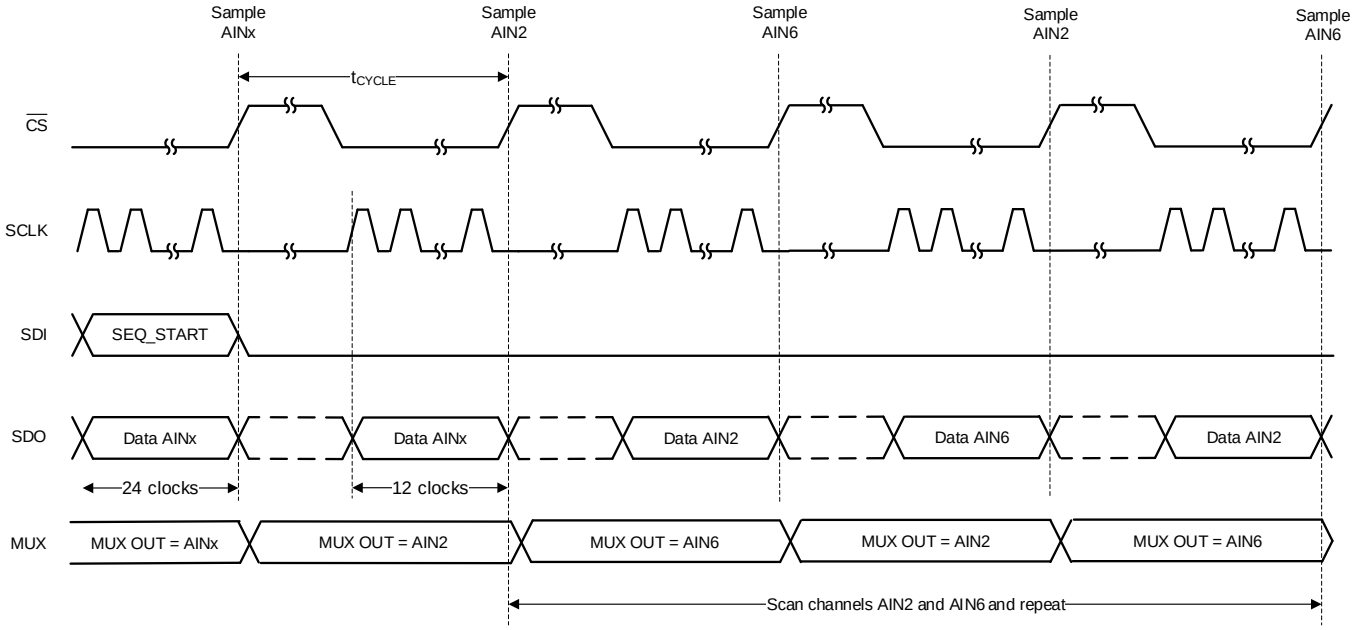

Figure 14. Starting Conversions and Reading Data in Auto-Sequence Mode

ADVANCE INFORMATION

7.5 TLA2518 Registers

Table 7 lists the TLA2518 registers. All register offset addresses not listed in Table 7 should be considered as reserved locations and the register contents should not be modified.

Table 7. TLA2518 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]
0x1	GENERAL_CFG		GENERAL_CFG Register (Address = 0x1) [reset = 0x0]
0x2	DATA_CFG		DATA_CFG Register (Address = 0x2) [reset = 0x0]
0x3	OSR_CFG		OSR_CFG Register (Address = 0x3) [reset = 0x0]
0x4	OPMODE_CFG		OPMODE_CFG Register (Address = 0x4) [reset = 0x0]
0x5	PIN_CFG		PIN_CFG Register (Address = 0x5) [reset = 0x0]
0x7	GPIO_CFG		GPIO_CFG Register (Address = 0x7) [reset = 0x0]
0x9	GPO_DRIVE_CFG		GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]
0xB	GPO_OUTPUT_VALUE		GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]
0xD	GPI_VALUE		GPI_VALUE Register (Address = 0xD) [reset = 0x0]
0x10	SEQUENCE_CFG		SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]
0x11	CHANNEL_SEL		CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]
0x12	AUTO_SEQ_CH_SEL		AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

Complex bit access types are encoded to fit into small table cells. Table 8 shows the codes that are used for access types in this section.

Table 8. TLA2518 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

7.5.1 SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]

SYSTEM_STATUS is shown in Figure 15 and described in Table 9.

Return to the Summary Table.

Figure 15. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	RESERVED		OSR_DONE	CRCERR_FUSE	RESERVED	BOR
R-1b	R-0b	R-0b		R/W-0b	R-0b	R-0b	R/W-1b

Table 9. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5-4	RESERVED	R	0b	Reserved. Reads return 0b.
3	OSR_DONE	R/W	0b	Averaging status. Clear this bit by writing 1b to this bit. 0b = Averaging in progress or not started; average result is not ready. 1b = Averaging complete; average result is ready.
2	CRCERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	RESERVED	R	0b	Reserved. Reads return 0b.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out from the last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

7.5.2 GENERAL_CFG Register (Address = 0x1) [reset = 0x0]

GENERAL_CFG is shown in Figure 16 and described in Table 10.

Return to the Summary Table.

Figure 16. GENERAL_CFG Register

7	6	5	4	3	2	1	0
RESERVED					CH_RST	CAL	RST
R-0b					R/W-0b	R/W-0b	W-0b

Table 10. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0b.
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation. 1b = All channels are set as analog inputs irrespective of configuration in other registers.
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b.

ADVANCE INFORMATION

7.5.3 DATA_CFG Register (Address = 0x2) [reset = 0x0]

DATA_CFG is shown in Figure 17 and described in Table 11.

Return to the Summary Table.

Figure 17. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED		CPOL_CPHA[1:0]	
R/W-0b	R-0b	R/W-0b		R-0b		R/W-0b	

Table 11. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device outputs fixed data bits which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A repeatitively when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0b.
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = Reserved. 11b = Reserved.
3-2	RESERVED	R	0b	Reserved. Reads return 0b.
1-0	CPOL_CPHA[1:0]	R/W	0b	This field sets the polarity and phase of SPI communication. 0b = CPOL = 0, CPHA = 0. 1b = CPOL = 0, CPHA = 1. 10b = CPOL = 1, CPHA = 0. 11b = CPOL = 1, CPHA = 1.

7.5.4 OSR_CFG Register (Address = 0x3) [reset = 0x0]

OSR_CFG is shown in Figure 18 and described in Table 12.

Return to the Summary Table.

Figure 18. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED						OSR[2:0]	
R-0b						R/W-0b	

Table 12. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0b.
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

7.5.5 OPMODE_CFG Register (Address = 0x4) [reset = 0x0]

OPMODE_CFG is shown in Figure 19 and described in Table 13.

Return to the Summary Table.

Figure 19. OPMODE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			OSC_SEL	CLK_DIV[3:0]			
R-0b			R/W-0b	R/W-0b			

Table 13. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0b.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Refer to section on oscillator and timing control for details.

7.5.6 PIN_CFG Register (Address = 0x5) [reset = 0x0]

PIN_CFG is shown in Figure 20 and described in Table 14.

Return to the Summary Table.

Figure 20. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

Table 14. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN / GPIO [7:0] as analog inputs or GPIOs. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

7.5.7 GPIO_CFG Register (Address = 0x7) [reset = 0x0]

GPIO_CFG is shown in Figure 21 and described in Table 15.

Return to the Summary Table.

Figure 21. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

Table 15. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

ADVANCE INFORMATION

7.5.8 GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]

GPO_DRIVE_CFG is shown in Figure 22 and described in Table 16.

Return to the Summary Table.

Figure 22. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

Table 16. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

7.5.9 GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]

GPO_OUTPUT_VALUE is shown in Figure 23 and described in Table 17.

Return to the Summary Table.

Figure 23. GPO_OUTPUT_VALUE Register

7	6	5	4	3	2	1	0
GPO_OUTPUT_VALUE[7:0]							
R/W-0b							

Table 17. GPO_OUTPUT_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_OUTPUT_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

7.5.10 GPI_VALUE Register (Address = 0xD) [reset = 0x0]

GPI_VALUE is shown in Figure 24 and described in Table 18.

Return to the Summary Table.

Figure 24. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

Table 18. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on channels configured digital inputs. 0b = Digital input is at logic 0. 1b = Digital input is at logic 1.

7.5.11 SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE_CFG is shown in Figure 25 and described in Table 19.

Return to the Summary Table.

Figure 25. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

Table 19. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0b.
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved. Reads return 0b.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by AUTO_SEQ_CH_SEL. 10b = On-the-fly sequence mode. 11b = Reserved.

7.5.12 CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL_SEL is shown in Figure 26 and described in Table 20.

Return to the Summary Table.

Figure 26. CHANNEL_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

Table 20. CHANNEL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved. Reads return 0b.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 1xxx = Reserved. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7

7.5.13 AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

AUTO_SEQ_CH_SEL is shown in Figure 27 and described in Table 21.

Return to the Summary Table.

Figure 27. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

Table 21. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register analog-to-digital converter (SAR ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the TLA2518.

8.2 Typical Applications

8.2.1 Mixed-Channel Configuration

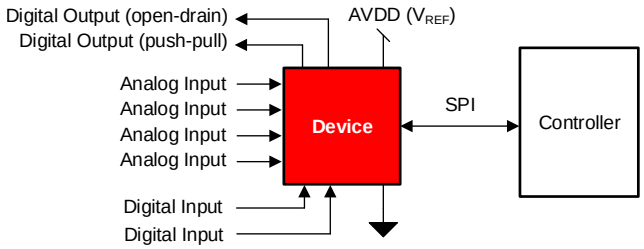

Figure 28. DAQ Circuit: Single-Supply DAQ

8.2.1.1 Design Requirements

The goal of this application is to configure some channels of the TLA2518 as digital inputs, open-drain digital outputs, and push-pull digital outputs.

8.2.1.2 Detailed Design Procedure

The TLA2518 can support GPIO functionality at each input pin. Any analog input pin can be independently configured as a digital input, a digital open-drain output, or a digital push-pull output though the PIN_CFG and GPIO_CFG registers; see Table 2.

8.2.1.2.1 Digital Input

The digital input functionality can be used to monitor a signal within the system. Figure 29 illustrates that the state of the digital input can be read from the GPI_VALUE register.

ADVANCE INFORMATION

Typical Applications (continued)

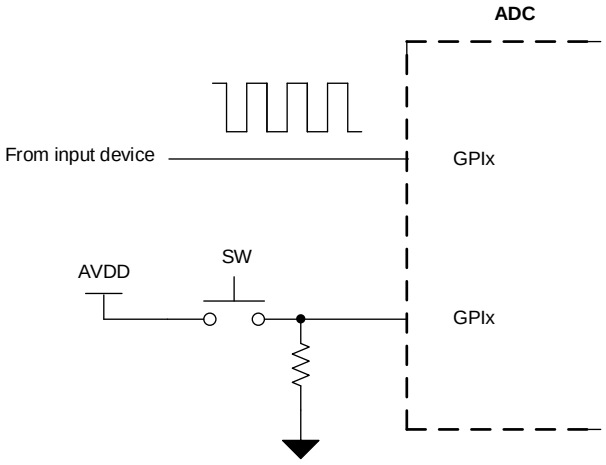

Figure 29. Digital Input

8.2.1.2.2 Digital Open-Drain Output

The channels of the TLA2518 can be configured as digital open-drain outputs supporting an output voltage up to 5.5 V. An open-drain output, as shown in Figure 30, consists of an internal FET (Q) connected to ground. The output is idle when not driven by the device, which means Q is off and the pullup resistor, R_{PULL_UP}, connects the GPOx node to the desired output voltage. The output voltage can range anywhere up to 5.5 V, depending on the external voltage that the GPIOx is pulled up to. When the device is driving the output, Q turns on, thus connecting the pullup resistor to ground and bringing the node voltage at GPOx low.

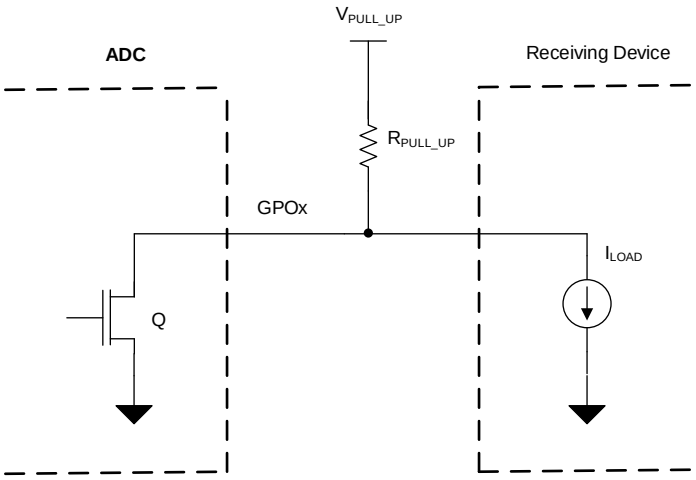

Figure 30. Digital Open-Drain Output

The minimum value of the pullup resistor, as calculated in Equation 3, is given by the ratio of V_{PULL_UP} and the maximum current supported by the device digital output (5 mA).

$$R_{MIN} = (V_{PULL\_UP} / 5\ mA) \quad (3)$$

The maximum value of the pullup resistor, as calculated in Equation 4, depends on the minimum input current requirement, I_{LOAD}, of the receiving device driven by this GPIO.

$$R_{MAX} = (V_{PULL\_UP} / I_{LOAD}) \quad (4)$$

Select R_{PULL_UP} such that $R_{MIN} < R_{PULL\_UP} < R_{MAX}$.

Typical Applications (continued)

8.2.2 Digital Push-Pull Output Configuration

The channels of the TLA2518 can be configured as digital push-pull outputs supporting an output voltage up to AVDD. As shown in Figure 31, a push-pull output consists of two mirrored opposite bipolar transistors, Q1 and Q2. The device can both source and sink current because only one transistor is on at a time (either Q2 is on and pulls the output low, or Q1 is on and sets the output high). A push-pull configuration always drives the line opposed to an open-drain output where the line is left floating.

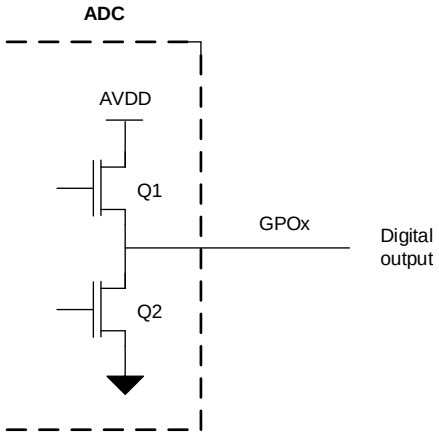

Figure 31. Digital Push-Pull Output

9 Power Supply Recommendations

9.1 AVDD and DVDD Supply Recommendations

The TLA2518 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. For supplies greater than 2.35 V, AVDD and DVDD can be shorted externally if single-supply operation is desired. The AVDD supply also defines the full-scale input range of the device. Decouple the AVDD and DVDD pins individually, as shown in Figure 32, with 1-µF ceramic decoupling capacitors. The minimum capacitor value required for AVDD and DVDD is 200 nF and 20 nF, respectively. If both supplies are powered from the same source, a minimum capacitor value of 220 nF is required for decoupling.

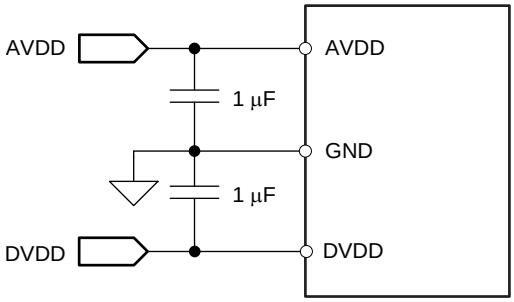

Figure 32. Power-Supply Decoupling

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Figure 33 shows a board layout example for the TLA2518. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the AVDD supply away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect the GND pin to the ground plane using short, low-impedance paths. The AVDD supply voltage also functions as the reference voltage for the TLA2518. Place the decoupling capacitor (C_{REF}) for AVDD close to the device AVDD and GND pins and connect C_{REF} to the device pins with thick copper tracks.

10.2 Layout Example

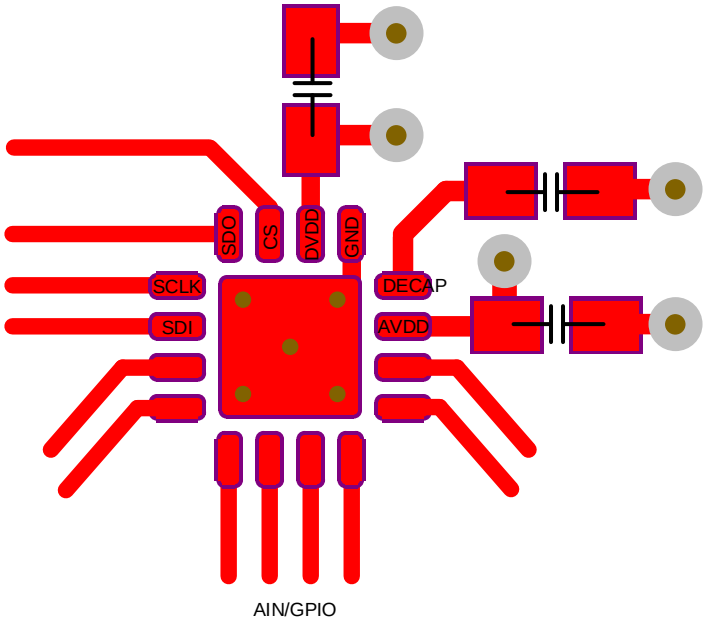

Figure 33. Example Layout

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLA2518IRTER	PREVIEW	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 85		
TLA2518IRTET	PREVIEW	WQFN	RTE	16	250	TBD	Call TI	Call TI	-40 to 85		
XTLA2518IRTER	ACTIVE	WQFN	RTE	16	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

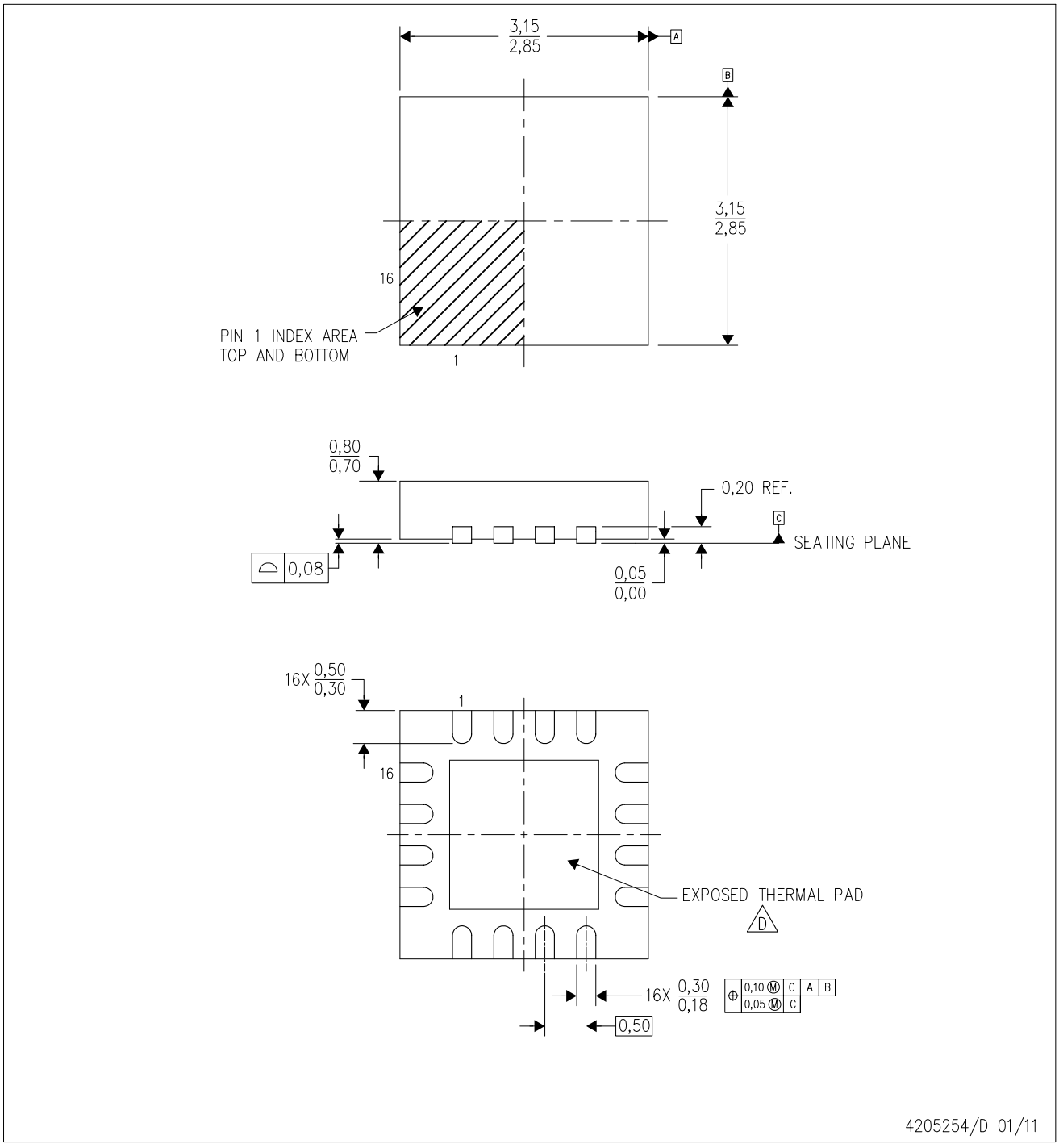
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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