TEA2017AAT/2

Digital configurable LLC and multimode PFC controller

Rev. 1.2 — 31 July 2023   Product data sheet

1   General description

The TEA2017AAT is a digital configurable LLC and PFC combo controller for high-efficiency resonant power supplies. It includes the LLC controller and PFC controller functionality. The PFC can be configured to operate in DCM/QR, CCM fixed frequency, or multimode which supports all operation modes to optimize the PFC efficiency. The TEA2017AAT enables building a complete resonant power supply which is easy to design and has a very low component count. The TEA2017AAT comes in a low profile and narrow body-width SO16 package.

The TEA2017AAT digital architecture is based on a high-speed configurable hardware state machine ensuring very reliable real-time performance. During the power supply development, many operation and protection settings of the LLC and PFC controller can be adjusted by loading new settings into the device to meet specific application requirements. The configurations can be fully secured to prevent unauthorized copying of the proprietary TEA2017AAT configuration content.

In contrast to traditional resonant topologies, the TEA2017AAT shows a very high efficiency at low loads due to the LLC low-power mode. This mode operates in the power region between continuous switching (also called high-power mode) and burst mode.

Because the TEA2017AAT regulates the LLC output voltage of the system via the primary capacitor voltage, it has accurate information about the power delivered to the output. This measured output power defines the mode of operation (burst mode, low-power mode, or high-power mode). The transition levels of the operating modes can be easily programmed into the device.

The TEA2017AAT contains all protections like overtemperature protection (OTP), overcurrent protection (OCP), overvoltage protection (OVP), overpower protection (OPP), open-loop protection (OLP), and capacitive mode regulation (CMR). Each of these protections can be configured independently and accurately by programming parameters inside the device.

The device contains both a low-voltage and high-voltage silicon technology for high-voltage start-up, integrated drivers, level shifter, protections, and circuitry assuring zero-voltage switching.

The TEA2017AAT/TEA2095T combination gives an easy to design, highly efficient, and reliable power supply, providing 90 W to 1000 W, with a minimum of external components. The system provides a very low no-load input power (< 75 mW; total system including the TEA2017AAT/TEA2095T combination) and high efficiency from minimum to maximum load. This power supply meets the efficiency regulations of Energy Star, the Department of Energy, the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. So, any auxiliary low-power supply can be omitted.

To enhance readability, only typical values are given in this document, except in the parametric tables (Section 9, Section 10, and Section 11). If values in the text differ from the values for the same parameter in the parametric tables, the values in these tables are leading.

2 Features and benefits

2.1 Distinctive features

- Complete functionality of a PFC and LLC controller in a single small-size SO16 package
- Integrated high-voltage start-up
- Integrated drivers and high-voltage level shifter (LS)
- High-side driver directly supplied from the low-side driver output
- Accurate boost voltage regulation
- PFC can be configured to operate in:
  – DCM/QR
  – DCM/QR/CCM (also called multimode operation)
  – CCM fixed frequency
- Integrated X-capacitor discharge without additional external components
- Power good function
- PFC jitter for optimized EMI performance
- Excellent power factor (PF) and total harmonic distortion (THD), as the PFC current compensates for the input filter current
- Several parameters can easily be configured during evaluation with use of the graphical user interface (GUI), like:
  – Operating frequencies to be outside the audible area at all operating modes
  – Soft start and soft stop in burst mode, reducing the audible noise
  – Accurate transition levels between operation modes (high-power mode/low-power mode/burst mode)
  – Enabling/disabling the lower power mode

2.2 Green features

- Valley/zero voltage switching for minimum switching losses
- Extremely high efficiency from low load to high load
- Compliant with latest energy-saving standards and directives (Energy Star, EuP)
- Excellent no-load input power (< 75 mW for TEA2017AAT/TEA2095T combination)

2.3 Protection features

- Independently configurable levels and timers
- Many protections can independently be set to latched, safe restart, or latched after several attempts to restart.
- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- Internal and external overtemperature protection (OTP)
- Capacitive mode regulation (CMR)
- Accurate overvoltage protection (OVP)
- Overcurrent protection (OCP)
- Inrush current protection (ICP)
- Brownin/brownout protection
- Disable input

3 Applications

- Desktop and all-in-one PCs
- Gaming power supplies
- LCD television
- Notebook adapters and general-purpose adapters
- Printers
- Server
- 5G supplies
- UHD LED television

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	**Description**	**Version**
TEA2017AAT/2	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

5 Marking

Table 2. Marking codes

Type number	Marking code
TEA2017AAT/2	TEA2017AAT

TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

3 / 66

6   Block diagram

Figure 1. Block diagram

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Product data sheet

Rev. 1.2 — 31 July 2023

4 / 66
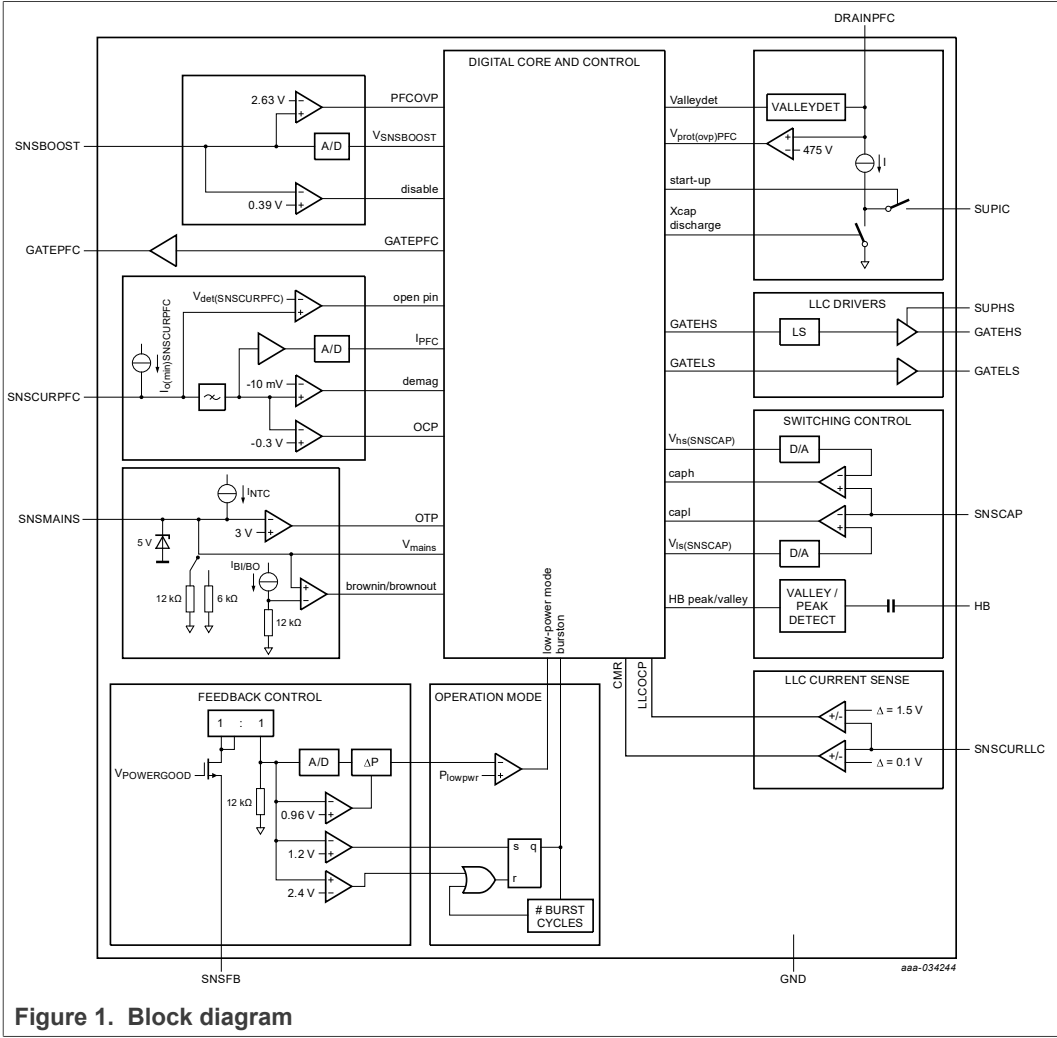
7 Pinning information

7.1 Pinning

Figure 2. TEA2017AAT pin configuration (SOT109-1)
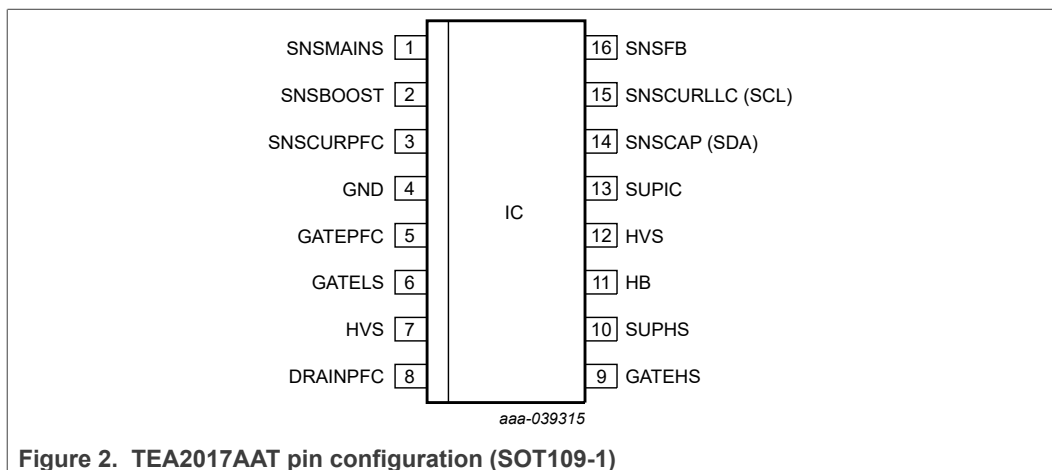
7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
SNSMAINS	1	sense input for mains voltage and external temperature
SNSBOOST	2	sense input for boost voltage; externally connected to resistive-divided boost voltage
SNSCURPFC	3	PFC current sense input
GND	4	ground
GATEPFC	5	PFC MOSFET gate driver output
GATELS	6	LLC low-side MOSFET gate driver output and supply for bootstrap capacitor
HVS	7	high-voltage spacer. Not to be connected.
DRAINPFC	8	internal HV start-up source also used for X- capacitor discharge, valley detection, and PFC OVP detection; connected to (PFC) drain voltage
GATEHS	9	LLC high-side MOSFET gate driver output
SUPHS	10	high-side driver supply input; externally connected to bootstrap capacitor (C_{SUPHS})
HB	11	low-level reference for high-side driver and input for half-bridge slope detection; externally connected to half-bridge node HB between the LLC MOSFETs
HVS	12	high-voltage spacer. Not to be connected.
SUPIC	13	input supply voltage and output of internal HV start-up source; externally connected to an auxiliary winding of the LLC via a diode or to an external DC supply
SNSCAP	14	LLC capacitor voltage sense input; externally connected to divider across LLC capacitor

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Product data sheet

Rev. 1.2 — 31 July 2023

5 / 66

Table 3. Pin description...*continued*

Symbol	Pin	Description
SNSCURLLC	15	LLC current sense input; externally connected to the resonant current sense resistor
SNSFB	16	output voltage regulation feedback sense input; externally connected to an optocoupler. Output for power good function.

TEA2017AAT_2

Product data sheet

Rev. 1.2 — 31 July 2023

6 / 66

8 Functional description

8.1 Supply voltages

The TEA2017AAT includes:

- A high-voltage supply pin for start-up (DRAINPFC)
- A general supply to be connected to an external auxiliary winding (SUPIC pin)
- A floating supply for the high-side driver (SUPHS pin)

8.1.1 Start-up and supply voltage

Initially, the capacitor on the SUPIC pin is charged via the DRAINPFC pin. The DRAINPFC pin is connected to the drain voltage of the PFC MOSFET. Internally, a high-voltage current source is located between the DRAINPFC pin and the SUPIC pin (see Figure 3).
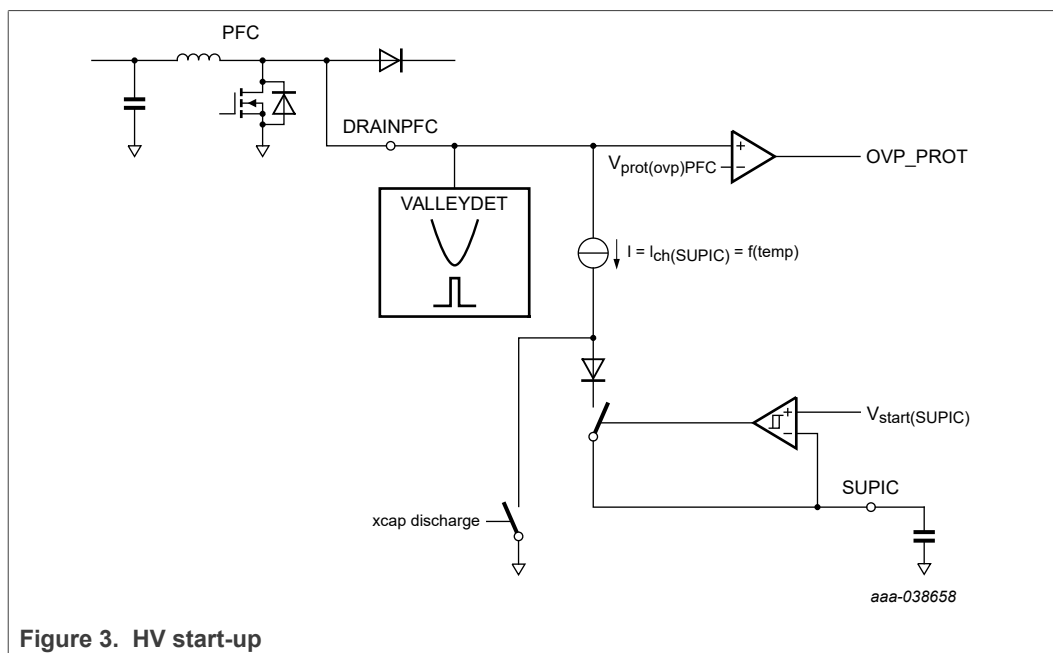
Figure 3. HV start-up

The maximum current of the internal current source is limited to $I_{ch(SUPIC)}$. To limit the IC dissipation, the charge current is reduced when the current source exceeds its maximum temperature.

At start-up, when the SUPIC reaches the $V_{start(SUPIC)}$ level, it is continuously regulated to this start level with a hysteresis ($V_{start(hys)SUPIC}$).
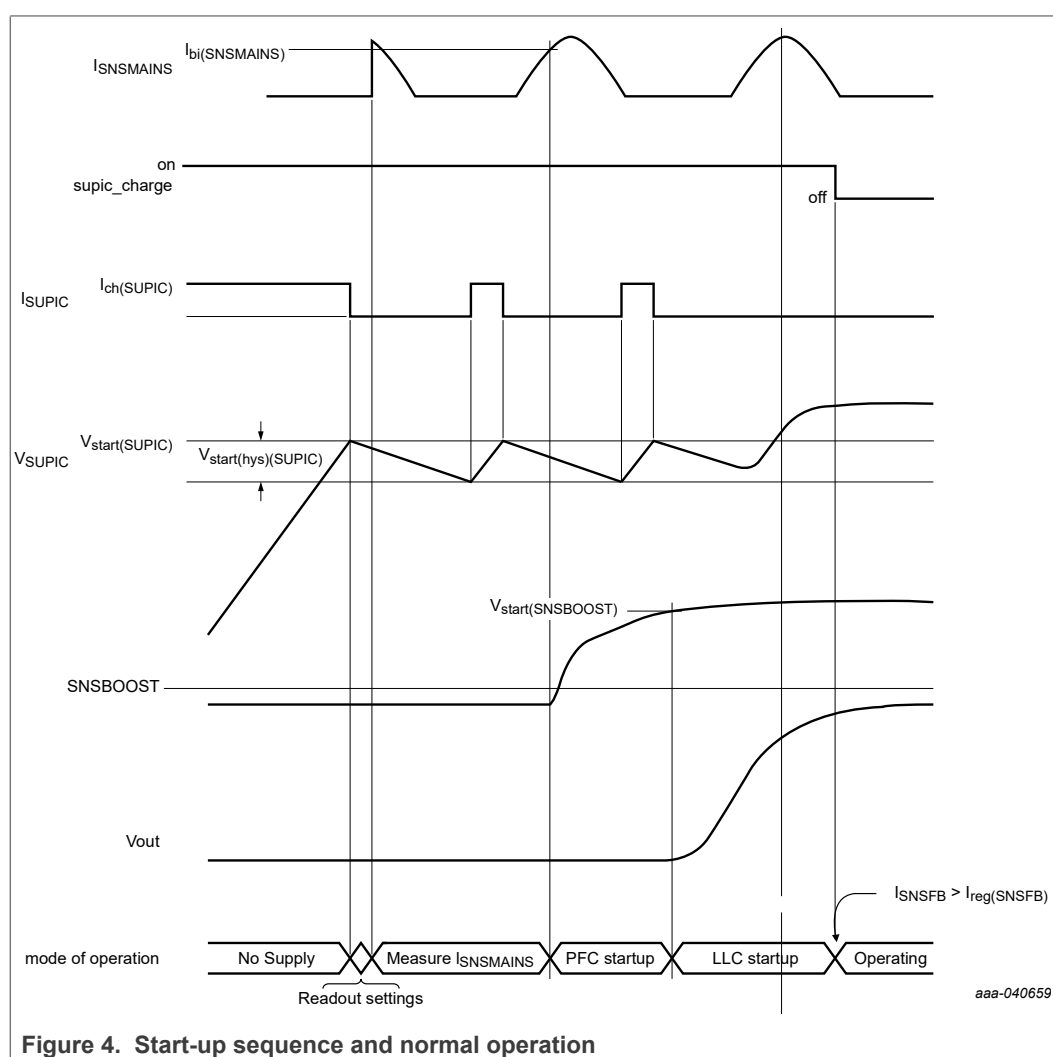
When the start level is reached, it reads the internal MTP (multi-time programmable memory) and defines the settings.

When the settings have been defined, the PFC starts up. When the SNSBOOST reaches the minimum level $V_{start(SNSBOOST)}$, the LLC also starts switching (see Figure 4 and Figure 5).

When start-up is complete and the LLC controller is operating, the LLC transformer auxiliary winding supplies the SUPIC pin. In this operational state, the HV start-up source is disabled.

TEA2017AAT_2

Product data sheet

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Rev. 1.2 — 31 July 2023

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7 / 66

When the system enters the protection mode, it cannot be supplied via the auxiliary winding. So, the SUPIC pin is regulated to $V_{start(SUPIC)}$ via the DRAINPFC pin.

During the non-switching period of the burst mode, the SUPIC is regulated to the $V_{low(SUPIC)}$ when SUPIC drops to below this level. It regulates the voltage with a hysteresis of $V_{low(hys)SUPIC}$. In this way, the system avoids that the SUPIC undervoltage protection ($V_{uvp(SUPIC)}$) is triggered because of a long non-switching period in burst mode. However, the system must be designed such that the internal current source at the DRAINPFC pin is only active at start-up and extreme output voltage overshoots, followed by a long time of non-switching. Continuous use of this current source increases the input power and affects the lifetime of the product. The DRAINPFC pin is also used for valley detection, for X-capacitor discharge, and for providing a second PFC OVP protection.
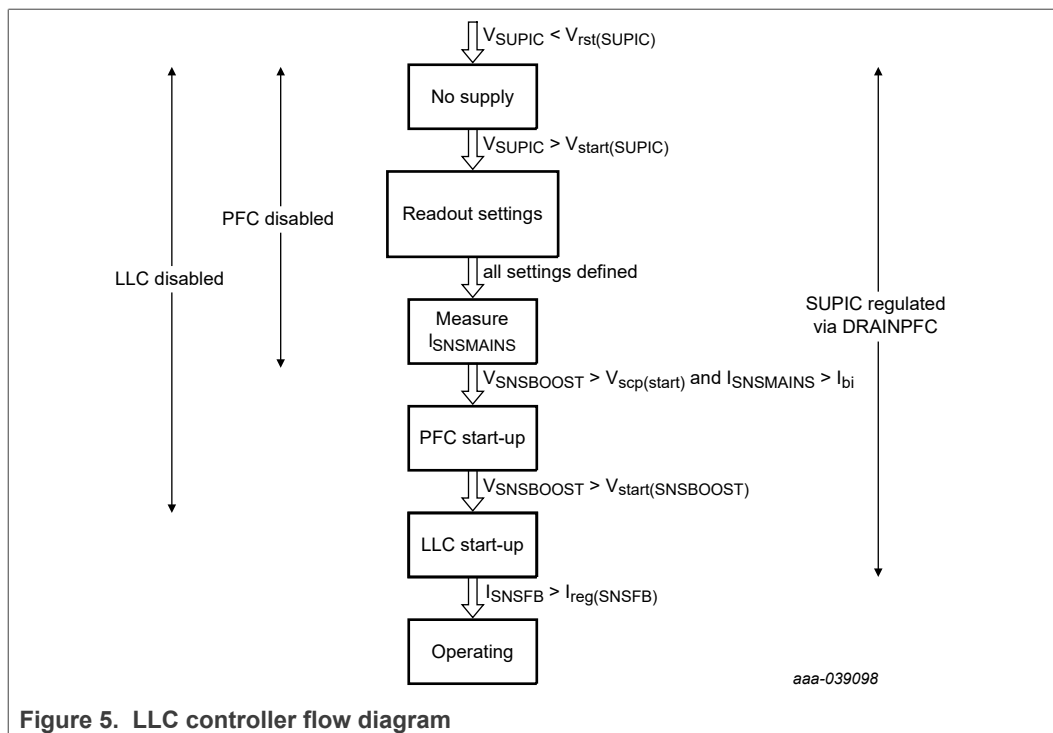

Figure 4. Start-up sequence and normal operation

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Product data sheet

Rev. 1.2 — 31 July 2023

8 / 66

Figure 5. LLC controller flow diagram

When the SUPIC voltage drops to below $V_{rst(SUPIC)}$, the TEA2017AAT restarts.

8.1.2 High-side driver-floating supply (SUPHS pin)

As the voltage range on the SUPIC pin exceeds that of the maximum external MOSFETs gate-source voltage, the external bootstrap capacitor C_{SUPHS} cannot directly be supplied from the SUPIC.

To provide an external supply for the high-side driver without the need of additional external components, the GateLS output is designed such that it can drive the low-side MOSFET and supply the high-side MOSFET (see Figure 6).

a. Curves   b. Circuit

Figure 6. High-side driver supply
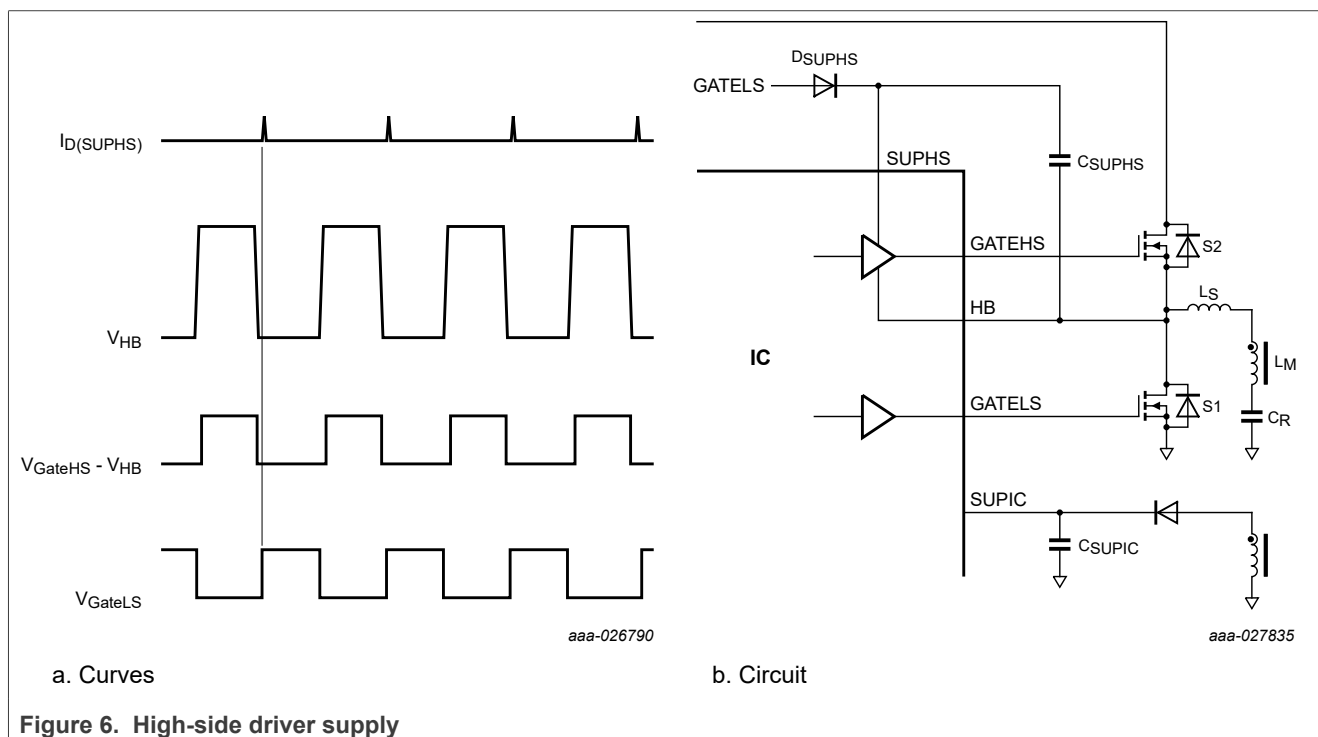
The external bootstrap buffer capacitor C_{SUPHS} supplies the high-side driver. The bootstrap capacitor is connected to the low-side driver supply, the GATELS pin, and the half-bridge node (HB) via an external diode (D_{SUPHS}). When GATELS is active high and the HB node is pulled low, C_{SUPHS} is charged.

Careful selection of the appropriate diode minimizes the voltage drop between the GATELS and SUPHS pins, especially when large MOSFETs and high switching frequencies are used. A great voltage drop across the diode reduces the gate drive of the high-side MOSFET.

8.2 LLC system regulation

The TEA2017AAT regulates the output power by adjusting the voltage across the primary capacitor. Compared to a standard frequency control loop, it has the advantage that the control loop has a constant gain and the IC has information about the output power. So, the operation mode transition levels are derived from the output power.

Although the TEA2017AAT uses the primary capacitor voltage as a regulation parameter, all application values, like the resonant inductances, resonant capacitor, and primary MOSFETs remain unchanged compared to a frequency-controlled LLC converter. A secondary TL431 circuitry with an optocoupler connected to the primary SNSFB pin continuously regulates the output voltage.

8.2.1 Output power regulation loop

Figure 7 shows the output power regulation loop of V_{cap} control as used by the TEA2017AAT. Figure 8 shows a corresponding timing diagram.

Figure 7. Regulation loop V_{cap} control

Figure 8. Timing diagram of the regulation loop
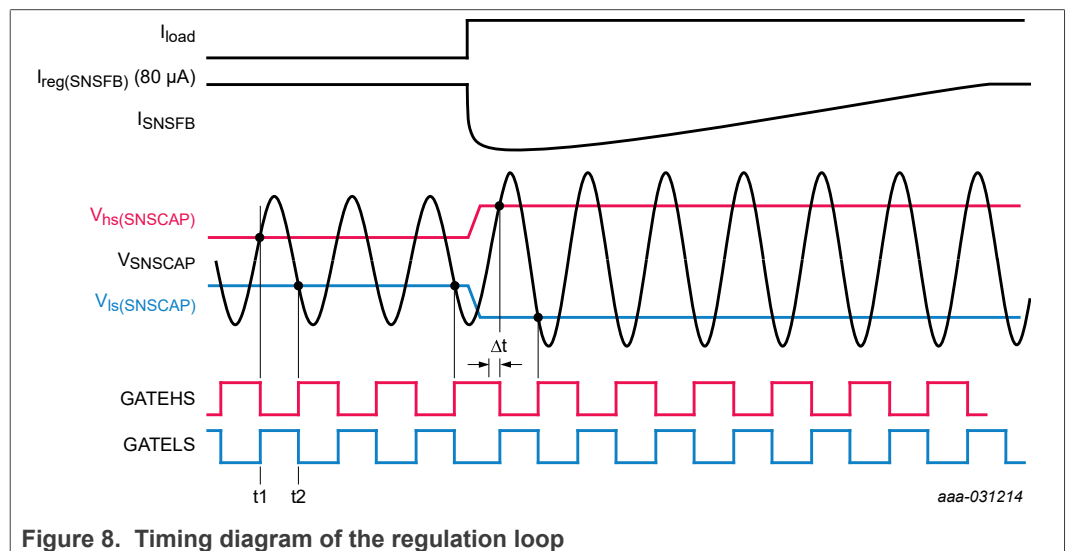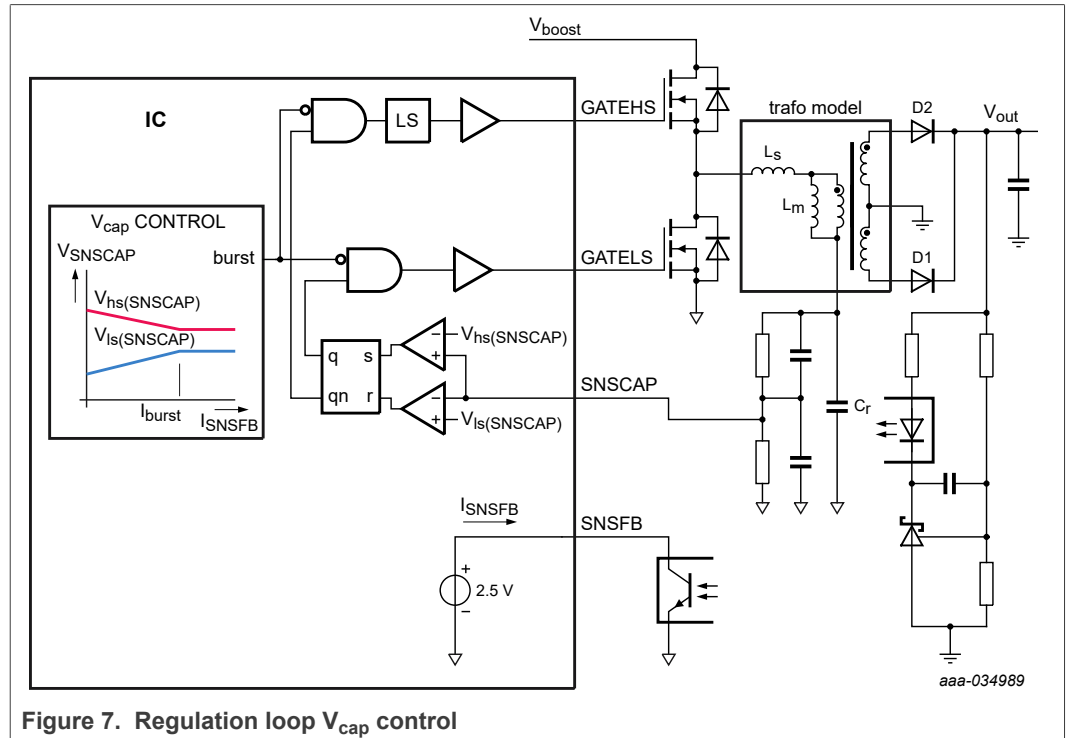
When the divided resonant capacitor voltage (V_{SNSCAP}) exceeds the capacitor voltage high level ($V_{hs(SNSCAP)}$), the high-side MOSFET is switched off (see Figure 8 (t1)). After a short delay, the low-side MOSFET is switched on. Because of the resonant current, the resonant capacitor voltage initially increases further but eventually drops.

When the divided capacitor voltage (V_{SNSCAP}) drops to below the capacitor voltage low level ($V_{ls(SNSCAP)}$), the low-side MOSFET is switched off (see Figure 8 (t2)). After a short delay, the high-side MOSFET is switched on. Figure 8 shows that the switching frequency is a result of this switching behavior. In a frequency-controlled system, the frequency is a control parameter and the output power is a result. The TEA2017AAT regulates the power and the frequency is a result.

The difference between the high and low capacitor voltage level is a measure of the delivered output power. The value of the primary optocurrent, defined by the secondary TL431 circuitry, determines the difference between the high and low capacitor voltages.

Figure 8 also shows the behavior at a transient. If the output load increases, the current pulled out of the SNSFB pin decreases. The result is that the TEA2017AAT increases the high-level capacitor voltage and lowers the low-level capacitor voltage. The output power increases and eventually the output voltage increases to its regulation level.

To minimize no-load input power of the system, the primary current into the optocoupler is continuously regulated to $I_{reg(SNSFB)}$ (see Section 8.4).

8.2.2 Output voltage start-up

At start-up, when the system slowly increases the ΔV_{SNSCAP}, it continuously monitors the primary current via the SNSCURLLC pin. When the voltage at this pin exceeds the $V_{lmtr(ocp)}$ level, increasing the ΔV_{SNSCAP} is on hold until the voltage at the SNSCURLLC pin drops below the $V_{lmtr(ocp)}$ level again (see Figure 9). The output current is regulated and its voltage shows a nice ramp during start-up. It also avoids that during startup the OCP (overcurrent protection) is triggered. In this way, the LLC converter behaves like a limited current source during start-up.
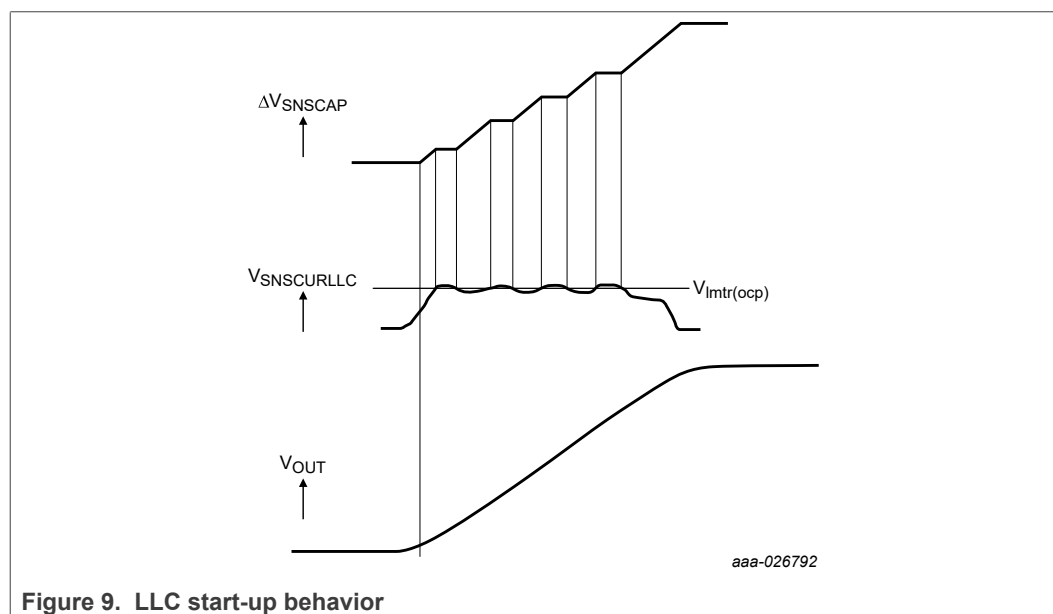

Figure 9. LLC start-up behavior

TEA2017AAT_2

Product data sheet

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Rev. 1.2 — 31 July 2023

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12 / 66

8.3 Modes of operation

Figure 10 shows the control curve between the output power and the voltage difference between the high and low capacitor voltage levels.
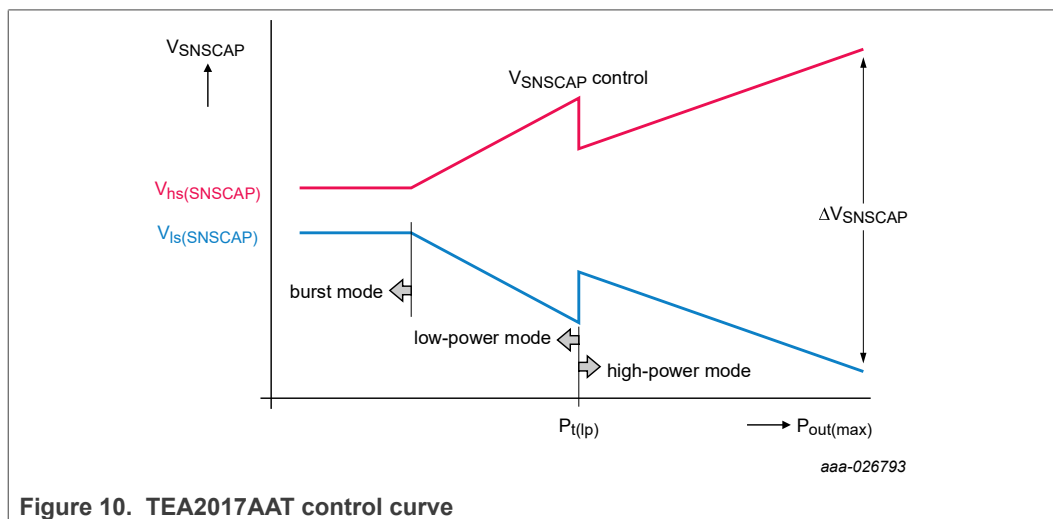

Figure 10. TEA2017AAT control curve

When the output power (P_{out}) is at its maximum, the low capacitor voltage level ($V_{ls(SNSCAP)}$) is at its minimum, and the high capacitor voltage ($V_{hs(SNSCAP)}$) is at its maximum level. The maximum ΔV_{SNSCAP} ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$), which is the divided ΔV_{Cr} voltage, corresponds to the maximum output power.

When the output load decreases, the ΔV_{SNSCAP} voltage decreases. As a result, the output power decreases and the output voltage is regulated. This mode is called high-power mode. Figure 8 shows a timing diagram of the system operating in high-power mode.

When the output power drops to below the transition level ($P_{t(lp)}$), the system enters the low-power mode. The $P_{t(lp)}$ level can be initialized via the MTP.

To compensate for the non-switching period in low-power mode, also called hold period, ΔV_{SNSCAP} is initially increased at entering the low-power mode (see Section 8.3.2). In low-power mode, the output power is regulated by adapting ΔV_{SNSCAP}, until it reaches a minimum. The system then enters the burst mode (see Section 8.3.3).

8.3.1 High-power mode

In high-power mode, the system operates as described in Section 8.2.1. Figure 11 shows a flow diagram of the high-power mode.

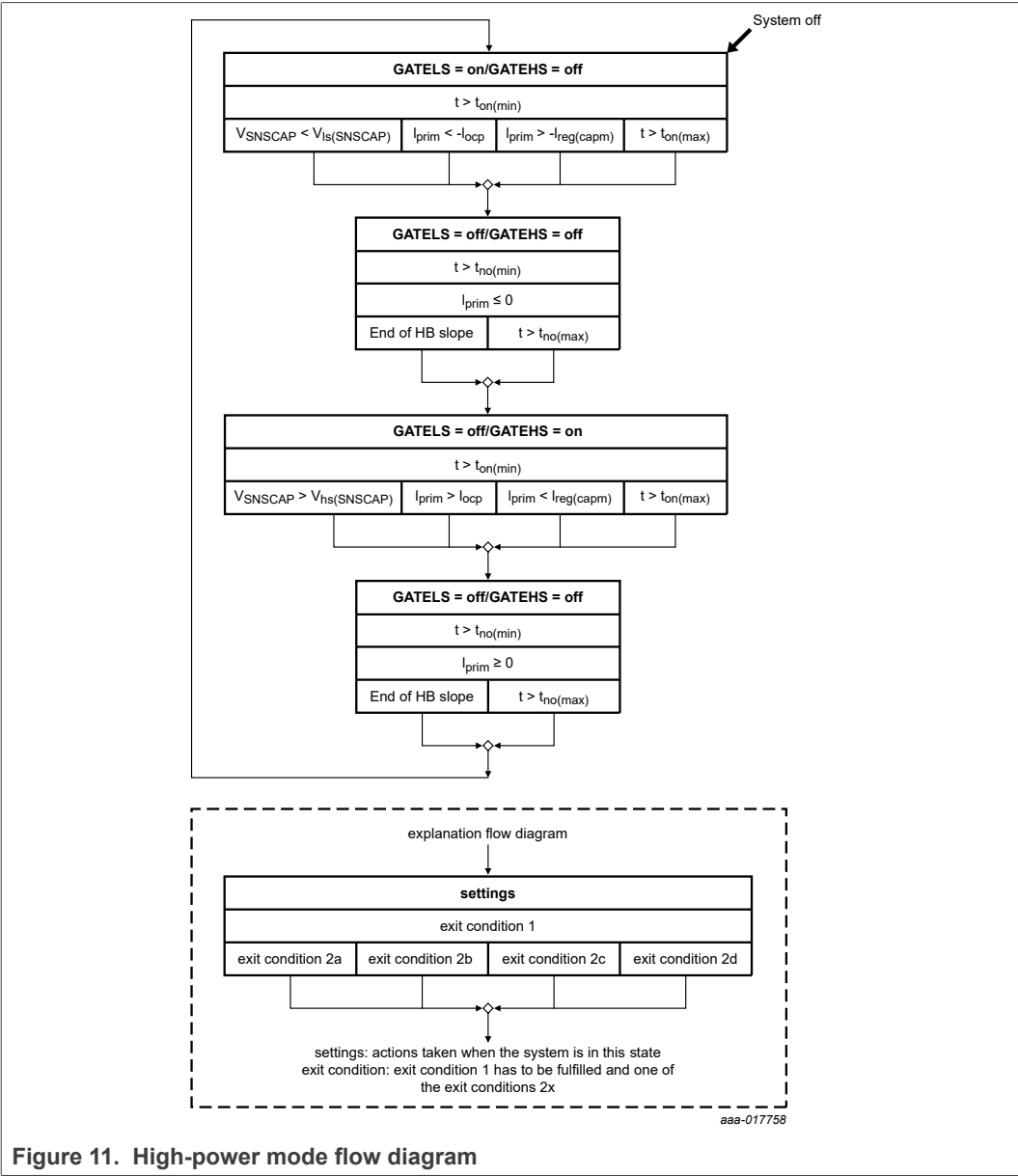**Figure 11. High-power mode flow diagram**

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Product data sheet

Rev. 1.2 — 31 July 2023

14 / 66

Initially, GATELS is on and GATEHS is off. The external bootstrap buffer capacitor (C_{SUPHS}) is charged via the GATELS pin and an external diode. The system remains in this state for at least the minimum on-time ($t_{on(min)}$) of GATELS. Before entering the next state, one of the following conditions must be fulfilled:

- The V_{SNSCAP} voltage drops to below the minimum V_{SNSCAP} voltage ($V_{ls(SNSCAP)}$)
- The measured current exceeds the OCP level (see Section 8.6.15)
- The system is close to capacitive mode (see Section 8.6.14)
- The maximum on-time ($t_{on(max)}$), a protection that maximizes the time the high-side or low-side MOSFET is kept on, is exceeded.

To avoid false detection of the HB peak voltage, the system remains in this state until the minimum non-overlap time ($t_{no(min)}$) is exceeded. When this time is exceeded and it detects the peak of the HB node and the measured resonant current is negative (or zero), it enters the next state.

If the system does not detect a peak at the HB node, it also enters the next state when the maximum non-overlap time ($t_{no(max)}$) is exceeded under the condition of a negative (or zero) resonant current.

Finally, the third and fourth states (see Figure 11) describe the GATEHS and GATEHS to GATELS transition criteria which are the inverse of the first two states.

8.3.2 Low-power mode

At low loads, the efficiency of a resonant converter drops as the magnetization and the switching losses become dominant. A low-power mode ensures high efficiency at lower loads because it reduces the magnetization and switching losses.
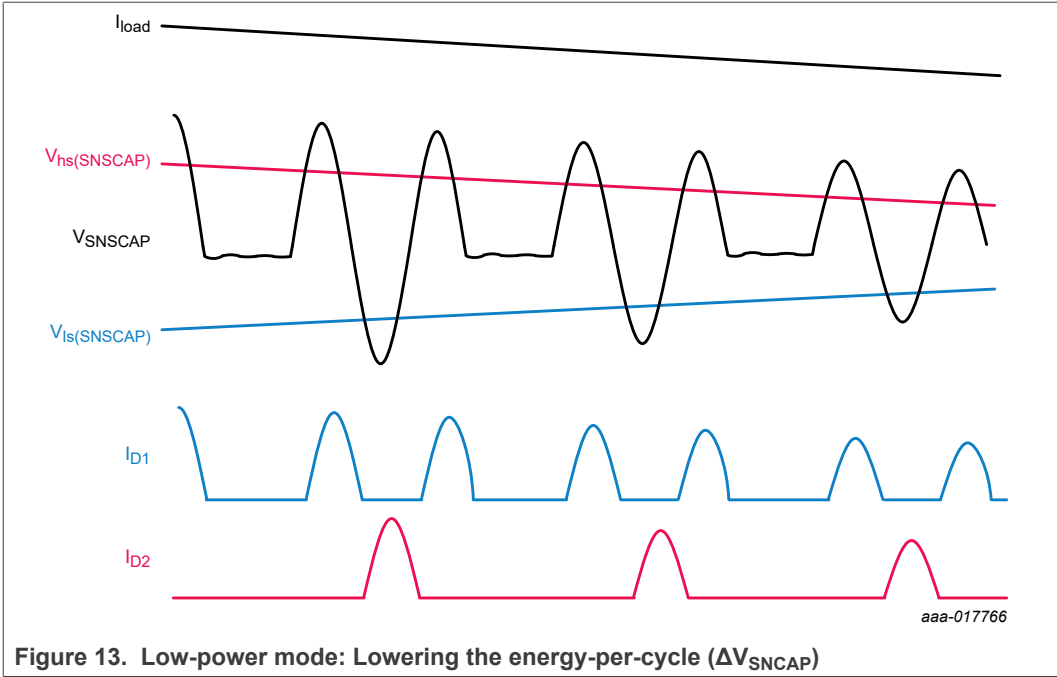
When the output power drops to below the $P_{t(lp)}$ level, the system enters the low-power mode (see Figure 10 and Figure 12). It continues switching for 3 half-cycles (low-side, high-side, low-side) with an MTP selectable duty cycle. To ensure a constant output power level, it increases the energy per cycle ($V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$) at the same time.

Figure 12. Timing diagram transition high-power mode to low-power mode
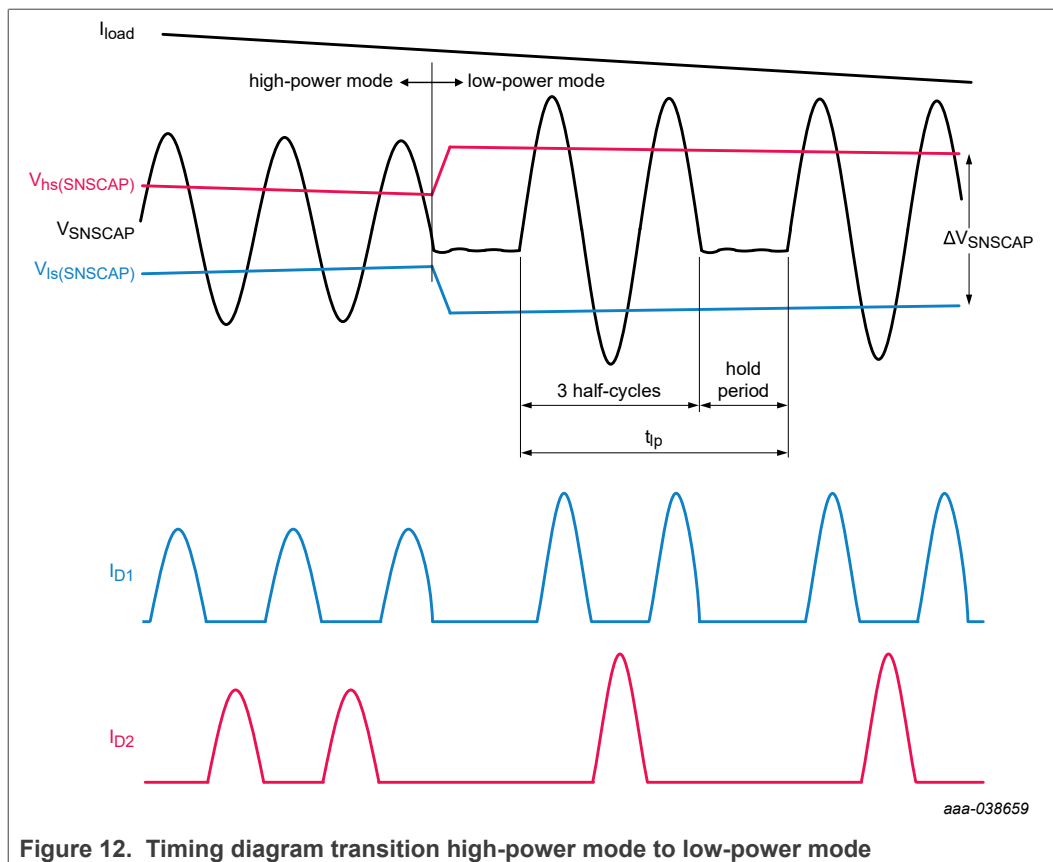
As the system continuously tracks the primary capacitor voltage, it knows exactly when to enter the "hold" period. It can also continue again at exactly the correct voltage and current levels of the resonant converter. In this way, a "hold" period can be introduced which reduces the magnetization and switching losses without any additional losses. The currents I_{D1} and I_{D2} (see Figure 12) are the secondary currents through diodes D1 and D2 (see Figure 7).

When in low-power mode the output power is further reduced, the amount of energy per cycle (= ΔV_{SNSCAP}) is reduced and the duty cycle remains the same (see Figure 13).
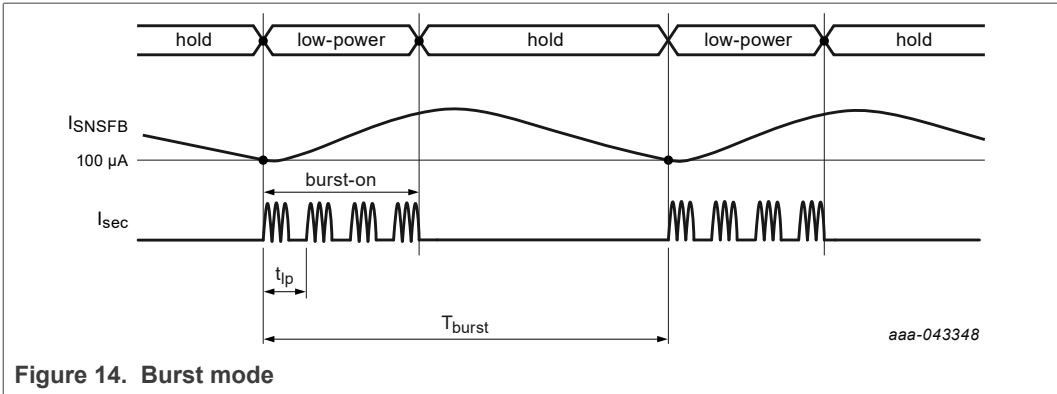
When in low-power mode the system reaches the programmable minimum energy per cycle (= ΔV_{SNSCAP}), it enters burst mode.

TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

16 / 66

Figure 13. Low-power mode: Lowering the energy-per-cycle (ΔV_{SNCAP})

8.3.3 Burst mode

In burst mode, the system alternates between operating in low-power mode and an extended hold state (see Figure 14). Because of this additional extended hold period, the magnetization and switching losses are further reduced. So, the efficiency of the system is increased.

Figure 14 shows that all operating frequencies are outside the audible area. The minimum low-power frequency can be set with a parameter. Within a low-power period, the system is switching at the resonant frequency of the converter, which is typically between 50 kHz and 200 kHz. The burst frequency ($1/T_{burst}$) can be programmed outside the audible noise area.

Figure 14. Burst mode

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Product data sheet

Rev. 1.2 — 31 July 2023

17 / 66

8.3.3.1 Frequency regulation

When the primary optocurrent (I_{SNSFB}) drops to below $I_{start(burst)}$ (100 µA typical), a new burst-on period is started. The end of the burst-on period depends on the calculated number of low-power cycles. The number of low-power cycles within a burst-on period is continuously adjusted so that the total burst period (T_{burst}) is at least the period defined by the setting (see Figure 15).

Figure 15. Burst mode: Regulating the number of low-power cycles
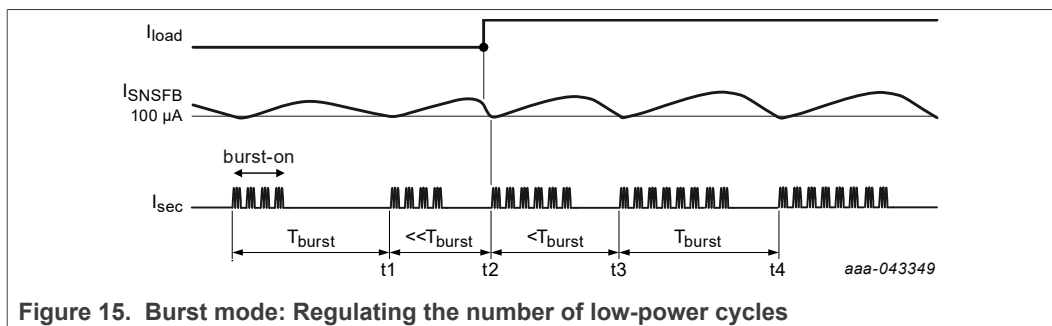
The system continuously measures the burst period from the start of the previous burst-on period to a new burst-on period. At t1, the measured burst period (T_{burst}) equals the required T_{burst}. So, the next number of low-power cycles equals the number of previous low-power cycles. At a constant output power, the system expects that when the next burst-on period has the same number of low-power cycles as the previous burst-on period, the burst period (T_{burst}) remains constant.

At a positive transient (t2), a new low-power cycle is started immediately to minimize the drop in output voltage. The measured time period, at time t2, is below the targeted burst period. The system increases the number of burst cycles. At t3, it measures the burst period again. In this example, the burst period is still below the targeted burst period. So, the system increases the number of low-power cycles again and again until the measured burst period equals the target burst period, which occurs at t4.

8.3.3.2 Negative transient response

When the system operates in burst mode, it defines the new number of cycles at the start of a new burst cycle. If the output load is reduced just after the start of a new burst cycle, the output voltage shows an overshoot (see Figure 16).
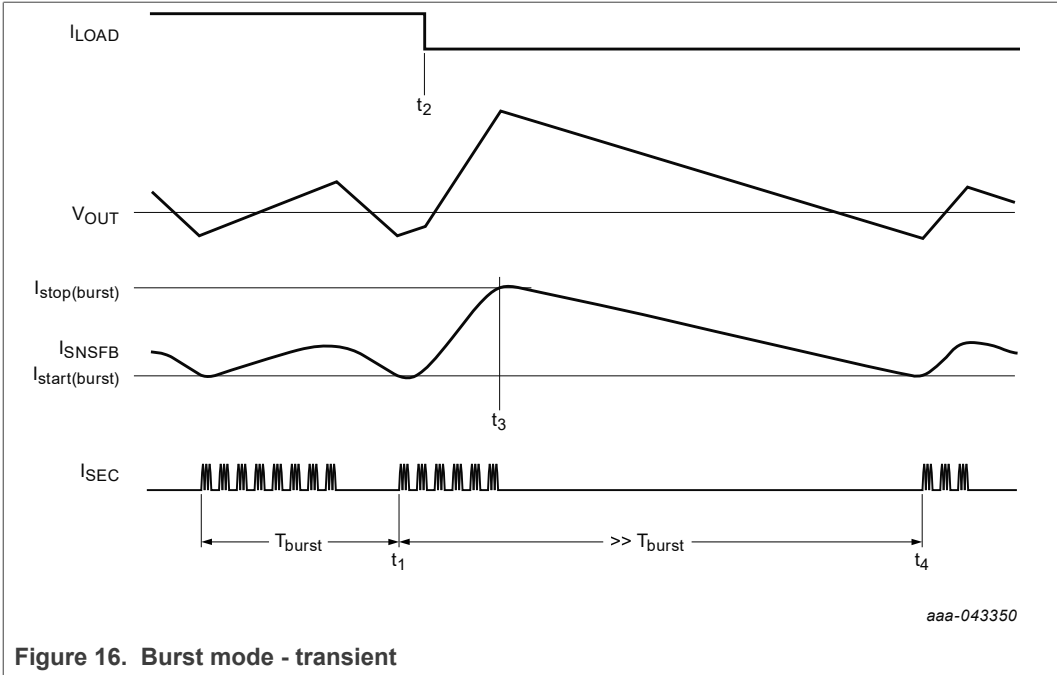
Figure 16. Burst mode - transient

At t1, the system starts with a new burst cycle period. Shortly later at t2, the output load is reduced. As a result the output voltage shows an overshoot and the optocoupler current increases. To limit the overshoot, the system also ends the burst cycle when the optocoupler current exceeds the $I_{stop(burst)}$ level.

8.3.3.3 Burst-mode delay function

When the output power drops to below the burst-mode power level, the system normally starts to operate in burst mode. If the output power is only below the burst-mode power level for a short time, to continue switching may be preferred, for example, to avoid audible noise or when using a multioutput configuration.

Entering burst mode can be delayed by using the burst-mode delay function. The output power has to be below the burst-mode power level for a minimum adjustable time then (see Figure 17).
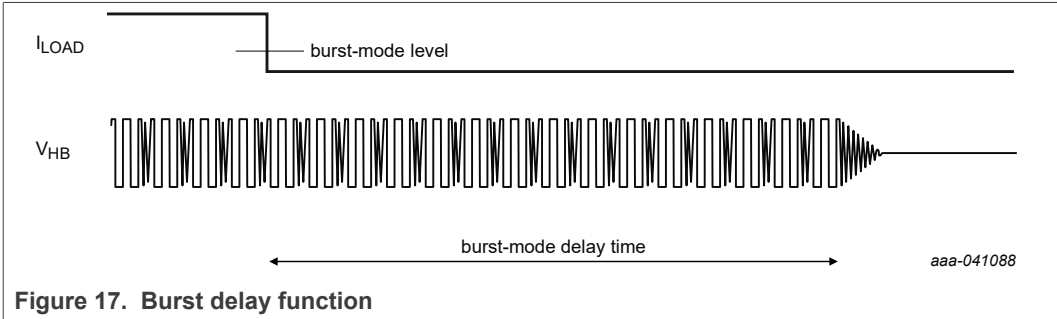

Figure 17. Burst delay function

If, during the burst-mode delay time, the output voltage cannot be regulated properly and continues to increase, the system enters burst mode anyway.

8.3.3.4 Burst-mode exit delay function

When the system is in burst mode and a positive transient occurs, it may be preferred to leave the burst mode and restart the burst-mode delay function (see Figure 18).
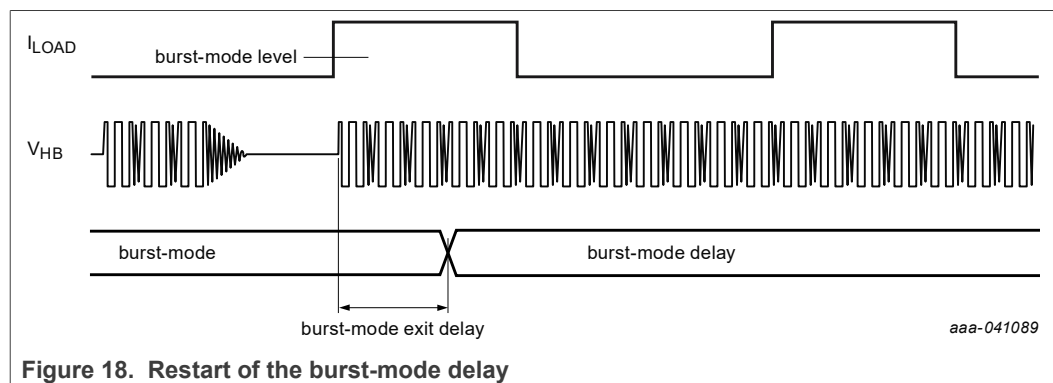

Figure 18. Restart of the burst-mode delay

When the LLC is switching for a time that exceeds the burst-mode exit delay time and the output load exceeds the burst-mode level, the system leaves the burst mode. The burst-mode delay function is activated again. The burst-mode exit delay time can be set with a parameter.

In this way, the transient response is improved at a variable load while the system was initially in burst mode.

8.4 Optobias regulation

In a typical application, the output voltage is sensed using a TL431 and connected to the SNSFB pin of the TEA2017AAT via an optocoupler (see Figure 29). Because of the behavior of the TL431, the current through the optocoupler is at the maximum level when the output power is at the minimum level. It is therefore one of the most critical parameters to achieve the required no-load input power. To achieve maximum efficiency at low load/no load, the TEA2017AAT continuously regulates the optocurrent to a low level that is independent of the output load.

Because of the parasitic capacitance at the optocoupler collector, a very low optocurrent reduces the transient response of the system. So, the TEA2017AAT applies a fixed voltage at the SNSFB pin. It measures the current through the optocoupler which defines the required output power. Via an additional internal circuitry, which adds an offset to the required output power, the optocurrent is continuously (slowly) regulated to the $I_{reg(SNSFB)}$ level (= 80 µA typical). This level is independent of the output power.

At a positive load transient, the optocurrent initially decreases (see Figure 8; I_{SNSFB}). The TEA2017AAT immediately increases the ΔV_{SNSCAP} which again increases the output power.
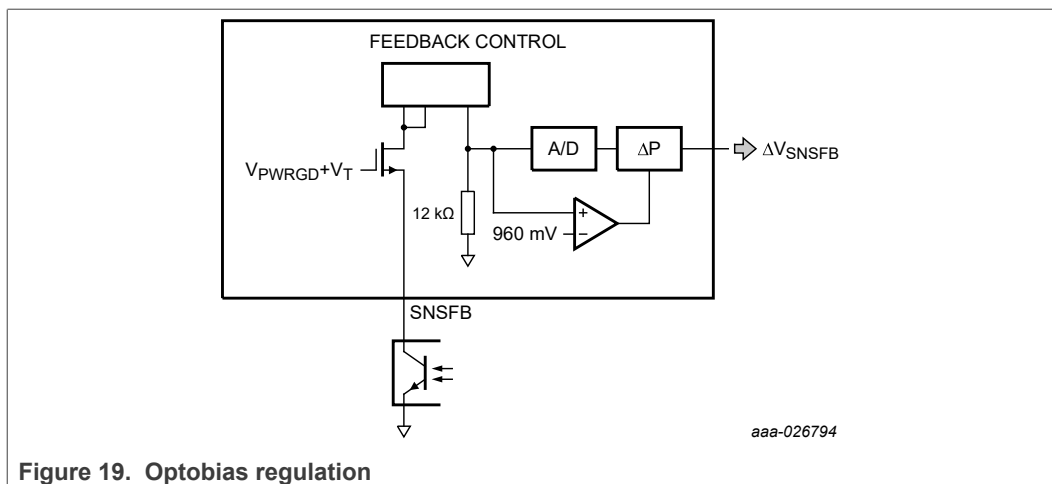
Figure 19. Optobias regulation

[Figure 19](#) shows that when the optocurrent decreases, the internal voltage across the 12 kΩ resistor drops to below the targeted level of 960 mV (= 80 μA (typical) × 12 kΩ). The TEA2017AAT then slowly increases an additional offset at the power level (ΔP). It continues to increase the additional offset until the optocurrent reaches the target of 80 μA (typical). When the optocurrent increases due to a transient, the additional offset to the power level is decreased. As a result, the output voltage decreases which again decreases the optocurrent. In this way, the optocurrent is continuously regulated to the $I_{reg(SNSFB)}$ level.

The behavior of the internal circuitry connected to the SNSFB pin is the same as the behavior of the traditional circuitry. The fixed voltage at the SNSFB pin and the continuous regulation of the optocurrent level does not influence the regulation level. The advantage, however, is a reduction in no-load input power and an optimization of the transient response.

When the system operates in low-power mode at the minimum energy per cycle and at minimum duty cycle, it can no longer reduce the optocurrent level to the $I_{reg(SNSFB)}$ target (» 80 μA typical). If the output power decreases further and the optocurrent increases to above the level of Istart(burst) (» 100 μA typical), the burst mode is triggered. When the output power drops to below this level again, a new burst cycle is started (see [Figure 14](#) and [Figure 15](#)).

8.5 Power factor correction (PFC) regulation

To achieve a high power factor (PF) and low total harmonic distortion (THD), the input current of the power supply must follow the mains input voltage. However, as the filter capacitances cause a shift of 90° between the mains input current and its voltage, the input filter disrupts PF and THD. To improve PF and THD, the average PFC current is in accordance with a shifted sine wave (see [Figure 20](#)).
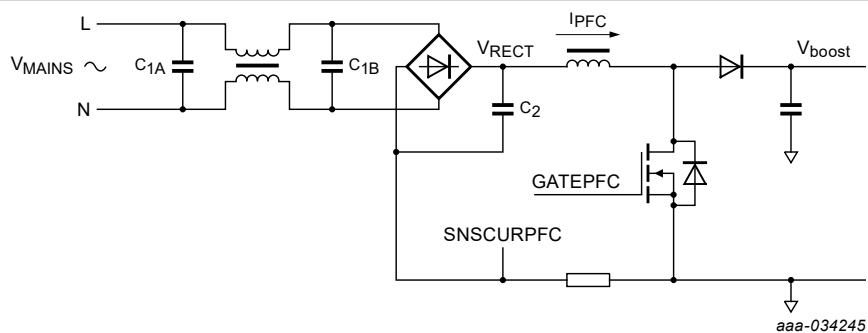
a. Circuit
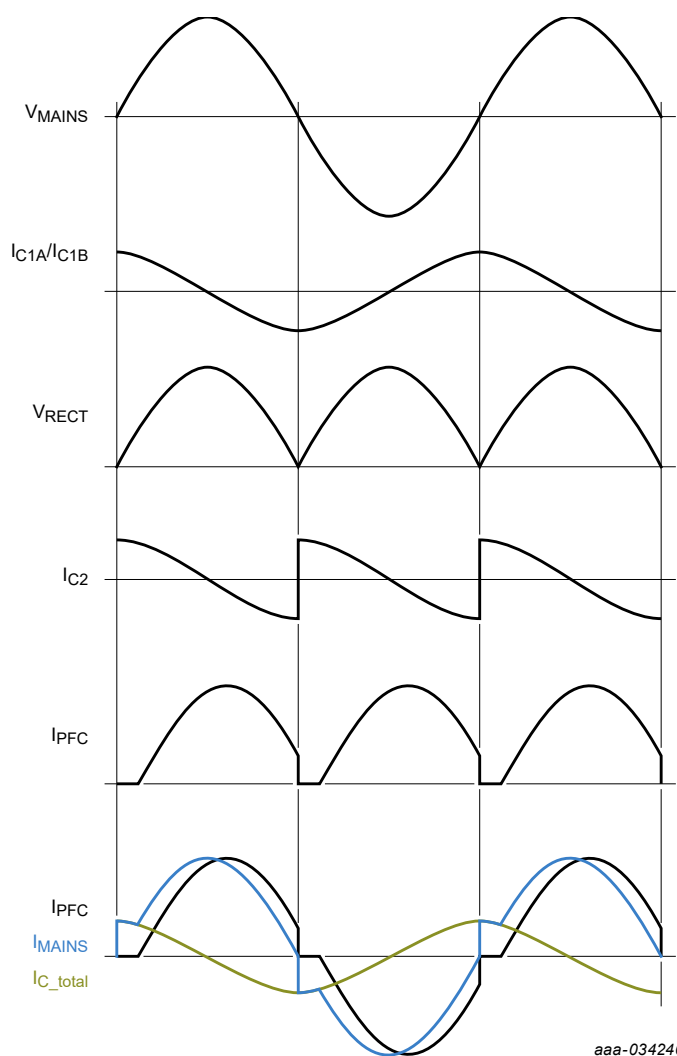
b. Waveform

Figure 20. PFC current waveforms

As the mains input current (I_{MAINS}) is the sum of the current through the filter capacitances (I_{C_total}) and the PFC current (I_{PFC}), it approaches a sine waveform.

TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

22 / 66

The output voltage control loop defines the amplitude of the shifted sine wave. If more power is requested to the output, the amplitude of the shifted sine wave increases.

The power factor correction circuit can be configured to the following mode of operation:

- DCM/QR/CCM, where the valley detection can be enabled/disabled
- DCM/QR
- Fixed frequency CCM

8.5.1 PFC switching frequency

The average PFC current is in accordance with a shifted sine wave. The PFC switching frequency is a function of this desired PFC current (see Figure 21). However, it is limited to the minimum and maximum frequency. These frequencies can be set using a parameter.

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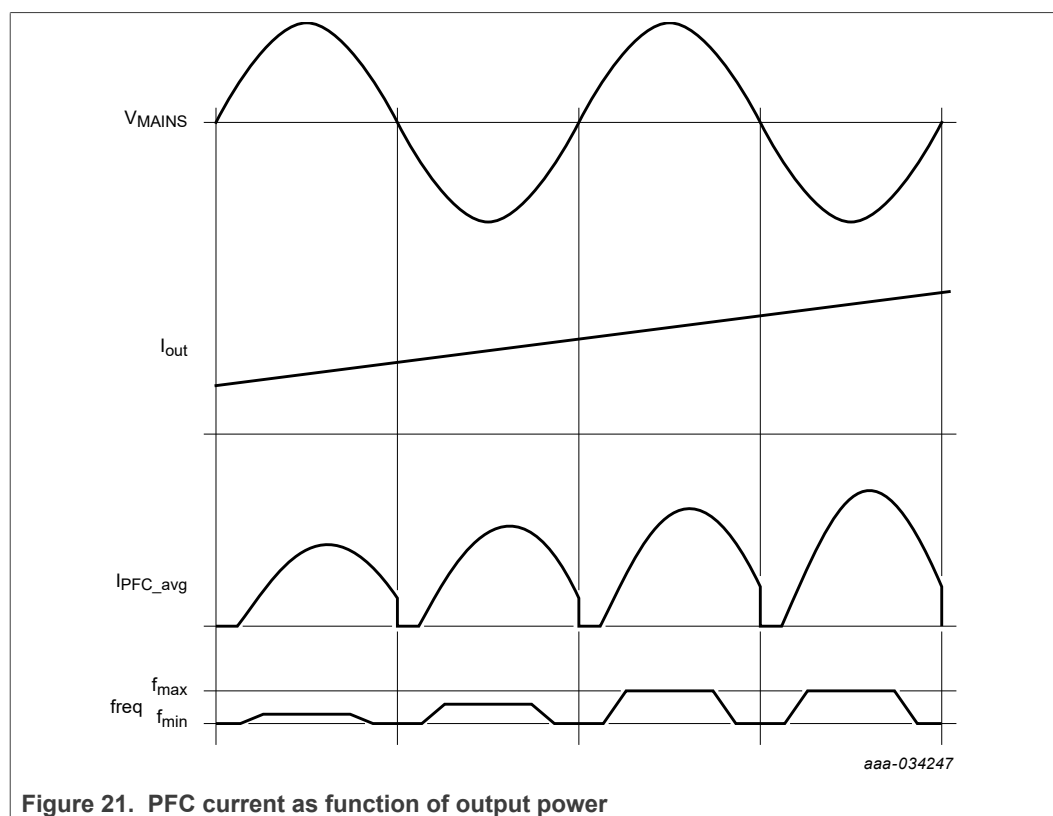
Figure 21. PFC current as function of output power

At the start of a mains cycle, the desired PFC current is zero and the PFC does not switch. When the PFC starts switching, the desired current is initially low and the PFC switching frequency is at minimum level. When the desired PFC current increases, the switching frequency increases as well until it reaches its maximum level.

Every switching cycle, the system calculates the PFC on-time such that its average current is in accordance with the desired PFC current and its frequency is in accordance with the above frequency curve. In this way, the system reaches the maximum efficiency at low loads, while keeping the ripple to a minimum at higher loads.

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Product data sheet

Rev. 1.2 — 31 July 2023

23 / 66

8.5.2 Frequency jitter

To optimize the EMI performance, an additional jitter can be added to the operating frequency of the PFC. The amplitude and modulation frequency of the jitter can be set using a parameter.

8.5.3 Multimode operation (DCM/QR/CCM)

At the start of a mains cycle, the desired PFC current is low and the PFC switching frequency is at minimum level. The PFC is then switching in DCM mode.

When the desired PFC current increases toward the center of the mains, the PFC switching frequency increases as well. The system automatically enters CCM mode (see Figure 22).
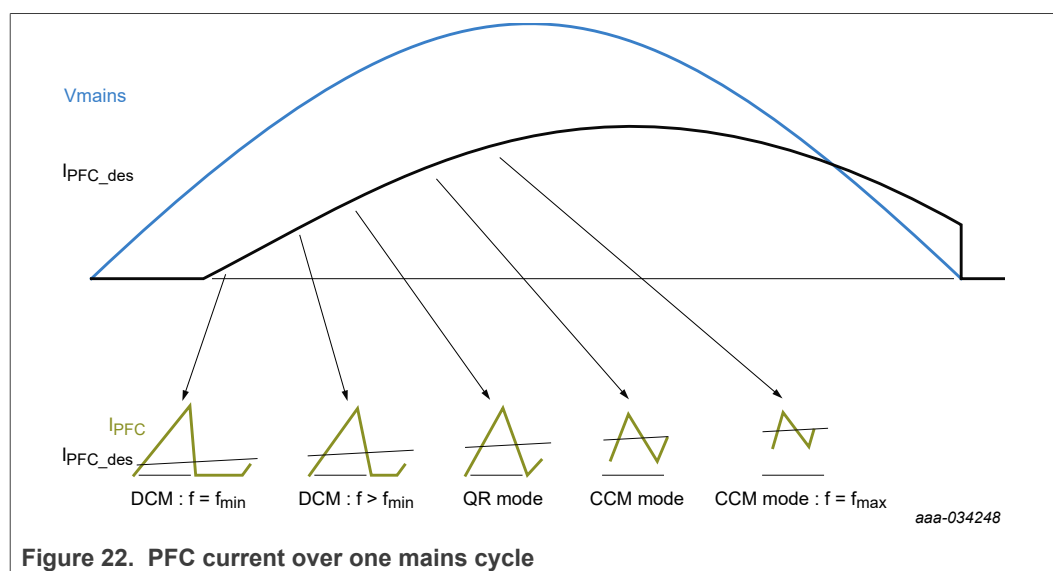
Figure 22. PFC current over one mains cycle

8.5.4 DCM/QR mode of operation

When the DCM/QR mode of operation is selected, the system actually operates the same as in the multimode operation (DCM/QR/CCM). However, the PFC MOSFET is only turned on when the previous secondary stroke has ended (transformer must be demagnetized) and the voltage across the PFC MOSFET has reached a minimum value. To detect transformer demagnetization and the minimum voltage across the PFC MOSFET switch, the control IC continuously monitors the voltage across the PFC MOSFET and the current through the PFC circuitry. As a result, the PFC switching frequency can drop to below the minimum set frequency.

8.5.5 Fixed-frequency CCM mode

In this mode, the system operates between DCM and CCM mode. The frequency is fixed and equals the set frequency.

8.5.6 PFC start-up

At start-up, the PFC output voltage increases in line with an RC curve (see Figure 23).
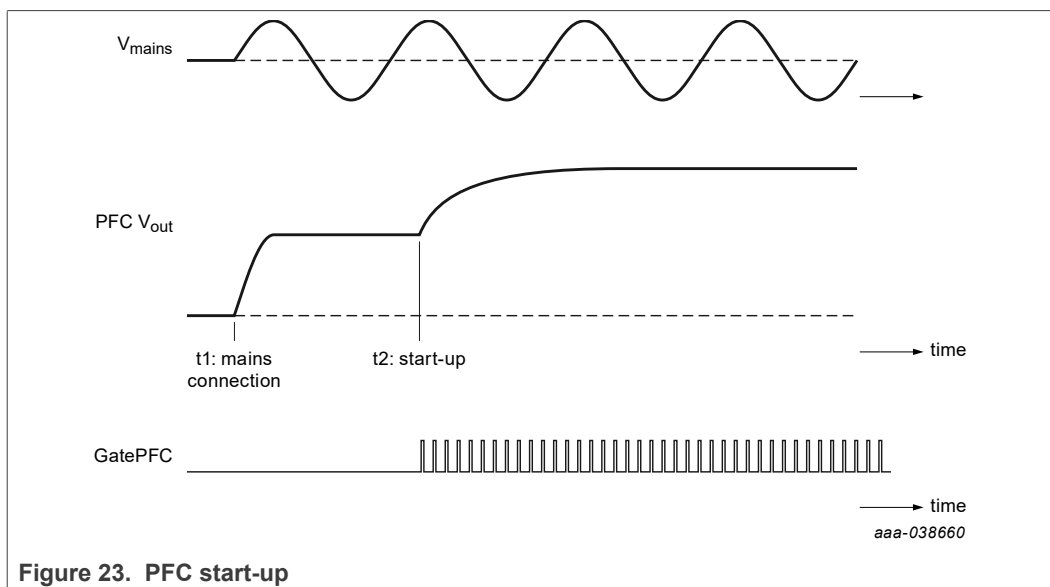
Figure 23. PFC start-up

At t1, the mains is connected and the PFC output voltage equals the peak voltage of the mains. At t2, the PFC starts switching and its output voltage increase in line with an RC curve.

Starting up with an RC curve has the advantage that after start-up, the PFC output voltage does not show any overshoot which avoids that the OVP is triggered. It also ensures that, at start-up, the on-time slowly increases from a minimum value to the regulation level, avoiding audible noise.

The RC time value can be programmed via the MTP.

8.5.7 Output voltage regulation

The PFC output voltage is externally divided using a high-ohmic resistive divider, which is connected to the SNSBOOST pin. The internal digital control loop, which compares the SNSBOOST voltage with an accurate trimmed reference voltage ($V_{reg(SNSBOOST)}$), regulates the amplitude of the desired PFC current (see Figure 21).

The PFC current is measured via an external sense resistor connected to the SNSCURPFC pin. To ensure proper switching, the measured PFC current is internally filtered.

8.5.8 PFC burst mode

When the LLC is in burst mode and its duty cycle is below an adjustable entry level, the PFC enters burst mode.

When the LLC is out of burst mode or its duty cycle exceeds the entry level plus adjustable hysteresis, the PFC leaves burst mode.

Figure 24 shows the behavior of the PFC in burst mode.

TEA2017AAT_2

Product data sheet Rev. 1.2 — 31 July 2023

25 / 66

Figure 24. PFC burst mode
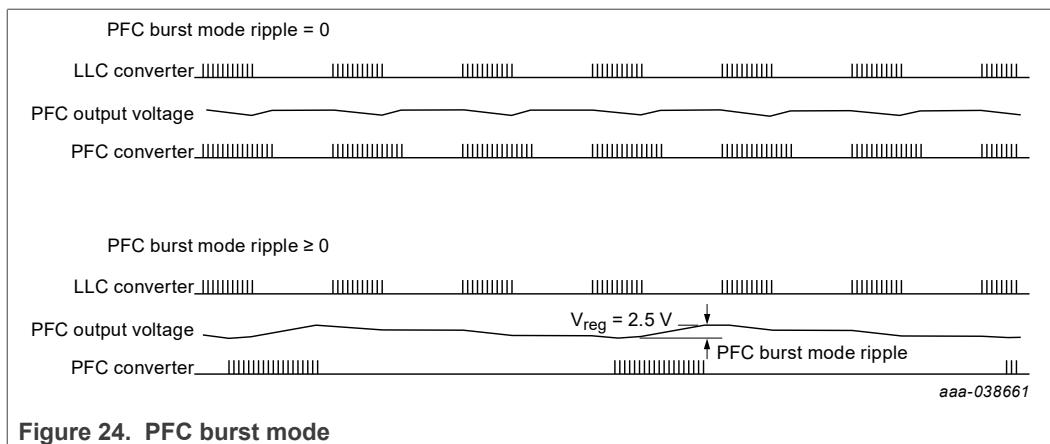
When the PFC is in burst mode and its output voltage drops to below the regulation level minus an adjustable ripple voltage, the PFC starts switching. When it reaches the regulation level again, the PFC stops switching.

When the ripple voltage is set to zero, the PFC always starts switching as soon as the LLC starts switching. When the output voltage reaches the regulation level and the LLC stops switching, the PFC stops switching as well.

When the PFC is activated in burst mode, it continues switching until it reaches the regulation level. As, during this time, the LLC may already have stopped switching, the system is not supplied via the auxiliary winding and the SUPIC capacitor is discharged.

To avoid that the SUPIC voltage reaches the $V_{uvp(SUPIC)}$ level, which causes the system to restart, the PFC stops switching when the SUPIC reaches $V_{low(SUPIC)}$ level. The system then enters the non-operating state and the internal current source is activated to supply the IC.

8.5.9 PFC burst mode soft start/soft stop

To reduce the audible noise, a soft start and a soft stop can be added to the PFC burst mode. During a soft start, the average PFC current starts at zero and increases to the required level. A soft stop implies that the average PFC current decreases from the regulation level down to zero. The rates of increase and decrease are independently adjustable.

8.5.10 Valley switching and demagnetization

When the TEA2017AAT operates in discontinuous conduction mode or quasi-resonant mode, the PFC MOSFET is switched on after the transformer is demagnetized. To reduce switching losses and electromagnetic interference (EMI), the next stroke is started when the PFC MOSFET drain-source voltage is at its minimum (valley switching). The demagnetization and valley detection are measured via the SNSCURPFC and the DRAINPFC pin.

If no valley signal is detected on the DRAINPFC pin, the controller generates a valley signal ($t_{to(vrec)}$; 7 μs typical) after demagnetization is detected.

8.5.11 Frequency limitation

To optimize the transformer and minimize switching losses, the PFC switching frequency is limited to $f_{sw(PFC)max}$.

To avoid audible noise, the minimum frequency is limited to $f_{sw(PFC)min}$.

To ensure correct control of the PFC MOSFET under all circumstances, the minimum off-time is limited at $t_{off(PFC)min}$.

All frequency limitation values are adjustable.

8.5.12 Mains voltage compensation (SNSMAINS pin)

The equation for the transfer function of a power factor corrector is a function of the mains input voltage. In a typical application, the result is a low bandwidth for low-mains input voltages. At high-mains input voltages, the mains harmonic reduction (MHR) requirements may be hard to meet.

To compensate for the mains input voltage influence, the TEA2017AAT contains a correction circuit. The input voltage is measured via the SNSMAINS pin (see Section 8.6.4). The information is fed to an internal mains compensation circuit. With this compensation, it is possible to keep the regulation loop bandwidth constant over the full mains input range. The result is that a mains voltage-independent transient response on load steps is yielded, while still complying with class-D MHR requirements.

8.5.13 Active X-capacitor discharge

The TEA2017AAT provides an active X-capacitor discharge after the mains voltage is disconnected. When the mains input voltage (and so also the measured current into the SNSMAINS pin) increases, the system assumes the presence of a mains voltage. When the mains voltage does not increase for a minimum period of $t_{d(dch)}$, the X-capacitor is discharged via the DRAINPFC pin. When the mains is reconnected, the discharge current is disabled again.

8.6 Protections

Table 4 gives an overview of the available protections.

Table 4. Protections overview

Protection	Description	Action	PFC	LLC	Protection register
General protections					
UVP SUPIC	undervoltage protection SUPIC pins	recharge via DRAINPFC; restart when $V_{SUPIC} >$ $V_{start(SUPIC)}$	off	off	-
MTPfail	reading of the internal MTP failed	continue reading until the data is valid; only checked once at start-up	off	off	Y
OTPint	internal overtemperature protection	LLC and PFC are either latched or safe restart [1]	off	off	Y
OTPext	external overtemperature protection	LLC and PFC are either latched or safe restart [1]	off	off	Y

Table 4. Protections overview...*continued*

Protection	Description	Action	PFC	LLC	Protection register
SCP SNSBOOST/ fast disable	short-circuit protection/ disable PFC and LLC	restart when $V_{SNSBOOST} > V_{scp(start)}$	off	off	Y
PFC protections					
brownout-mains	undervoltage protection mains	restart when the mains voltage exceeds the brownin level	off	on/ off [1]	-
OVP SNSBOOST	overvoltage protection boost voltage	restart when $V_{SNSBOOST} < V_{reg(SNSBOOST)}$	off	on/ off [1]	Y
OVP DRAINPFC	overvoltage protection DRA INPFC voltage	LLC and PFC are either latched or safe restart protections [1]	off	off	Y
Maximum on-time	maximum on-time of the PFC MOSFET	PFC MOSFET switched off; continue operation	-	-	N
OCP	overcurrent protection	PFC MOSFET switched off; continue operation	-	-	N
PFCcoil short	-	LLC and PFC are off, followed by a safe restart	off	off	Y
Iinrush	inrush current protection	PFC MOSFET switched off; PFC switching postponed	off	-	-

Table 4. Protections overview...*continued*

Protection	Description	Action	PFC	LLC	Protection register
LLC protections					
UVP SUPHS	undervoltage protection SUPHS pin	GATEHS = off	-	off	-
UVP SNSBOOST	undervoltage protection boost	restart when $V_{SNSBOOST} > V_{start(SNSBOOST)}$	-	off	-
OVP SUPIC	output overvoltage protection; measured via the SUPIC pin	LLC and PFC are either latched or safe restart [1]	off	off	Y
Maximum on-time	maximum on-time of the LLC MOSFET	LLC MOSFET switched off; continue operation	-	-	Y
CMR	capacitive mode regulation	system ensures that mode of operation is inductive	-	-	Y
OCP	overcurrent protection	switch off cycle-by-cycle; After several consecutive cycles, LLC and PFC are either latched or safe restart [1]	off	off	Y
STARTUP MAX	maximum start-up time	LLC and PFC are either latched or safe restart [1]	off	off	Y
OPP	overpower protection	LLC and PFC are either latched or safe restart [1]	off	off	Y

[1]   Selectable via a parameter at the MTP.

When the system is in a latched or safe restart protection, the SUPIC voltage is regulated to its start level via the DRAINPFC pin.

8.6.1 Undervoltage protection SUPIC

When the voltage on the SUPIC pin is below its undervoltage level $V_{uvp(SUPIC)}$, both the PFC and LLC converter stop switching. The capacitors at the SUPIC pin are recharged via the DRAINPFC pin.

When the SUPIC supply voltage exceeds its start level, the system restarts.

8.6.2 MTP fail

At start-up, when the SUPIC reaches 12 V, the system reads the parameters from the internal MTP. If reading the MTP failed, a protection is triggered. A mains reset is required before the system starts. During this time, the PFC and LLC remain off.

8.6.3 Internal overtemperature protection (OTP)

An accurate internal temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the PFC and the LLC stop switching.

TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

29 / 66

The response of the internal OTP follows the setting of the external OTP. It can be either latched or safe restart.

8.6.4 Brownin/brownout and external overtemperature protection

On the TEA2017AAT, the mains measurement and external temperature measurement are combined at the SNSMAINS pin (see).

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Product data sheet　　　　　**Rev. 1.2 — 31 July 2023**

30 / 66

a. Circuit

b. Timing diagram

Figure 25. Mains and external OTP management
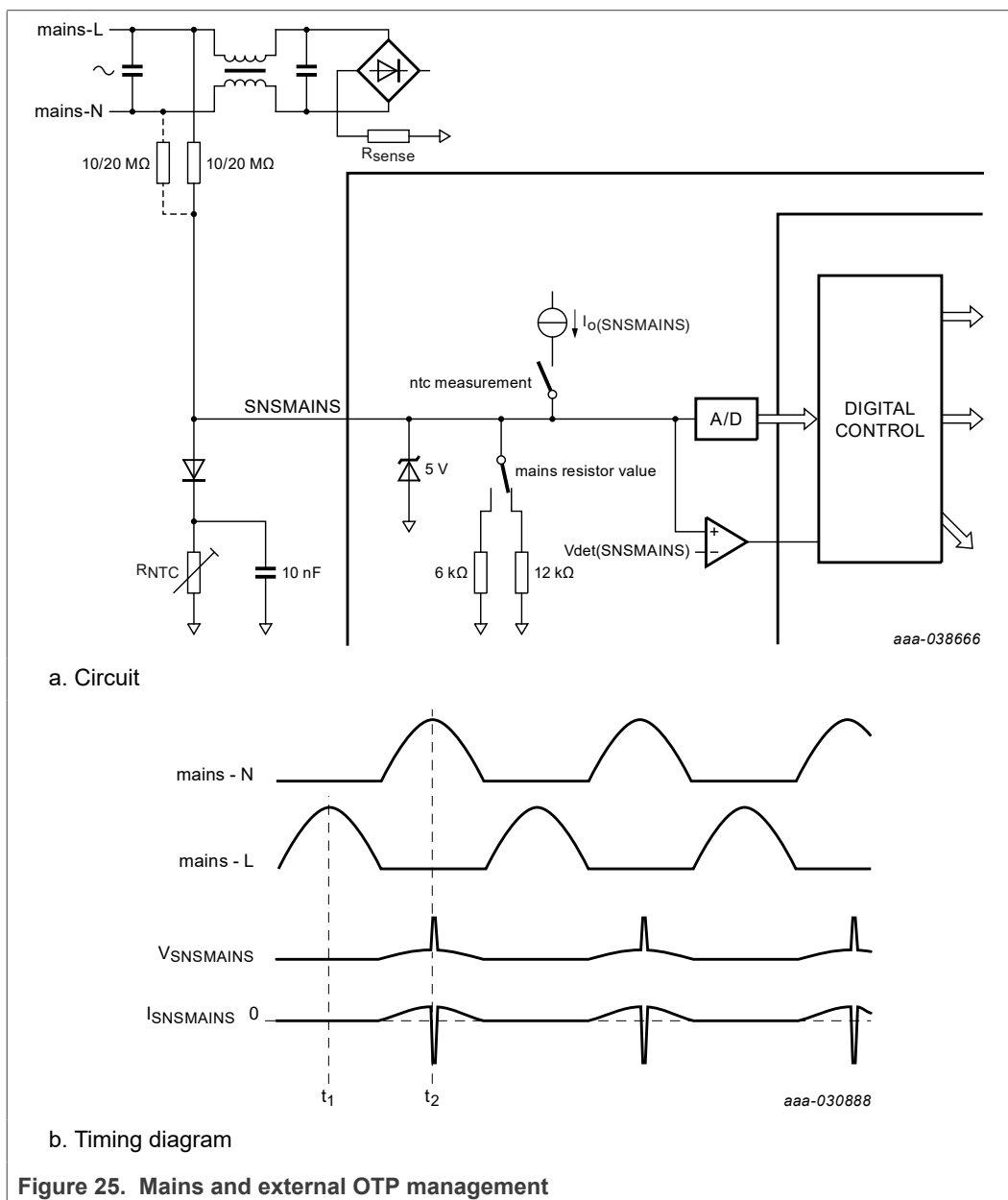
The TEA2017AAT continuously measures the SNSMAINS voltage via an A/D converter and waits until it detects a peak (t1). This peak value is internally stored and used for the mains compensation. The output of the A/D converter is used for brownout/brownin detection.

During an NTC measurement, which is enabled during the peak of the mains, an internal current source of $I_{o(SNSMAINS)}$ is switched on. With the external NTC and diode, the internal current source generates a voltage at the SNSMAINS pin. If this voltage remains below the $V_{det(SNSMAINS)}$ level, the external OTP protection is triggered after $t_{d(otp)}$. The internal current source is turned on until the SNSMAINS voltage exceeds the $V_{det(SNSMAINS)}$ level level or a maximum time of $t_{det(max)NTC}$.

The external resistor, which is connected between mains_L/mains_N and the SNSMAINS pin, can be either 20 MΩ or 10 MΩ. The amount of mains resistor can either be one (only

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Product data sheet

Rev. 1.2 — 31 July 2023

31 / 66

connected to the mains-L or mains-N) or two (one connected to the mains-L and the other to the mains-N). However, the selected parameter of the resistor value and number of resistors must correspond to the application.

8.6.5 Short-circuit protection/fast disable

The PFC and LLC do not start switching until the voltage on the SNSBOOST pin exceeds $V_{scp(start)}$. This function acts as short circuit protection for the boost voltage.

When the SNSBOOST pin is shorted to ground or the SNSBOOST pull-up resistor is disconnected, this protection inhibits switching.

This function can also be used as a fast disable. If this pin is shorted to ground via an external MOSFET, the system either stops switching or enters the protection mode followed by safe restart or latched protection. In this way, an additional external protection can be added.

8.6.6 Brownout mains

To prevent the PFC from operating at very low mains input voltages, the PFC stops switching with a soft stop when the measured mains voltage drops to below the brownout level. When the mains voltage exceeds the brownin level, the PFC restarts with a soft start. To avoid that the system is interrupted during a short mains interruption, a delay can be set before the brownout function is active.

Typically, only the PFC stops switching and the LLC continues at a brownout. Due to the large PFC bulk capacitor, the LLC can continue for a long period while the mains is already disconnected. So, the option to stop the LLC at a brownout after a given delay can be selected with a parameter.

8.6.7 Overvoltage protection (SNSBOOST pin)

To prevent output overvoltage during load steps and mains transients, a PFC output overvoltage protection circuit is built in. When the voltage on the SNSBOOST pin exceeds the $V_{stop(ovp)PFC}$ level, switching of the power factor correction circuit is inhibited. When the SNSBOOST pin voltage drops to below the regulation level ($V_{reg(SNSBOOST)}$) again, the switching of the PFC recommences.

When an OVP at the SNSBOOST is detected for a minimum period (can be set using a parameter), the LLC can also be disabled.

8.6.8 Overvoltage protection (DRAINPFC pin)

To prevent output overvoltage of the PFC due to a disturbed SNSBOOST pin, an additional PFC output overvoltage protection is available. This overvoltage protection is measured via the DRAINPFC pin.

To avoid false triggering, measuring the DRAINPFC is blanked for $t_{leb(OVP)PFC}$ after the PFC MOSFET is switched off.

The DRAINPFC overvoltage protection level and the delay before it enters the protection state can be set with parameters.

The DRAINPFC overvoltage protection can be a latched, a safe restart, or a latched after safe restart protection.

8.6.9 Overcurrent protection, inrush protection (SNSCURPFC pin)

The PFC current is measured via an external sense resistor (R_{SENSE}) connected to the SNSCURPFC pin (see Figure 29). If the voltage drops to below $V_{ocp(PFC)}$, the PFC MOSFET is turned off. It resumes switching at the next cycle, under the condition that the voltage at the SNSCURPFC is above the $V_{ocp(PFC)}$ level. Otherwise, it remains off until this requirement is fulfilled. It avoids that the PFC MOSFET is turned on during an inrush.

To ensure that the OCP level is not exceeded due to disturbance caused by a turn-on of the PFC MOSFET, the OCP level is filtered via an internal 1 MHz filter.

8.6.10 PFC coil short protection (SNSCURPFC pin)

If the PFC coil is shorted, the overcurrent protection is triggered continuously. To avoid overheating, the system enters the protection state when the OCP is continuously triggered for a selectable number of switching cycles. The PFC and LLC converters stop switching and a restart follows.

8.6.11 Undervoltage protection SUPHS

To ensure a minimum drive voltage at the high-side driver output (GATEHS), this driver is turned off when its voltage is below the minimum level ($V_{SUPHS} < V_{rst(SUPHS)}$).

8.6.12 Undervoltage protection boost

The PFC output voltage is measured via a resistive divider connected to the SNSBOOST pin. The voltage at the SNSBOOST pin must exceed the start level ($V_{SNSBOOST} > V_{start(SNSBOOST)}$) before the LLC converter is allowed to start switching.

When the system is operating and the voltage at the SNSBOOST pin drops to below the minimum level ($V_{SNSBOOST} < V_{uvp(SNSBOOST)}$), the LLC converter stops switching. When it exceeds the start level, it restarts.

8.6.13 Overvoltage protection

When the voltage at the SUPIC pin exceeds the $V_{O(ovp)SUPIC}$ level for $t_{d(ovp)SUPIC}$, the OVP protection is triggered. The voltage at the SUPIC pin is continuously monitored via an internal A/D converter.

The OVP protection level and the OVP delay time can be selected with a parameter.

The OVP function can also be disabled.

8.6.14 Capacitive mode regulation (CMR)

The TEA2017AAT has a capacitive mode regulation (CMR) which ensures that the system is always operating in inductive mode and avoids operation in capacitive mode.

At lower input voltage or higher output power and depending on the resonant design, the resonant current can already approach zero before the capacitor voltage reaches the regulation level.

When the resonant current has changed polarity before the switches are turned off and the other switch is turned on, hard switching occurs. This event is called capacitive mode. To avoid that the LLC operates in capacitive mode, the system also switches off the high-side/low-side switch when the resonant current approaches zero.

Figure 26 shows the signals that occur when a resonant converter is switching in CMR mode. At t1 (and also at t3), the low-side switch is on while the resonant current approaches zero before V_{SNSCAP} reaches $V_{ls(SNSCAP)}$. At t2, the resonant current is also close to changing polarity while the divided capacitor voltage (V_{SNSCAP}) has not reached the $V_{hs(SNSCAP)}$ level yet. To avoid a turn-off of the high side switch at a negative current or the low side at a positive current, the system also turns off the high-side/low-side switch when the primary current approaches zero. So at t2, the high-side switch is turned off because the primary current is close to zero. At t_3 (and also at t_1), the low-side switch is turned off, although V_{SNSCAP} did not reach the regulation level ($V_{ls(SNSCAP)}$) yet. The primary current is measured via an external sense resistor connected to the SNSCURLLC pin. The capacitive mode protection levels are $V_{reg(capm)}$ (−100 mV typical and +100 mV typical). These levels can be adjusted with a parameter.

In this mode, the amount of output power is reduced and the output voltage decreases.

The TEA2017AAT does not enter a so-called "capacitive mode protection", but avoids this mode of operation.

Figure 26. Near capacitive mode switching

TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

34 / 66
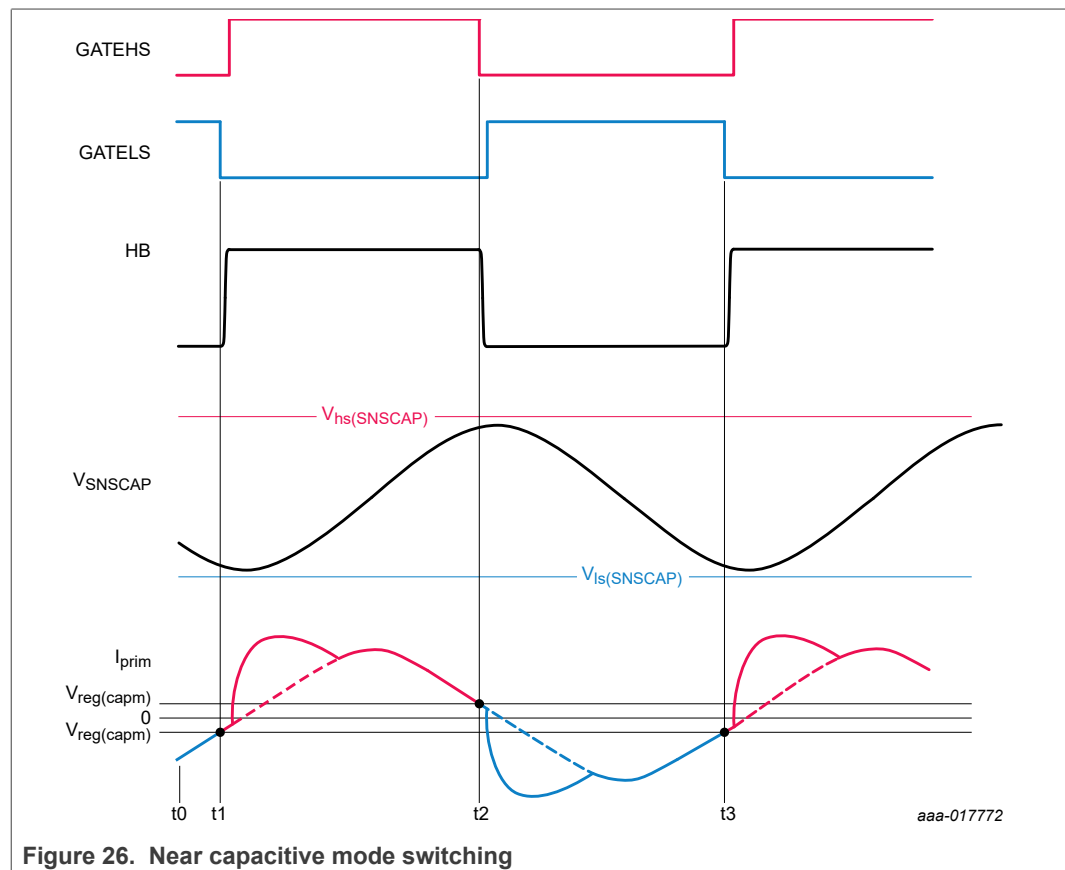
8.6.15 Overcurrent protection

The system measures the LLC primary current continuously via a sense resistor connected to the SNSCURLLC pin. If the measured voltage exceeds the fixed overcurrent level ($V_{ocp(LLC)}$), the corresponding switch (GATELS/GATEHS) is turned off, but the system continues to switch. In this way, the primary current is limited to the OCP level.

The OCP level can be adjusted via the external sense resistor.

If the OCP is continuously triggered for an adjustable time, the system enters the OCP protection state. The OCP protection state can also be disabled. However, the primary current is always limited to the OCP level cycle-by-cycle.

8.6.16 Maximum start-up time

At start-up, the PFC starts switching. When the PFC output voltage exceeds a minimum level, the LLC starts switching as well.

If the output voltage of the LLC is not in regulation within an adjustable time after the PFC has started switching, the maximum start-up time protection is triggered.

The maximum start-up time ($t_{startup(max)}$) can be set with the parameter "Maximum start-up time". If this protection is triggered, the system is latched, safe restart, or latched after safe restart, which follows the setting of the OPP.

8.6.17 Overpower protection

For the overpower protection, three levels can be set:

- Absolute maximum output power, which is the highest output power level.
  When the output power exceeds this maximum level, it is limited cycle-by-cycle. If the output power exceeds this maximum, the output voltage decreases.
  The maximum output power can be set to a percentage of the rated output power.
- A first overpower level, which is below the maximum output power level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. Both PFC and LLC are switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the maximum output power is set to 170 % and this first overpower level is set to −20 %, the timer is started at 150 % of the rated output power.
  The timer of the first overpower level can also be set. The first overpower level can also be disabled.
- A second overpower level, which is typically below the first overpower level.
  When the output power exceeds this power level, a timer is started. When this timer exceeds a predefined value, the system enters the protection state. PFC and LLC are switched off.
  This power level can be set to a predefined level below the selected maximum output power. So, if the output power is set to 170 % and this second overpower level is set to −50 %, the timer is started at 120 % of the rated output power.
  The timer of the second overpower level can be set to a predefined level. The second overpower level can also be disabled.

The overpower function can be either latched, safe restart, or latched after safe restart. Section 8.6.18 describes this function.

TEA2017AAT_2

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Product data sheet **Rev. 1.2 — 31 July 2023**

35 / 66

8.6.18 Latched, safe restart, or latched after safe restart

When a protection is selected to be latched, the system stops switching when this protection is triggered. The system only restarts after a fast latch reset (see Section 8.6.19) or when the SUPIC supply voltage drops below the UVP level.

When a protection is selected to be safe restart, the system continuously restarts after a predefined safe restart time. This safe restart time is the same for all protection functions. It can be set with a parameter.

When selecting "latched after safe restart", a protection is initially a safe restart protection. If the failure occurs again within a specific time, it latches eventually.

Figure 27. Latched after safe restart
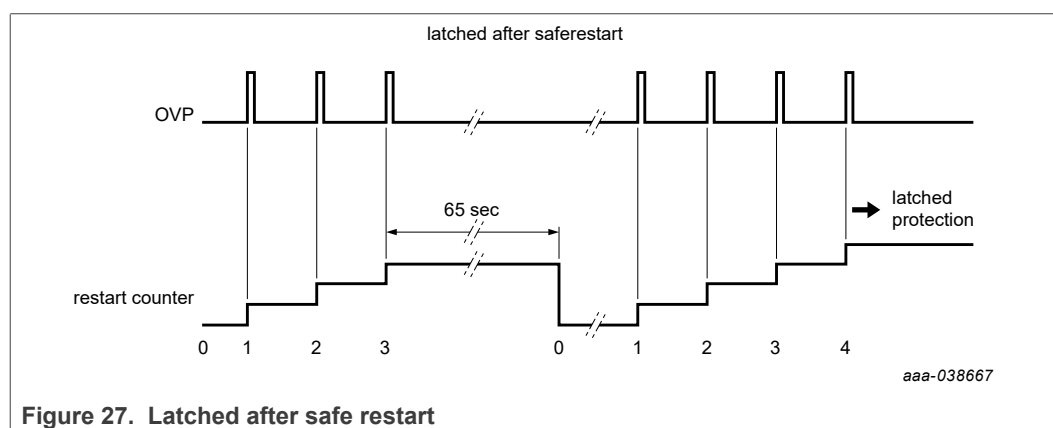
Figure 27 shows an example of when the OVP is set to latched after safe restart. Initially at an OVP, the system restarts after the safe restart time. An internal counter is then set to '1'. If the protection is triggered again, the counter is increased. If the counter reaches the number as set with a parameter, the system latches. If no protection is triggered within 65 seconds, the counter is reset.

8.6.19 Fast latch reset

If a protection is triggered, the system enters the protection state. Especially when the protection is latched, this function is inconvenient during production tests. So, when the mains voltage is below the brownout level for a specified time, the system also restarts. This time can be set with a parameter. This function is called fast latch reset.

8.7 Power good function

The TEA2017AAT provides a power good function via the SNSFB pin.

Figure 28. Power good function

a. Primary side

b. Secondary side
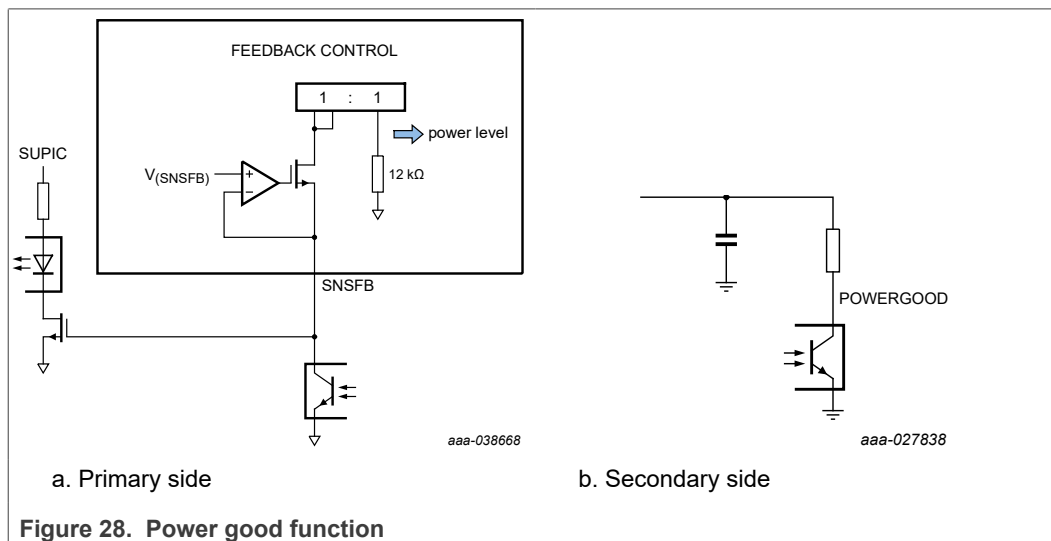
The primary function of the SNSFB pin is to regulate the output voltage via an optocoupler. So, it measures the current that is drawn from the SNSFB. Via an internal 12 kΩ resistor, it regulates the output power. The output power regulation is independent of the voltage level of the SNSFB pin. So, the voltage level at the SNSFB pin is used to indicate if the system is about to stop operating, a so-called power good signal. The voltage at the SNSFB pin can be used to generate a secondary power good signal using an external MOSFET and an optocoupler.

At start-up, the SNSFB voltage is at a high level, pulling down the secondary power good signal. As soon as the system enters the operating state (see Figure 4), the SNSFB goes low. The external power good signal becomes active high.

The SNSFB voltage becomes active high, lowering the secondary power good signal when:

- The voltage on the SNSBOOST pin drops to below $V_{det(SNSBOOST)}$
- The OPP counter is close to its end value
- The converter is about to stop due to an OTP protection
- When the LLC converter is about to stop due to an OVP on the SNSBOOST when this function is enabled
- When the LLC converter is about to stop due to a mains brownout when this function is enabled

To avoid any disturbance of the regulation loop, the increase and decrease of the SNSFB voltage is in alignment with a predefined ramp.

When the system enters protection mode (OVP, OCP, or UVP), it pulls high the SNSFB pin and stops switching immediately.

8.8 Settings

The TEA2017AAT has an internal MTP at which different settings can be programmed.

The TEA2017AAT settings can be found in Section 13.

Disclaimer:

The MTP parameter settings can be changed using the "Ringo" GUI software of NXP Semiconductors. Before the user can change any MTP parameters using the GUI, the terms and conditions in the start-up pop-up screen must be accepted.

8.8.1 General settings

8.8.1.1 Protection register

When the TEA2017AAT triggers a protection, it can be read which protection was triggered. Even when the root cause of the protection is solved and the converter continues switching, the information about the protection remains until the software program (Ringo GUI) clears it.

8.8.1.2 Supply start level

The SUPIC start level can be selected between 12 V and 19 V. Typically, a level of 19 V is selected. When the TEA2017AAT is externally supplied, for instance via a standby supply, the lower start level of 12 V can be used.

After start-up, when the MTP is read and a 12 V start level is selected, charging via the PFCDRAIN is disabled, as the system assumes that it is externally supplied.

8.8.1.3 Read lock

Normally, the software tool can read all the programmed settings. This option can be used to verify the correct settings or for failure analyses.

However, once in production, enabling the "Read lock" bit protects the parameters. Then it is not possible anymore to read the MTP content. It can however still be reset to the default values and also clear the read lock parameter.

8.8.1.4 Write lock

To avoid that the MTP content (accidentally) gets overwritten, a write-lock bit can be set. It can, however, still be reset to the default values and clear the write lock parameter.

8.8.1.5 Reset to the default values

When the MTP is reset, it implies that all parameters are set to a default value. The default values normally do not correspond to the original MTP values. They are chosen such that a general application works properly.

When the MTP is reset, the MTP can be read and written again.

8.8.1.6 Customer MTP code

When in production, the content of the MTP can be hidden when the read lock bit is enabled. To get access to the content of the MTP, a unique customer code can be programmed. This customer code provides information about the MTP content.

This customer code can always be read, even when the read lock bit is enabled.

8.8.2 PFC settings

8.8.2.1 Soft-start time

For the start-up time of the PFC, the following RC time periods can be selected: 13 ms, 25 ms, 51 ms, or 102 ms.

8.8.2.2 Active X-capacitor discharge

When the TEA2017AAT detects that the mains is disconnected, the X-capacitor discharge is activated after a delay of $t_{d(dch)}$. The following delays can be selected: 100 ms, 200 ms, and 400 ms. This function can also be disabled.

8.8.2.3 Mains measurement impedance

To realize a low no-load input power level, the external resistor connected to the SNSMAINS pin for measuring the mains input voltage is typically 20 MΩ.

However, some applications request a maximum resistance of 10 MΩ. With this bit, 10 MΩ or 20 MΩ can be selected for the external resistor without affecting the mains voltage-related levels like brownin and brownout.

8.8.2.4 Number of mains resistors

To achieve the lowest possible no-load input power, a single mains sense resistor can be used. If continuously measuring the mains voltage is necessary, two mains resistors can be used.

For proper functionality, the resistor value and number of resistors in the application are required to correspond to the IC settings.

8.8.2.5 PFC mode of operation

When all modes are enabled, the PFC can operate in DCM, QR, or CCM mode. However, the frequency varies between the minimum and maximum frequency.

It is also possible to either disable CCM mode or select the fixed frequency mode. For evaluation purposes, the option to disable the PFC is available as well.

8.8.2.6 PFC minimum and maximum frequency

The minimum switching frequency of the PFC can be set within a range from 25 kHz to 80 kHz. When the CCM mode of operation is disabled, the PFC always waits until the PFC coil is demagnetized before starting the next cycle. As a result, the switching frequency can drop to below the minimum frequency.

The maximum frequency can be set within a range from 75 kHz to 250 kHz. When the PFC operating mode is set to fixed frequency, the frequency can be set between 55 kHz and 200 kHz.

8.8.2.7 Burst mode: Output voltage ripple

When the PFC enters burst mode, it stops switching when the SNSBOOST voltage, which reflects the PFC output voltage, reaches its regulation level and the LLC stops switching. When the voltage at the SNSBOOST pin has dropped to a programmed level, the PFC is enabled again. For the difference between these two levels the following values can be selected: 70 mV, 105 mV, 140 mV, 175 mV, 210 mV, 245 mV, and 280 mV.

TEA2017AAT_2

Product data sheet

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Rev. 1.2 — 31 July 2023

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39 / 66

These values typically correspond with a ripple on the PFC output voltage of 10 V, 16 V, 22 V, 28 V, 34 V, 40 V, and 46 V.

The PFC burst mode can also be synchronized to the LLC burst mode. It then follows the on and off periods of the LLC. However, it ensures that the SNSBOOST reaches its regulation level.

8.8.2.8 Burst mode: Soft-start/soft-stop time

To minimize audible noise of the PFC, a burst mode soft start and soft stop can be independently selected. The selectable values are: normal, short, and long. The additional soft-start and soft-stop can also be disabled.

8.8.3 LLC settings

8.8.3.1 LLC disable

Especially for validation purposes, an option is available to disable the LLC. When the LLC is disabled, a restart is required.

8.8.3.2 Start-up

Maximum (start-up) frequency

The maximum switching frequency of the LLC is limited to a value, which is defined using a parameter. This value also defines the maximum switching frequency during start-up. The maximum frequency can be set to different values ranging from 150 kHz to 800 kHz.

LLC soft-start time

The LLC soft-start time defines the rate at which the converter lowers its switching frequency. This rate can be selected between 2 and 20 which leads to a start-up time of approximately between 1 ms and 10 ms. However, it depends on the LLC design. A higher speed lowers the start-up time. However, it can cause a high charge current and an overshoot at the output voltage.

Maximum primary current during start-up

At start-up, the LLC starts switching at the maximum frequency and ramps down the frequency until the ΔV_{SNSCAP} reaches the required level. If during this start-up time the primary current, which reflects the output current, reaches a predefined level, the frequency is temporarily not further reduced until the primary current drops to below the level again. This level is measured via the SNSCURLLC pin. The following values can be selected: 0.5 V, 0.75 V, 1.0 V, or 1.25 V.

8.8.3.3 LLC switching

ΔV_{SNSCAP} dump level

When the system is in low-power mode, a switching period is followed by a waiting period. The system ensures that it continues at the same stage as where it stopped. To reach the maximum efficiency, the end of the last switching cycle can be fine-tuned. For the ΔV_{SNSCAP} dump level, values between 2.525 V and 2.7 V can be selected in steps of 25 mV.

Minimum non-overlap time

To ensure that the GATEHS is properly turned off before the GATELS is turned on, and vice versa, there is a minimum non-overlap time. For the minimum non-overlap time, the following values can be selected: 100 ns, 230 ns, 350 ns, 500 ns.

Maximum non-overlap time

When the system does not detect a valley at the HB node after turning off GATEHS, the system turns on the GATELS after the maximum non-overlap time. The same counts when a peak at the HB node is not detected after turning off the GATELS and turning on the GATEHS. For the maximum non-overlap time, the following values can be selected: 0.5 µs, 0.7 µs, 0.9 µs, or 1.1 µs.

Maximum on-time

When the on-time of the GATELS or GATEHS exceeds the maximum on-time, the switch is turned off, and the LLC converter starts the next cycle. For the maximum on-time, the following values can be selected: 10 µs, 20 µs, 30 µs, or 38 µs.

Capacitive mode regulation

When the voltage at the SNSCURLLC pin, which reflects the resonant current, drops to below a predefined value, the LLC converter starts the next switching cycle. In this way, the TEA2017AAT avoids that the converter operates in capacitive mode. For the capacitive mode regulation, the following values can be selected: 20 mV to 160 mV in steps of 20 mV.

LLC maximum ringing time

When the LLC operates in LP mode, it counts the amount of ringings. If a ringing is not detected, it assumes a peak after the timeout. This timeout can be set to 3 µs, 5 µs, 7.5 µs, or 10 µs. The appropriate value depends on the application. It must be chosen just above the maximum ringing period.

8.8.3.4 Feedback

Optocoupler current

To achieve a low no-load input power, the current through the optocoupler must be set at a low level. However, depending on the selected optocoupler, a higher optocoupler current may be requested. So, the optocoupler current can be set to different values ranging from 80 µA to 1.2 mA.

8.8.3.5 Operation modes

HP-LP transition level

When the output power drops to below a predefined level, the system switches from the HP to the LP mode. The HP-LP transition level can be set to different values ranging from 10 % to 54 %.

HP-LP transition hysteresis

When the system operates in LP mode, it switches over to HP mode when the output power exceeds the selected HP-LP transition level plus a hysteresis. For the hysteresis, the following values can be selected: 10 %, 20 %, 30 %, or 40 % of the selected HP-LP transition level. So, if the rated output at 100 % is 100 W, the HP-LP transition level is set at 30 % and the hysteresis is set at 10 %. The eventual hysteresis is 3 W.

TEA2017AAT_2

Product data sheet

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Rev. 1.2 — 31 July 2023

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41 / 66

LP-BM transition level

When the output power drops below the LP-BM transition level, the system enters burst mode. The LP-BM transition level can be set to different values ranging from 1 % to 25 %.

The actual LP-BM transition level can deviate from the selected value due to delays in the system. The deviation is most noticeable at low LP-BM transition levels. In this case, the LP-BM transition level can be fine-tuned in steps of 1 %.

BM-LP transition level

When the system operates in burst mode and output power increases to exceed the LP-BM transition level plus a hysteresis level, the system enters low-power mode. For the hysteresis, levels in the range from 5 % to 50 % can be selected, which are related to the selected LP-BM transition level. So, if the rated output at 100 % is 100 W, the LP-BM transition is set at 10 %, and the hysteresis at 50 %, the system switches from burst mode to low-power mode at a level of 15 W.

BM-LP transition level filter

When the output power slowly increases, the system ensures a smooth transition when leaving burst mode and entering low-power mode by setting a burst-mode-to-low-power-mode transition filter. When the output power exceeds the BM-LP transition level plus hysteresis for 2, 4, 8, or 16 burst cycles, it leaves the burst mode and enters the low-power mode. At a large transient at the output, the system immediately leaves burst mode.

BM repetition frequency

When the system operates in burst mode, it is regulated to a fixed frequency. This frequency can be set to different values ranging from 20 Hz to 3.2 kHz.

BM E/C (Energy-per-cycle) increase

As the TEA2017AAT regulates the output via the primary capacitor voltage, it offers the ability to increase the output power per switching cycle when it enters burst mode. For the increase of output power per switching cycle, also called E/C (Energy-per-cycle), different values can be set ranging from 1 to 4. When, for instance, the E/C is set to 4, the system increases the E/C with a factor of 4 when it enters burst mode. The initial duty cycle is then 25 %. Increasing the E/C in burst mode increases the efficiency of the system, but at the cost of a higher output voltage ripple.

BM soft start/soft stop

To minimize the audible noise in burst mode, a soft start and a soft stop can be added. The soft start and soft stop can be independently initialized, whereas the number of soft-start/soft-stop cycles can be set between 0 and 4. In this way, the soft-start and soft-stop cycle can be optimized depending on the selected transformer.

BM minimum cycles

As additional soft-start and soft-stop cycles reduces the audible noise, it increases the switching losses. To optimize the number of normal switching cycles in relation to the added soft-start and soft-stop switching cycles, the minimum number of normal switching cycles that can be selected ranges from 1 to 12.

Burst end SNSFB current

When the system operates in burst mode, it adjusts the number of switching cycles such that burst frequency corresponds to the selected burst frequency. If during these

switching cycles the output load decreases, the output voltage increases as the system has calculated the number of required switching cycles. If the measured optocoupler current at the SNSFB pin exceeds a certain level, the system ends the burst switching cycle. This level can be between a factor of 2.5, 3.75, 5, or 7.5 times the selected optocoupler current level.

Burst delay

Entering the burst mode can be postponed with a delay from 0.2 s to 4 s. The delay can also be set to 0, implying that when the output power drops to below the burst mode entry level, the system immediately enters burst mode. The burst mode delay can also be set to infinite. The system does not enter burst mode and remains switching.

Burst-mode exit delay

When the LLC is switching for a time that exceeds the burst-mode exit delay time and the output load exceeds the burst-mode level, the system leaves the burst mode. The burst-mode exit delay time ($t_{burst-exit}$) can be set from 160 μs to 4 ms in 16 steps.

Low-power frequency

The frequency of the low-power mode can be selected by defining the ringing number at which the next low-power cycle must be started. The selection options are from 1 to 8 in steps of 1.

SNSBOOST compensation

A ripple at the input voltage of an LLC converter normally results in a ripple in the output voltage. To minimize the ripple at the output voltage, the TEA2017AAT measures the input voltage of the LLC via the SNSBOOST pin and compensates the SNSCAP voltage via a feed-forward compensation. As the required compensation depends on the external components, it can be set at 8 different compensation levels.

8.8.4 Protection settings

8.8.4.1 General protections

Fast latch reset delay time

When the system does not detect a mains voltage for a programmed period, it assumes that the mains is disconnected and resets all protections. When the mains voltage exceeds the brownin level again, the system restarts. The delay between detecting a brownout (including the brownout delay time) and resetting all protections can be programmed to different values ranging from 0 s to 10 s.

Safe restart time

When the system is in protection mode and the triggered protection is programmed as safe restart, it restarts after a safe-restart time. This time can be set at different values ranging from 0.5 s to 10 s.

Fast disable

When the SNSBOOST voltage is pulled below the $V_{scp(stop)}$ level, the system enters the protection state. The response can be set to on/off, latched, or safe restart.

External OTP level

The external application temperature is measured via an NTC connected to the SNSMAINS pin. To be able to set the appropriate NTC value and OTP level, the internal

current used to measure the external NTC value can be set between 150 µA and 1050 µA in steps of 150 µA.

To avoid false triggering, an internal delay occurs before the system enters protection. This delay can be set to different values between 0.5 s and 8 s.

The response of the external OTP can be latched, safe restart, or latched after safe restart. The external OTP function can also be disabled.

Internal OTP level

The internal OTP is fixed at 135 °C. When the internal OTP is triggered, it follows the same response as selected for the external OTP, being either latched, safe restart, or latched after safe restart.

8.8.4.2 PFC general protections

Brownin/brownout level

For the brownin level, several values can be selected ranging from 67 V (AC) to 185 V (AC). For the hysteresis between the brownin and brownout level, several values can be selected from 2 V (AC) to 17 V (AC). The given values depend on the resistor values in the application and their tolerances.

When the mains voltage is below the brownout period for a selectable amount of time, the system enters the brownout state. For this time, several values can be selected ranging from 25 ms to 1.2 s.

PFC OCP level

The PFC OCP level is fixed to $V_{ocp(PFC)}$. The external sense resistor can select the corresponding current value.

PFC maximum on-time

The maximum on-time of the PFC equals 1 / minimum frequency. Where the minimum frequency set by the MTP and the possible additional frequency jitter defines the minimum frequency.

PFC coil short protection

When the PFC continuously triggers the OCP, the system eventually enters the protection state. A counter is increased by 3 every PFC switching cycle where the OCP level is exceeded. It is decreased by 1 every cycle where the level is below the OCP level. When the counter reaches 2500, 5000, or 12500, the system enters the protection state. This function can also be disabled.

PFC output OVP

The PFC output voltage is measured via the SNSBOOST pin and the DRAINPFC pin. For the OVP at the SNSBOOST pin, the following values can be selected: 2.60 V, 2.63 V, 2.65 V, or 2.70 V.

When an OVP is detected at the SNSBOOST pin, the PFC stops switching and continues again when its voltage drops below the regulation level.

For the OVP at the DRAINPFC pin, the following values can be selected: 475 V, 500 V, 525 V, or 550 V. To avoid false triggering, a delay can be selected of 100 cycles, 250 cycles, or 1000 switching cycles. During this delay, the output voltage of the PFC is limited to this maximum value.

TEA2017AAT_2

Product data sheet

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Rev. 1.2 — 31 July 2023

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44 / 66

The response of an OVP at the DRAINPFC pin can be latched, safe restart, or latched after safe restart. This function can also be disabled.

Valley detection timeout

When the PFC MOSFET is off and the current through the PFC coil becomes zero, the coil is demagnetized. Normally, shortly after the demagnetization, the drain voltage starts to ring and a valley is detected. When the system detects demagnetization but does not detect a valley shortly after, the ringing may be too small to detect a valley. So, when demagnetization is detected, it assumes a valley within a specified time. For this time, the following values can be selected: 2 µs, 3 µs, 5 µs, or 7 µs.

PFC minimum off-time

To avoid false triggering of the demagnetization and valley detection, a minimum off-time of the PFC driver output can be selected. The available values are 500 ns, 750 ns, 1000 ns, and 1500 ns.

8.8.4.3 LLC general protections

Maximum start-up time

When the LLC starts switching, it expects that its output voltage reaches the regulation level within a maximum start-up time. For the maximum start-up time, the following values can be selected: 25 ms, 50 ms, 100 ms, and 200 ms.

LLC brownout level (SNSBOOST)

When the voltage at the SNSBOOST drops below a predefined level, the LLC converter enters the protection state. When the SNSBOOST voltage exceeds the brownin level, the LLC converter starts switching again.

For the LLC brownout level at the SNSBOOST, a level in the range from 1.0 V to 2.05 V can be selected.

LLC brownin level (SNSBOOST)

The LLC brownin level defines the minimum voltage at the SNSBOOST pin before the LLC starts switching. For this level, a value ranging from 1.5 V to 2.4 V can be selected.

LLC brownout timer (SNSMAINS)

When the mains is disconnected, the PFC stops switching after its brownout delay. Normally, the LLC converter continues switching until the input voltage of the LLC drops to below a minimum ($V_{uvp(SNSBOOST)}$) level. Especially at a minimum load at the output, the LLC dropping to the minimum level can take a long time.

A timer can be initialized that also disables the LLC converter when a brownout is detected at the mains input. For this time, a value can be selected ranging from 125 ms to 6 s. The option that the LLC converter remains switching until its input voltage drops to below a minimum level can also be selected.

LLC maximum input voltage (SNSBOOST)

When an OVP is detected on the SNSBOOST pin, the PFC always stops switching. The response of the LLC can be set to either continue operation or stop switching. A delay can be set to either 5 ms, 50 ms, or 1250 ms.

Power limit

The maximum output power of the converter is limited by the controller. The limitation ensures that the applied load is below the maximum rating-selected components. For the maximum output power, several levels between 100 % and 200 % of the rated power can be selected.

OPP level 1

When the output power exceeds a first OPP level, a first counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level between 0 % and −50 % below the selected power limit can be selected.

For the time, a value between 50 ms to 40 s can be selected. The response of this protection can be latched, safe restart, or latched after safe restart. This OPP level can also be disabled.

OPP level 2

When the output power exceeds a second OPP level, a second counter is started. When the output power continuously exceeds this OPP level for a selected period, the system enters protection state. For the OPP level, a level in the range from −10 % to −50 % below the selected power limit can be selected.

For the time, a value ranging from 50 ms to 3 s can be selected. The response of this protection follows the selected response of the OPP level 1. This OPP level can also be disabled.

OPP duty cycle

When the output power exceeds the OPP with a duty cycle of 50 %, the OPP may or may not be triggered. So, the duty cycle at which the OPP is triggered eventually can be set using a parameter to 11 %, 20 %, 33 %, or 50 %.

OVP protection

In a resonant converter, the voltage at the SUPIC pin reflects the output voltage. When the SUPIC voltage exceeds a defined level, the OVP protection is triggered. The level can be set between 1 V and 16 V above the start level in steps of 1 V.

To avoid false triggering, a delay can be set at different values ranging from 10 μs to 800 μs. The response of this protection can be latched, safe restart, or latched after safe restart. This OVP function can also be disabled.

OVP duty cycle

To minimize the sensitivity of the OVP function, a duty cycle can be set at which the OVP is eventually triggered. This parameter can be set to 11 %, 20 %, 33 %, or 50 %. If, for example, the OVP delay is set to 800 μs, the duty cycle to 50 %, and the SUPIC voltage exceeds the OVP level for 300 μs and drops to below the OVP level for 500 μs, the OVP is never triggered.

OCP protection

The current in the resonant tank is measured at the SNSCURLLC pin. When the voltage at this pin exceeds the OCP level, the corresponding switch (GATELS or GATEHS) is turned off and the system starts the next cycle. So, the LLC current is limited cycle-by-cycle.

If the OCP occurs for a defined number of cycles, the OCP protection is triggered. The number of cycles can be set to different values between 5 and 1000.

The response of this protection can be latched, safe restart, or latched after safe restart. The OCP protection function can also be disabled. However, the LLC current remains limited cycle-by-cycle.

8.8.5 Power good settings

The power good function gives a prewarning to the load that the converter is switched off due to disconnected mains or a triggered protection.

Power good time

The power good time is the time between the power good signal indicating that the converter is about to be switched off and the time the converter eventually stops switching. This delay can be set to 4 ms, 6 ms, 8 ms, or 10 ms.

Power good at OTP

The power good signal can give a prewarning when the converter is switched off due to an OTP detection. The OTP can be either an internal or an external OTP.

This function can be enabled or disabled. The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time.

Power good at OPP

The power good signal can give a prewarning when the converter is switched off due to an OPP detection. The prewarning can be given when the output power exceeds the OPP level1 or OPP level2 for the defined time.

This function can be enabled or disabled. The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time.

Power good at mains brownout

The power good signal can give a prewarning when the LLC converter is switched off due to a brownout detection at the mains input of the converter.

This function can be enabled or disabled. The delay between the transition of the power good signal and the moment that the converter stops switching equals the power good time.

Power good at LLC brownout level (SNSBOOST)

When the measured voltage at the SNSBOOST pin drops to below the selected LLC brownout level, the LLC converter stops switching. It normally occurs due to a disconnected mains.

The power good signal can give a prewarning when the converter is switched off due to this LLC brownout detection. When the voltage at the SNSBOOST drops to below a selectable value, the power good feature is triggered. The level can be selected between 1 V and 2.05 V.

Power good at OVP (SNSBOOST)

The TEA2017AAT offers a setting option to stop the LLC operation at an SNSBOOST OVP. When the LLC converter is switched off due to an SNSBOOST OVP, the power good signal can give a prewarning. This function can be enabled or disabled. The delay

between the transition of the power good signal and the moment the converter stops switching equals the power good time.

Power good ready delay

When the output voltage is in regulation after start-up, power good indicates that the output voltage is in regulation. A delay can be set between the time the output voltage reaches the regulation level and the transition of the power good signal. This delay can be set at different values between 0 s and 1 s.

Power good transition time

The power good function is combined with the feedback network connected at the SNSFB pin. To avoid that a trigger of the power good function disturbs the regulation loop, its transition time must have a predefined value. This time can be set at 0.85 ms, 1.8 ms, 2.6 ms, or 3.5 ms.

9   Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
$V_{DRAINPFC}$	voltage on pin DRAINPFC	during mains surge t < 0.5 s; 10 times at a 0.1 Hz interval	−0.4	+685	V
$SR_{max(DRAINPFC)}$	maximum slew rate on pin DRAINPFC		−50	+50	V/ns
V_{SUPIC}	voltage on pin SUPIC		−0.4	+36	V
V_{SUPHS}	voltage on pin SUPHS	during mains surge t < 0.5 s; 10 times at a 0.1 Hz interval	−0.3	+685	V
		regarding pin HB	− 0.4	+13	V
V_{GATEHS}	voltage on pin GATEHS		V_{HB} − 0.4	V_{SUPHS} + 0.4	V
V_{HB}	voltage on pin HB	during mains surge; t < 0.5 s; 10 times at a 0.1 Hz interval	−3	+685	V
		t < 1 µs	−13	-	V
$SR_{max(HB)}$	maximum slew rate on pin HB		−70	+70	V/ns
V_{GATELS}	voltage on pin GATELS	[1]	−0.4	+14	V
$V_{GATEPFC}$	voltage on pin GATEPFC	[1]	−0.4	+14	V
V_{SNSCAP}	voltage on pin SNSCAP		−0.4	+12	V
$V_{SNSCURLLC}$	voltage on pin SNSCURLLC		−0.4	+12	V
$V_{SNSCURPFC}$	voltage on pin SNSCURPFC	t < 0.1 s; voltage at external series resistance of 100 Ω, connected to pin SNSCURPFC	−18	+12	V
		DC; maximum	−0.4	+12	V

Table 5. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{SNSFB}	voltage on pin SNSFB		−0.4	+12	V
$V_{SNSBOOST}$	voltage on pin SNSBOOST		−0.4	+12	V
$V_{SNSMAINS}$	voltage on pin SNSMAINS		−0.4	+12	V
General					
P_{tot}	total power dissipation	T_{amb} < 75 °C	-	0.7	W
T_j	junction temperature		−40	+150	°C
T_{stg}	storage temperature		−55	+150	°C
Latch-up					
I_{lu}	latch-up current	all pins; according to JEDEC; standard 78D	−100	+100	mA
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	human body model			
		SUPHS, GATEHS, HB, and DRA INPFC pins	−1000	+1000	V
		other pins	−2000	+2000	V
		charged device model			
		all pins	−500	+500	V

[1] Although the GATE pins are output pins, the maximum voltage of these pins must not exceed the maximum drive output voltage by 20 %.

10 Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	In free air; JEDEC test board	107	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	In free air; JEDEC test board	60	K/W

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Product data sheet

Rev. 1.2 — 31 July 2023

50 / 66

11 Characteristics

Table 7. Characteristics

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DRAINPFC pin						
$I_{off(DRAINPFC)}$	off-state current on pin DRA INPFC	$V_{DRAINPFC}$ = 400 V; V_{SUPIC} = 19 V	2	4	8	µA
ΔV_I	input voltage difference	input voltage difference between DRAINPFC and SUPIC pins; $I_{DRAINPFC}$ = 8.5 mA	9	11	13	V
$I_{ch(SUPIC)}$	charge current on pin SUPIC	$V_{DRAINPFC}$ = 30 V; V_{SUPIC} = 0 V	−10.0	−8.5	−7.0	mA
SUPIC pin						
$V_{start(SUPIC)}$	start voltage on pin SUPIC		18.2	19.0	19.7	V
$V_{start(hys)SUPIC}$	start voltage hysteresis on pin SUPIC		−0.9	−0.7	−0.5	V
$V_{low(hys)SUPIC}$	low voltage hysteresis on pin SUPIC		0.5	0.7	0.9	V
$V_{low(SUPIC)}$	low voltage on pin SUPIC		11.5	12.0	12.5	V
$V_{uvp(SUPIC)}$	undervoltage protection voltage on pin SUPIC		9.6	10.0	10.4	V
$\Delta_{(vlow\text{-}vuvp)SUPIC}$	low voltage to undervoltage protection voltage difference on pin SUPIC	$V_{low} - V_{uvp}$	1.7	2.0	2.3	V
$V_{rst(SUPIC)}$	reset voltage on pin SUPIC		8.6	9.0	9.4	V
$I_{CC(SUPIC)}$	supply current on pin SUPIC	non-operating mode; I_{snsfb} = −100 µA; I_{snscap} = −100 µA [1]	700	890	1100	µA
		operating mode; f_{HB} = 100 kHz; I_{snsfb} = −80 µA; I_{snscap} = −100 µA; driver pins open [1]	6	8	10	mA
Output overvoltage protection						
$V_{O(ovp)SUPIC}$	output overvoltage protection voltage on pin SUPIC		27.9	28.7	29.5	V
$t_{d(ovp)SUPIC}$	overvoltage protection delay time on pin SUPIC		45	50	55	µs
Mains voltage sensing (SNSMAINS pin)						
$I_{clamp(max)}$	maximum clamp current	$V_{SNSMAINS}$ = 9.5 V	2.5	3.5	4.5	mA
$I_{I(lim)SNSMAINS}$	limiting input current on pin SNSMAINS	SNSMAINS limit-measuring input current	17.2	18.6	20.0	µA

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Product data sheet

Rev. 1.2 — 31 July 2023

51 / 66

Table 7. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{bi}	brownin current		5.3	5.5	5.7	μA
I_{bo}	brownout current		4.6	4.8	5.0	μA
$I_{bo(hys)}$	hysteresis of brownout current	$I_{bi} - I_{bo}$	0.66	0.73	0.80	μA
$t_{d(det)bo}$	brownout detection delay time	PFC	45	50	55	ms
		LLC	225	250	275	ms
External overtemperature measurement						
$I_{o(SNSMAINS)}$	output current on pin SNS MAINS		−645	−600	−565	μA
$t_{det(max)NTC}$	NTC maximum detection time		45	50	55	μs
$V_{det(SNSMAINS)}$	detection voltage on pin SNS MAINS	NTC measurement; $I_{SNSMAINS}$ = −600 μA	2.89	3.08	3.27	V
$t_{d(otp)}$	overtemperature protection delay time		3.6	4.0	4.4	s
X-capacitor discharge						
$t_{d(dch)}$	discharge delay time		180	200	220	ms
SNSCURPFC pin						
$I_{o(min)SNSCURPFC}$	minimum output current on pin SNSCURPFC	for open pin protection; $V_{SNSCURPFC}$ = 500 mV	−0.8	−0.6	−0.4	μA
$V_{det(SNSCURPFC)}$	detection voltage on pin SNS CURPFC	open pin detection level	190	235	280	mV
$V_{det(demag)}$	demagnetization detection voltage		−15	−10	−5	mV
$V_{ocp(PFC)}$	PFC overcurrent protection voltage		−320	−300	−275	mV
$t_{d(swoff)driver}$	driver switch-off delay time	dV/dt ≤ −0.5 V/μs	300	375	450	ns
Valley sensing (DRAINPFC pin)						
$\Delta V_{det(min)}/\Delta t$	minimum slope detection voltage		−50	-	-	V/μs
$\Delta V_{det(min)}$	minimum detection voltage change	ringing frequency = 1 MHz	9	15	21	V
$t_{to(vrec)}$	valley recognition time-out time		6.3	7.0	7.7	μs
PFC						
PFC timing						
$t_{off(PFC)min}$	PFC minimum off-time		0.45	0.50	0.55	μs
PFC start-up soft-start time						
$t_{start(soft)}$	soft start time		23	25	28	ms

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Product data sheet

Rev. 1.2 — 31 July 2023

52 / 66

Table 7. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PFC frequency						
$f_{sw(PFC)min}$	minimum PFC switching frequency		36	40	44	kHz
$f_{sw(PFC)max}$	maximum PFC switching frequency		67	75	83	kHz
GATEPFC pin						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC}$ = 4 V; V_{SUPIC} ≥ 13 V [1]	−0.60	−0.45	−0.30	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC}$ = 2 V; V_{SUPIC} ≥ 13 V [1]	0.45	0.60	0.75	A
		$V_{GATEPFC}$ = 11 V; V_{SUPIC} ≥ 13 V [1]	2.0	2.5	3.0	A
$V_{o(max)GATEPFC}$	maximum output voltage on pin GATEPFC	V_{SUPIC} = 19 V	11.0	-	14.0	V
SNSBOOST pin						
PFC part						
$I_{pd(SNSBOOST)}$	pull-down current on pin SNS BOOST	at $V_{SNSBOOST}$ = $V_{scp(stop)}$	25	50	75	nA
$V_{reg(SNSBOOST)}$	regulation voltage on pin SNS BOOST		2.475	2.500	2.525	V
$V_{stop(ovp)PFC}$	PFC overvoltage protection stop voltage		2.59	2.63	2.67	V
$V_{prot(ovp)PFC}$	PFC overvoltage protection protection voltage	via pin DRAINPFC	450	475	500	V
$t_{leb(ovp)PFC}$	PFC overvoltage protection leading-edge blanking time	via pin DRAINPFC	360	400	440	ns
LLC part						
$V_{uvp(SNSBOOST)}$	undervoltage protection voltage on pin SNSBOOST		1.60	1.65	1.70	V
$V_{start(SNSBOOST)}$	start voltage on pin SNS BOOST		2.23	2.30	2.37	V
$V_{det(SNSBOOST)}$	detection voltage on pin SNS BOOST	Power good detection voltage	1.715	1.750	1.785	V
$\Delta V_{reg-det}$	voltage difference between regulation and detection	pin SNSBOOST; indication of the power good delay	0.72	0.75	0.78	V
Fast disable function						
$V_{scp(stop)}$	stop short-circuit protection voltage		0.37	0.39	0.41	V

Table 7. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{scp(start)}$	start short-circuit protection voltage		0.40	0.45	0.50	V
$t_{fltr(scp)}$	short-circuit protection filter time		4	10	15	µs
SNSCAP pin						
$V_{AV(regd)SNSCAP}$	regulated average voltage on pin SNSCAP	regulated average of $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$	2.44	2.50	2.56	V
$I_{bias(max)SNSCAP}$	maximum bias current on pin SNSCAP		−245	−210	−175	µA
$V_{range(SNSCAP)}$	voltage range on pin SNSCAP	SNSCAP voltage range for the high-side comparator, $V_{hs(SNSCAP)}$.	2.35	-	4.50	V
		SNSCAP voltage range for the low-side comparator, $V_{ls(SNSCAP)}$.	0.50	-	2.65	V
V_{acc}	voltage accuracy	SNSCAP comparator voltage accuracy	−10	-	+10	mV
$\Delta V_{th(SNSCAP)}$	threshold voltage difference on pin SNSCAP	$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 200 %; $V_{SNSBOOST}$ < 1.9 V	3.12	3.27	3.42	V
		$V_{hs(SNSCAP)} - V_{ls(SNSCAP)}$; P_{out} = 100 %; $V_{SNSBOOST}$ = 2.5 V	0.93	1.01	1.09	V
t_d	delay time	delay between exceeding V_{caph}/V_{capl} and driver off; dV/dt = 0.1 V/µs	-	-	125	ns
SNSCURLLC pin						
$V_{bias(SNSCURLLC)}$	bias voltage on pin SNS CURLLC		2.4	2.5	2.6	V
$R_{O(SNSCURLLC)}$	output resistance on pin SNS CURLLC		45	55	65	kΩ
$V_{lmtr(ocp)}$	overcurrent protection voltage limiter	soft-start overcurrent limiter	0.66	0.75	0.83	V
negative level $V_{SNS CURLLC} - V_{bias(SNSCURLLC)}$			−1.65	−1.50	−1.35	V
negative level $V_{SNS CURLLC} - V_{bias(SNSCURLLC)}$			−115	−100	−83	mV
$V_{det(zero)}$	zero detection voltage	detected as ≥ 0	−16	−11	−6	mV
		detected as ≤ 0	6	11	16	mV

Table 7. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SNSFB pin						
$V_{low(SNSFB)}$	low voltage on pin SNSFB	indicating iPowerGood = '1'; 0 µA < I_{opto} < 3.5 mA.	0.43	0.50	0.57	V
$V_{high(SNSFB)}$	high voltage on pin SNSFB	indicating iPowerGood = '0'; 0 µA < I_{opto} < 3.5 mA.	3.3	3.5	3.8	V
t_t	transition time	PowerGood transition time	1.5	1.8	2.0	ms
Optobias regulator						
$I_{reg(SNSFB)}$	regulation current on pin SNSFB		−90	−80	−70	µA
Burst mode regulator						
$I_{start(burst)}$	burst mode start current	LLC burst mode	−110	−100	−90	µA
$I_{stop(burst)}$	burst mode stop current		−220	−200	−180	µA
Burst mode						
$f_{burst(max)}$	maximum burst mode frequency		720	800	880	Hz
$\delta_{en(burst)}$	burst mode duty cycle enable	enable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst-on time / set LLC burst period	49	50	51	%
$N_{cy(en)burst}$	burst mode enable number of cycles	enable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst-on time / set LLC burst period	16	16	16	-
$\delta_{dis(burst)}$	burst mode disable duty cycle	disable of PFC burst mode; duty cycle of LLC burst mode; duty cycle = measured LLC burst-on time / set LLC burst period	74	75	76	%
$t_{d(burst)exit}$	burst-mode exit delay time		3.6	4	4.4	ms
Power good characteristics (pin SNSFB)						
t_d	delay time	delay power good after output voltage ready	4.5	5.0	5.5	ms
		power good delay before protection	3.6	4.0	4.4	ms
LLC timing						
$t_{on(min)LLC}$	LLC minimum on-time		1105	1230	1355	ns
$t_{on(max)LLC}$	LLC maximum on-time		18	20	22	µs

Table 7. Characteristics...*continued*

T_{amb} = 25 °C; V_{SUPIC} = 19.5 V; all voltages are measured with respect to GND; currents are positive when flowing into the IC; unless otherwise specified. Expected values for different MTP settings (min/typ/max) are provided in the documentation in the Ringo software.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Overpower protection						
$t_{startup(max)}$	maximum start-up time		90	100	110	ms
$t_{d(opp)}$	overpower protection delay time	OPP 1	45	50	55	ms
HB pin						
$\Delta V_{det(min)}/\Delta t$	minimum slope detection voltage	positive and negative minimum slope detection level	-	-	120	V/µs
$\Delta V_{det(max)}/\Delta t$	maximum slope detection voltage	positive and negative maximum slope detection level	50	-	-	V/ns
$t_{no(min)}$	minimum non-overlap time		200	230	260	ns
$t_{no(max)}$	maximum non-overlap time		0.99	1.10	1.21	µs
GATELS and GATEHS pins						
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{GND}$ = 4 V; [1] $V_{SUPIC} \geq$ 13 V	−0.55	−0.40	−0.25	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{GND}$ = 2 V; [1] $V_{SUPIC} \geq$ 13 V	0.4	0.5	0.6	A
		$V_{GATELS} - V_{GND}$ = 11 V; [1] $V_{SUPIC} \geq$ 13 V	2.0	2.5	3.0	A
$V_{O(min)GATELS}$	minimum output voltage on pin GATELS	$V_{SUPIC} \geq$ 9.5 V; on-time $\geq$ 4 µs	8	-	-	V
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 4 V [1]	−0.55	−0.40	−0.25	A
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB}$ = 2 V [1]	0.4	0.5	0.6	A
		$V_{GATEHS} - V_{HB}$ = 11 V [1]	2.0	2.5	3.0	A
$V_{O(min)GATEHS}$	minimum output voltage on pin GATEHS	$V_{SUPHS} - V_{HB} \geq$ 9.5 V	9	-	-	V
SUPHS pin						
$V_{rst(SUPHS)}$	reset voltage on pin SUPHS	+25 °C < T < 125 °C	5.5	7.2	8.2	V
$t_{d(flr)}$	fast latch reset delay time		45	50	55	ms
I²C communication						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		1.4	-	5.0	V
$I_{pd(SNSCAP)}$	pull-down current on pin SNSCAP	To ensure proper operation, [2] the external pull-up must always be lower than 6.8 mA.	6.8	-	-	mA
Overtemperature protection						
T_{otp}	overtemperature protection trip		120	135	150	°C

[1] Covered by correlating measurement
[2] As the minimum limit determines the application design, the maximum limit is not relevant.
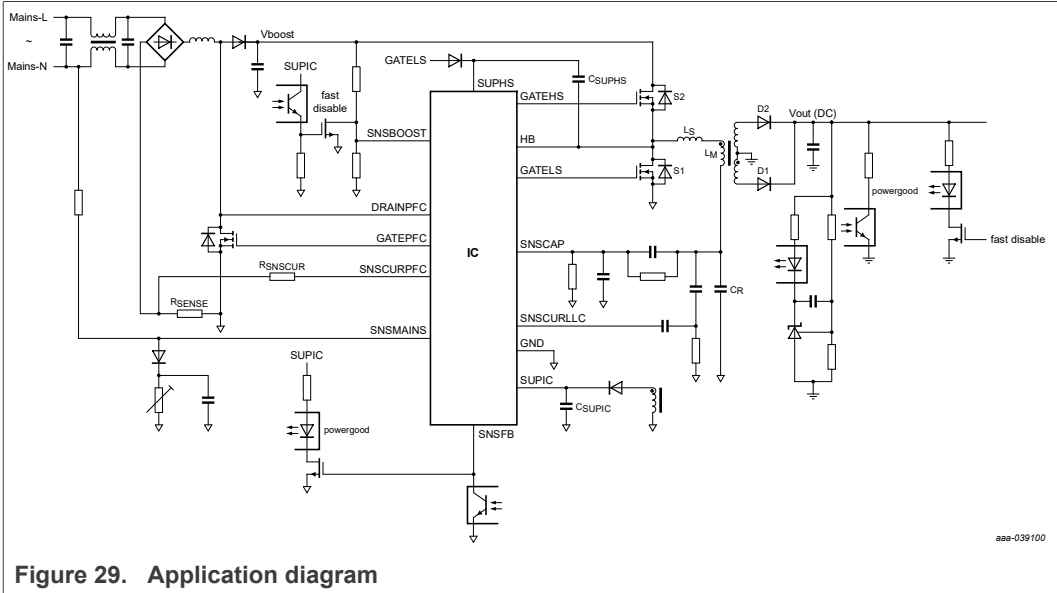
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Product data sheet

Rev. 1.2 — 31 July 2023

56 / 66

12 Application information

Figure 29. Application diagram

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Product data sheet

Rev. 1.2 — 31 July 2023

57 / 66

13 Ringo parameter settings

Table 8. Ringo parameter/IC parameter settings

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
1	NXP ID code	nxp_id_code	0x02	-	2
2	PFC OCP	pfc_ocp	OK	-	0
3	PFC OVP (DRAINPFC)	pfc_ovp_pfcdrain	OK	-	0
4	PFC OVP (SNSBOOST)	pfc_ovp_snsboost	OK	-	0
5	LLC OPP 1	llc_opp1	OK	-	0
6	LLC OPP 2	llc_opp2	OK	-	0
7	LLC maximum start-up time	llc_max_startup_time	OK	-	0
8	LLC OCP	llc_ocp	OK	-	0
9	LLC OVP	llc_ovp_prot	OK	-	0
10	External OTP	ext_otp	OK	-	0
11	Internal OTP	int_otp	OK	-	0
12	Fast disable	fast_disable	OK	-	0
13	LLC maximum on-time	llc_max_on_time	OK	-	0
14	LLC maximum Iopto	llc_max_iopto	OK	-	0
15	LLC capacitive mode	llc_cap_mode	OK	-	0
16	MTP read failure	mtp_read_fail	OK	-	0
17	OPP via SUPIC UVP	opp_via_supic_uvp	OK	-	0
18	PFC soft-start time	t_start	25	ms	0
19	PFC gain	pfc_gain	0.5	-	8
20	PFC current scaler	pfc_cur_scaler	1.138	-	4
21	Write lock	write_lock	write enabled	-	0
22	Read lock	read_lock	read enabled	-	0
23	PFC burst mode level	pfc_burstmode_lvl	50	%	0
24	PFC burst mode level hysteresis	pfc_burstmode_lvl_hyst	25	%	0
25	PFC burst mode SNSBOOST ripple	vburst_ripple	70	mV	1
26	PFC minimum off-time	tmin_off	500	ns	0
27	Brownin level	brownin_lvl	5.5	µA	0
28	Brownin/brownout hysteresis	brownin_hys	0.75	µA	0
29	Brownout delay	t_brownout	50	ms	0
30	PFC valley detection	pfc_valley_disable	enabled	-	0
31	dV/dt ratio switch-on/maximum	ratio_valley_detect	0.5	-	0
32	Mains resistor value	rmains	20	MΩ	0
33	Ipfc_peak for Fmin	vrsense_fmin	55	-	0
34	Delta Ipfc_peak for Fmax-Fmin	vrsense_fmax_fmin	110	-	0

Table 8. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
35	Min PFC freq phase value	phi_imin	0.18	-	0
36	Max-min PFC freq phase value	phi_imin_imax	0.14	-	0
37	PFC minimum switching frequency	min_pfc_freq	40	kHz	0
38	PFC maximum switching frequency	max_pfc_freq	75	kHz	1
39	PFC mode	pfc_mode	DCM/QR/CCM	-	1
40	PFC jitter frequency modulation	freq_jitter_mod	disabled	-	0
41	PFC jitter frequency amplitude	freq_jitter_ampl	15	%	0
42	PFC gamma value	pfc_gamma	36	-	36d
43	Mains SNS resistors	nr_mains_resistors	1	resistor	0
44	PFC phase factor	pfc_phase	0.9375	-	15d
45	LLC soft-start speed	llc_tsoftstart	7	X	0
46	SUPIC control near UVP	dis_vlow	enabled	-	0
47	SUPIC start level	sup_start	19	V	0
48	LLC converter	llc_disable	enabled	-	0
49	Vdump level	vdump	2.55	V	1
50	Capacitive mode regulation level	capm_lvl	100	mV	0
51	Maximum on-time	llc_max_on	20	µs	0
52	LLC LP mode	lpmode_dis	enabled	-	0
53	OTP/external burst mode select	ext_burstmode	Ext OTP	-	0
54	LLC non-overlap mode	llc_non_overlap	adaptive	-	0
55	Maximum non-overlap time	t_no_max	1.1	µs	0
56	Minimum non-overlap time	t_no_min	230	ns	0
57	Opto current level	iopto	80	µA	0
58	Burst-on end by opto current	iopto_bm_end	2.5	X	0
59	SNSBOOST compensation	snsb_comp	−1.4	-	0
60	HP-LP transition level	hp_lp_lev	30	%	0
61	HP-LP hysteresis	hp_lp_hys	20	%	0
62	Opto regulation level	opto_reg_level	standard	-	0
63	Opto regulation gain increase	opto_reg_gain_incr	96	-	0
64	LP number of peaks	lp_nr_peaks	2	-	0
65	LP-BM transition level	lp_bm_lev	10	%	0
66	BM-LP hysteresis	bm_lp_hys	50	%	7
67	BM LP hysteresis filter	bm_lp_filt	4	-	0
68	LP-BM delay time	lp_bm_del	0	s	0
69	Zero power slope	min_slope	6	mV/µs	0
70	dVcap offset	vcap_offset	0	mV	0

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TEA2017AAT/2

Digital configurable LLC and multimode PFC controller

Table 8. **Ringo parameter/IC parameter settings**...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
71	BM frequency	bm_freq	800	Hz	0
72	BM energy-per-cycle increase	bm_incr	1	X	0
73	Minimum cycles in burst	min_nr_cycl	3	-	0
74	Number of BM soft-start cycles	nr_bm_sstart	2	-	2
75	Number of BM soft-stop cycles	nr_bm_sstop	2	-	2
76	Burst mode exit delay	bm_exit_del	4000	µs	0
77	Allow CCM at demag timeout	allow_ccm_demag_to	disable	-	0
78	PFC current gain	pfc_cur_gain	344	-	344d
79	Slope of 4th BM soft-start cycle	start_cycle4	2	-	0
80	Slope of 3rd BM soft-start cycle	start_cycle3	6	-	0
81	Slope of 2nd BM soft-start cycle	start_cycle2	10	-	5
82	Slope of 1st BM soft-start cycle	start_cycle1	96	-	0
83	Slope of 4th BM soft-stop cycle	stop_cycle4	96	-	0
84	Slope of 3rd BM soft-stop cycle	stop_cycle3	24	-	0
85	Slope of 2nd BM soft-stop cycle	stop_cycle2	10	-	4
86	Slope of 1st BM soft-stop cycle	stop_cycle1	4	-	2
87	External OTP current level	eotp_lvl	600	µA	0
88	External OTP delay time	t_eotp	4	s	0
89	OTP mode	otp_ltch	safe restart	-	0
90	OTP number of restarts to latch	otp_nr_rest	0	-	0
91	Fast disable by SNSBOOST	llc_fast_disable	latched	-	3
92	X-cap discharge delay time	t_xcap_disch	200	ms	0
93	Fast latch reset delay time	t_flr	50	ms	0
94	Safe restart timer	sr_time	1	s	0
95	PFC OVP level (SNSBOOST)	ovp_lvl	2.63	V	0
96	PFC OVP (DRAINPFC)	ovpprot_lvl	475	V	0
97	OVP-DRAINPFC protection delay	t_ovpprot	250	cycles	0
98	OVP-DRAINPFC mode	ovp_ltch	safe restart	-	0
99	OVP-DRAINPFC no. of restarts	ovp_nr_rest	0	-	0
100	PFC short-winding delay	pfc_shortwinding_delay	5000	-	0
101	PFC maximum ringing time	max_tring_pfc	7	µs	3
102	LLC soft-start current limit	max_llc_istartup	0.75	V	0
103	Maximum (start-up) frequency	max_llc_freq	350	kHz	0
104	Maximum start-up time	t_start_max	100	ms	0
105	LLC maximum ringing time	max_tring_llc	5	µs	0
106	LLC OCP filter	llc_tocp	5	-	0

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Product data sheet

Rev. 1.2 — 31 July 2023

60 / 66

Table 8. Ringo parameter/IC parameter settings...*continued*

	Ringo parameter name	IC parameter name	Value	Unit	Binary value
107	LLC OCP mode	llc_ocp_ltch	safe restart	-	0
108	OCP restarts to latch	llc_ocp_nr_rest	0	-	0
109	LLC (SUPIC) OVP level	llc_ovp	10	V	0
110	LLC (SUPIC) OVP delay	llc_tovp	50	μs	0
111	Down-counts/up-count (SUPIC) OVP	llc_ovp_nr_dwn	1	-	0
112	(SUPIC) OVP mode	llc_ovp_ltch	safe restart	-	0
113	OVP restarts to latch	llc_ovp_nr_rest	0	-	0
114	LLC brownin level (SNSBOOST)	snsb_start	2.3	V	6
115	LLC brownout level (SNSBOOST)	snsb_stop	1.65	V	3
116	Disable LLC after SNSBOOST OVP	dis_ovp_snsb	off	-	3
117	Disable LLC after mains brownout	llc_dis_bo	250	ms	0
118	OPP1 level	opp1_lvl	−20	%	0
119	OPP1 time delay	opp1_time	50	ms	0
120	OPP2 level	opp2_lvl	−10	%	0
121	OPP2 time delay	opp2_time	infinite	-	0
122	Down-counts/up-count OPP	opp_nr_dwn	1	-	0
123	OPP mode	opp_ltch	safe restart	-	0
124	OPP restarts to latch	opp_nr_rest	0	-	0
125	LLC power limitation level	pow_lim	155	%	0
126	Power good inverted	pgood_inv	disabled	-	0
127	Power good SNSBOOST reset level	pgd_lvl	1.75	V	0
128	Power good at mains brownout	pgd_bo	enabled	-	0
129	Power good at OPP	pgd_opp	enabled	-	0
130	Power good at OTP	pgd_otp	enabled	-	0
131	Power good signal at SNSBOOST OVP	pgd_ovp_sbo	enabled	-	0
132	Power good signal edge (SNSFB)	pgd_tr	1.8	ms	0
133	Power good delay	pgd_del	5	ms	0
134	Power good time to protection	pgd_tim	4	ms	0
135	Vendor code	mtp_code	0	-	0
136	PFC soft-start time burst mode	-	short	-	-
137	PFC soft-stop time burst mode	-	normal	-	-

TEA2017AAT_2

Product data sheet

Rev. 1.2 — 31 July 2023

61 / 66

14 Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm　　　　　**SOT109-1**
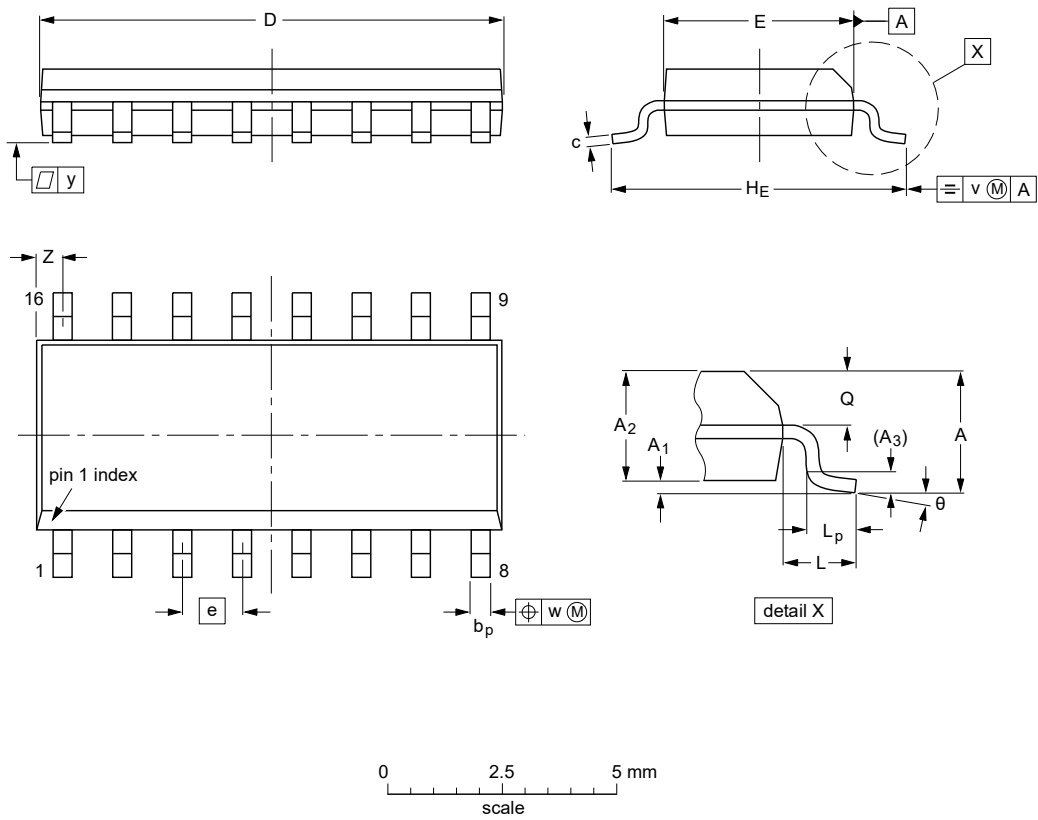
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	HE	L	Lₚ	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Figure 30. Package outline SOT109-1 (SO16)

Product data sheet　　　　　**Rev. 1.2 — 31 July 2023**

15 Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA2017AAT_2 v.1.2	20230731	Product data sheet	-	TEA2017AAT_2 v.1.1
Modification:	• Table 8 has been added to Section 13.			
TEA2017AAT_2 v.1.1	20220224	Product data sheet	-	TEA2017AAT_2 v.1
TEA2017AAT_2 v.1	20210519	Product data sheet	-	-

16 Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1]   Please consult the most recently issued document before initiating or completing a design.
[2]   The term 'short data sheet' is explained in section "Definitions".
[3]   The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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TEA2017AAT_2

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Product data sheet

Rev. 1.2 — 31 July 2023

64 / 66

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