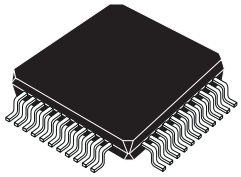
TDA7502

In-car remote amplifier DSP

Features

- 24-Bit fixed-point dsp core delivering up to 50 MIPS
- 2 x 1024 x 24 Bit of RAM for X and Y data memory.
- 3072 x 24 Bit of RAM for program also usable for delay
- Serial audio interface.
- Debug port.
- Control interface for external GPIOs, interrupts, and reset.
- SPI and I^2C for communication between external micro and DSP. Both master and slave operating modes.
- PLL clock oscillator
- 5V-tolerant 3.3V I/O interface



LQFP44 (10x 10x 1.4mm)

The computational power and the memory configuration make this device particularly suitable for in car equalisation. This device will offer the best trade-off between performance and cost when coupled with the TDA7535, or other devices of the same family. A library of sound processing functions is available for this device; some of these functions are: parametric equaliser, cross over filters, acoustic delay, dynamic compression, vol/bass/treble/fader, active equalisation, Stereo spatial enhancement and more.

Description

This device is a high-performance, fully programmable DSP, suitable for a wide range of applications and particularly for audio and sound processing. It contains a 24-bit 50 MIPS DSP core, several interfaces for control and data, plus a configurable PLL.

Order codes

Part numbers	Package	Packing
TDA7502	LQFP44 (10x 10x 1.4mm)	Tube
TDA7502013TR	LQFP44 (10x 10x 1.4mm)	Tape and Reel

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1 Block diagram and PIN description

Figure 1. Block diagram

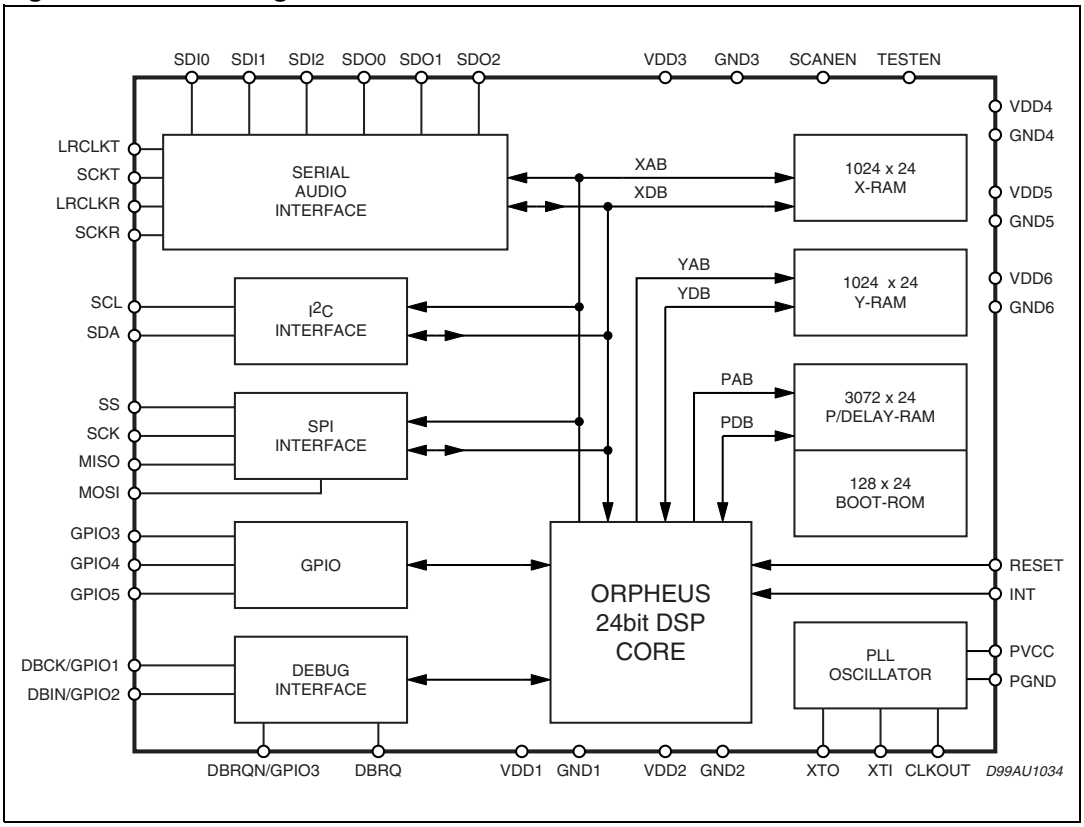


Figure 2. Pin connection (Top view)

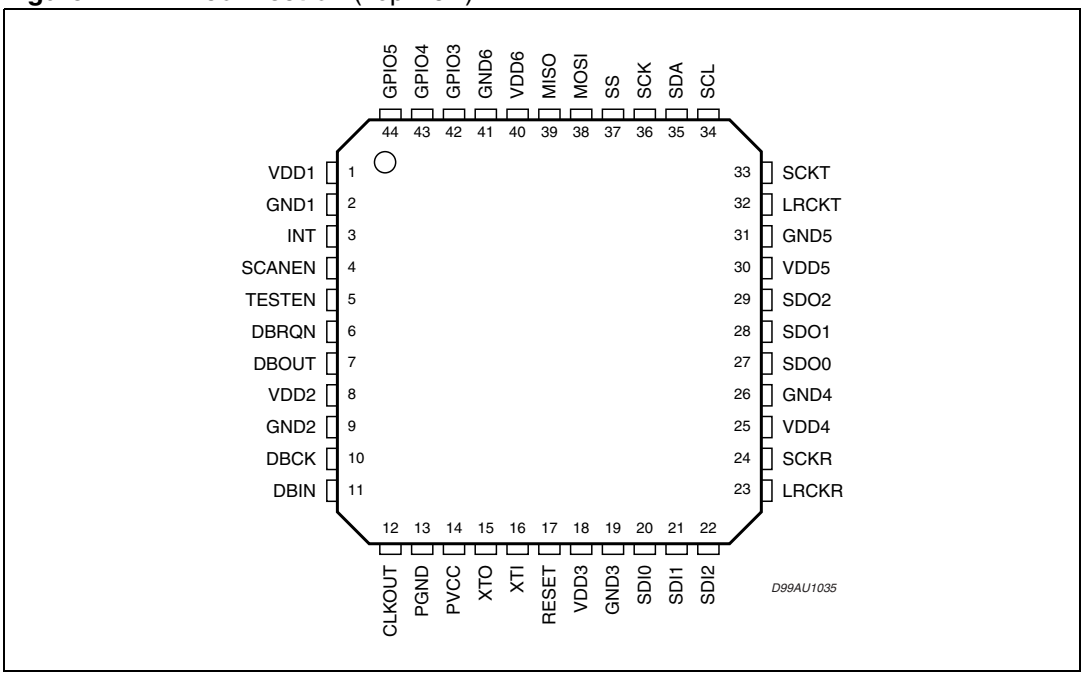


Table 1. Pin description

N.	Name	Type	Reset status	Function
1	VDD1	P	–	3.3V core supply.
2	GND1	G	–	Core ground.
3	INT	I/O	–	External interrupt line (Input/Output). When this line is asserted low, the DSP may be interrupted. Acts as IRQA line of DSP core.
4	SCANEN	I	–	SCAN enable when active with TESTEN also active, controls theshifting of the internal scan chains.
5	TESTEN	I	–	Test enable when active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting
6	DBRQN	I	–	Debug port request Input. A means of entering the Debug mode of operation.
7	DBOUT/GPIO2	I/O	I	The serial data output for the Debug port. Can also be used as a GPIO.
8	VDD2	I	–	3.3V core supply.
9	GND2	I	–	Core ground.
10	DBCK/GPIO0	I/O	I	Debug port Bit Clock/Chip status 1. The serial clock for the Debug Port is provided when an input. When an output, provides information about the chip status. Can also be used as GPIO
11	DBIN/GPIO1	I/O	I	Debug port Serial Input/Chip status 0. The serial data input for the Debug Port is provided when an input. When an output, provides information about the chip status. Can also be used as GPIO.
12	CLKOUT	O	–	Output clock.
13	PGND	G	–	PLL clock ground Input. Ground connection for oscillator circuit.
14	PVCC	P	–	PLL clock power supply. Positive supply for PLL clock oscillator.
15	XTO (1)	O	High	Crystal oscillator output. Crystal oscillator output drive.
16	XTI (1)	I	–	Crystal oscillator input. External clock input or crystal connection.
17	RESET	I/O	I	System reset. A logic low level applied to RESET input initializes DSPs. During debug mode if this pin is pulled low in while the DBRQN line is pulled low then the DSP pointed to by the DBSEL pin will be reset.
18	VDD3	P	–	3.3V supply.
19	GND3	G	–	Ground.
20	SDI0	I	–	SDI0 is a stereo digital audio data input pin channel 0.
21	SDI1	I	–	SDI1 is a stereo digital audio data input pin channel 1.
22	SDI2	I	–	SDI2 is a stereo digital audio data input pin channel 2.

Table 1. Pin description (continued)

N.	Name	Type	Reset status	Function
23	LRCKR	I/O	–	Left-right clock for SAI Receiver. Master or slave.
24	SCKR	I/O	–	SAI receive bit clock. Master or slave.
25	VDD4	P	–	3.3V supply.
26	GND4	G	–	Ground.
27	SDO0	O	High	SDO0 is a stereo digital audio data output pin channel 0.
28	SDO1	O	High	SDO1 is a stereo digital audio data output pin channel 1.
29	SDO2	O	High	SDO2 is a stereo digital audio data pin channel 2.
30	VDD5	P	–	3.3V supply.
31	GND5	G	–	Ground.
32	LRCKT	I/O	–	SAI transmit left/right clock. Master or slave.
33	SCKT	I/O	–	SAI transmit bit clock. Master or slave.
34	SCL	I/O	–	Clock line for I^2C bus. Schmitt trigger input.
35	SDA	I/O	–	Data line for I^2C bus. Schmitt trigger input.
36	SCK	I	–	Bit clock for SPI control interface.
37	SS	I	–	Slave select input pin for SPI control interface.
38	MOSI	I/O	–	Serial data output for SPI type serial port when in SPI master mode and serial data input when in SPI slave mode.
39	MISO	I/O	–	Serial data input for SPI style serial port when in SPI master mode and serial data output when in SPI slave mode.
40	VDD6	P	–	3.3V supply.
41	GND6	G	–	Ground.
42	GPIO3	I/O	–	This pin is dedicated as general I/O.
43	GPIO4	I/O	–	This pin is dedicated as general I/O.
44	GPIO5	I/O	–	This pin is dedicated as general I/O.

1. XTI and XTO are not 5V tolerant

2 Electrical specifications

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{dd}	DC supply voltage	-0.5 to 4.6	V
V_{in}	Digital input voltage (XTI and XTO only)	-0.5 to (V_{DD} +0.5)	V
V_{in}	Digital input voltage (1)	6.5	V
T_j	Operating junction temperature range	-40 to 125	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. When the IC is powered.

Warning: Operation at or beyond these limit may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$ (1)	Thermal resistance junction to ambient	68	°C/W

1. In still air.

Table 4. Recommended DC operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{dd}	3.3V power supply voltage		3.15	3.3	3.45	V

Table 5. Current consumption

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{dd}	Maximum current	@3.3V and T_j =125°C			250	mA

Note: 50MHz internal DSP clock

Table 6. PII characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	Lock time (1)	@3.3V and T_j = 125°C			3	ms
F_{vco}	VCO frequency (2)		70		140	MHz

1. Depending on VCO output frequency.
2. $F_{dsp} = F_{vco}/2$ when PLL is running

Table 7. Oscillator characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{osc}	Max oscillator frequency (XTI)	@ 3.3V and T_j = 125°C	8		12.5	MHz

Table 8. General interface electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{il}	Low level input current without pullup device	V_i = 0V (1)			1	µA
I_{ih}	High level input current without pullup device	$V_i = V_{dd}$ (1)			1	µA
I_{oz}	Tri-state output leakage without pull up/down device	V_o = 0V or V_{dd} (1)			1	µA
I_{ozFT}	5V tolerant tri-state output leakage without pull up/down device	V_o = 0V or V_{dd} (1)			1	µA
		V_o = 5.5V		1	3	µA
$I_{latchup}$	I/O latch-up current	V < 0V, V > V_{dd}	200			mA
V_{esd}	Electrostatic protection	Leakage , 1µA (2)	1500			V

1. The leakage currents are generally very small, <1nA. The value given here, 1mA, ia amaximum that can occur after an electrostatic stress on the pin.
2. Human body model.

Table 9. Low voltage TTL interface DC electrical characteristics

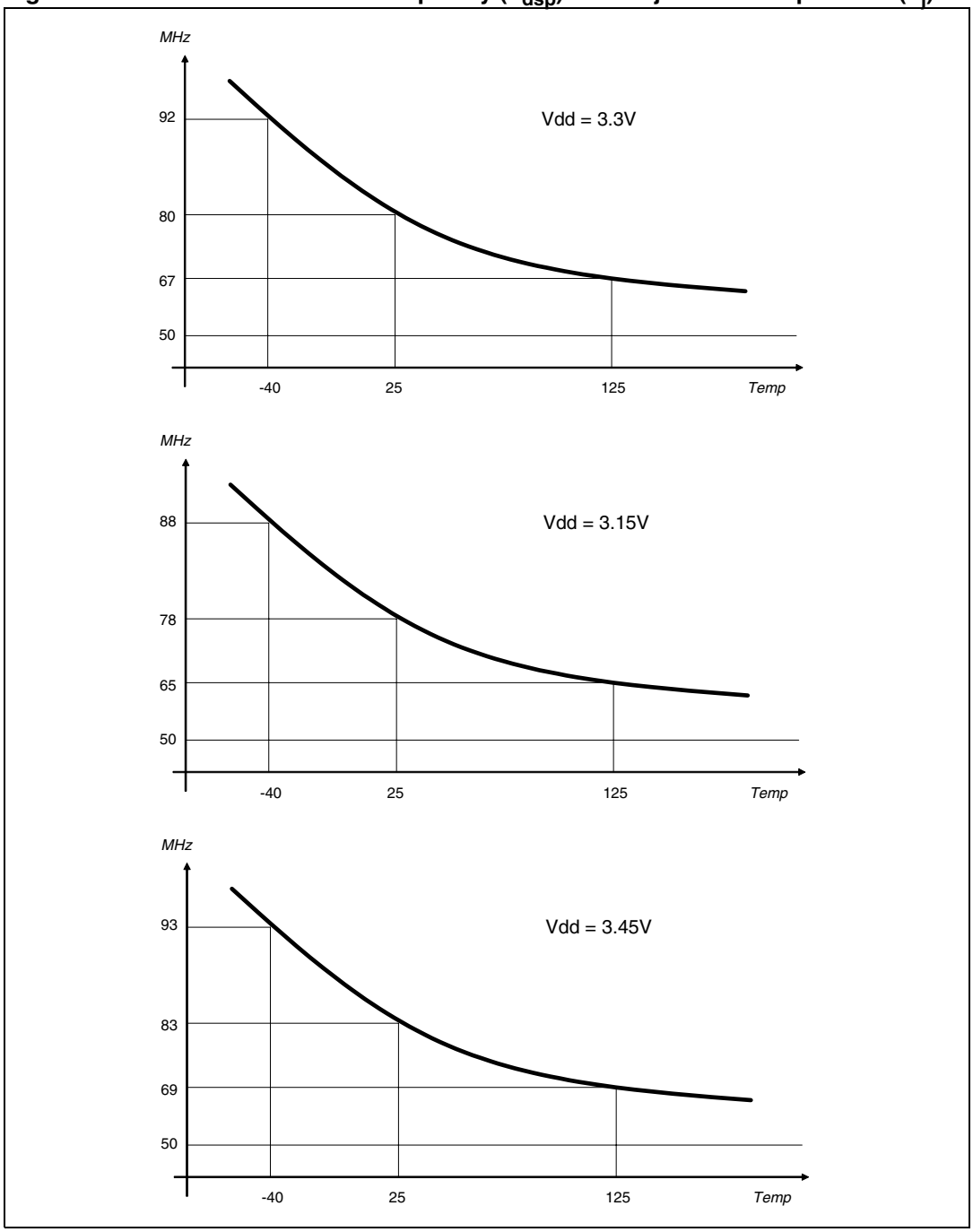
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{il}	Low level input voltage	(1)			0.8	V
V_{ih}	High level input voltage	(1)	2			V
V_{ilhyst}	Low level threshold input falling	(1)	0.9		1.35	V
V_{ihhyst}	Low level threshold input falling	(1)	1.3		1.9	V
V_{hyst}	Schmitt trigger hysteresis	(1)	0.4		0.7	V
V_{ol}	Low level output voltage	I_{ol} = XmA (1) (2) (3)			0.4	V
V_{oh}	High level output voltage		2.4			V

1. TTL specifications only apply to the supply voltage range Vdd = 3.0V to 3.6V.
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 10. DSP core

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
F_{dsp}	Maximum DSP clock frequency	@3.15V and T_j = 125°C	50			MHz

Figure 3. Maximum DSP clock frequency (F_{dsp}) versus junction temperature (T_j)



3 SAI interface

Figure 4. SAI timings

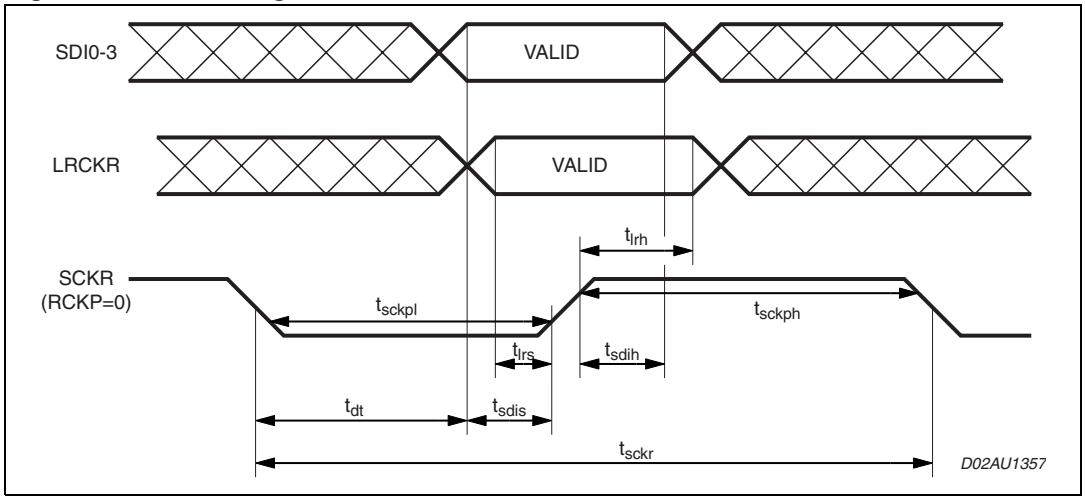


Table 11. Cycles

Timing	Description	Value	Unit
t_{sckr}	Minimum Clock Cycle	$4T_{DSP}$	ns
t_{dt}	SCKR active edge to data out valid	10	ns
t_{lrs}	LRCK setup time	5	ns
t_{lrh}	LRCK hold time	5	ns
t_{sdid}	SDI setup time	15	ns
t_{sdih}	SDI hold time	15	ns
t_{sckph}	Minimum SCK high time	0.35 t_{sckr}	ns
t_{sckpl}	Minimum SCK low time	0.35 t_{sckr}	ns

Note: T_{DSP} = dsp master clock cycle time = $1/F_{DSP}$

Figure 5. SAI protocol when RLRS=0; RREL=0; RCKP=1; RDIR=0

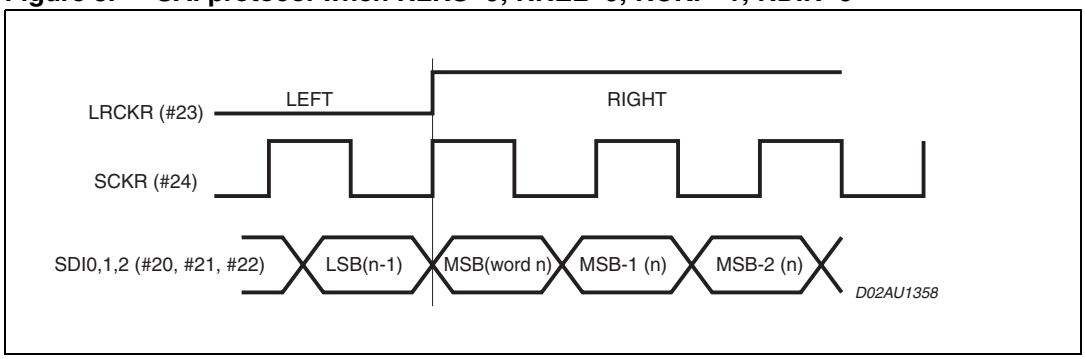


Figure 6. SAI protocol when RLRS=1; RREL=0; RCKP=1; RDIR=1.

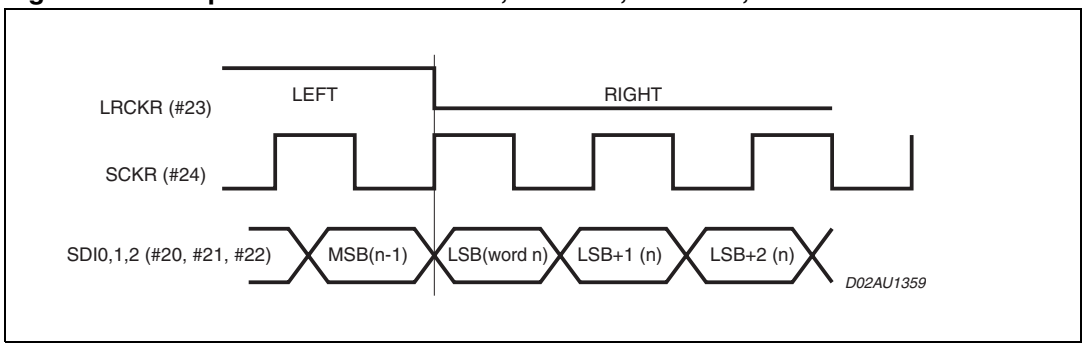


Figure 7. SAI protocol when RLRS=0; RREL=0; RCKP=0; RDIR=0.

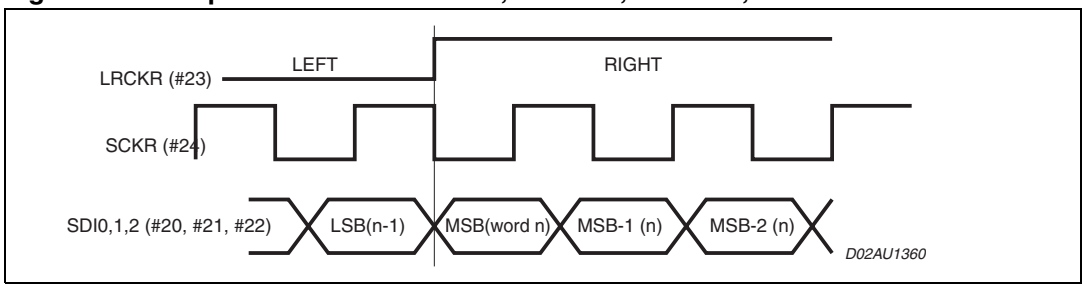
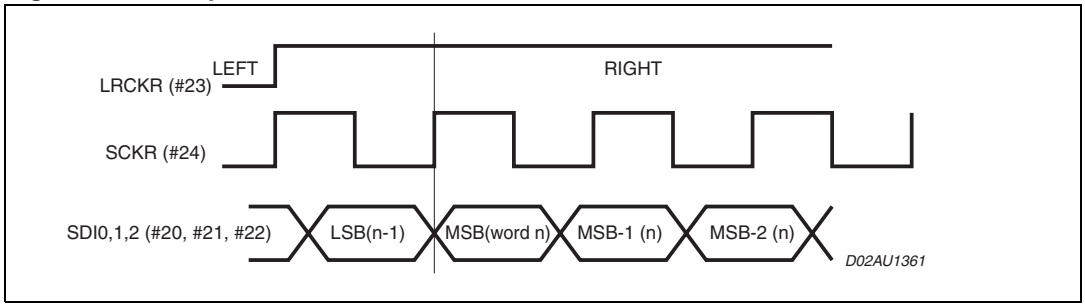


Figure 8. SAI protocol when RLRS=0; RREL=1; RCKP=1; RDIR=0.



4 SPI interfaces

Table 12. SPI interfaces

Symbol	Description	Min Value	Unit
Master			
t_{sclk}	Clock cycle	$12T_{DSP}$	ns
t_{dtr}	Sclk edge to MOSI valid	40	ns
$t_{misosetup}$	MISO setup time	16	ns
$t_{misohold}$	MISO hold time	4	ns
t_{sclkh}	SCK high time	$0.5t_{sclk}$	ns
t_{sclkl}	SCK high low	$0.5t_{sclk}$	ns
Slave			
t_{sclk}	Clock cycle	$12T_{DSP}$	ns
t_{dtr}	Sclk edge to MOSI valid	40	ns
$t_{mosisetup}$	MOSI setup time	16	ns
$t_{mosihold}$	MOSI hold time	4	ns
t_{sclkh}	SCK high time	$0.5t_{sclk}$	ns
t_{sclkl}	SCK high low	$0.5t_{sclk}$	ns

Figure 9. SPI clocking scheme.

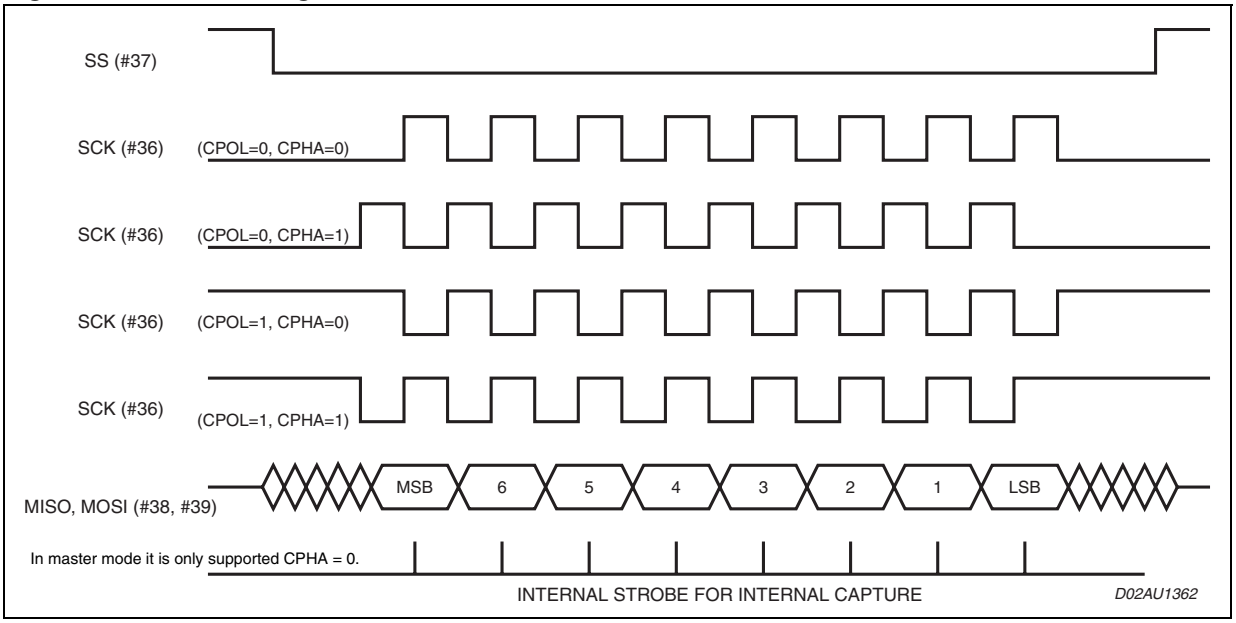


Table 13. Debug port interface

No.	Characteristics	dclk = 40MHz		Unit
		Min.	Max.	
1	DBCK rise time	--	3	ns
2	DBCK fall time	--	3	ns
3	DBCK low	40	--	ns
4	DBCK high	40	--	ns
5	DBCK cycle time	200	--	ns
6	DBRQN asserted to DBOUT (ACK) asserted	5 TDSP	--	ns
7	DBCK high to DBOUT valid	--	42	ns
8	DBCK high to DBOUT invalid	3	--	ns
9	DBIN valid to DBCK low (set-up)	15	--	ns
10	DBCK low to DBIN invalid (hold)	3	--	ns
	DBOUT (ACK) asserted to first DBCK high	2 Tc	--	ns
	DBOUT (ACK) assertion width	4.5 TDSP - 3	5 TDSP + 7	ns
11	Last DBCK low of read register to first DBCK high of next command	7 TDSP + 10	--	ns
12	Last DBCK low to DBOUT invalid (Hold)	3	--	ns
	DBSEL setup to DBCK	TDSP		ns

Figure 10. Debug port serial clock timing.

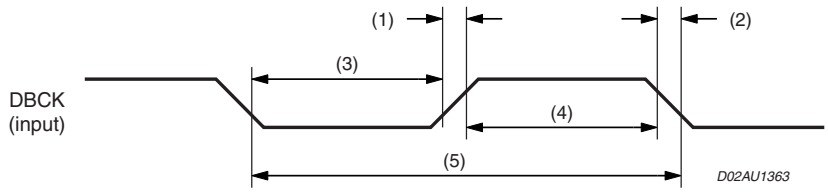


Figure 11. Debug port acknowledge timing.

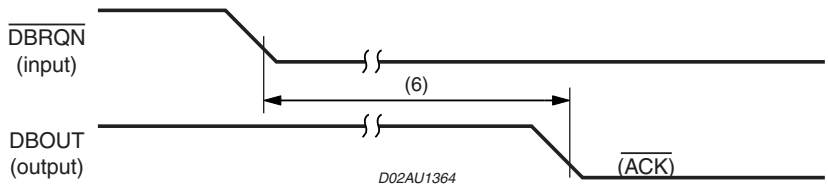


Figure 12. Debug port data I/O to status timing.

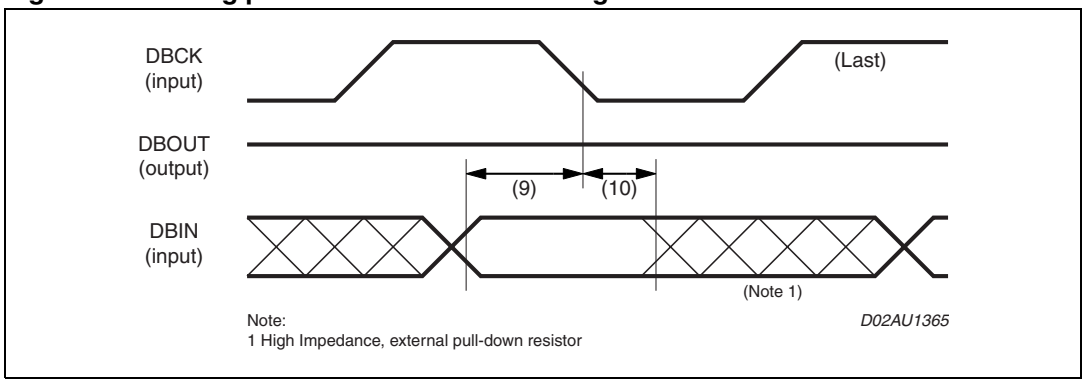


Figure 13. Debug port read timing.

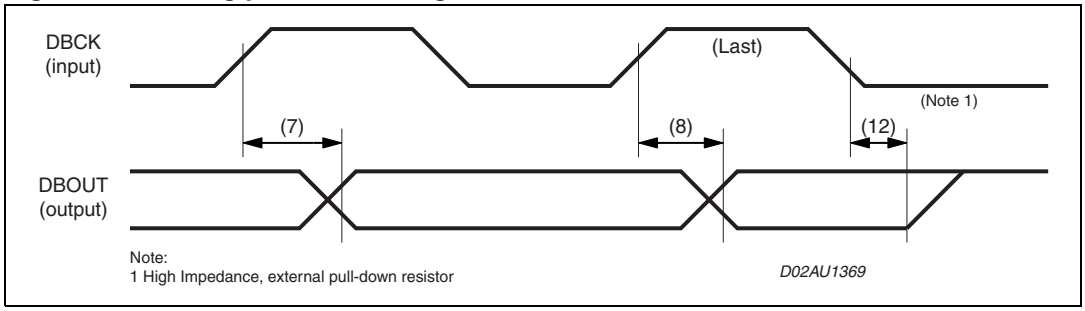
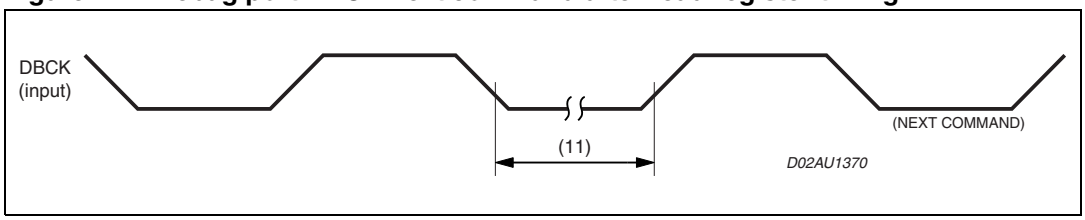


Figure 14. Debug port DBCK next command after read register timing.



5 I²C timing

Figure 15. Definition of timing for the I²C bus.

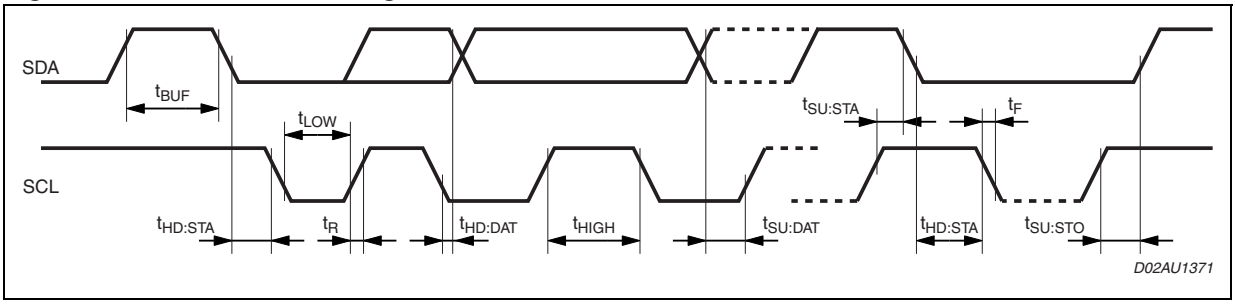


Table 14. Definitions

Symbol	Parameter	Test condition	Standard mode I²C bus		Fast mode I²C bus		Unit
			Min.	Max.	Min.	Max.	
F_{SCL}	SCLI clock frequency		0	100	0	400	kHz
t_{BUF}	Bus free between a STOP and Start Condition		4.7	–	1.3	–	µs
$t_{HD:STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated		4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock		4.7	–	1.3	–	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	–	0.6	–	µs
$t_{SU:STA}$	Set-up time for a repeated start condition		4.7	–	0.6	–	µs
$t_{HD:DAT}$	DATA hold time		0	–	0	0.9	µs
t_R	Rise time of both SDA and SCL signals	Cb in pF	–	1000	$20+0.1C_b$	300	ns
t_F	Fall time of both SDA and SCL signals	Cb in pF	–	300	$20+0.1C_b$	300	ns
$t_{SU;STO}$	Set-up time for STOP condition		4	–	0.6	–	µs
$t_{SU:DAT}$	Data set-up time		250	--	--	100	ns
C_b	Capacitive load for each bus line		–	400	–	400	pF

6 Functional description

The TDA7502 contains one DSP core and associated peripherals.

6.1 24-BIT DSP core.

The DSP core is used to process the converted analog audio data coming from the CODEC chip via the SAI and return it for analog conversion. Functions such as volume, tone, balance, and fader control, as well as spatial enhancement and general purpose signal processing may be performed by the DSP.

Some capabilities of the DSPs are listed below:

Single cycle multiply and accumulate with convergent rounding and condition code generation

- 2 x 56-bit accumulators.
- Double precision multiply.
- Scaling and saturation arithmetic.
- 48-bit or 2 x 24-bit parallel moves.
- 64 interrupt vector locations.
- Fast or long interrupts possible.
- Programmable interrupt priorities and masking.
- 8 each of address registers, address offset registers and address modulo registers.
- linear, reverse carry, multiple buffer modulo, multiple wrap-around modulo address arithmetic.
- Post-increment or decrement by 1 or by offset, index by offset, predecrement address.
- Repeat instruction and zero overhead DO loops.
- Hardware stack capable of nesting combinations of 7 DO loops or 15 interrupts/subroutines.
- Bit manipulation instructions possible on all registers and memory locations. Also jump on bit test..
- 4 pin serial debug interface.
- Debug access to all internal registers, buses and memory locations.
- 5 word deep program address history FIFO.
- Hardware and software breakpoints for both program and data memory accesses.
- Debug single stepping, Instruction injection and disassembly of program memory.

6.2 DSP peripherals

There are a number of peripherals that are tightly coupled to the DSP Core. Each of the peripherals are listed below and described in the following sections.

- 1024 x 24-Bit X-RAM.
- 1024 x 24-Bit Y-RAM.
- 3072 x 24-Bit program RAM.
- 512 x 24-Bit Boot ROM.
- Serial audio interface (SAI).
- Programmable control interface (SPI/I^2C).
- GPIO.
- PLL clock oscillator.

6.3 Data and program memory

Each of the memories are described below.

6.3.1 1024 x 24-Bit X-RAM (XRAM)

This is a 1024 x 24-Bit single port SRAM used for storing coefficients. The 16-Bit XRAM address, XABx(15:0) is generated by the address generation unit of the DSP core. The 24-Bit XRAM Data, XDBx(23:0), may be written to and read from the data ALU of the DSP core. The XDBx Bus is also connected to the internal bus switch so that it can be routed to and from all peripheral blocks.

6.3.2 1024 x 24 Bit Y-RAM (YRAM)

This is a 1024 x 24-Bit single port SRAM used for storing coefficients. The 16-Bit address, YABx(15:0) is generated by the address generation unit of the DSP core. The 24-Bit Data, YDBx(23:0), is written to and read from the Data ALU of the DSP core. The YDBx Bus is also connected to the internal bus switch so that it can be routed to and from other blocks.

6.3.3 3072 X 24-Bit Program RAM

This is a 3072 x 24-Bit single port SRAM used for storing and executing program code. The 16-Bit PRAM Address, PABx(15:0) is generated by the program address generator of the DSP core for instruction fetching, and by the AGU in the case of the move program memory (MOVEM) instruction. The 24-Bit PRAM Data (program code), PDBx(23:0), can only be written to using the MOVEM instruction.

During instruction fetching the PDBx bus is routed to the program decode controller of the DSP core for instruction decoding.

Spare space in the program area may be used as data memory to implement delay lines for example.

6.3.4 512 x 24-Bit Bootstrap ROM (Boot ROM)

This is a 512 x 24-Bit factory programmed Boot ROM used for storing the program sequence for initializing the DSP.

Essentially this consists of a routine that is called when the DSP comes out of reset. There are four different boot modes supported by the boot ROM. The first mode loads the application program via SPI interface where Casper's SPI is in master mode. The second boot mode enables the debug port and waits. The third and fourth modes load the application program via the I^2C interface, one with Casper's I^2C Interface configured in slave mode and the other in master mode. Which boot mode to enter is configured by sampling the states of the GPIO4 and GPIO3 pins at reset as shown in the table below.

Table 15. Casper IC boot modes

Modes	Description	GPIO3	GPIO4
0-SPI Master	load PRAM, XRAM and YRAM from SPI	0	0
1-Debug	enable Debug Port	0	1
2-I^2C Master	load PRAM, XRAM and YRAM from I^2C	1	0
3-I^2C Slave	oad PRAM, XRAM and YRAM from I^2C	1	1

6.3.5 Serial audio interface (SAI)

The SAI is used to deliver digital audio to the DSPs from an external source. Once processed by the DSPs, it can be returned through this interface. The features of the SAI are listed below.

- Three synchronized stereo data transmission lines
- Three synchronized stereo data reception lines
- Master/Slave operating modes
- Transmit and receive interrupt logic triggers on left/right data pairs
- Receive and transmit data registers have two locations to hold left and right data.

6.3.6 Serial peripheral interface

A serial interface allows to receive commands and data over the LAN. During an SPI transfer, data is transmitted and received simultaneously. Both master and slave modes are supported.
In master mode the SPI supports combination of CPOL =0/1 and CPHA =0 only, while in slave mode all the 4 possible combinations of CPOL and CPHA are supported. See *Figure 9.*
A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device.

When an SPI transfer occurs an 8-bit word is shifted out one data pin while another 8-bit character is simultaneously shifted in a second data pin.The central element in the SPI system is the shift register and the read data buffer. The system is single buffered in the transfer direction and double buffered in the receive direction.

6.3.7 I^2C interface

The inter integrated circuit bus is a single bidirectional two-wire bus used for efficient inter IC control. All I^2C bus compatible devices incorporate an on-chip interface which allows them communicate directly with each other via the I^2C bus.

Every component hooked up to the I^2C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and /or transmitter on its functionality.

6.3.8 General purpose input/output

The DSP requires a set of external general purpose input/output lines, and a reset line. These signals are used by external devices to signal events to the DSP. The GPIO lines are implemented as DSP's peripherals.

6.3.9 PLL clock oscillator

The PLL clock oscillator can accept an external clock at XTI or it can be configured to run an internal oscillator when a crystal is connected across pins XTI & XTO. There is an input divide block IDF (1 -> 32) at the XTI clock input and a multiply block MF (9 -> 128) in the PLL loop. Hence the PLL can multiply the external input clock by a ratio MF/IDF to generate the internal clock. This allows the internal clock to be within 2 MHz of any desired frequency even when XTI is much greater than 1 MHz. It is recommended that the input clock is not divided down to less than 1 MHz as this reduces the phase detector's update rate.

The clocks to the DSP can be selected to be either the VCO output divided by 2 to 16, or be driven by the XTI pin directly.

The crystal oscillator and the PLL will be gated off when entering the power-down mode (by setting a register on DSP0).

7 Application scheme

Figure 16. Application schematic for TDA7502

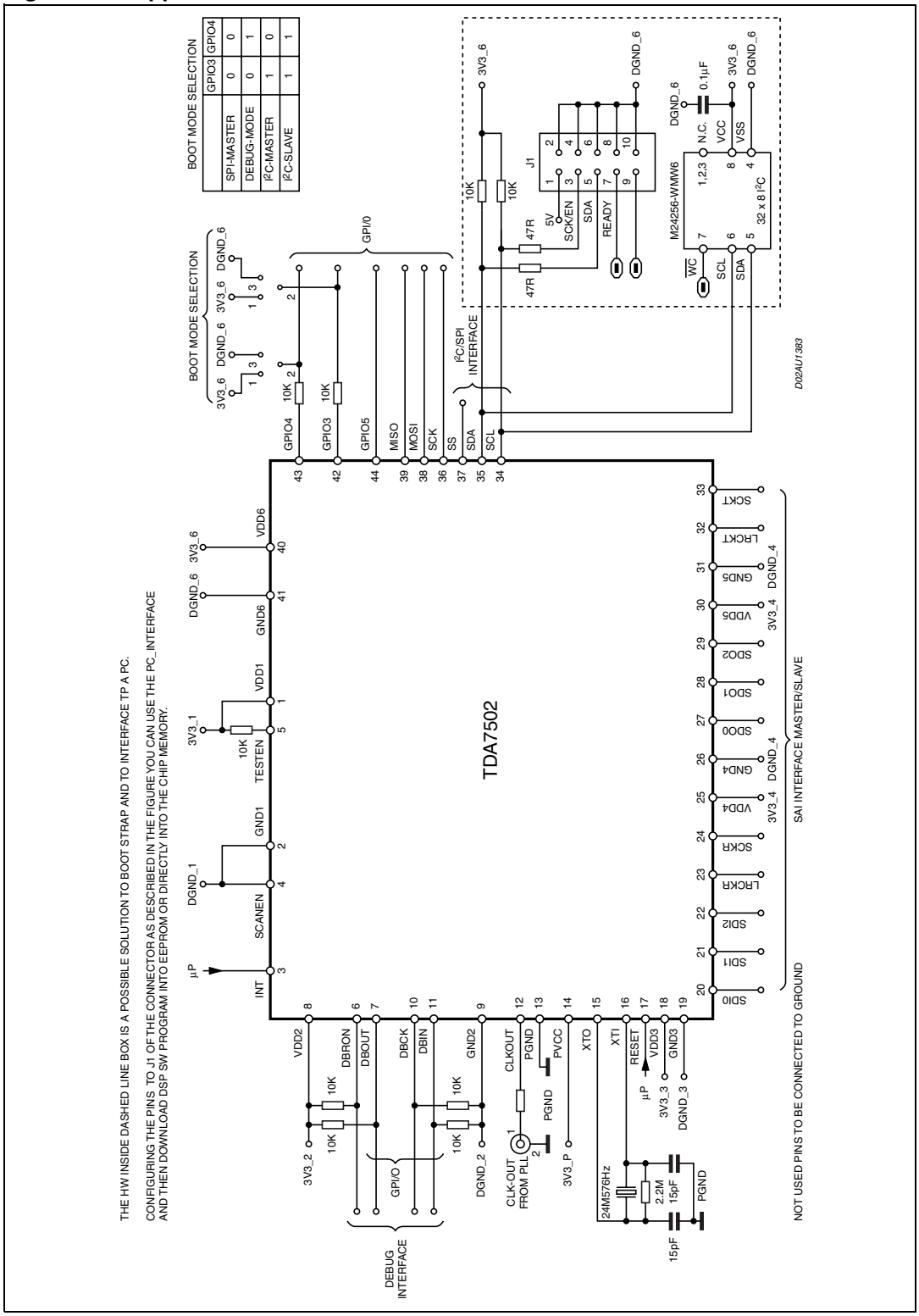
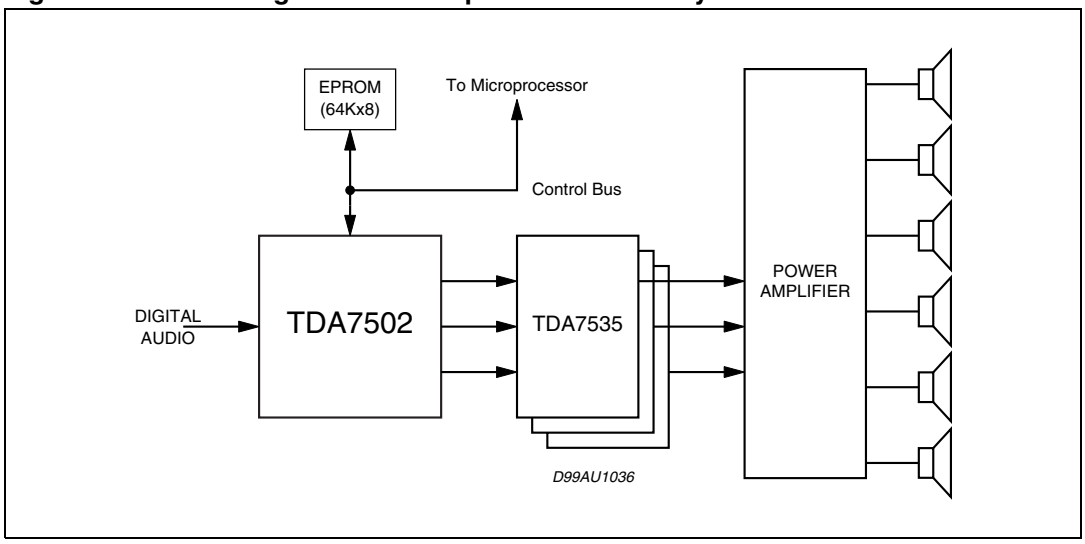


Figure 17. Block diagram of car amplifier audio sub-system.



8 Package information

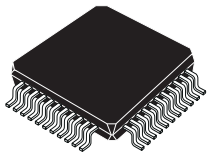
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

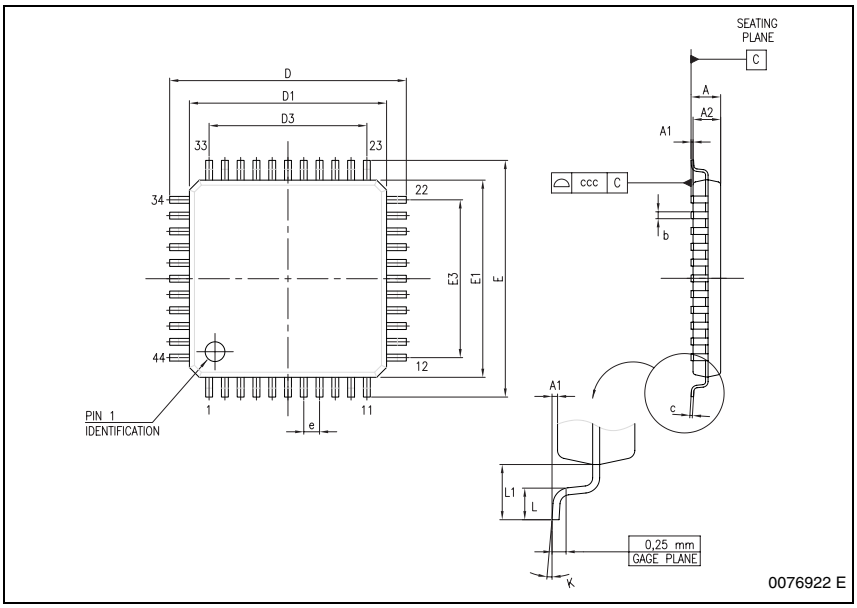
Figure 18. TQFP44 (10x10) mechanical data & package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					
ccc			0.10			0.0039

OUTLINE AND MECHANICAL DATA



LQFP44 (10 x 10 x 1.4mm)



9 Revision history

Table 16. Revision history

Date	Revision	Description of changes
January 2004	8	First Issue in EDOCS dms.
September 2004	9	Changed the style-sheet look. Cancelled the “Package Marking” information.
March 2005	10	Changed SPI interface description and Figure 4.
24-Nov-2006	11	Package changed, layout changes, text modifications.

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