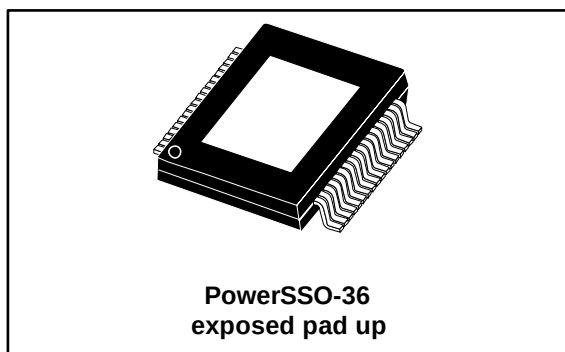


79 W + 79 W dual BTL class-D audio amplifier

Datasheet - production data



Features

- Wide-range single-supply operation (7 - 26 V)
- Possible output configurations:
 - 2 x PBTL
 - 1 x Parallel BTL
- BTL output capabilities ($V_{CC} = 26\text{ V}$):
 - 61 W + 61 W, 4 Ω , THD 1%
 - 79 W + 79 W, 4 Ω , THD 10%
 - 44 W + 44 W, 6 Ω , THD 1%
 - 57 W + 57 W, 6 Ω , THD 10%
 - 34 W + 34 W, 8 Ω , THD 1%
 - 44 W + 44 W, 8 Ω , THD 10%
- Parallel BTL output capabilities ($V_{CC} = 26\text{ V}$):
 - 86 W, 3 Ω , THD 1%
 - 110 W, 3 Ω , THD 10%
- High efficiency

- Four selectable, fixed-gain settings of nominally 20.8 dB, 26.8 dB, 30 dB and 32.8 dB
- Differential inputs minimize common-mode noise
- Standby, mute and play operating modes
- Short-circuit protection
- Output power limited by P_{LIMIT} function
- Detection of shorted output pins during startup
- Thermal overload protection
- ECOPACK® environmentally friendly package

Description

The TDA7492E is a dual BTL class-D audio amplifier with single power supply designed for home audio applications.

The device is housed in a 36-pin PowerSSO package with exposed pad up (EPU), and as a result of its high efficiency, a simple heatsink is required.

Table 1: Device summary

Order code	Operating temp. range	Package	Packaging
TDA7492ETR	-40 to +85°C	PowerSSO-36 EPU	Tape and reel

Contents

1	Device block diagram.....	5
2	Pin description	6
2.1	Pinout.....	6
2.2	Pin list	7
3	Electrical specifications.....	8
3.1	Absolute maximum ratings.....	8
3.2	Thermal data.....	8
3.3	Electrical specifications	9
3.4	Stereo BTL application.....	10
3.5	Parallel BTL (mono) application	10
4	Application information	11
4.1	Gain setting.....	11
4.2	Stereo and mono applications.....	11
4.3	Smart protections	11
4.3.1	Overcurrent protection (OCP)	11
4.3.2	Thermal protection.....	12
4.3.3	Power limit	12
4.4	Mode selection.....	13
5	Schematic diagram.....	15
6	Characterization curves.....	16
6.1	Stereo configuration	16
7	Package information	20
7.1	PowerSSO36 EPU package information.....	20
8	Revision history	23

List of tables

Table 1: Device summary	1
Table 2: Pin description list	7
Table 3: Absolute maximum ratings	8
Table 4: Thermal data	8
Table 5: Electrical specifications	9
Table 6: Stereo BTL application	10
Table 7: Stereo BTL (mono) application	10
Table 8: Gain settings	11
Table 9: Overcurrent protection	11
Table 10: Overcurrent protection (mute mode)	12
Table 11: Max effective voltage of PLIMIT pin vs. power supply and load	13
Table 12: Mode settings	13
Table 13: PowerSSO-36 EPU package mechanical data	22
Table 14: Document revision history	23

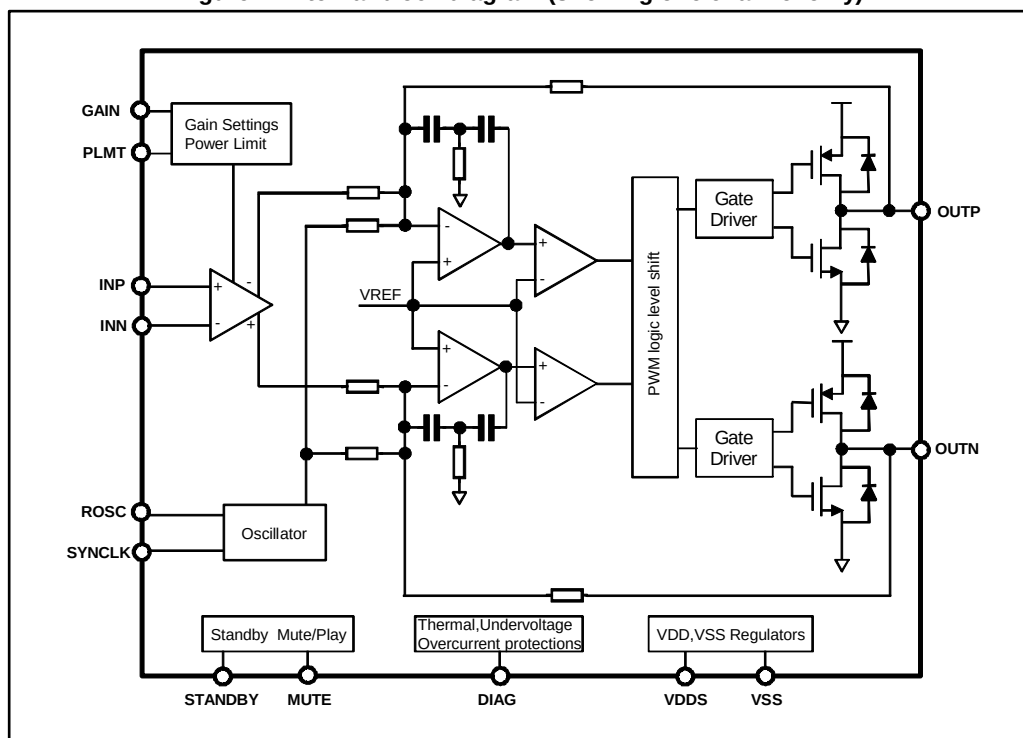
List of figures

Figure 1: Internal block diagram (showing one channel only)	5
Figure 2: Pin connections (top view, PCB view)	6
Figure 3: Mono BTL settings.....	11
Figure 4: Recommended power limit pin connections.....	12
Figure 5: Standby and mute circuits	14
Figure 6: Turn-on/off sequence for minimizing speaker "pop"	14
Figure 7: Application circuit.....	15
Figure 8: Output power vs. supply voltage	16
Figure 9: THD vs. Pout ($V_s = 26\text{ V}$, $f = 1\text{ kHz}$).....	16
Figure 10: THD vs. Pout ($V_s = 26\text{ V}$, $f = 100\text{ Hz}$)	16
Figure 11: THD vs. Pout ($V_s = 26\text{ V}$, $f = 6\text{ kHz}$).....	16
Figure 12: THD vs. frequency ($V_s = 26\text{ V}$, $P_o = 1\text{ W}$).....	17
Figure 13: Frequency response $V_s = 26\text{ V}$	17
Figure 14: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 32.6 dB, not weighted)	17
Figure 15: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 20.6 dB, not weighted)	17
Figure 16: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 32.6 dB, A-weighted).....	18
Figure 17: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 20.6 dB, A-weighted).....	18
Figure 18: Crosstalk $V_s = 26\text{ V}$	18
Figure 19: FFT (0 dB) $V_s = 26\text{ V}$	18
Figure 20: FFT (-60 dB) $V_s = 26\text{ V}$	19
Figure 21: PowerSSO-36 EPU package outline	21

1 Device block diagram

Figure 1: "Internal block diagram (showing one channel only)" shows the block diagram of one of the two identical channels of the TDA7492E.

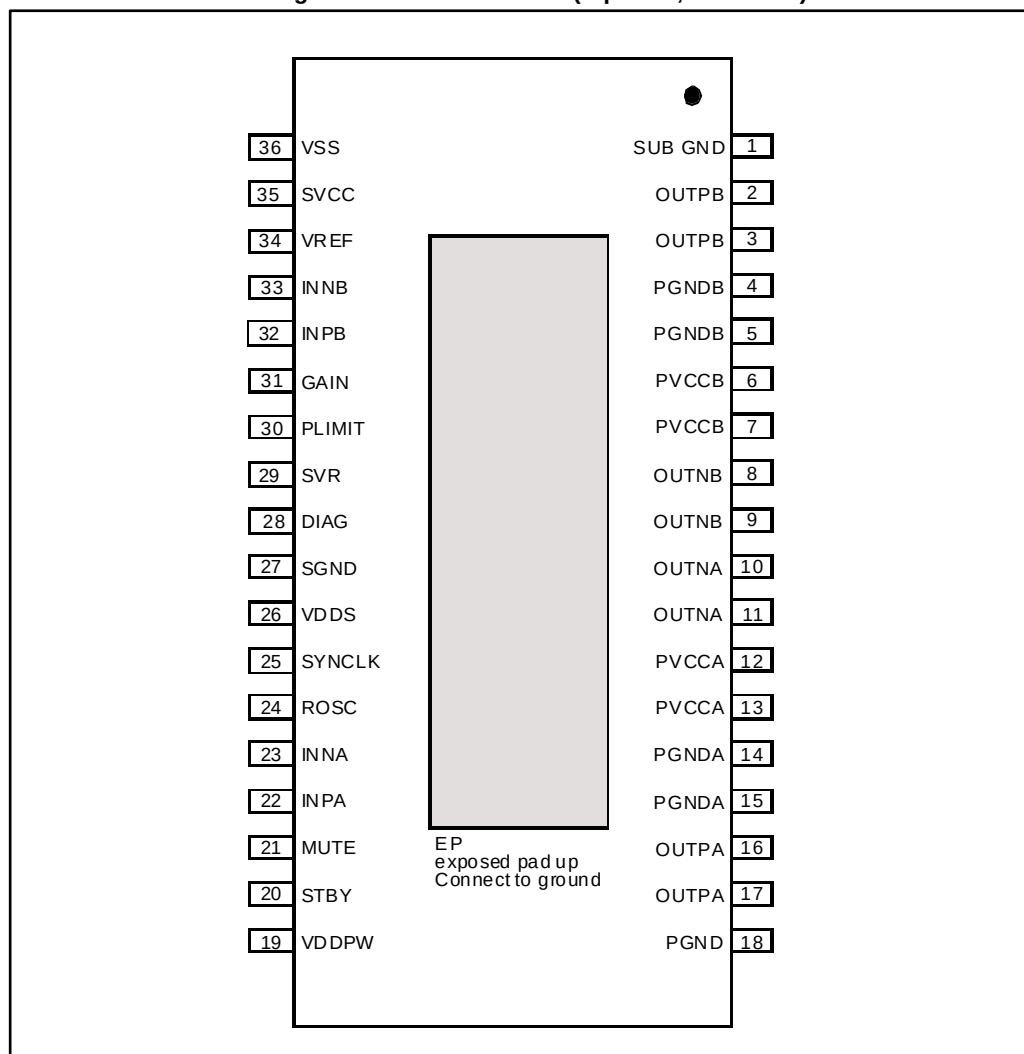
Figure 1: Internal block diagram (showing one channel only)



2 Pin description

2.1 Pinout

Figure 2: Pin connections (top view, PCB view)



2.2 Pin list

Table 2: Pin description list

Number	Name	Type	Description
1	SUB_GND	PWR	Connect to the frame
2, 3	OUTPB	O	Positive PWM for right channel
4, 5	PGNDB	PWR	Power stage ground for right channel
6, 7	PVCCB	PWR	Power supply for right channel
8, 9	OUTNB	O	Negative PWM output for right channel
10, 11	OUTNA	O	Negative PWM output for left channel
12, 13	PVCCA	PWR	Power supply for left channel
14, 15	PGNDA	PWR	Power stage ground for left channel
16, 17	OUTPA	O	Positive PWM output for left channel
18	PGND	PWR	Power stage ground
19	VDDPW	O	3.3 V (nominal) regulator output referred to ground for power stage
20	STBY	I	Standby mode control
21	MUTE	I	Mute mode control
22	INPA	I	Positive differential input of left channel
23	INNA	I	Negative differential input of left channel
24	ROSC	O	Master oscillator frequency-setting pin
25	SYNCLK	I/O	Clock in/out for external oscillator
26	VDDS	O	3.3 V (nominal) regulator output referred to ground for signal blocks
27	SGND	PWR	Signal ground
28	DIAG	O	Open-drain diagnostic output
29	SVR	O	Supply voltage rejection
30	PLIMIT	I	Output voltage level setting
31	GAIN	I	Gain setting input
32	INPB	I	Positive differential input of right channel
33	INNB	I	Negative differential input of right channel
34	VREF	O	Half VDDS (nominal) referred to ground
35	SVCC	PWR	Signal power supply
36	VSS	O	3.3 V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage for pins PVCCA, PVCCB, SVCC	30	V
V _I	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN, MODE	-0.3 to +4.6	V
T _{op}	Operating temperature	-40 to +85	°C
T _j	Junction temperature	-40 to +150	°C
T _{stg}	Storage temperature	-40 to +150	°C

3.2 Thermal data

Table 4: Thermal data

Symbol	Parameter	Min.	Typ.	Max.	Unit
R _{th j-case}	Thermal resistance, junction-to-case	-	2.98		°C/W

3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5: "Electrical specifications"](#) below are given for the conditions: $V_{CC} = 26 \text{ V}$, $R_L = 6 \text{ }\Omega$, $R_{OSC} = 33 \text{ k}\Omega$, $f = 1 \text{ kHz}$, $G_V = 20.8 \text{ dB}$ and $T_{amb} = 25 \text{ }^\circ\text{C}$.

Table 5: Electrical specifications

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage for pins PVCCA, PVCCB, SVCC	-	7	-	26	V
I _q	Total quiescent current	Without LC, no load	-	40		mA
I _{qSTBY}	Quiescent current in standby	-	-	1	-	μA
V _{OS}	Output offset voltage	V _i = 0, A _v = 20 dB, no load		20		mV
I _{OCP}	Overcurrent protection threshold	R _L = 0 Ω	9	10	13	A
T _j	Junction temperature at thermal shutdown	-	140	150	160	°C
R _i	Input resistance	Differential input		60	-	kΩ
R _{dsON}	Power transistor on-resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
G _v	Closed-loop gain	GAIN < 0.25*Vdd		20.8	-	dB
		0.25*Vdd < GAIN < 0.5*Vdd	-	26.8	-	
		0.5*Vdd < GAIN < 0.75*Vdd	-	30	-	
		GAIN1>0.75*Vdd	-	32.8	-	
ΔG _v	Gain matching	-	-	-	±1	dB
CT	Crosstalk	f = 1 kHz	-	70	-	dB
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 0.5 V, C _{SVR} = 10 μF	-	60	-	dB
T _r , T _f	Rise and fall times	PWM signal 50% duty cycle	-	24	40	ns
f _{sw}	Switching frequency	Internal oscillator with external R _{osc} = 33 kΩ	-	500	-	kHz
f _{SWR}	Output switching frequency range	With internal oscillator by changing R _{osc} ⁽⁴⁾	450	-	550	kHz
V _{inH}	Digital input high (H)	-	2.0	-	-	V
V _{inL}	Digital input low (L)		-	-	0.8	
Function mode	Standby, Mute, Play	STBY < 0.5 V Mute = 'X'	Standby			
		STBY > 2.5 V Mute < 0.8 V	Mute			
		STBY > 2.5 V Mute > 2.5 V	Play			
A _{MUTE}	Mute attenuation	V _{MUTE} = 1 V	60	80	-	dB

Notes:

⁽¹⁾ $f_{SW} = 10^6 / [(12 \cdot R_{OSC} + 110) \cdot 4] \text{ kHz}$, $f_{SYNCLK} = 2 \cdot f_{SW}$ (where R_{OSC} is in k Ω and f_{SW} in kHz) with $R_{osc} = 33 \text{ k}\Omega$.

3.4 Stereo BTL application

All specifications are for $V_{CC} = 22\text{ V}$, $R_{osc} = 33\text{ k}\Omega$, $f = 1\text{ kHz}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified.

Table 6: Stereo BTL application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	$R_L = 6\text{ }\Omega$, THD = 10%	-	41	-	W
		$R_L = 6\text{ }\Omega$, THD = 1%	-	32	-	
		$R_L = 6\text{ }\Omega$, THD = 10%, $V_{CC} = 26\text{ V}$	-	57	-	
		$R_L = 6\text{ }\Omega$, THD = 1%, $V_{CC} = 26\text{ V}$	-	44	-	
THD	Total harmonic distortion	$P_o = 1\text{ W}$, $f_{in} = 1\text{ kHz}$	-	0.04	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, $G_V = 20.8\text{ dB}$	-	150	-	μV

3.5 Parallel BTL (mono) application

All specifications are for $V_{CC} = 22\text{ V}$, $R_{osc} = 33\text{ k}\Omega$, $f = 1\text{ kHz}$, $T_{amb} = 25\text{ }^{\circ}\text{C}$, INPB, INN connected to VDD, unless otherwise specified.

Table 7: Stereo BTL (mono) application

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
P_o	Output power	$R_L = 3\text{ }\Omega$, THD = 10%	-	90	-	W
		$R_L = 3\text{ }\Omega$, THD = 1%	-	70	-	
		$R_L = 3\text{ }\Omega$, THD = 10%, $V_{CC} = 26\text{ V}$	-	110	-	
		$R_L = 3\text{ }\Omega$, THD = 1%, $V_{CC} = 26\text{ V}$	-	86	-	
THD	Total harmonic distortion	$P_o = 1\text{ W}$, $f_{in} = 1\text{ kHz}$	-	0.04	-	%
VN	Total output noise	Inputs shorted and connected to GND, A curve, $G_V = 20.8\text{ dB}$	-	150	-	μV

4 Application information

4.1 Gain setting

The four gain settings of the TDA7492E are set by GAIN (pin 31). Internally, gain is set by changing the feedback resistors of the amplifier.

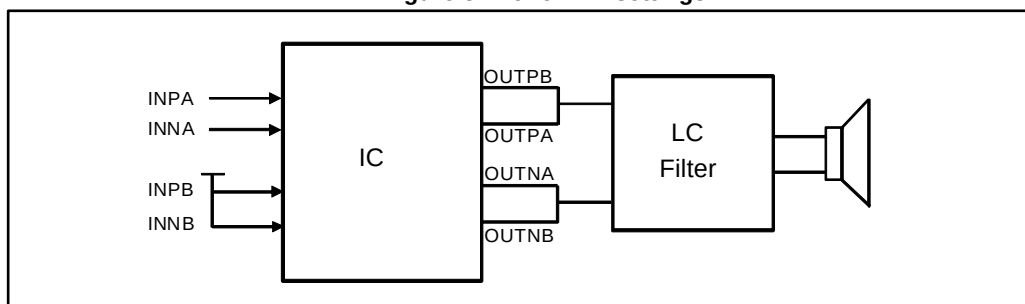
Table 8: Gain settings

Voltage on GAIN pin	Total gain	Application recommendations
$V_{\text{GAIN}} < 0.25 \cdot V_{\text{DD}}S$	20.8 dB	GAIN pin connected to SGND
$0.25 \cdot V_{\text{DD}}S < V_{\text{GAIN}} < 0.5 \cdot V_{\text{DD}}S$	26.8 dB	External resistor divider <100 k
$0.5 \cdot V_{\text{DD}}S < V_{\text{GAIN}} < 0.75 \cdot V_{\text{DD}}S$	30 dB	External resistor divider <100 k
$V_{\text{GAIN}} > 0.75 \cdot V_{\text{DD}}S$	32.8 dB	GAIN pin connected to VDD

4.2 Stereo and mono applications

The TDA7492E can be used in stereo BTL or in mono BTL configuration. When the input pins, INPB and INNB of the right channel are directly shorted to VDD (without input capacitors) the device is in mono configuration as shown in [Figure 3: "Mono BTL settings"](#).

Figure 3: Mono BTL settings



4.3 Smart protections

4.3.1 Overcurrent protection (OCP)

If the overcurrent protection threshold is reached, the power stage will be shut down immediately. The device will recover automatically when the fault is removed.

The overcurrent protection scheme is shown in [Table 9: "Overcurrent protection"](#). Two typical thresholds are as follows.

Table 9: Overcurrent protection

	I (Shutdown)
High side (A)	11.2
Low side (A)	10.0

The thresholds in MUTE mode are reduced to about 1/2 and two typical thresholds are as follows.

Table 10: Overcurrent protection (mute mode)

	I (Shutdown)
High side (A)	6.2
Low side (A)	5.9

4.3.2 Thermal protection

When internal die temperature exceeds 140 °C, the device enters into Mute by pulling the MUTE pin low first.

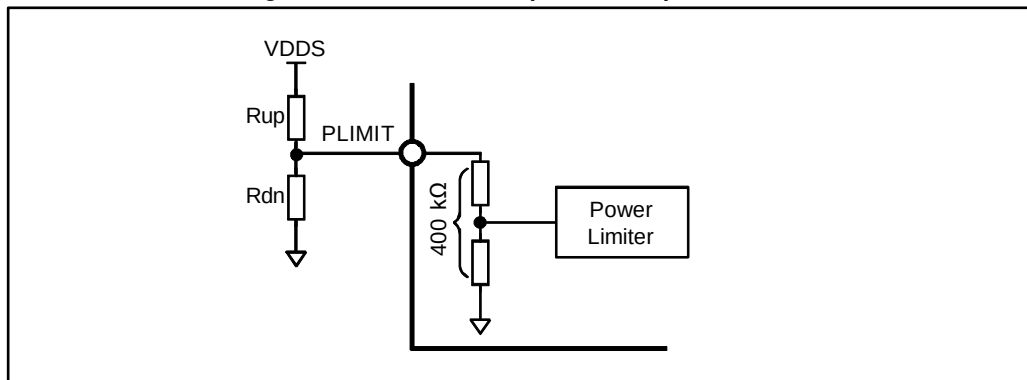
When internal die temperature exceeds 150 °C, the device directly shuts down the power stage. The TDA7492E automatically recovers when the temperature become lower than the threshold.

4.3.3 Power limit

A built-in power limit is used to limit the output voltage level below the supply rail by limiting the duty cycle. The limit level is set through the voltage at PLIMIT (pin 30). The pin voltage is set by the following equation:

$$V_{PLIMIT} = V_{DD} \left[\frac{(R_{dn}/400k)}{(R_{dn}/400k + R_{up})} \right]$$

Figure 4: Recommended power limit pin connections



It is recommended that external resistors are less than 40 kΩ if a voltage divider is used as shown in [Figure 4: "Recommended power limit pin connections"](#). The relationship of the maximum duty cycle (D_{max}) and the voltage at P_{LIMIT} is:

$$D_{max} = \frac{\left\{ 8.8 \times \frac{V_{PLIMIT}}{V_{cc} - \frac{2 \times V_{cc} \times R_s}{R_{load} \times 2 \times R_s}} + 1 \right\}}{2}$$

Where V_{CC} is the power supply voltage, V_{PLIMIT} is the voltage applied at the P_{LIMIT} pin, R_s is the series resistance including $R_{ds(on)}$ of power transistor, output filter resistance and bonding wire resistance. R_{load} is the load resistance.

An example of maximum effective control voltage at P_{LIMIT} vs. power supply and load resistance is shown in [Table 11: "Max effective voltage of PLIMIT pin vs. power supply and load"](#).

Table 11: Max effective voltage of PLIMIT pin vs. power supply and load

Rload	Power supply		
	7 V	13 V	24 V
4 Ω	0.71 V	1.32 V	2.44 V
6 Ω	0.74 V	1.37 V	2.53 V
8 Ω	0.75 V	1.39 V	2.57 V

4.4 Mode selection

The three operating modes of the TDA7492E are set by two inputs: STBY (pin 20) and MUTE (pin 21).

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle
- Play mode: the amplifiers are active.

The protection functions of the TDA7492E are implemented by pulling down the voltages of the STBY and MUTE inputs shown in [Figure 5: "Standby and mute circuits"](#). The input current of the corresponding pins must be limited to 200 μ A.

Table 12: Mode settings

Mode	STBY	MUTE
Standby	L ⁽¹⁾	X (don't care)
Mute	H	L
Play	H	H

Notes:

⁽¹⁾Drive levels defined in [Table 5: "Electrical specifications"](#).

Figure 5: Standby and mute circuits

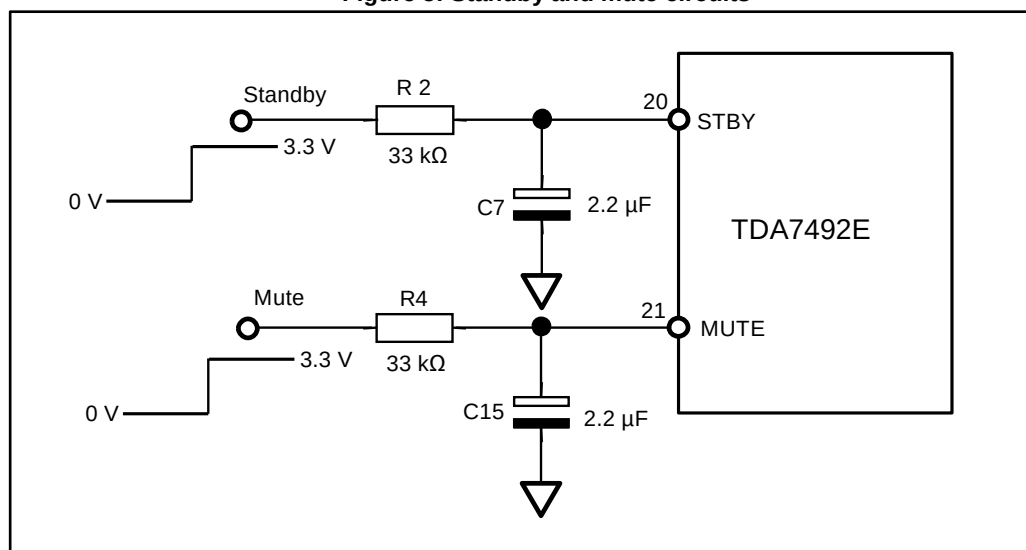
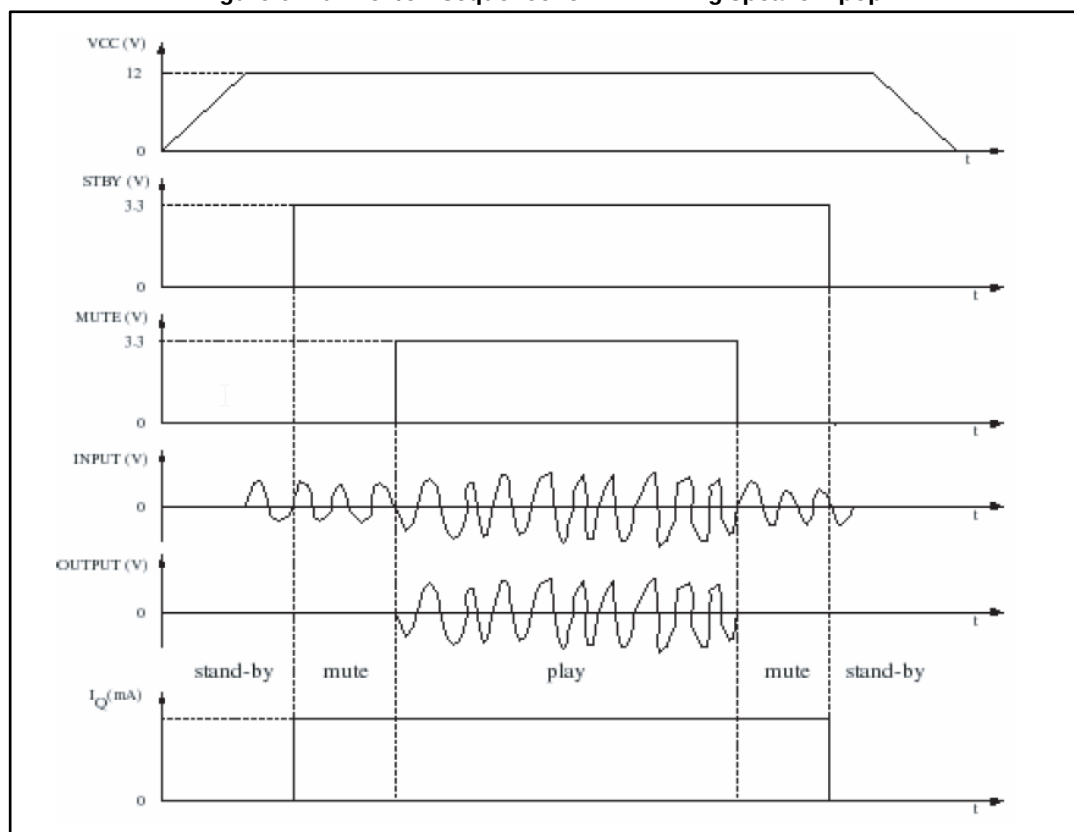
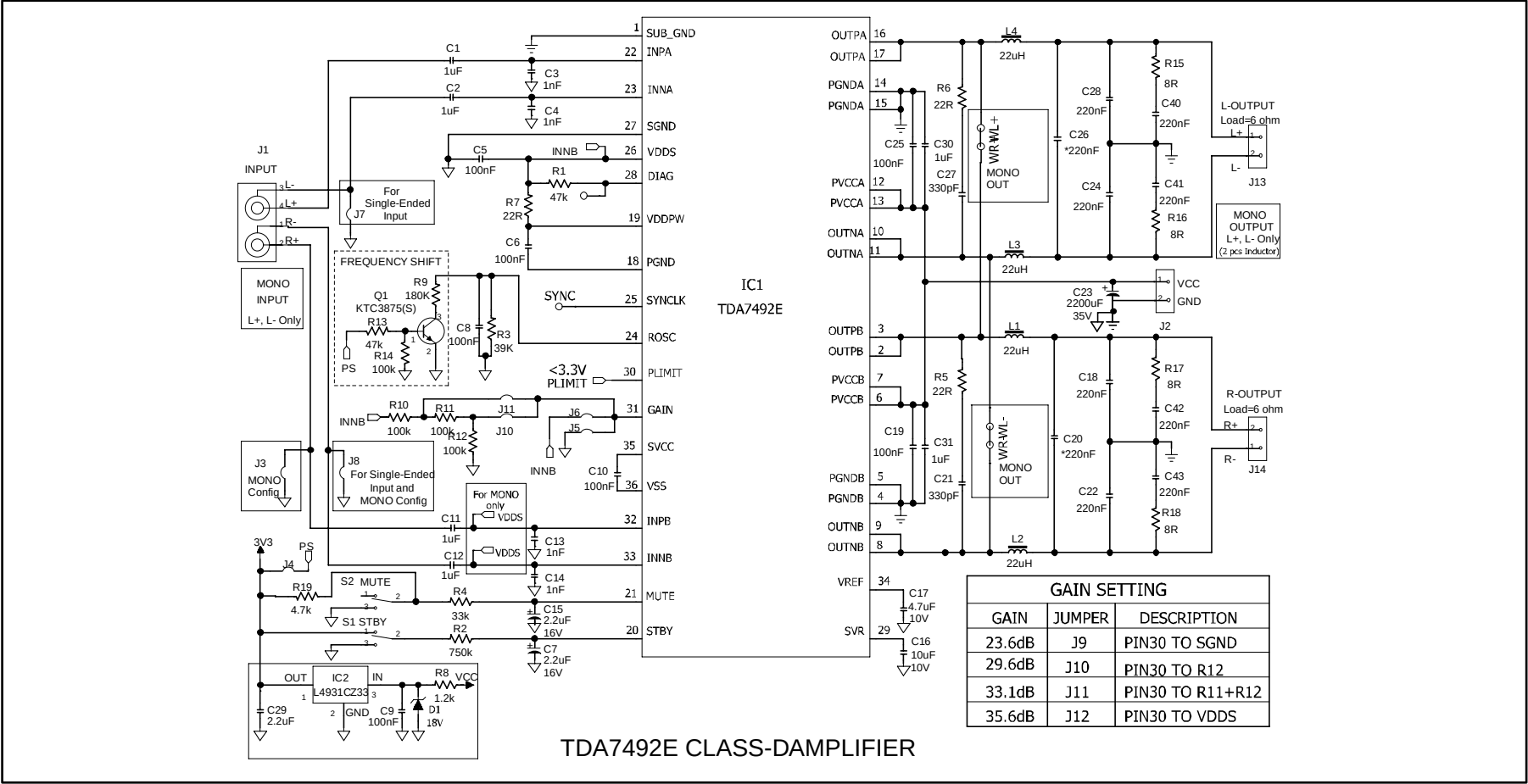


Figure 6: Turn-on/off sequence for minimizing speaker “pop”



5 Schematic diagram

Figure 7: Application circuit



6 Characterization curves

Unless otherwise stated, measurements were made under the following conditions:
 $V_{CC} = 22\text{ V}$, $R_I = 6\ \Omega$, $f = 1\text{ kHz}$, $G_v = 20.8\text{ dB}$, $R_{OSC} = 33\text{ k}\Omega$, $T_{amb} = 25\text{ }^\circ\text{C}$.

Note: Maximum output power must be derated according to case temperature.

6.1 Stereo configuration

The following characterization curves were made using the TDA7492E demonstration board ([Figure 7: "Application circuit"](#)). The characterization curves were made under the following test conditions:

$V_s = 7$ and 26 V , $R_I = 6\ \Omega$, $R_{osc} = 33\text{ k}\Omega$, $C_{osc} = 100\text{ nF}$, $\text{Gain} = 20.8\text{ dB}$ and $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Figure 8: Output power vs. supply voltage

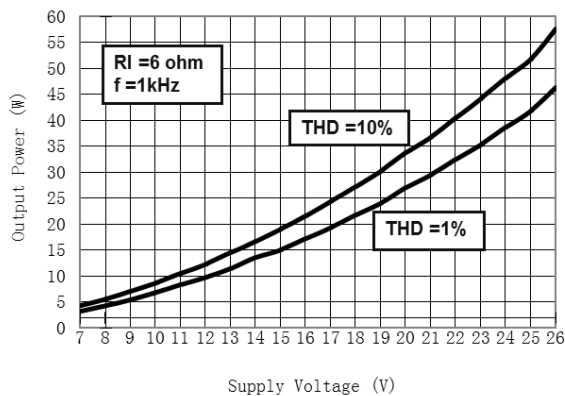


Figure 9: THD vs. Pout ($V_s = 26\text{ V}$, $f = 1\text{ kHz}$)

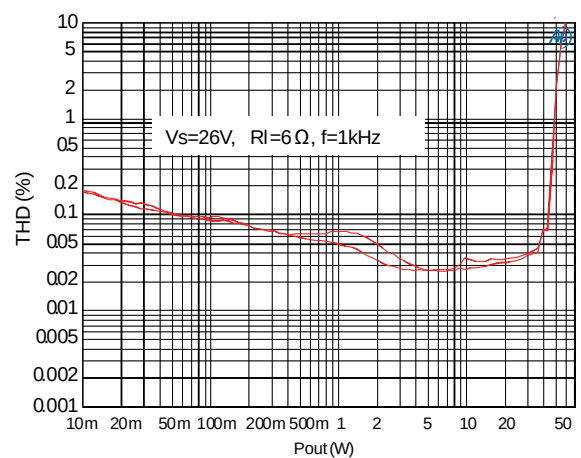


Figure 10: THD vs. Pout ($V_s = 26\text{ V}$, $f = 100\text{ Hz}$)

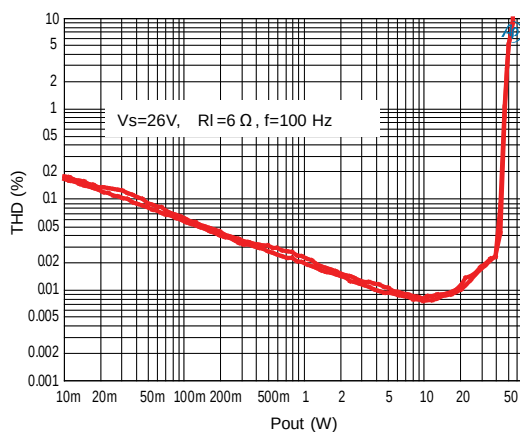


Figure 11: THD vs. Pout ($V_s = 26\text{ V}$, $f = 6\text{ kHz}$)

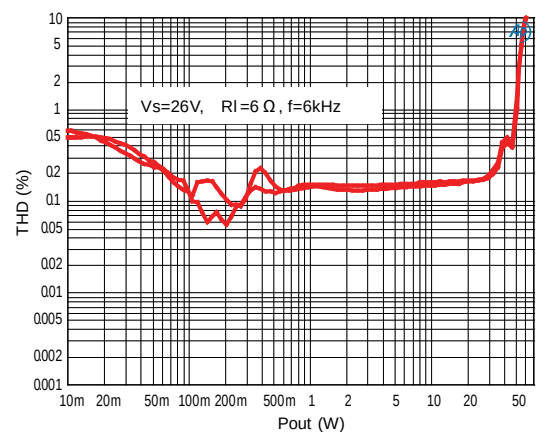


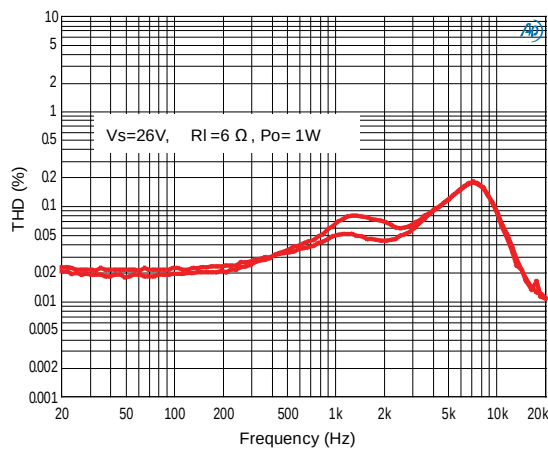
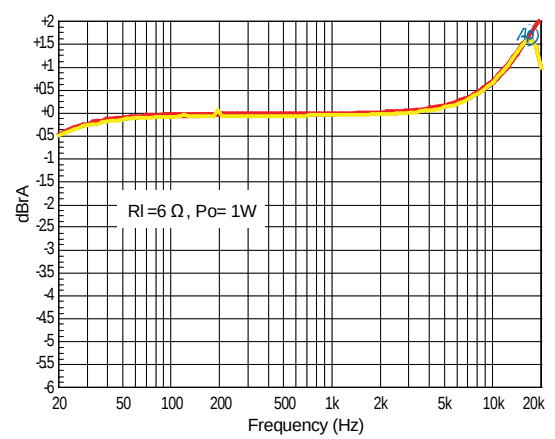
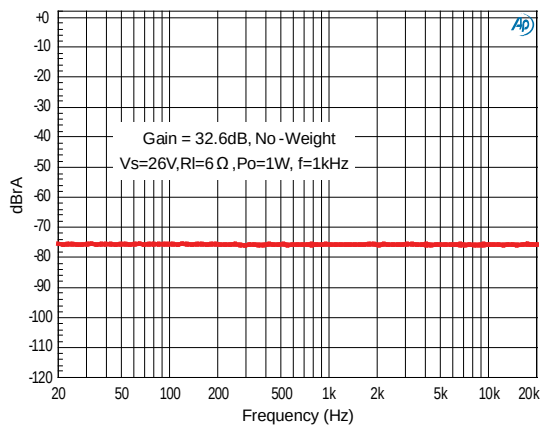
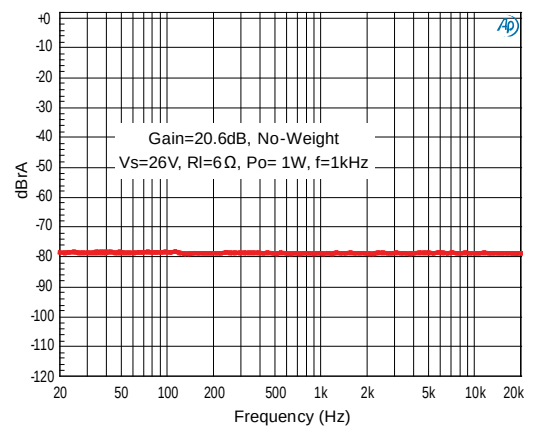
Figure 12: THD vs. frequency ($V_s = 26\text{ V}$, $P_o = 1\text{ W}$)Figure 13: Frequency response $V_s = 26\text{ V}$ Figure 14: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 32.6 dB, not weighted)Figure 15: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 20.6 dB, not weighted)

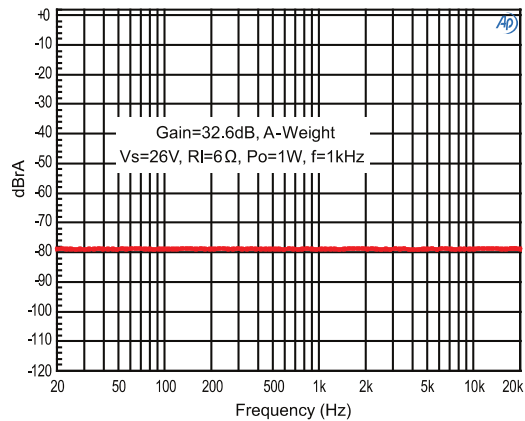
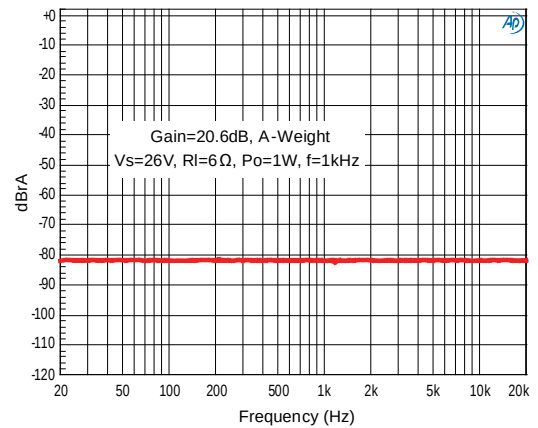
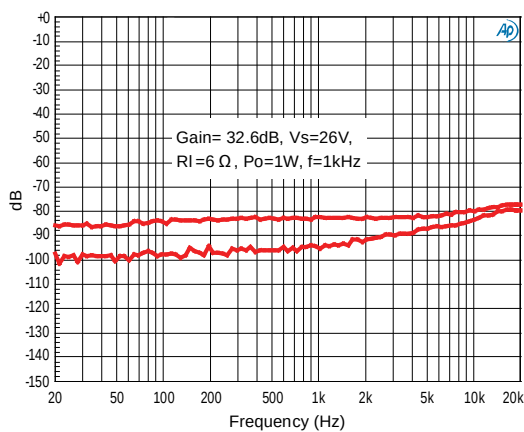
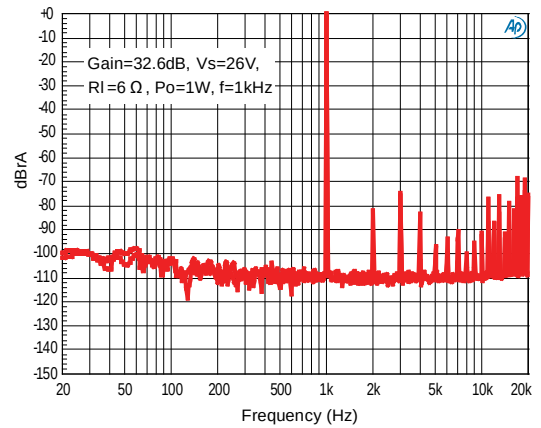
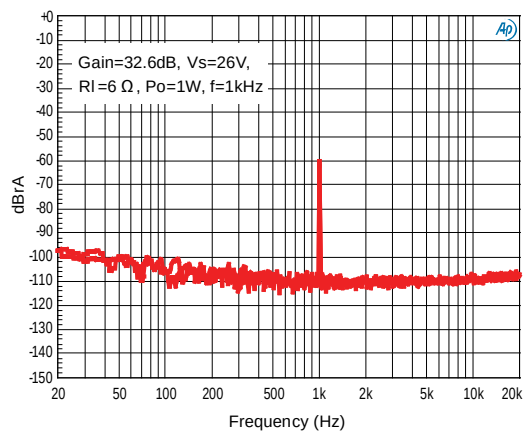
Figure 16: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 32.6 dB, A-weighted)**Figure 17: Signal-to-noise ratio ($V_s = 26\text{ V}$, gain = 20.6 dB, A-weighted)****Figure 18: Crosstalk $V_s = 26\text{ V}$** **Figure 19: FFT (0 dB) $V_s = 26\text{ V}$** 

Figure 20: FFT (-60 dB) $V_s = 26\text{ V}$ 

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 PowerSSO36 EPU package information

The device comes in a 36-pin PowerSSO package with exposed pad up (EPU).

Figure 21: "PowerSSO-36 EPU package outline" shows the package outline and Table 13: "PowerSSO-36 EPU package mechanical data" gives the dimensions.

Figure 21: PowerSSO-36 EPU package outline

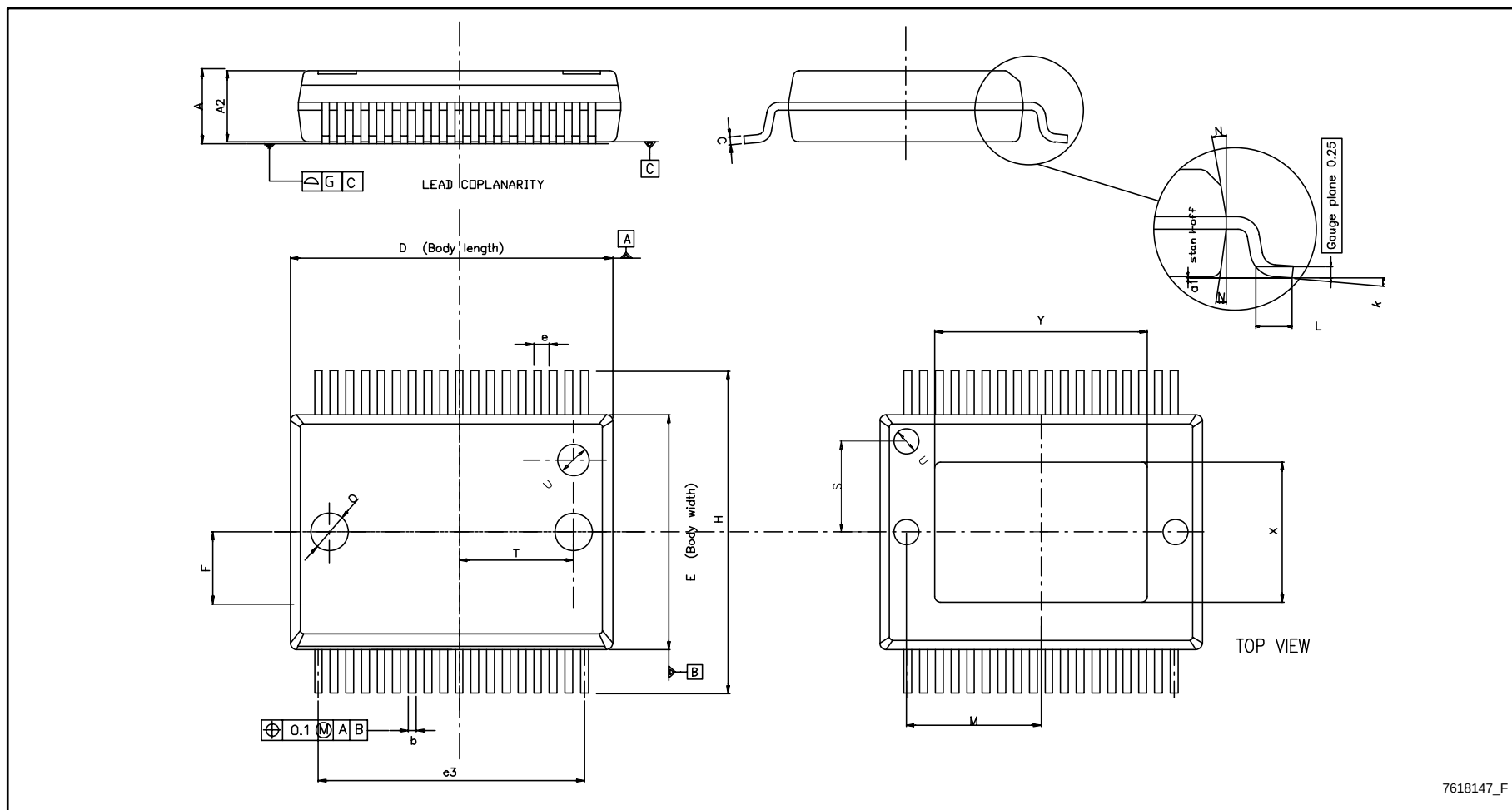


Table 13: PowerSSO-36 EPU package mechanical data

Symbol	Dimensions in mm			Dimensions in inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.15	-	2.45	0.085	-	0.096
A2	2.15	-	2.35	0.085	-	0.093
a1	0	-	0.10	0	-	0.004
b	0.18	-	0.36	0.007	-	0.014
c	0.23	-	0.32	0.009	-	0.013
D	10.10	-	10.50	0.398	-	0.413
E	7.40	-	7.60	0.291	-	0.299
e	-	0.5	-	-	0.020	-
e3	-	8.5	-	-	0.335	-
F	-	2.3	-	-	0.091	-
G	-	-	0.10	-	-	0.004
H	10.10	-	10.50	0.398	-	0.413
h	-	-	0.40	-	-	0.016
k	0	-	8 degrees	0	-	8 degrees
L	0.55	-	0.85	0.022	-	0.033
M	-	4.30	-	-	0.169	-
N	-	-	10 degrees	-	-	10 degrees
O	-	1.20	-	-	0.047	-
Q	-	0.80	-	-	0.031	-
S	-	2.90	-	-	0.114	-
T	-	3.65	-	-	0.144	-
U	-	1.00	-	-	0.039	-
X	4.10	-	4.70	0.161	-	0.185
Y	4.90	-	7.10	0.193	-	0.280

8 Revision history

Table 14: Document revision history

Date	Revision	Changes
24-Feb-2017	1	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2017 STMicroelectronics – All rights reserved