TDA4865J; TDA4865AJ

Vertical deflection booster

Rev. 02 — 3 November 2006 Product data sheet

1. General description

The TDA4865J and TDA4865AJ are deflection boosters for use in vertical deflection systems for frame frequencies up to 200 Hz.

The TDA4865J needs a separate flyback supply voltage, so the supply voltages are independently adjustable to optimize power consumption and flyback time.

For the TDA4865AJ the flyback supply voltage will be generated internally by doubling the supply voltage and therefore a separate flyback supply voltage is not needed.

Both circuits provide differential input stages.

2. Features

- Power amplifier with differential inputs
- Output current up to 3.8 A (p-p)
- High vertical deflection frequency up to 200 Hz
- High linear sawtooth signal amplification
- Flyback generator:
  - TDA4865J: separate adjustable flyback supply voltage up to 70 V
  - TDA4865AJ: internally doubled supply voltage (two supply voltages only for DC-coupled outputs)

3. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{P1}	supply voltage 1		9	-	35	V
V_{P2}	supply voltage 2		$V_{P1} - 1$	-	70	V
V_{FB}	flyback supply voltage of TDA4865J		$V_{P1} - 1$	-	70	V
V_{P3}	flyback generator output voltage of TDA4865AJ	$I_{VOUT} = -1.9$ A	0	-	$V_{P1} + 2.2$	V
$V_{i(INN)}$	input voltage on pin INN		1.6	-	$V_{P1} - 0.5$	V
$V_{i(INP)}$	input voltage on pin INP		1.6	-	$V_{P1} - 0.5$	V
I_{P1}	supply current 1	during scan	-	6	10	mA

Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{P2}	quiescent supply current 2	I_{VOUT} = 0	-	25	60	mA
$I_{VOUT(p-p)}$	vertical deflection output current (peak-to-peak value)		-	-	3.8	A
T_{amb}	ambient temperature		–20	-	+75	°C

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA4865J	DBS7P	plastic DIL-bent-SIL power package; 7 leads (lead length 12/11 mm); exposed die pad	SOT524-1
TDA4865AJ			

5. Block diagram

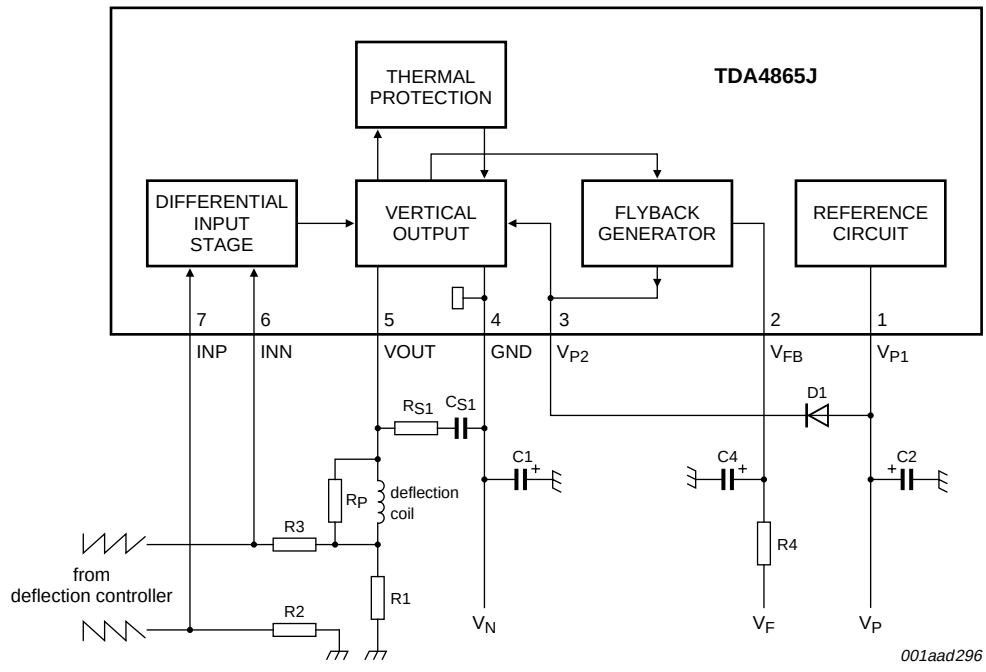


Fig 1. Block diagram of TDA4865J

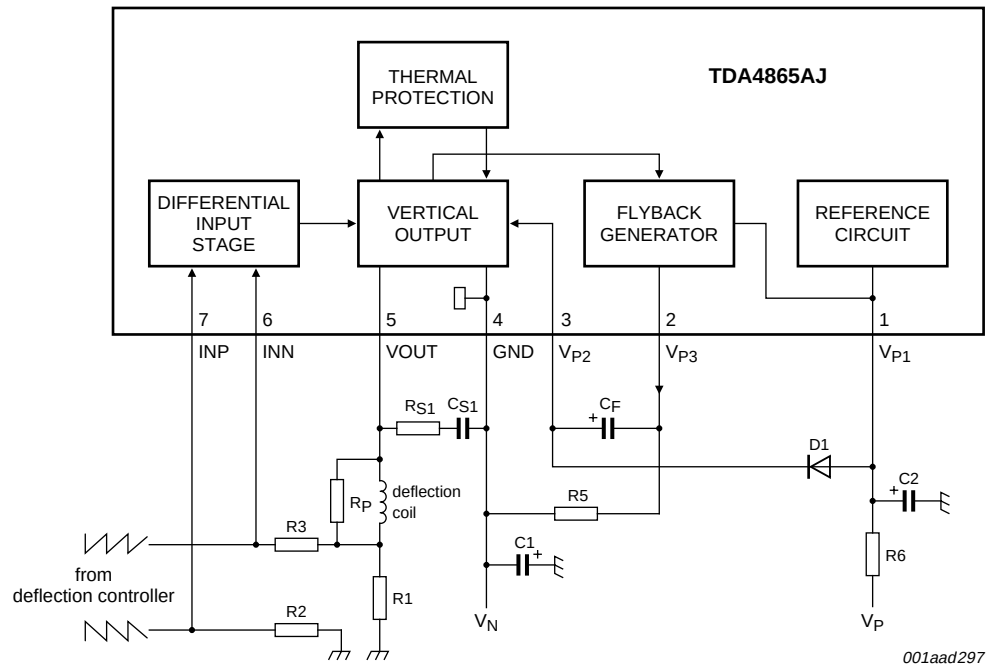


Fig 2. Block diagram of TDA4865AJ

6. Pinning information

6.1 Pinning

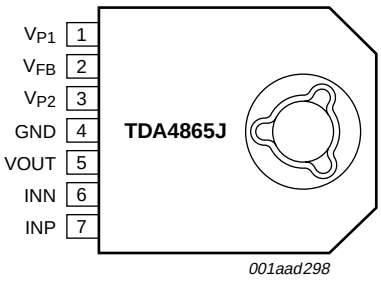


Fig 3. Pin configuration for DBS7P (TDA4865J)

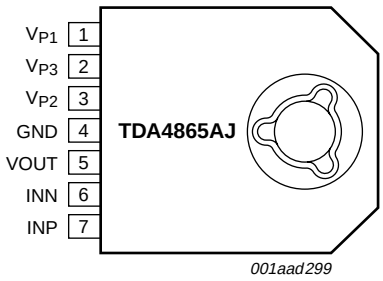


Fig 4. Pin configuration for DBS7P (TDA4865AJ)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TDA4865J	TDA4865AJ	
V_{P1}	1	1	positive supply voltage 1
V_{FB}	2	-	flyback supply voltage
V_{P3}	-	2	flyback generator output
V_{P2}	3	3	supply voltage 2 for vertical output
GND	4	4	ground or negative supply voltage
VOUT	5	5	vertical output
INN	6	6	inverted input of differential input stage
INP	7	7	non-inverted input of differential input stage

7. Functional description

Both the TDA4865J and TDA4865AJ consist of a differential input stage, a vertical output stage, a flyback generator, a reference circuit and a thermal protection circuit.

The TDA4865J operates with a separate flyback supply voltage (see Figure 1) while the TDA4865AJ generates the flyback voltage internally by doubling the supply voltage (see Figure 2).

7.1 Differential input stage

The differential sawtooth input current signal (from the deflection controller) is connected to the inputs (inverted signal to pin INN and non-inverted signal to pin INP). The vertical feedback signal is superimposed on the inverted signal on pin INN.

7.2 Vertical output and thermal protection

The vertical output stage is a quasi-complementary class-B amplifier with a high linearity.

The output stage is protected against thermal overshoots. For a junction temperature of $T_j > 150$ °C the protection will be activated and will reduce the deflection current (I_{VOUT}).

7.3 Flyback generator

The flyback generator supplies the vertical output stage during flyback.

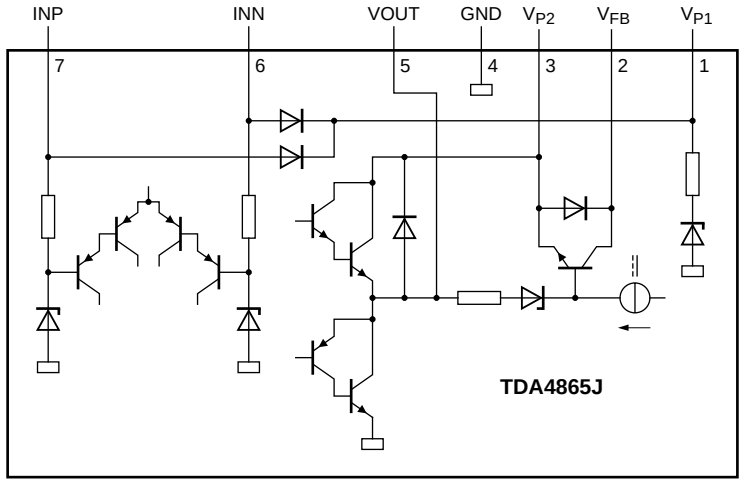
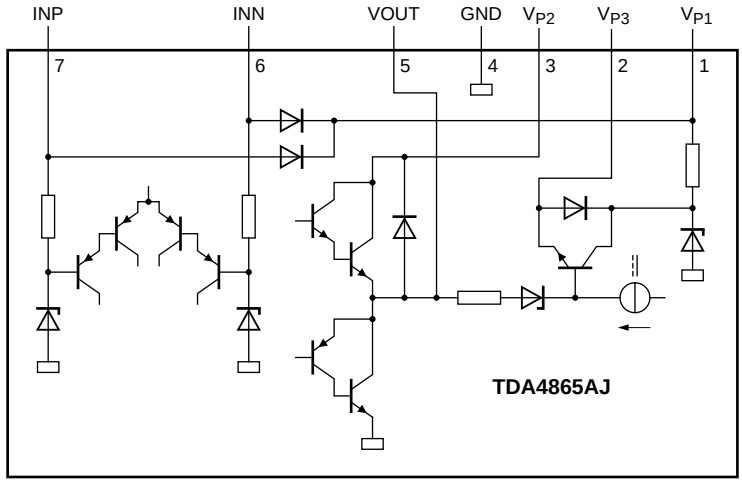
The TDA4865J is used with a separate flyback supply voltage to achieve a short flyback time with minimized power dissipation.

The TDA4865AJ needs a capacitor (C_F) connected between pins V_{P3} and V_{P2} (see Figure 2). Capacitor C_F is charged during scan, using the external diode D1 and resistor R5. During flyback the cathode of capacitor C_F is connected to the positive supply voltage and the flyback voltage is then twice the supply voltage. For the TDA4865AJ the resistor R6 in the positive supply line can be used to reduce the power consumption.

In parallel with the deflection coil a damping resistor R_P and an RC combination (R_{S1} = 5.6 Ω and C_{S1} = 100 nF) are needed. Furthermore, another additional RC combination (R_{S2} = 5.6 Ω and C_{S2} = 47 nF to 150 nF) can be used to minimize the noise effect and the flyback time (see Figure 7 and Figure 8).

8. Internal circuitry

Table 4. Internal circuits

Symbol	Pin	Equivalent circuit
TDA4865J		
V_{P1}	1	
V_{FB}	2	
V_{P2}	3	
GND	4	
VOUT	5	
INN	6	
INP	7	
TDA4865AJ		
V_{P1}	1	
V_{P3}	2	
V_{P2}	3	
GND	4	
VOUT	5	
INN	6	
INP	7	

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9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages referenced to pin GND; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{P1}	supply voltage 1			-	40	V
V_{P2}	supply voltage 2			-	70	V
V_{FB}	flyback supply voltage of TDA4865J			-	70	V
V_{P3}	flyback generator output voltage of TDA4865AJ			0	V_{P1} + 3	V
$V_{i(INN)}$	input voltage on pin INN			-	V_{P1}	V
$V_{i(INP)}$	input voltage on pin INP			-	V_{P1}	V
$V_{o(VOUT)}$	output voltage on pin VOUT			-	72	V
I_{P2}	supply current 2			-	±2.0	A
$I_{o(VOUT)}$	output current on pin VOUT		[1]	-	±2.0	A
I_{VFB}	current during flyback of TDA4865J			-	±2.0	A
I_{VP3}	current during flyback of TDA4865AJ			-	±2.0	A
T_{stg}	storage temperature			–25	+150	°C
T_{amb}	ambient temperature			–20	+75	°C
T_j	junction temperature		[1]	-	150	°C
V_{esd}	electrostatic discharge voltage	machine model	[2]	–400	+400	V
		human body model	[3]	–4000	+4000	V

[1] Internally limited by thermal protection; will be activated for $T_j \geq 150$ °C.

[2] Class C according to EIA/JESD22-A115-A.

[3] Class 3A according to JESD22-A114C.01.

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		[1]	4	K/W

[1] To minimize the thermal resistance from mounting base to heat sink [$R_{th(mb-h)}$] follow the recommended mounting instruction: screw mounting preferred; torque = 40 Ncm; use heat sink compound; isolation plate increases $R_{th(mb-h)}$.

11. Characteristics

Table 7. Characteristics

V_{P1} = 25 V; T_{amb} = 25 °C; voltages referenced to pin GND; unless otherwise specified.

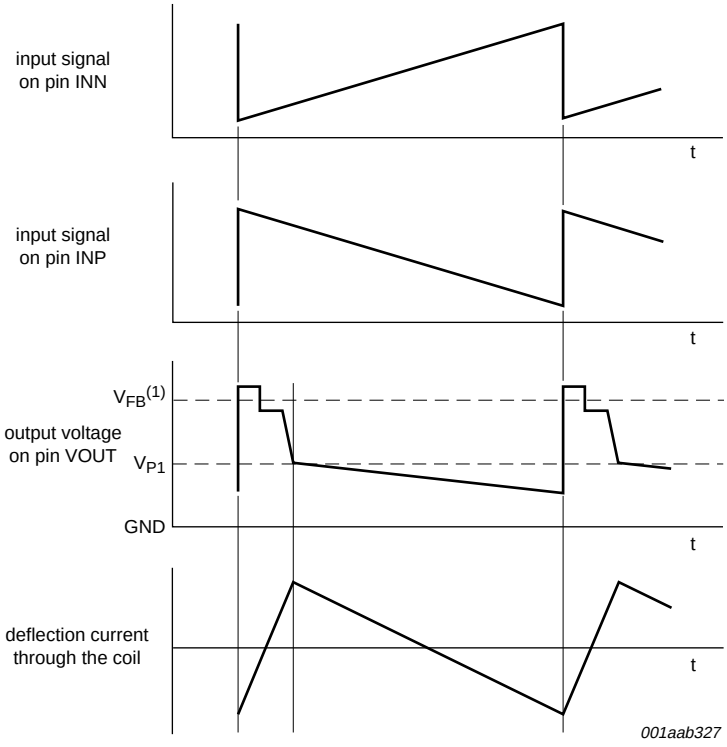
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{P1}	supply voltage 1		9	-	35	V
V_{P2}	supply voltage 2		V_{P1} – 1	-	70	V
V_{FB}	flyback supply voltage of TDA4865J		V_{P1} – 1	-	70	V

Table 7. Characteristics *...continued*

V_{P1} = 25 V; T_{amb} = 25 °C; voltages referenced to pin GND; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{P3}	flyback generator output voltage of TDA4865AJ	I_{VOUT} = –1.9 A	0	-	V_{P1} + 2.2	V
I_{P1}	supply current 1	during scan	-	6	10	mA
I_{P2}	quiescent supply current 2	I_{VOUT} = 0	-	25	60	mA
Differential input stage						
$V_{i(INN)}$	input voltage on pin INN		1.6	-	V_{P1} – 0.5	V
$V_{i(INP)}$	input voltage on pin INP		1.6	-	V_{P1} – 0.5	V
$I_{q(INN)}$	input quiescent current on pin INN		-	–100	–500	nA
$I_{q(INP)}$	input quiescent current on pin INP		-	–100	–500	nA
Flyback generator						
I_{VFB}	current during flyback of TDA4865J		-	-	±1.9	A
I_{VP3}	current during flyback of TDA4865AJ		-	-	±1.9	A
$V_{VP2-VFB(r)}$	reverse voltage drop during flyback of TDA4865J	I_{VOUT} = –1 A	-	–2	-	V
		I_{VOUT} = –1.25 A	-	–2.2	-	V
		I_{VOUT} = –1.9 A	-	–2.7	-	V
$V_{VP2-VFB(f)}$	forward voltage drop during flyback of TDA4865J	I_{VOUT} = 1 A	-	1.5	-	V
		I_{VOUT} = 1.25 A	-	1.7	-	V
		I_{VOUT} = 1.9 A	-	2.1	-	V
$V_{VP3-VP1(r)}$	reverse voltage drop during flyback of TDA4865AJ	I_{VOUT} = –1 A	-	–2	-	V
		I_{VOUT} = –1.25 A	-	–2.2	-	V
		I_{VOUT} = –1.9 A	-	–2.7	-	V
$V_{VP3-VP1(f)}$	forward voltage drop during flyback of TDA4865AJ	I_{VOUT} = 1 A	-	1.5	-	V
		I_{VOUT} = 1.25 A	-	1.7	-	V
		I_{VOUT} = 1.9 A	-	2.1	-	V
Vertical output stage; see Figure 5						
I_{VOUT}	vertical deflection output current		-	-	±1.9	A
$I_{VOUT(p-p)}$	vertical deflection output current (peak-to-peak value)		-	-	3.8	A
$V_{o(sat)n}$	output saturation voltage to ground	I_{VOUT} = 1 A	-	1.3	1.7	V
		I_{VOUT} = 1.25 A	-	1.5	2.3	V
		I_{VOUT} = 1.9 A	-	2.6	3.0	V
$V_{o(sat)p}$	output saturation voltage to V_{P2}	I_{VOUT} = 1 A	–2.3	–2.0	-	V
		I_{VOUT} = 1.25 A	–2.8	–2.2	-	V
		I_{VOUT} = 1.9 A	–3.5	–2.6	-	V
LIN	non-linearity of output signal	[1]	-	-	1	%

[1] Deviation of the output slope at a constant input slope.



(1) V_{FB} for TDA4865J; $2V_{P1}$ for TDA4865AJ.

Fig 5. Timing diagram

12. Application information

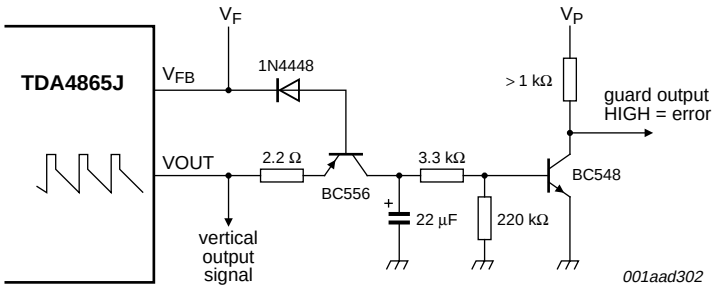
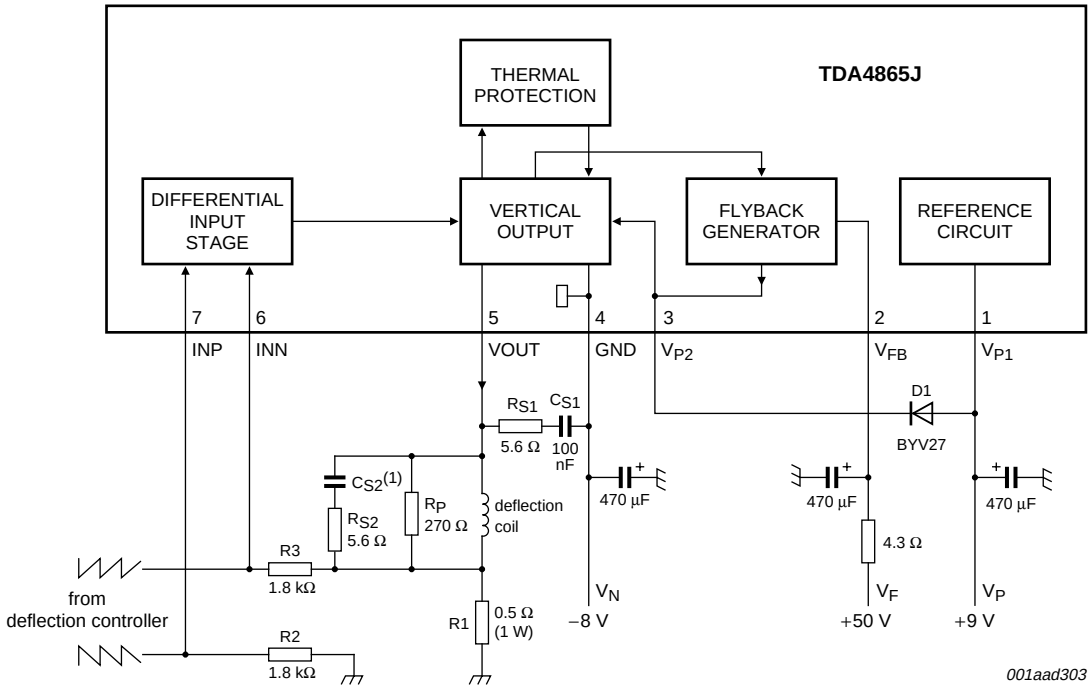


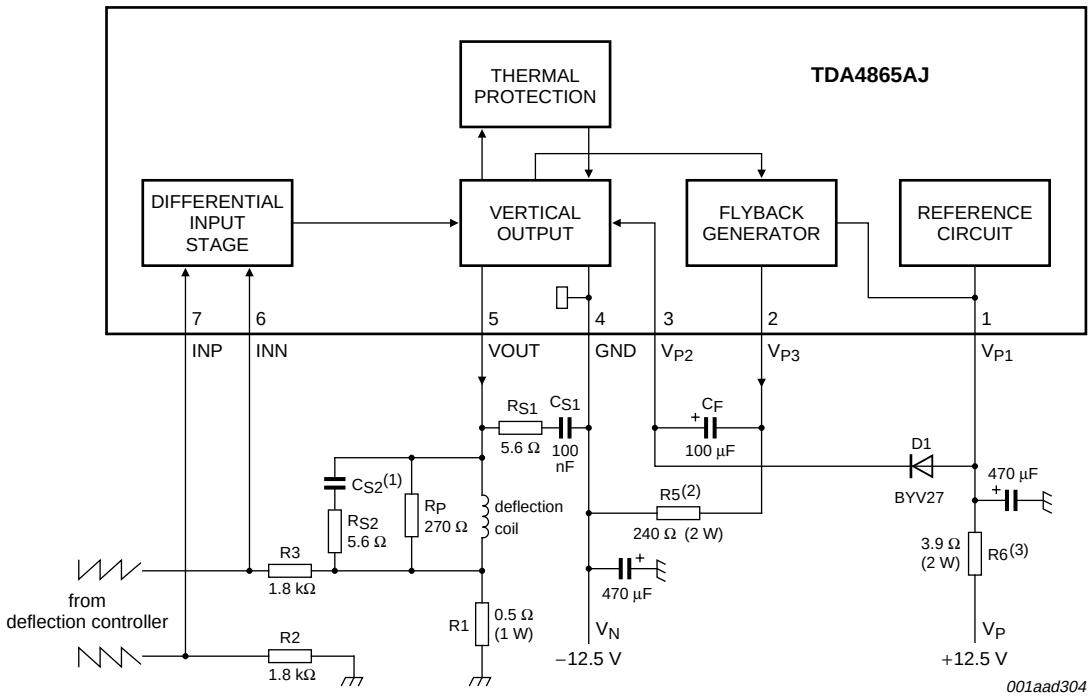
Fig 6. Application diagram with TDA4865J for external guard signal generation



Remark: the heat sink of the IC must be isolated against ground of the application (it is connected to pin GND).

(1) With C_{S2} (typical value between 47 nF and 150 nF) the flyback time and the noise behavior can be optimized.

Fig 7. Application diagram with TDA4865J



Remark: the heat sink of the IC must be isolated against ground of the application (it is connected to pin GND).

(1) With C_{S2} (typical value between 47 nF and 150 nF) the flyback time and the noise behavior can be optimized.

(2) With R5 capacitor C_F will be charged during scan and the value (typical value between 150 Ω and 270 Ω) depends on I_{defl}, t_{flb} and C_F.

(3) R6 reduces the power dissipation of the IC. The maximum possible value depends on the application.

Fig 8. Application diagram with TDA4865AJ

12.1 Example for both TDA4865J and TDA4865AJ

Table 8. Values given from application

Symbol	Value	Unit
$I_{defl(max)(M)}$	1.6 (peak value)	A
$L_{deflcoil}$	10	mH
$R_{deflcoil}$	4	Ω
R_P	270	Ω
R1	0.5	Ω
R2	1.8	kΩ
R3	1.8	kΩ
V_F[1]	50	V
T_{amb}	50	°C
$T_{deflcoil}$	75	°C
$R_{th(j-mb)}$	4	K/W
$R_{th(mb-h)}$	0.5	K/W
$R_{th(h-a)}$	2	K/W

[1] Flyback voltage measured against 0 V; for TDA4865J only.

Table 9. Calculated values

Symbol	Value		Unit
	TDA4865J	TDA4865AJ	
V_{P1}	8	15	V
V_N	–13	–15	V
P_{tot}	8.5	12.1	W
P_{defl}	3.85	3.85	W
P_{IC}	4.65	8.25	W
$R_{th(tot)(max)}$	12.9	7.27	K/W
$T_{j(max)}$[1]	93	103.6	°C
t_{flb}	650	720	µs

[1] With a heat sink of 2 K/W.

V_{P1}, V_N and V_{FB} are referenced to ground of application; voltages are calculated with +10 % tolerances.

The calculation formulae for supply voltages are as follows:

$$V_{P1} = -V_{o(sat)p} + (R1 + R_{deflcoil}) \times I_{defl(max)} - U'_L + U_{D1} \quad (1)$$

$$|V_N| = V_{o(sat)n} + (R1 + R_{deflcoil}) \times I_{defl(max)} + U'_L \quad (2)$$

where:

$U'_L = L_{deflcoil} \times 2I_{defl(max)} \times f_v$

f_v = vertical deflection frequency

U_{D1} = forward voltage drop across D1

The calculation formulae for power consumption is:

$$P_{IC} = P_{tot} - P_{defl} \quad (3)$$

$$P_{tot} = (V_{P1} - U_{D1}) \times \frac{I_{defl(max)}}{4} + |V_N| \times \frac{I_{defl(max)}}{4} + (V_{P1} + |V_N|) \times 0.01 + 0.2 \quad (4)$$

$$P_{defl} = \frac{R_{deflcoil} + R1}{3} \times I^2_{defl(max)} \quad (5)$$

where:

P_{IC} = power dissipation of the IC

P_{tot} = total power dissipation

P_{defl} = power dissipation of the deflection coil

Calculation formulae for maximum required thermal resistance for the heat sink at $T_{j(max)}$ = 110 °C:

$$R_{th(tot)} = R_{th(j\text{-}mb)} + R_{th(mb\text{-}h)} + R_{th(h\text{-}a)} \quad (6)$$

$$R_{th(h\text{-}a)} = \frac{T_{j(max)} - T_{amb}}{P_{IC}} - R_{th(j\text{-}mb)} - R_{th(mb\text{-}h)} \quad (7)$$

Calculation formulae for flyback time (for TDA4865J only):

$$t_{flb} = \frac{L_{deflcoil}}{R_{deflcoil} + R1} \times ln\left(\frac{V_F + (R_{deflcoil} + R1) \times I_{defl(max)}}{V_F - (R_{deflcoil} + R1) \times I_{defl(max)}}\right) \quad (8)$$

where:

V_F measured against 0 V

12.2 Application example for different driver circuits

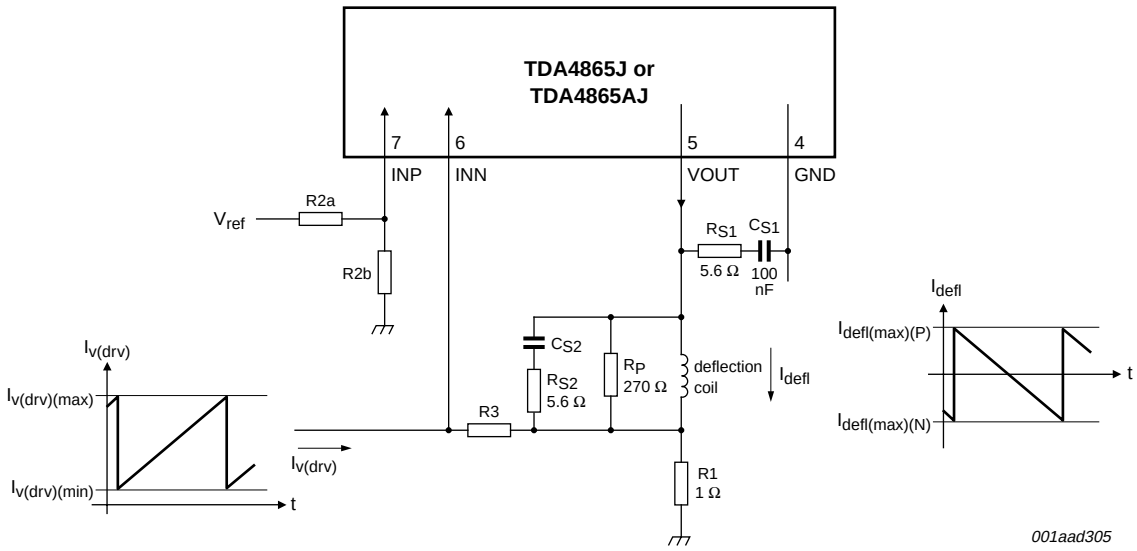


Fig 9. Application for single-ended driver currents with inverting amplifier

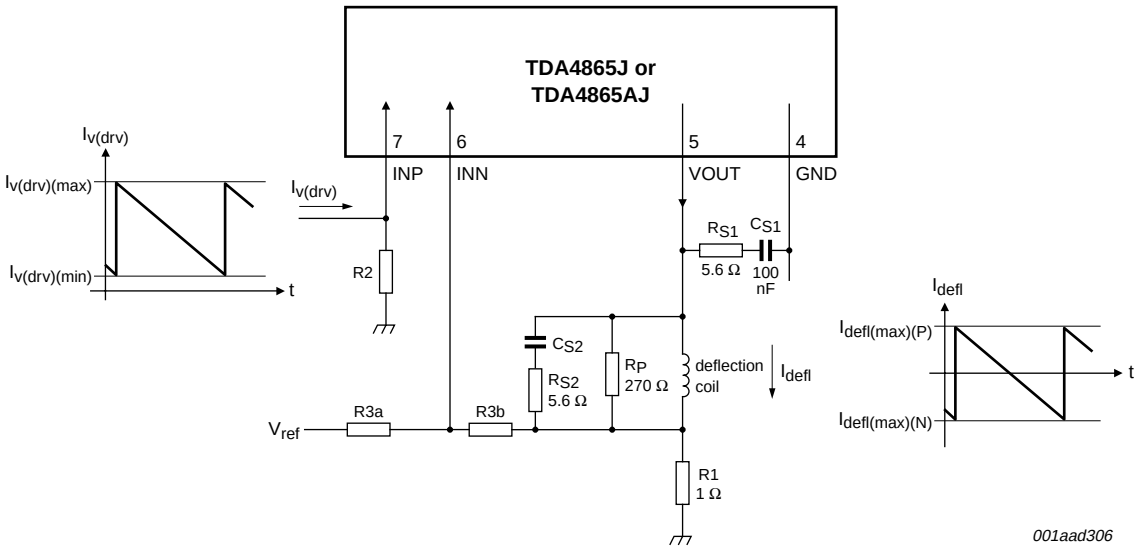


Fig 10. Application for single-ended driver currents with non-inverting amplifier

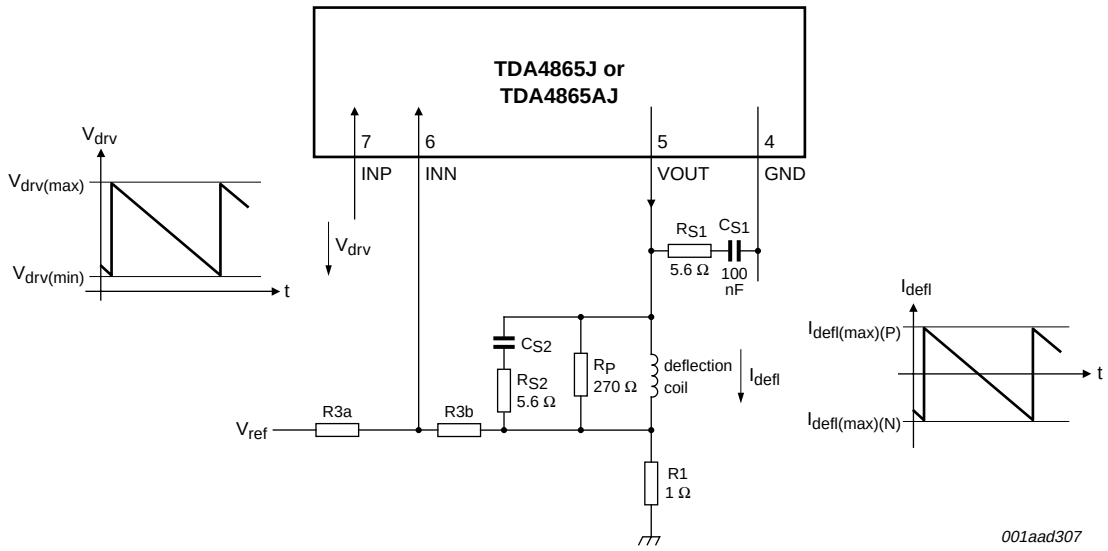
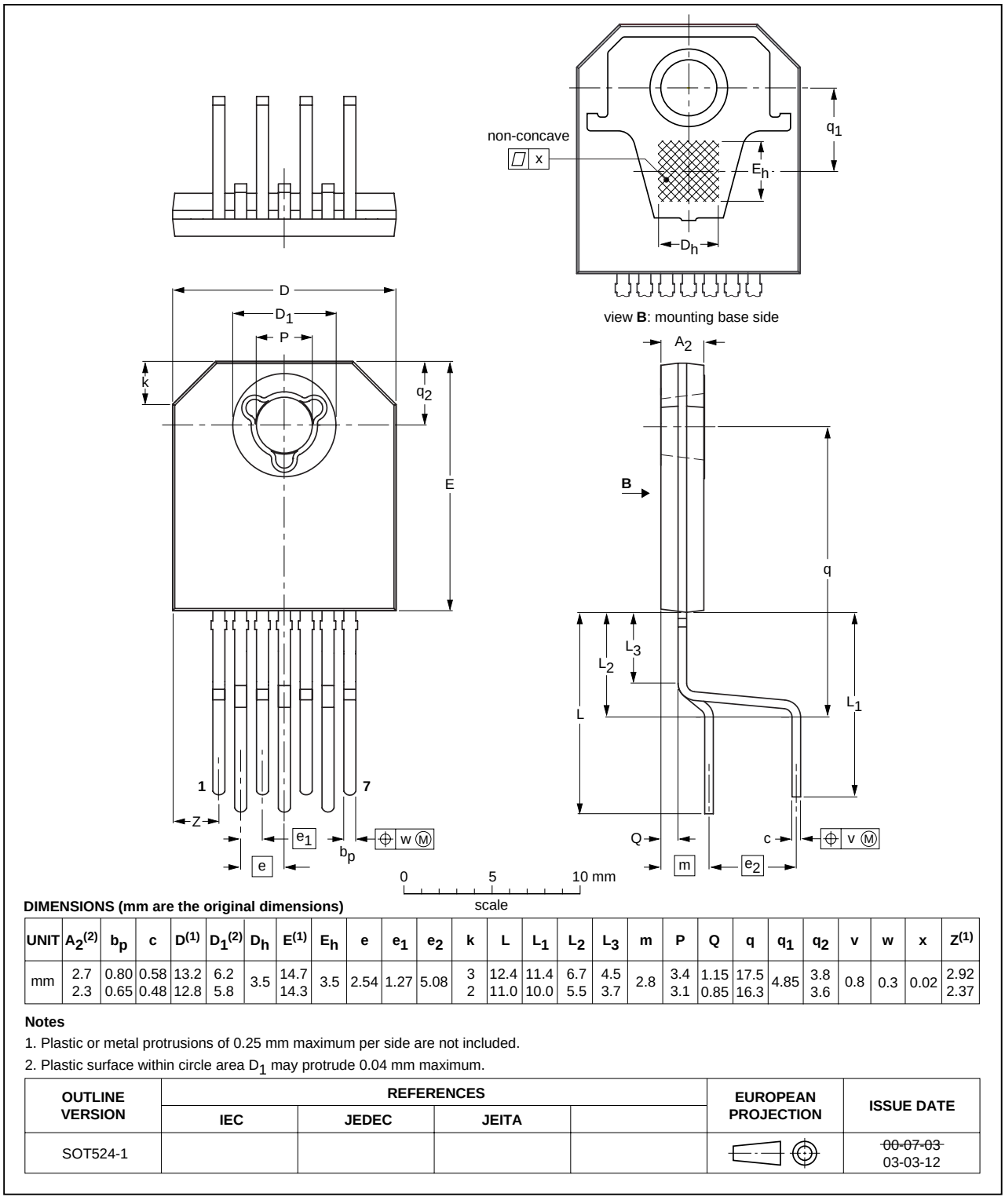


Fig 11. Application for single-ended driver voltage output with non-inverting amplifier

13. Package outline

DBS7P: plastic DIL-bent-SIL power package; 7 leads (lead length 12/11 mm); exposed die pad **SOT524-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A_2 (2)	b_p	c	D (1)	D_1 (2)	D_h	E (1)	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	q_2	v	w	x	Z (1)
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3 2	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	2.92 2.37

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D_1 may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT524-1						~~00-07-03~~ 03-03-12

Fig 12. Package outline SOT524-1 (DBS7P)

14. Soldering

14.1 Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering.

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

14.2 Soldering by dipping or by solder wave

Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing. Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.3 Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 °C and 400 °C, contact may be up to 5 seconds.

14.4 Package related soldering information

Table 10. Suitability of through-hole mount IC packages for dipping and wave soldering

Package	Soldering method	
	Dipping	Wave
CPGA, HCPGA	-	suitable
DBS, DIP, HDIP, RDBS, SDIP, SIL	suitable	suitable[1]
PMFP[2]	-	not suitable

[1] For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

[2] For PMFP packages hot bar soldering or manual soldering is suitable.

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA4865J_TDA4865AJ_2	20061103	Product data sheet	-	TDA4865_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors • Legal texts have been adapted to the new company name where appropriate			
TDA4865_1	19921208	Preliminary specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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