Datasheet, Version 2.1, 22 Feb 2005

PFC-DCM IC

Boost Controller

TDA4863-2/TDA4863-2G

Power-Factor Controller (PFC)
IC for High Power Factor
and Low THD

Power Management & Supply

Never stop thinking.

TDA4863-2/TDA4863-2G

Revision History:	**2005-02-22**	Datasheet

Previous Version: V2.0

Page	Subjects (major changes since last revision)
	Update package information

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Power-Factor Controller (PFC)
IC for High Power Factor
and Low THD

TDA4863-2

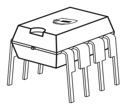
Final Data

Boost Controller

1 Overview

1.1 Features

- IC for sinusoidal line-current consumption
- Power factor achieves nearly 1
- Controls boost converter as active harmonic filter for low THD
- Start up with low current consumption
- Zero current detector for discontinuous operation mode
- Output overvoltage protection
- Output undervoltage lockout
- Internal start up timer
- Totem pole output with active shut down
- Internal leading edge blanking LEB
- Pb-free lead plating ; RoHS compliant



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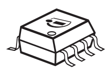


PG-DSO-8-3

1.2 Improvements Referred to TDA 4862 and TDA 4863

- Suitable for universal input applications with low THD at low load conditions
- Very low start up current
- Accurate OVR and $V_{\mathrm{ISENSEmax}}$ threshold
- Competition compatible V_{CC} thresholds
- Enable threshold referred to V_{VSENSE}
- Compared to TDA4863 a bigger MOS Transistor can be driven (see 2.10)

Type	Ordering Code	Package
TDA4863-2	Q67040-S4620	PG-DIP-8-4
TDA4863-2G	Q67040-S4621	PG-DSO-8-3

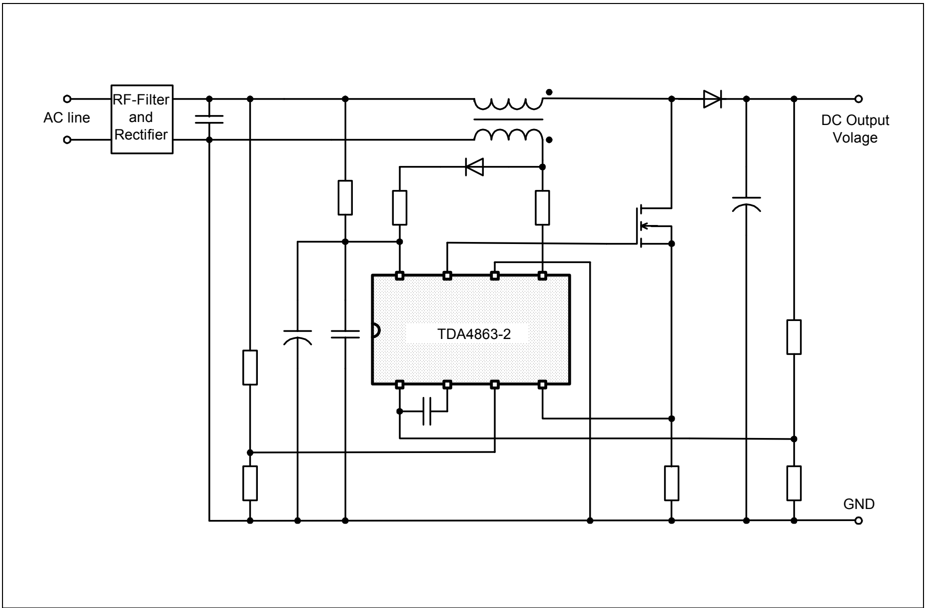


Figure 1 Typical application

1.3 Description

The TDA4863-2 IC controls a boost converter in a way that sinusoidal current is taken from the single phase line supply and stabilized DC voltage is available at the output. This active harmonic filter limits the harmonic currents resulting from the capacitor pulsed charge currents during rectification. The power factor which decibels the ratio between active and apparent power is almost one. Line voltage fluctuations can be compensated very efficiently.

1.4 Pin Configuration

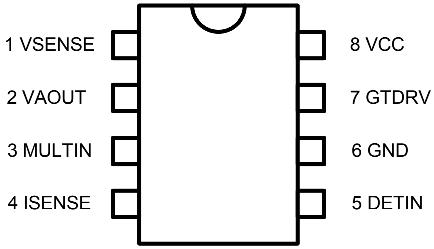


Figure 2 Pin Configuration of TDA4863-2

Pin Definitions and Functions

Pin	Symbol	Description
1	VSENSE	**Voltage Amplifier Inverting Input** VSENSE is connected via a resistive divider to the boost converter output. With a capacitor connected to VAOUT the internal error amplifier acts as an integrator.
2	VAOUT	**Voltage Amplifier Output** V_{VAOUT} is connected internally to the first multiplier input. To prevent overshoot the input voltage is clamped internally at 5 V. IfV_{VAOUT} is less then 2.2 V the gate driver is inhibited. If the current flowing into this pin exceeds an internal threshold the multiplier output voltage is reduced to prevent the MOSFET from overvoltage damage.
3	MULTIN	**Multiplier Input** MULTIN is the second multiplier input and is connected via a resistive divider to the rectifier output voltage.
4	ISENSE	**Current Sense Input** ISENSE is connected to a sense resistor controlling the MOSFET source current. The input is internally clamped at -0.3 V to prevent negative input voltage interaction. A leading edge blanking circuitry suppresses voltage spits when turning the MOSFET on.
5	DETIN	**Zero Current Detector Input** DETIN is connected to an auxiliary winding monitoring the zero crossing of the inductor current.
6	GND	**Ground**
7	GTDRV	**Gate Driver Output** GTDRV is the output of a totem-pole circuitry for direct driving a MOSFET. Compared with TDA4863 the TDA4863-2 can drive 20A MOSFETS. To achieve this the gate output voltage V_{GTL}at I_{GT} =0A has been set to 0.85V. An active shutdown circuitry ensures that GTDRV is set to low if the IC is switched off.
8	VCC	**Positive Voltage Supply** If V_{CC} excees the turn-on threshold the IC is switched on. When Vcc falls below the turn-off threshold the IC is switched off. In switch off mode power consumption is very low. Two capacitors should be connected to Vcc. An electrolytic capacitor and 100nF cermanic capacitor which is used to absorb fast supply current spikes. Make sure that the electrolytic capacitor is discharged before the IC is plugged into the application board.

1.5 Block Diagram

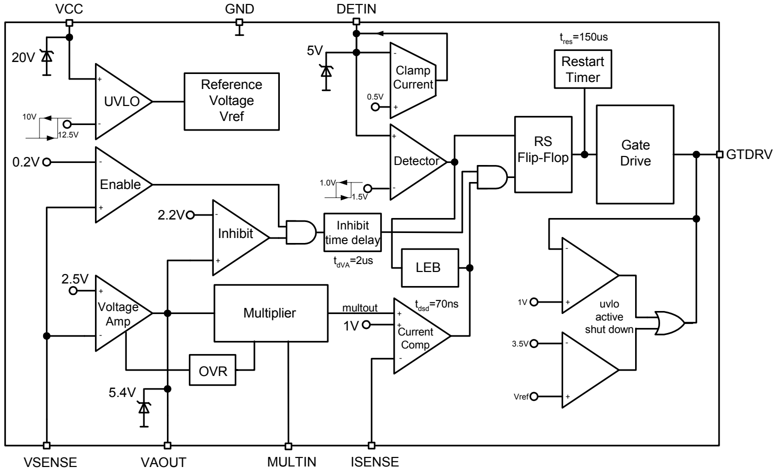


Figure 3 Internal Bolck Diagram

2 Functional Description

2.1 Introduction

Conventional electronic ballasts and switch mode power supplies are designed with a bridge rectifier and a bulk capacitor. Their disadvantage is that the circuit draws power from the line when the instantaneous AC voltage exceeds the capacitors voltage. This occurs near the line voltage peak and causes a high charge current spike with following characteristics: The apparent power is higher than the real power that means low power factor condition, the current spikes are non sinusoidal with a high content of harmonics causing line noise, the rectified voltage depends on load condition and requires a large bulk capacitor, special efforts in noise suppression are necessary.

With the TDA4863-2 preconverter a sinusoidal current is achieved which varies in direct instantaneous proportional to the input voltage half sine wave and so provides a power factor near 1. This is due to the appearance of almost any complex load like a resistive one at the AC line. The harmonic distortions are reduced and comply with the IEC555 standard requirements.

2.2 IC Description

The TDA4863-2 contains a wide bandwidth voltage amplifier used in a feedback loop, an overvoltage regulator, an one quadrant multiplier with a wide linear operating range, a current sense comparator, a zero current detector, a PWM and logic circuitry, a totem-pole MOSFET driver, an internal trimmed voltage reference, a restart timer and an undervoltage lockout circuitry.

2.3 Voltage Amplifier

With an external capacitor between the pins VSENSE and VAOUT the voltage amplifier acts like an integrator. The integrator monitors the average output voltage over several line cycles. Typically the integrator´s bandwidth is set below 20 Hz in order to suppress the 100 Hz ripple of the rectified line voltage. The voltage amplifier is internally compensated and has a gain bandwidth of 5 MHz (typ.) and a phase margin of 80 degrees. The non-inverting input is biased internally at 2.5 V. The output is directly connected to the multiplier input.

The gate drive is disabled when VSENSE voltage is less than 0.2 V or VAOUT voltage is less than 2.2 V.

If the MOSFET is placed nearby the controller switching interferences have to be taken into account. The output of the voltage amplifier is designed in a way to minimize these inteferences.

2.4 Overvoltage Regulator

Because of the integrator´s low bandwidth fast changes of the output voltage can't be regulated within an adequate time. Fast output changes occur during initial start-up, sudden load removal, or output arcing. While the integrator´s differential input voltage remains zero during this fast changes a peak current is flowing through the external capacitor into pin VAOUT. If this current exceeds an internal defined margin the overvoltage regulator circuitry reduces the multiplier output voltage. As a result the on time of the MOSFET is reduced.

2.5 Multiplier

The one quadrant multiplier regulates the gate driver with respect of the DC output voltage and the AC half wave rectified input voltage. Both inputs are designed to achieve good linearity over a wide dynamic range to represent an AC line free from distortion. Special efforts are made to assure universal line applications with respect to a 90 to 270 V AC range.

The multiplier output is internally clamped at 1.3 V. So the MOSFET is protected against critical operating during start up.

2.6 Current Sense Comparator, LEB and RS Flip-Flop

The source current of the MOS transistor is transferred into a sense voltage via the external sense resistor. The multiplier output voltage is compared with this sense voltage. Switch on time of the MOS transistor is determined by the comparison result.

To protect the current comparator input from negative pulses a current source is inserted which sends current out of the ISENSE pin every time when V_{ISENSE}-signal is falling below ground potential. An internal RC-filter is connected to the ISENSE pin which smoothes the switch-on current spike. The remaining switch-on current spike is blanked out via a leading edge blanking circuit with a blanking time of typ. 200 ns.

The RS Flip-Flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle (double pulse suppression).

2.7 Zero Current Detector

The zero current detector senses the inductor current via an auxiliary winding and ensures that the next on-time of the MOSFET is initiated immediately when the inductor current has reached zero. This reduces the reverse recovery losses of the boost converter diode to a miniumum. The MOSFET is switched off when the voltage drop of the shunt resistor reaches the voltage level of the multiplier output. So the boost current waveform has a triangular shape and there are no deadtime gaps between the cycles. This leads to a continuous AC line current limiting the peak current to twice of the average current.

To prevent false tripping the zero current detector is designed as a Schmitt-Trigger with a hysteresis of 0.5 V. An internal 5 V clamp protects the input from overvoltage breakdown, a 0.6 V clamp prevents substrate injection. An external resistor has to be used in series with the auxiliary winding to limit the current through the clamps.

2.8 Restart Timer

The restart timer function eliminates the need of an oscillator. The timer starts or restarts the TDA4863-2 when the driver output has been off for more than 150 µs after the inductor current reaches zero.

2.9 Undervoltage Lockout

An undervoltage lockout circuitry switches the IC on when V_{CC} reaches the upper threshold V_{CCH} and switches the IC off when V_{CC} is falling below the lower threshold V_{CCL}. During start up the supply current is less then 100 µA.

An internal voltage clamp has been added to protect the IC from V_{CC} overvoltage condition. When using this clamp special care must be taken on power dissipation.

Start up current is provided by an external start up resistor which is connected from the AC line to the input supply voltage V_{CC} and a storage capacitor which is connected from V_{CC} to ground. Be aware that this capacitor is discharged before the IC is plugged into the application board. Otherwise the IC can be destroyed due to the high capacitor voltage.

Bootstrap power supply is created with the previous mentioned auxiliary winding and a diode (see **“Application Circuit” on Page 21**).

2.10 Gate Drive

The TDA4863-2 totem pole output stage is MOSFET compatible. An internal protection ciruitry is activated when V_{CC} is within the start up phase and ensures that the MOSFET is turned off. The totem pole output has been optimized to achieve minimized cross conduction current during high speed operation.

Compared to TDA4863 a bigger MOS Transistor can be driven by the TDA4863-2. When a big MOSFET is used in applications with TDA4863, for example SPP20N60C3, the falling edge of the gate drive voltage can swing under GND and can cause false triggering of the IC. To prevent false traiggering the gate drive voltage of theTDA4863-2 at low state and gate current I_{GT} = 0mA is set to V_{GTL}= 0.85V (TDA4863: V_{GTL}=0.25V).

The difference between TDA4863-2 and TDA4863 is also depicted in the diagram: gate drive voltage low state on page 20.

2.11 Signal Diagrams

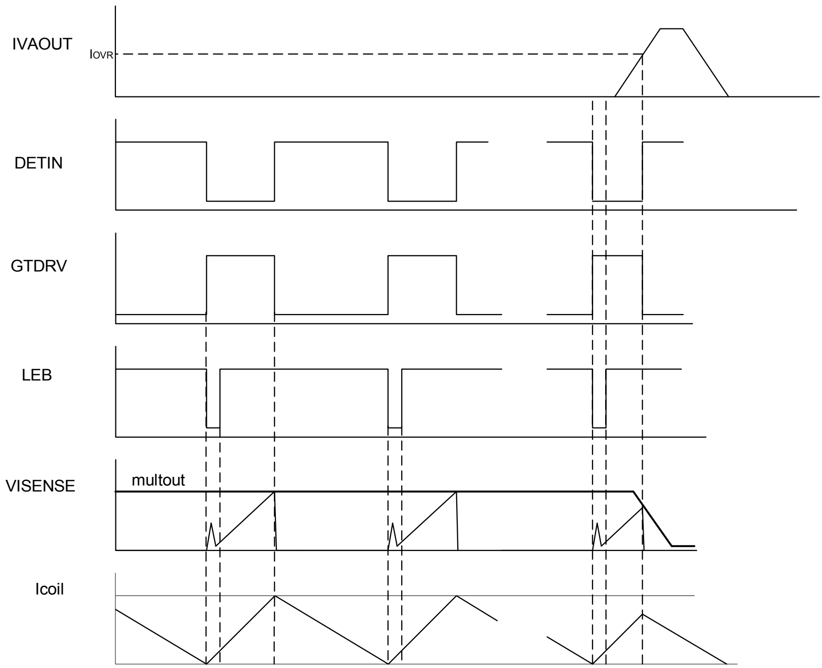


Figure 4 Typical signals

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply + Zener Current	$I_{CCH} + I_Z$		20	mA	
Supply Voltage	V_{CC}	-0.3	V_Z	V	V_Z = Zener Voltage $I_{CC}+I_Z$ = 20 mA
Voltage at Pin 1,3,4		-0.3	6.5		
Current into Pin 2	I_{VAOUT}	 -10	30	mA	V_{VAOUT} = 4 V, V_{VSENSE} = 2.8 V V_{VAOUT} = 0 V, V_{VSENSE} = 2.3 V t < 1 ms
Current into Pin 5	I_{DETIN}	 -10	10		DETIN > 6 V DETIN < 0.4 V t < 1 ms
Current into Pin 7	I_{GTDRV}	-500	500		t < 1 ms
ESD Protection			2000	V	MIL STD 883C method 3015.6, 100 pF,1500 Ω
Storage Temperature	T_{stg}	-50	150	°C	
Operating Junction Temperature	T_J	-40	150		
Thermal Resistance Junction-Ambient	R_{thJA}		100 180	K/W	PG-DIP-8-4 PG-DSO-8-3

3.2 Characteristics

Unless otherwise stated, -40°C < T_j < 150°C, V_{CC} = 14.5 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start-Up circuit						
Zener Voltage	V_Z	18	20	22	V	$I_{CC} + I_Z$ = 20 mA
Start-up Supply Current	I_{CCL}		20	100	µA	$V_{CC} = V_{CCON}$ -0.5 V
Operating Supply Current	I_{CCH}		4	6	mA	Output low
V_{CC} Turn-ON Threshold	V_{CCON}	12	12.5	13	V	
V_{CC} Turn-OFF Threshold	V_{CCOFF}	9.5	10	10. 5		
V_{CC} Hysteresis	V_{CCHY}		2.5			
Voltage Amplifier						
Voltage feedback Input Threshold	V_{FB}	2.45	2.5	2.55	V	
Line Regulation	V_{FBLR}			5	mV	V_{CC} = 12 V to 16 V
Open Loop Voltage Gain[1)]	G_V		100		dB	
Unity Gain Bandwidth[1)]	B_W		5		MHz	
Phase Margin[1)]	M		80		Degr	
Bias Current VSENSE	$I_{BVSENSE}$	-1.0	-0.3		µA	
Enable Threshold	V_{VSENSE}	0.17	0.2	0.25	V	
Inhibit Threshold Voltage	V_{VAOUTI}	2.1	2.2	2.3		V_{ISENSE} = -0.38 V
Inhibit Time Delay	t_{dVA}		3		µs	V_{ISENSE} = -0.38 V
Output Current Source	I_{VAOUTH}		-6		mA	V_{VAOUT} = 0 V V_{VSENSE} = 2.3 V, t < 1 ms
Output Current Sink	I_{VAOUTL}		30			V_{VAOUT} = 4 V V_{VSENSE} = 2.8 V, t < 1 ms
Upper Clamp Voltage	V_{VAOUTH}	4.8	5.4	6.0	V	V_{VSENSE} = 2.3 V, I_{VAOUT} = -0.2 mA
Lower Clamp Voltage	V_{VAOUTL}	0.8	1.1	1.4	V	V_{VSENSE} = 2.8 V, I_{VAOUT} = 0.5 mA

1) Guaranteed by design, not tested

3.2 Characteristics (cont'd)

Unless otherwise stated, -40°C < T_j < 150°C, V_{CC} = 14.5 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overvoltage Regulator						
Threshold Current	I_{OVR}	35	40	45	µA	T_j = 25°C , V_{VAOUT} = 3.5 V
Current Comparator						
Input Bias Current	$I_{BISENSE}$	-1	-0.2	1	µA	V_{ISENSE} = 0 V
Input Offset Voltage (T_j = 25 °C)	$V_{ISENSEO}$		25		mV	V_{VAOUT} = 2.7 V V_{MULTIN} = 0 V
Max Threshold Voltage	$V_{ISENSEM}$	0.95	1.0	1.05	V	
Threshold at OVR	$V_{ISENOVR}$		0.05			I_{OVR} = 50 µA
Leading Edge Blanking	t_{LEB}	100	200	300	ns	
Shut Down Delay	t_{dISG}		80	130		
Detector						
Upper Threshold Voltage	V_{DETINU}		1.5	1.6	V	
Lower Threshold Voltage	V_{DETINL}	0.95	1.1			
Hysteresis	$V_{DETINHY}$	0.25	0.4	0.55		
Input Current	I_{BDETIN}	-1	-0.2	1	µA	V_{DETIN} = 2 V
Input Clamp Voltage High State Low State	 $V_{DETINHC}$ $V_{DETINLC}$	 4.5 0.1	 4.9 0.4	 5.3 0.7	V	 I_{DETIN} = 5 mA I_{DETIN} = -5 mA
Multiplier						
Input bias current	$I_{BMULTIN}$	-1	-0.2	1	µA	V_{MULTIN} = 0 V
Dynamic voltage range MULTIN	V_{MULTIN}		0 to 4		V	V_{VAOUT} = 2.75 V
Dynamic voltage range VAOUT	V_{VAOUT}		V_{FB} to V_{FB} + 1.5			V_{MULTIN} = 1 V
Multiplier Gain	K_{low} K_{high}		0.3 0.7			V_{VAOUT} < 3 V, V_{MULTIN} = 1 V V_{VAOUT} > 3.5V, V_{MULTIN} = 1 V

K = deltaV_{ISENSE}/deltaV_{VAOUT} at V_{MULTIN} = constant

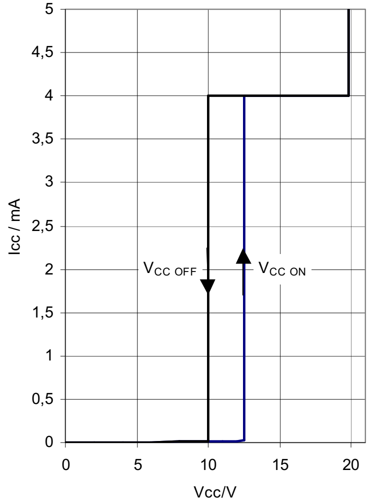
3.2 Characteristics (cont'd)

Unless otherwise stated, -40°C < T_j < 150°C, V_{CC} = 14.5 V

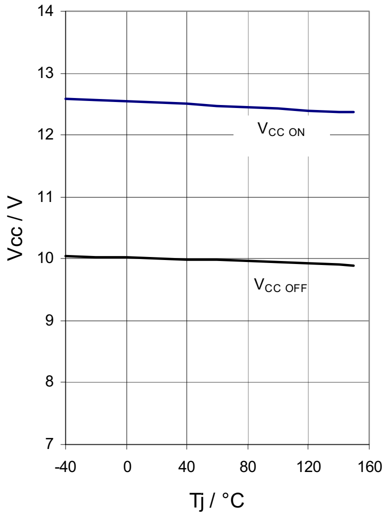
Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Restart Timer						
Restart time	t_{RES}	100	160	250	µs	
Gate Drive						
Gate drive voltage low state	V_{GTL}		0.85		V	I_{GT} = 0 mA
	V_{GTL}		1.0		V	I_{GT} = 2 mA
			1.7			I_{GT} = 20 mA
			2.2			I_{GT} = 200 mA
Gate drive voltage high state	V_{GTH}		10.8			I_{GT} = -5 mA, see **"Gate Drive Voltage High State versus V_{cc}" on Page 20**
Output voltage active shut down	V_{GTSD}		1	1.25		I_{GT} = 20 mA, V_{CC} = 9 V
Rise time	t_{rise}		80	130	ns	C_{GT} = 4.7 nF V_{GT} = 2...8 V
Fall time	t_{fall}		55	130		

3.3 Electrical Diagrams

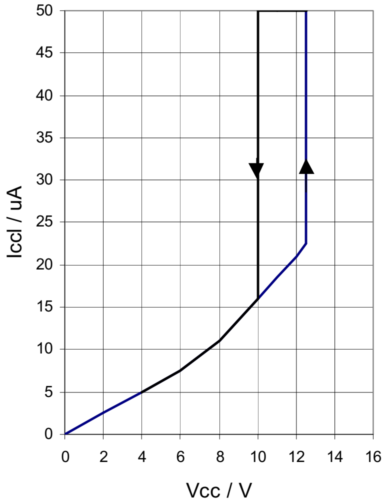
I_{cc} versus V_{cc}



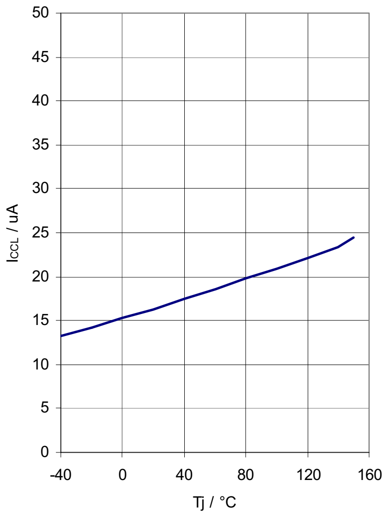
$V_{CCON/OFF}$ versus Temperature



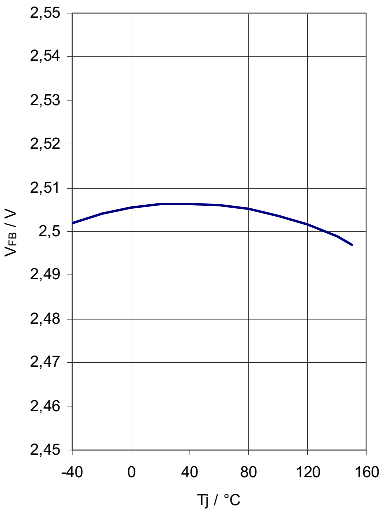
I_{ccl} versus V_{cc}



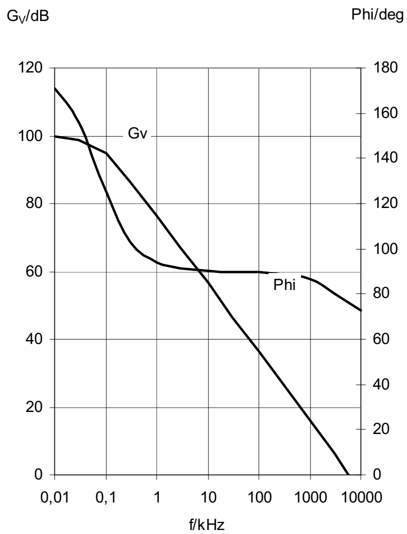
I_{CCL} versus Temperature, V_{CC} = 10 V



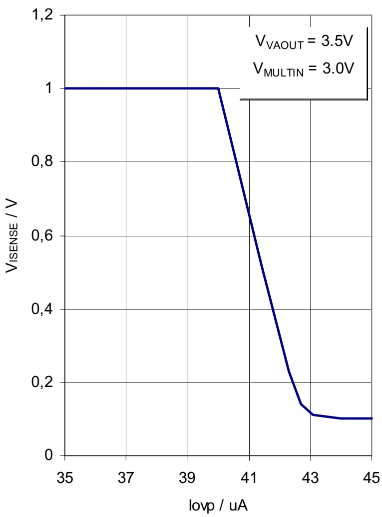
V_{FB} versus Temperature (pin1 connected to pin2)



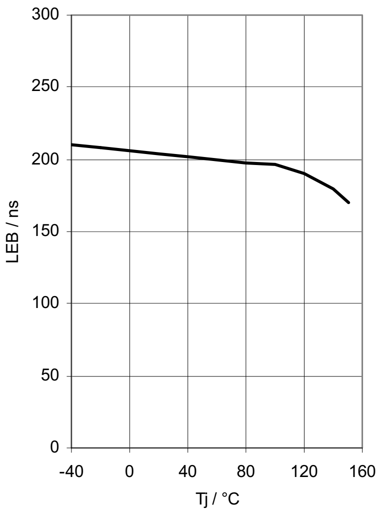
Open Loop Gain and Phase versus Frequency



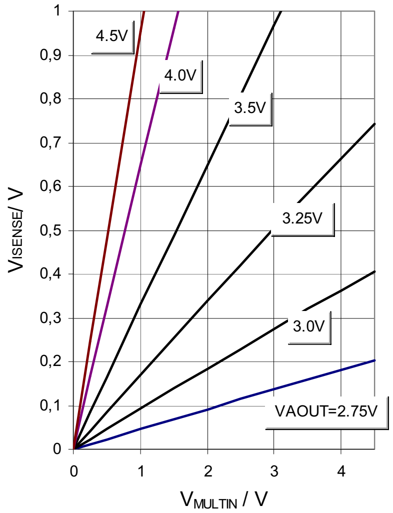
Overvoltage Regulator V_{ISENSE} versus Threshold Voltage



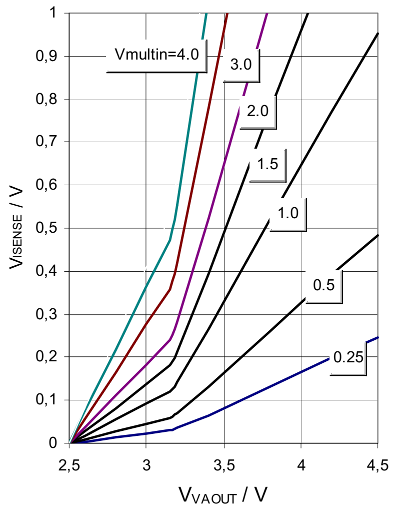
Leading Edge Blanking versus Temperature



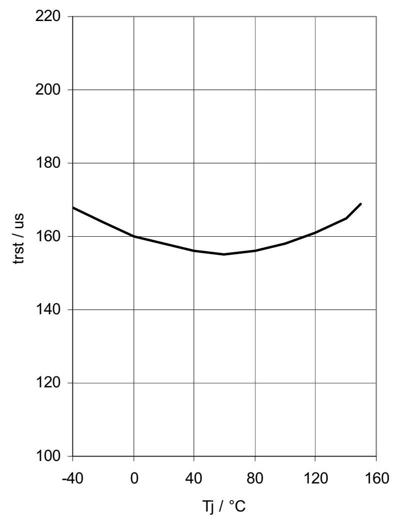
Current Sense Threshold V_{ISENSE} versus V_{MULTIN}



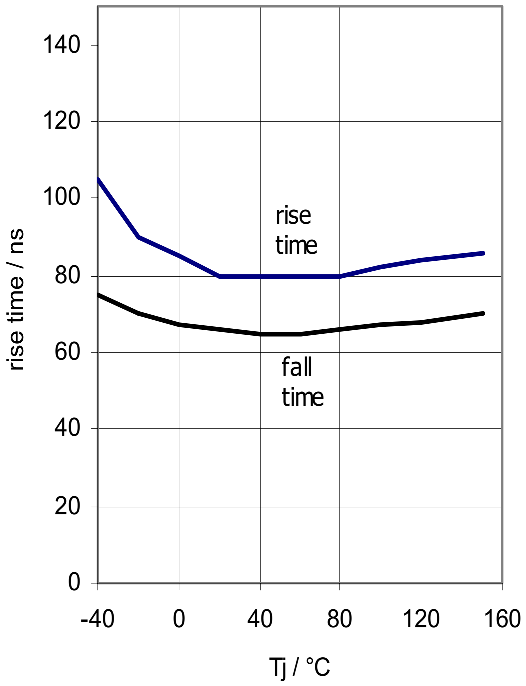
Current Sense Threshold V_{ISENSE} versus V_{VAOUT}



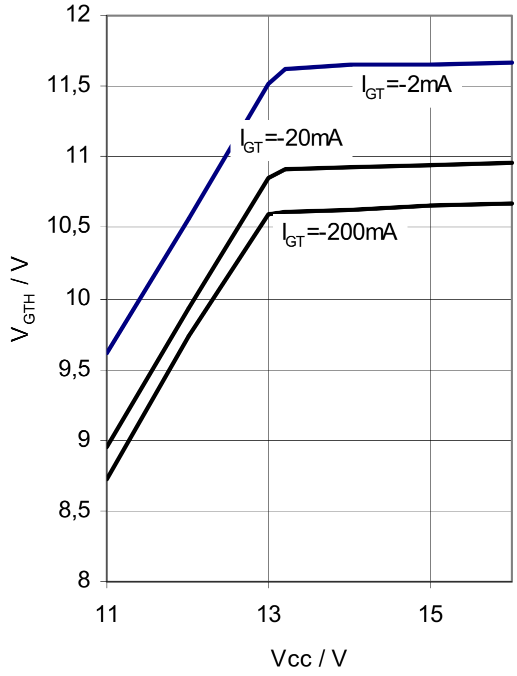
Restart Time versus Temperature



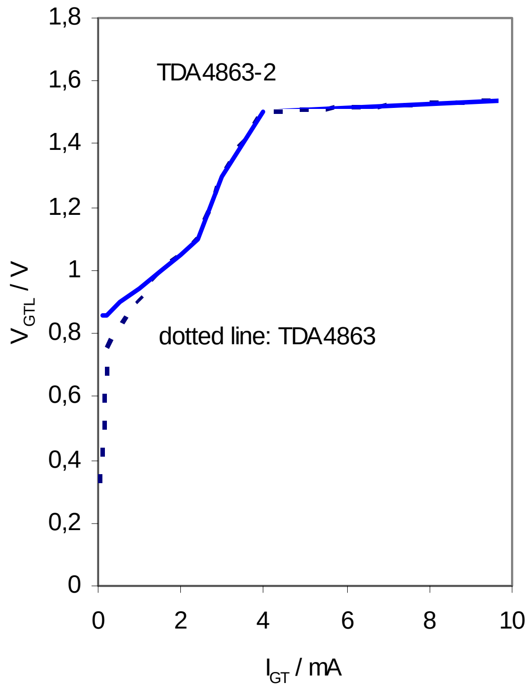
Gate Drive Rise Time and Fall Time versus Temperature



Gate Drive Voltage High State versus V_{cc}



Gate Drive Voltage Low State versus I_{GT}



4 Application Circuit

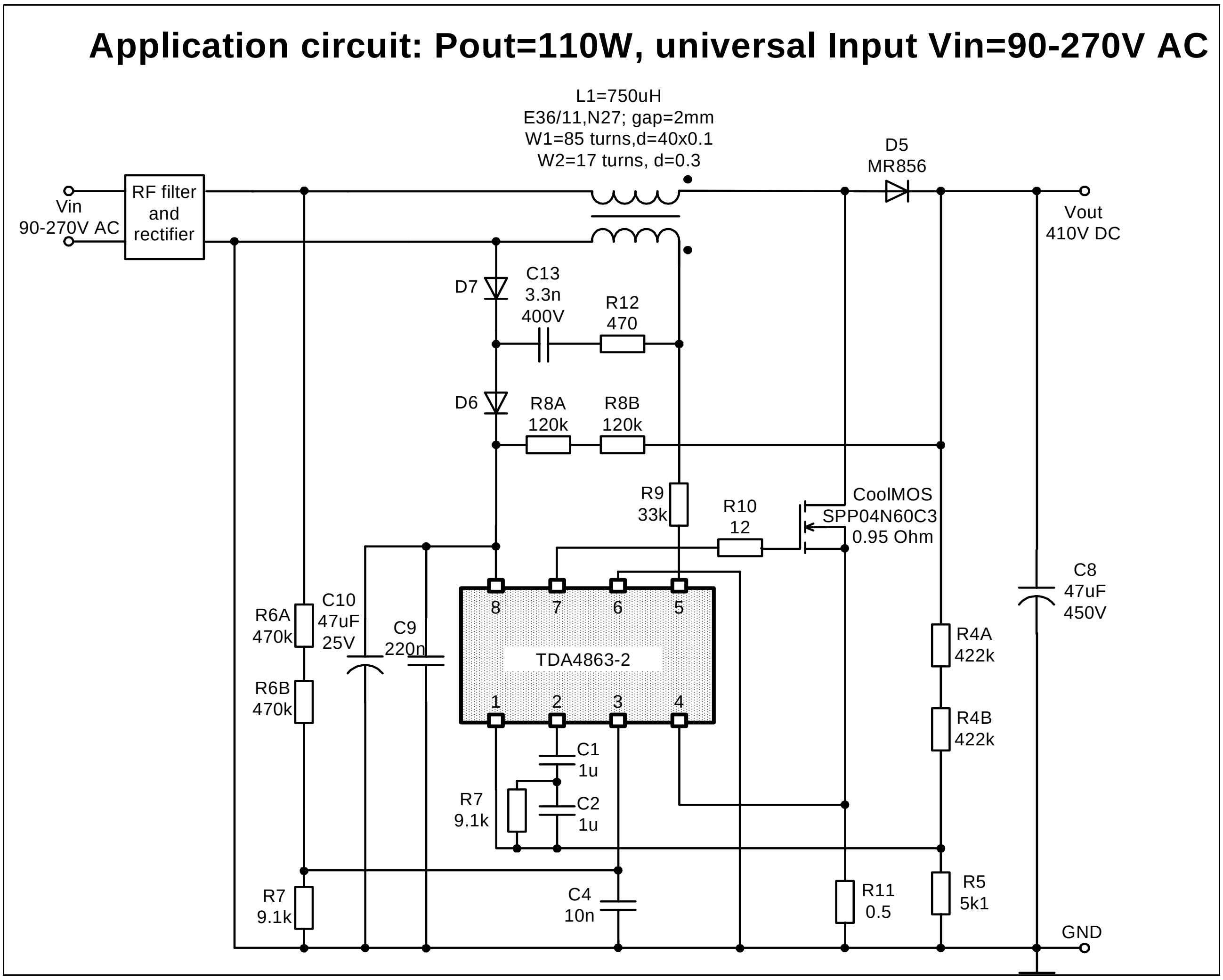


Figure 5 P_{out} **= 110 W, Universal Input** V_{in} **= 90 - 270 V AC**

4.1 Results of THD Measurements with Application Board P_{out} = 110 W

(Measurements according to IEC61000-3-2.
150% limit (red line): Momentary measured value must be below this limit.
100% limit (blue line): Average of measured values must be below this limit.
The worst measured momentary value is shown in the diagrams.)

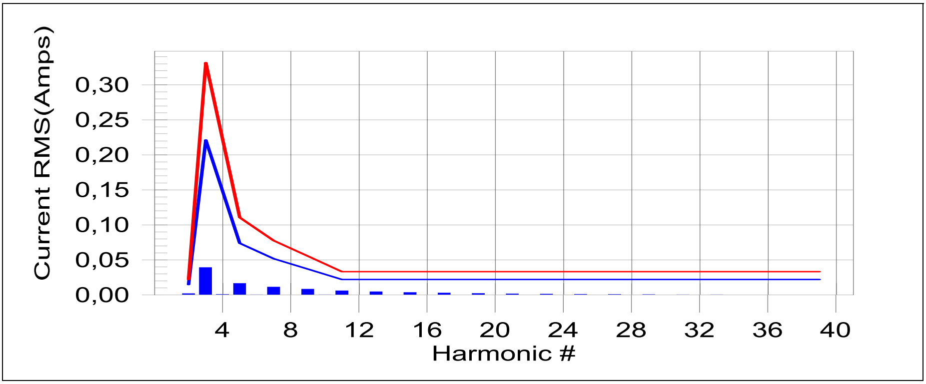


Figure 6 **THD Class C:**
P_{max} = 110 W, V_{inac} = 90 V, I_{out} = 250 mA, V_{out} = 420 V, PF = 0.998

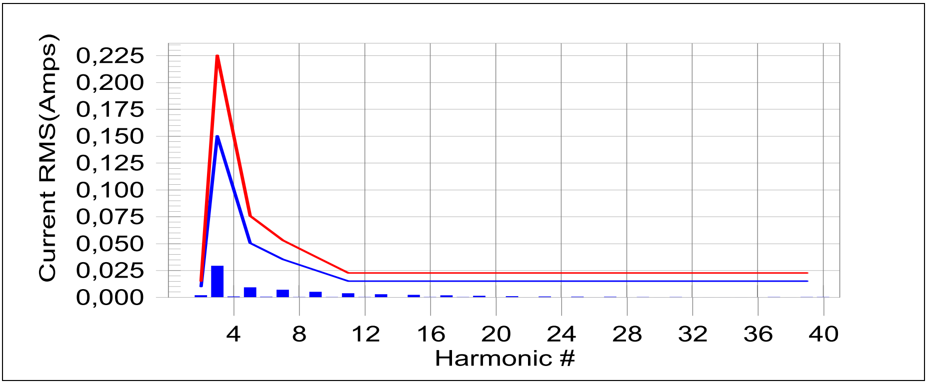


Figure 7 **THD Class C:**
P_{max} = 110 W, V_{inac} = 220 V, I_{out} = 250 mA, V_{aout} = 420 V, PF = 0.992

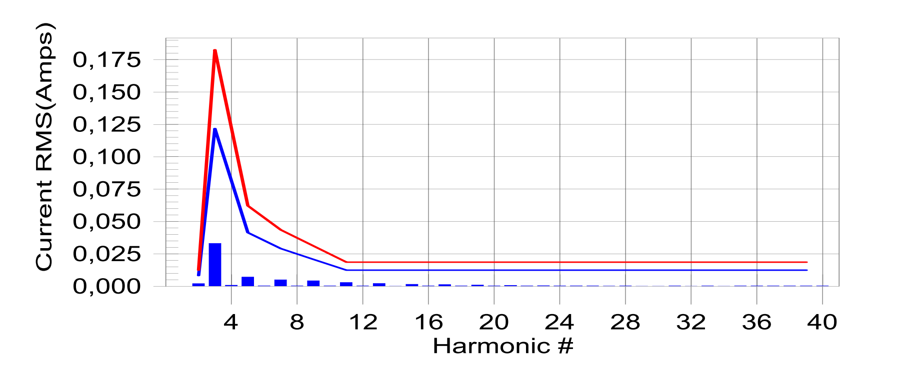


Figure 8 **THD Class C:**
P_{max} **= 110 W,** V_{inac} **= 270 V,** I_{out} **= 250 mA,** V_{aout} **= 420 V, PF = 0.978**

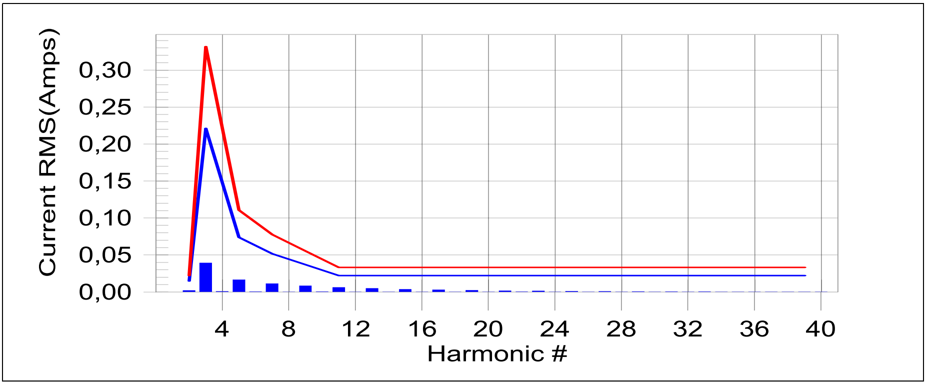


Figure 9 **THD Class C:**
P_{max} **= 110 W,** V_{inac} **= 90 V,** I_{out} **= 140 mA,** V_{aout} **= 420 V, PF = 0.999**

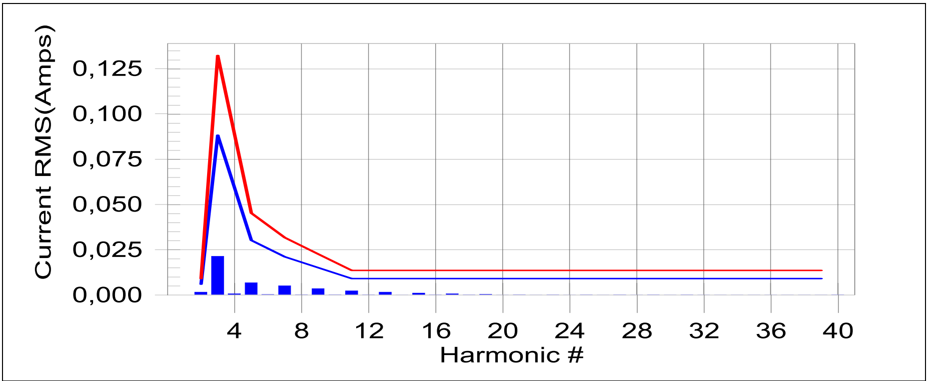


Figure 10 **THD Class C:**
P_{max} = 110 W, V_{inac} = 220 V, I_{out} = 140 mA, V_{aout} = 420 V, PF = 0.975

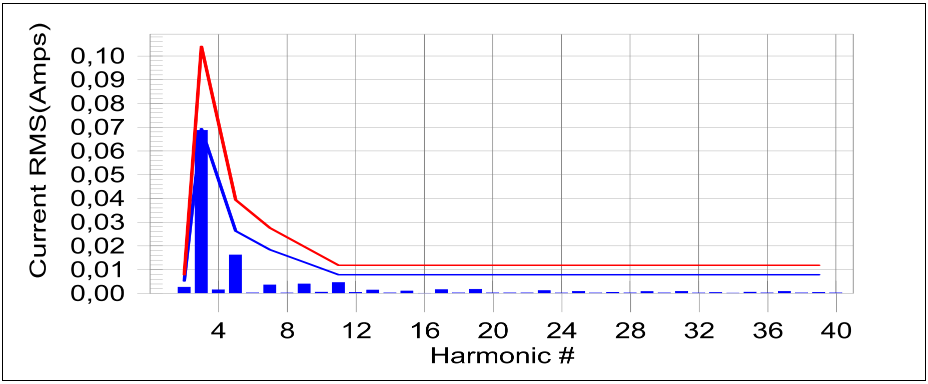


Figure 11 **THD Class C:**
P_{max} = 110 W, V_{inac} = 270 V, I_{out} = 140 mA, V_{aout} = 420 V, PF = 0.883

5 Package Outlines

PG-DIP-8-4
(Plastic Dual In-line Package)

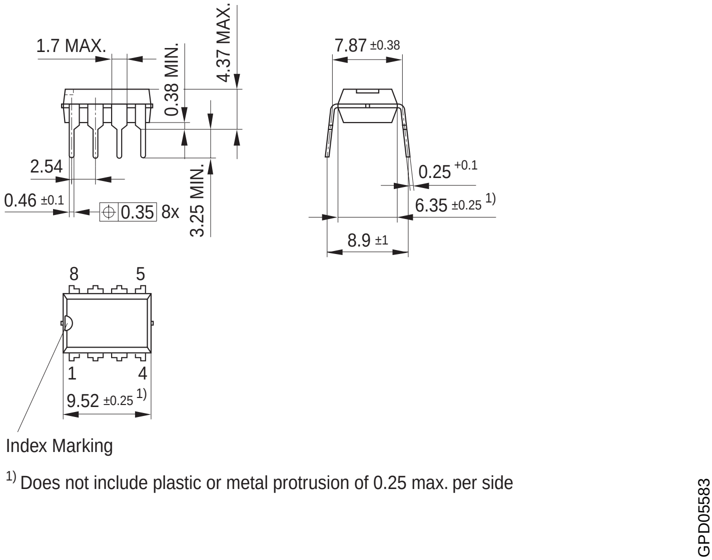


Figure 12

PG-DSO-8-3
(Plastic Dual Small Outline)

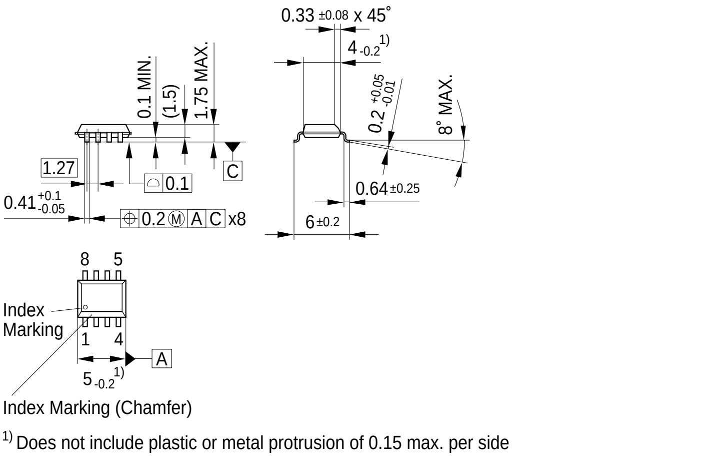


Figure 13

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products.

Dimensions in mm

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern" zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top" (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is "do everything with zero defects", in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

http://www.infineon.com

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