

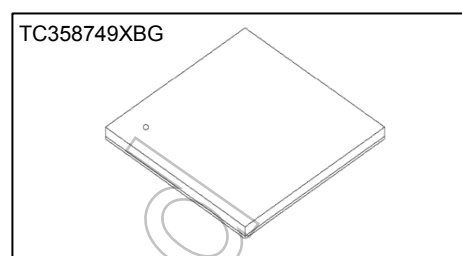
CMOS Digital Integrated Circuit Silicon Monolithic

TC358749XBG

Mobile Peripheral Devices

Overview

The HDMI-RX to MIPI CSI-2-TX is a bridge device that converts HDMI® stream to MIPI® CSI-2 while providing de-interlacing (for test purpose) and auto-scaling features. TC358749XBG shares the same 80-pin package as that of TC358779XBG.



P-VFBGA80-0707-0.65-001

Weight: 77mg (Typ.)

Features

- **HDMI-RX Interface**
 - ✧ HDMI 1.4b
 - Video Formats Support (Up to 1080p @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - HDCP1.4a Support (optional)
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - Maximum HDMI clock speed: 165 MHz
 - ✧ Does not support Audio Return Path and HDMI Ethernet Channels
- **CSI-2 TX Interface**
 - ✧ MIPI CSI-2 compliant (Version 1.1 22 November 2011)
 - ✧ Supports up to 4 data lanes @1Gbps/lane
 - ✧ Supports video data formats
 - RGB888, RGB666, YCbCr422* 16 & 24bit and YCbCr444
- **I²C Slave Interface**
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
 - ✧ Configure all TC358749 XBG internal registers
 - ✧ Support 2 I²C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
- **Audio Output Interface**

Any of the four audio interfaces are available: I2S, TDM, IEC60958 or SLIMbus (pins are multiplexed)

I2S Audio Interface

 - ✧ Up to 4 data lanes for 8-channel data
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
 - ✧ Support Left or Right-justify with MSB first
 - ✧ Support 32 bit-wide time-slot only
 - ✧ Output Audio Over Sampling clock (256fs)
 - ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream) over I2S
 - ✧ Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz
- **TDM (Time Division Multiplexed) Audio Interface**
 - ✧ Fixed to 8 channels
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
 - ✧ Support 32 bit-wide time slot only
 - ✧ Output Audio OverSampling clock (256fs)
- **Digital Audio Interface**
 - ✧ Supports 2 channels (any 2 of the total 8) (depend on HDMI input stream)
 - ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream)
- **SLIMbus Audio Interface**
 - ✧ Up to 8-channel data (2, 4, 6 or 8)
 - ✧ Supports Active Framer (Host) mode as well as active framer outside the chip
 - ✧ Active Manager is not supported.
 - ✧ Supports Isochronous, Pushed & Pulled protocols
 - Isochronous protocol supported only in Active manager scenario
 - ✧ Supports up to 28.8 MHz Root Clock Frequency (in Active Framer mode)
 - ✧ Supports up to 22 MHz clock frequency on Clk lane (in Active Framer mode)
- **Video Processing**
 - ✧ Input formats accepted:
 - RGB or YCbCr422
 - Interlaced or Progressive
 - 2D or 3D
 - Limited to 165 MHz PClk, 640x480, 720x480, 720x576, 1280x720, 1920x1080 or 1920x1200 are expected when scalar is used
 - ✧ Output formats supported:
 - RGB888, RGB666, YCbCr444 or YCbCr422
 - Interlaced (in case of no video processing) or Progressive
 - 2D or 3D
 - Limited by 4Gbps D-PHY bandwidth, 720x480, 1280x720, 1920x1080 or 1920x1200^{note1} are expected when scalar is invoked

- ✧ Scaling:
 - Hardware performs scaling automatically based on input and output frame size
 - HDMI Rx received input frame size and Panel size programmed in registers
 - Can be overwritten by Software if necessary
 - Horizontal Scaling factors supported:
 - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
 - 2-to-3 and 1-to-3
 - Vertical Scaling factors supported:
 - 1-to-2, 3-to-2 and 3-to-4
 - 2-to-1 and 3-to-1
 - 2-to-3 and 4-to-9
 - 4-to-5 and 8-to-15
 - Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.
- ✧ Color Space Conversion
 - RGB ⇔ YCbCr
 - Two sets of coefficients provided – 1 set for each direction
 - Both color space convertors can be enabled/disabled independent of each other.
- InfraRed (IR)
 - ✧ Support NEC InfraRed protocol.
- System
 - ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is “always-on” power domain
 - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2V
 - ✧ I/O: 1.8V – 3.3V
 - ✧ HDMI: 3.3V
 - ✧ AVDDPLL: 1.2V

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4. I²C bus specification, version 2.1, January 2000, Philips Semiconductor
5. IEC 60958, Digital Audio Interface, First Edition, 1999
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7. MIPI SlimBus, "MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus) Version 1.01.01 – 14 July 2008"

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1. Overview

The HDMI-RX to MIPI CSI-2-TX (H2C+) is a bridge device that converts HDMI stream to MIPI CSI-2 while providing de-interlacing (for test purpose) and auto-scaling features. System Overview block diagrams are shown below.

TC358749XBG share the same 80-pin package as that of TC358779XBG.

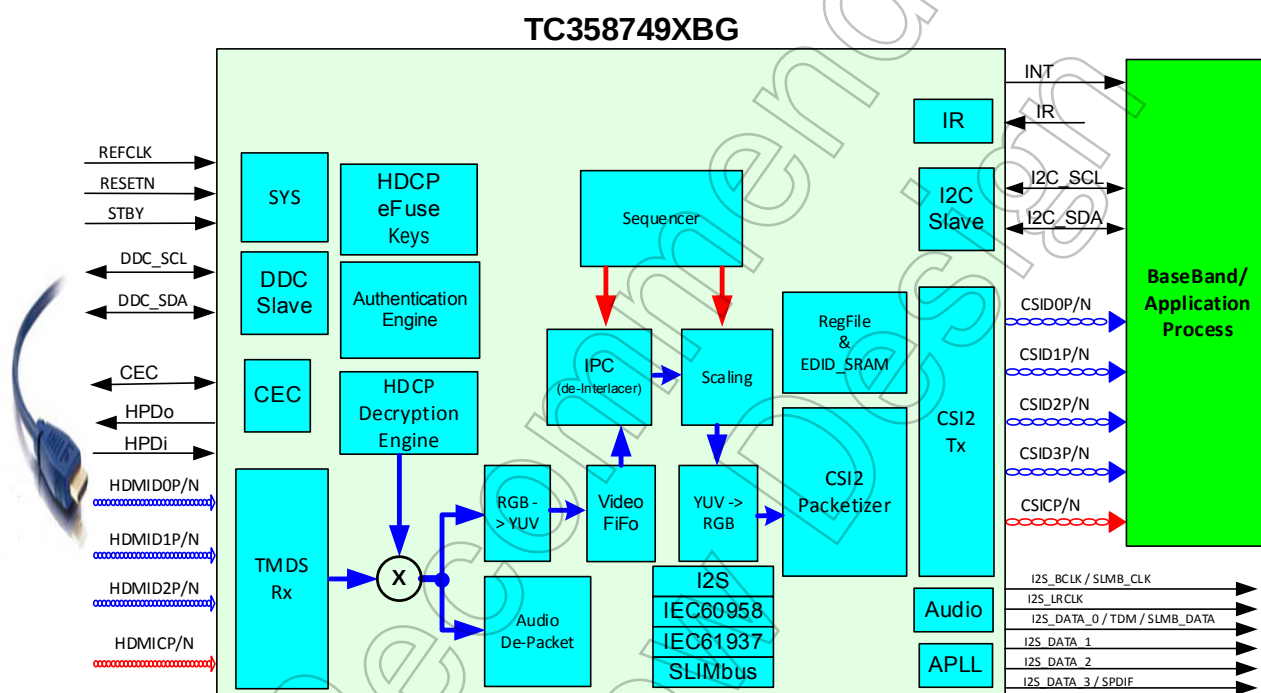


Figure 1.1 TC358749XBG System Overview

2. Features

Below are the main features supported by TC358749XBG.

- HDMI-RX Interface
 - ✧ HDMI 1.4b
 - Video Formats Support (Up to 1080p @60fps)
 - RGB, YCbCr444: 24-bpp @60fps
 - YCbCr422 24-bpp @60fps
 - Audio Supports
 - Internal Audio PLL to track N/CTS value transmitted by the ACR packet.
 - 3D Support
 - HDCP1.4a Support (optional)
 - EDID Support
 - Release A, Revision 1 (Feb 9, 2000)
 - First 128 byte (EDID 1.3 structure)
 - First E-EDID Extension: 128 bytes of CEA Extension version 3 (specified in CEA-861-D)
 - Embedded 1K-byte SRAM (EDID_SRAM)
 - Maximum HDMI clock speed: 165 MHz
 - ✧ Does not support Audio Return Path and HDMI Ethernet Channels
- CSI-2 TX Interface
 - ✧ MIPI CSI-2 compliant (Version 1.1 22 November 2011)
 - ✧ Supports up to 4 data lanes @1Gbps/lane
 - ✧ Supports video data formats
 - RGB888, RGB666, YCbCr422* 16 & 24bit and YCbCr444
- I²C Slave Interface
 - ✧ Support for normal (100 kHz), fast mode (400 kHz) and ultra-fast mode (2 MHz)
 - ✧ Configure all TC358749XBG internal registers
 - ✧ Support 2 I²C Slave Addresses (7'h0F & 7'h1F) selected through boot-strap pin (INT)
- Audio Output Interface

Any of the four audio interfaces are available: I2S, TDM, IEC60958 or SLIMbus (pins are multiplexed)

I2S Audio Interface

 - ✧ Up to 4 data lanes for 8-channel data
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit data (depend on HDMI input stream)
 - ✧ Support Left or Right-justify with MSB first
 - ✧ Support 32 bit-wide time-slot only
 - ✧ Output Audio Over Sampling clock (256fs)
 - ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream) over I2S
 - ✧ Supports HBR audio stream split across 4 I2S lines if bandwidth higher than 12 MHz

TDM (Time Division Multiplexed) Audio Interface

 - ✧ Fixed to 8 channels
 - ✧ Support Master Clock mode only
 - ✧ Support 16, 18, 20 or 24-bit PCM audio data word (depend on HDMI input stream)
 - ✧ Support 32 bit-wide time slot only
 - ✧ Output Audio OverSampling clock (256fs)

Digital Audio Interface

 - ✧ Supports 2 channels (any 2 of the total 8) (depend on HDMI input stream)
 - ✧ Support IEC 60958 & 61937 formats (depending upon HDMI input stream)

- SLIMbus Audio Interface
 - ✧ Up to 8-channel data (2, 4, 6 or 8)
 - ✧ Supports Active Framer (Host) mode as well as active framer outside the chip
 - ✧ Active Manager is not supported.
 - ✧ Supports Isochronous, Pushed & Pulled protocols
 - Isochronous protocol supported only in Active manager scenario
 - ✧ Supports up to 28.8 MHz Root Clock Frequency (in Active Framer mode)
 - ✧ Supports up to 22 MHz clock frequency on Clk lane (in Active Framer mode)
- Video Processing
 - ✧ Input formats accepted:
 - RGB or YCbCr422
 - Interlaced or Progressive
 - 2D or 3D
 - Limited to 165 MHz PClk, 640x480, 720x480, 720x576, 1280x720, 1920x1080 or 1920x1200 are expected when scalar is used
 - ✧ Output formats supported:
 - RGB888, RGB666, YCbCr444 or YCbCr422
 - Interlaced (in case of no video processing) or Progressive
 - 2D or 3D
 - Limited by 4Gbps D-PHY bandwidth, 720x480, 1280x720, 1920x1080 or 1920x1200 ^{note1} are expected when scalar is invoked
 - ✧ Scaling:
 - Hardware performs scaling automatically based on input and output frame size
 - HDMI Rx received input frame size and Panel size programmed in registers
 - Can be overwritten by Software if necessary
 - Horizontal Scaling factors supported:
 - 3-to-2, 1-to-2, 3-to-4, 3-to-8, 9-to-4 and 9-to-16
 - 2-to-3 and 1-to-3
 - Vertical Scaling factors supported:
 - 1-to-2, 3-to-2 and 3-to-4
 - 2-to-1 and 3-to-1
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 - Special handling of 3D formats FP, SBS & T&B to avoid boundary artifacts.
 - ✧ Color Space Conversion
 - RGB ⇔ YCbCr
 - Two sets of coefficients provided – 1 set for each direction
 - Both color space converters can be enabled/disabled independent of each other.
- InfraRed (IR)
 - ✧ Support NEC InfraRed protocol.
- System
 - ✧ Internal core has two power domains (VDDC1 and VDDC2)
 - VDDC1 is “always-on” power domain
 - VDDC2 can be shut-off during deep sleep mode
- Power supply inputs
 - ✧ Core and MIPI D-PHY: 1.2V
 - ✧ I/O: 1.8V – 3.3V
 - ✧ HDMI: 3.3V
 - ✧ AVDDPLL: 1.2V
 - ✧ Power Consumption during typical operation at room temperature

Table 2-1 Power Consumption

		VDDC1	VDDC2	VDDIO1	VDDIO2	VDDMIPI	AVDD33	AVDD12	AVDDPLL	Total Power (mW)
		1.2V	1.2V	3.3V	1.8V	1.2V	3.3V	1.2V	1.2V	
1080p @ 60fps	Current (mA)	61.13		0.80	0.89	20.50	72.80	67.82	0.01	423.83
	Power (mW)	73.36		2.64	1.60	24.60	240.24	81.38	0.01	
720p → 1080p @ 30fps	Current (mA)	170.40		0.80	0.89	20.02	72.66	56.67	1.12	541.87
	Power (mW)	204.48		2.64	1.60	24.02	239.78	68.00	1.34	

Note:

TC358749XBG can support (includes scaling) most valid video stream resolutions; we only list some popular ones here.

3. External Pins

3.1. TC358749XBG Pin Summary

Following table gives the signals of TC358749XBG and their function.

Table 3-1 TC358749XBG Pin Name

Group	Pin Name	I/O	Init (O)	Type	Function	Note
SYSTEM: RESET & CLOCK (5)	RESETN	I	-	Sch	System reset input, active low	1.8V - 3.3V
	REFCLK	I	-	N	Reference clock input (27/26MHz or 42MHz range)	1.8V - 3.3V
	TEST	I	-	N	TEST mode select 0: Normal mode 1: Test mode	1.8V - 3.3V
	STBY	I	-	N	Standby pin, active low	1.8V - 3.3V
	INT	O	L	N	Interrupt Output signal – active high (Level) I ² C Slv_Addr_Sel at boot-strap	1.8V - 3.3V
CSI-2 TX (10)	CSICP	O	H	MIPI-PHY	MIPI-CSI-2 clock positive	1.2V
	CSICN	O	H	MIPI-PHY	MIPI-CSI-2 clock negative	1.2V
	CSID0P	O	H	MIPI-PHY	MIPI-CSI-2 Data 0 positive	1.2V
	CSID0N	O	H	MIPI-PHY	MIPI-CSI-2 Data 0 negative	1.2V
	CSID1P	O	H	MIPI-PHY	MIPI-CSI-2 Data 1 positive	1.2V
	CSID1N	O	H	MIPI-PHY	MIPI-CSI-2 Data 1 negative	1.2V
	CSID2P	O	H	MIPI-PHY	MIPI-CSI-2 Data 2 positive	1.2V
	CSID2N	O	H	MIPI-PHY	MIPI-CSI-2 Data 2 negative	1.2V
	CSID3P	O	H	MIPI-PHY	MIPI-CSI-2 Data 3 positive	1.2V
	CSID3N	O	H	MIPI-PHY	MIPI-CSI-2 Data 3 negative	1.2V
HDMI-RX (8)	HDMICP	I	-	HDMI-PHY	HDMI Clock channel positive	3.3V
	HDMICN	I	-	HDMI-PHY	HDMI Clock channel negative	3.3V
	HDMID0P	I	-	HDMI-PHY	HDMI Data 0 channel positive	3.3V
	HDMID0N	I	-	HDMI-PHY	HDMI Data 0 channel negative	3.3V
	HDMID1P	I	-	HDMI-PHY	HDMI Data 1 channel positive	3.3V
	HDMID1N	I	-	HDMI-PHY	HDMI Data 1 channel negative	3.3V
	HDMID2P	I	-	HDMI-PHY	HDMI Data 2 channel positive	3.3V
	HDMID2N	I	-	HDMI-PHY	HDMI Data 2 channel negative	3.3V
DDC (2)	DDC_SCL	O D	-	FS-SOD	DDC Slave Clock	3.3V (Note1)
	DDC_SDA	O D	-	FS-SOD	DDC Slave data	3.3V (Note1)
CEC	CEC	O D	-	FS-SOD	CEC signal	3.3V
HPD (2)	HPDI	I	-	N	Hot Plug Detect Input	3.3V (Note1)
	HPDO	O	L	N	Hot Plug Detect Output	3.3V
AUDIO (7)	A_SCK	IO	L	N	I2S/TDM Bit/SLIMbus Clock signal	1.8V - 3.3V
	A_WFS	O	L	N	I2S Word Clock or TDM Frame Sync signal	1.8V - 3.3V
	A_SD[0]	IO	L	N	I2S (ch. 0,1)/TDM/SLIMbus data signal	1.8V - 3.3V
	A_SD[2:1]	O	LL	N	I2S (ch. 2,3,4,5) data signal	1.8V - 3.3V
	A_SD[3]	O	L	N	I2S (ch. 6,7) data signal	1.8V - 3.3V
	A_OSCK	O	L	N	Audio Over Sampling Clock	1.8V - 3.3V
IR	IR	I	-	Sch	InfraRed signal	1.8V - 3.3V
I ² C (2)	I2C_SCL	O D	-	FS-SOD	I ² C serial clock	1.8V - 3.3V
	I2C_SDA	O D	-	FS-SOD	I ² C serial data	1.8V - 3.3V
APLL (4)	BIASDA	O	L	-	BIAS signal	-
	DAOUT	O	H	-	Audio PLL clock Reference Output clock Please leave open when not used	-
	PCKIN	I	-	-	Audio PLL Reference Input clock Connect to AVSS through 0.1μF when not used	-
	PFIL	O	L	-	Audio PLL Low Pass Filter signal Connect to AVSS through 0.1μF when not used	-
POWER (11)	VDDC1	-	-	-	VDD for Internal Core (always ON) (1)	1.2V
	VDDC2	-	-	-	VDD for Internal Core (can be powered down) (2)	1.2V
	VDDIO1	-	-	-	VDDIO1 IO power supply (1)	3.3V
	VDDIO2	-	-	-	VDDIO2 IO power supply (1)	1.8V - 3.3V
	VDD_MIPI	-	-	-	VDD for the MIPI CSI-2 (1)	1.2V

Group	Pin Name	I/O	Init (O)	Type	Function	Note
	VDD_PLL11	-	-	-	VDD for PLL11 (1)	1.2V
	AVDD12	-	-	-	HDMI Phy 1.2V power supply (2)	1.2V
	AVDD33	-	-	-	HDMI Phy & APLL 3.3V power supply (2)	3.3V
GROUND (25)	VSS	-	-	-	Ground (25)	-
MISC	REXT ^(Note2)	-	-	-	External Reference Resistor	-
	VPGM ^(Note3)	-	-	-	eFuse program power supply	-

Total 80 pins

Note1: These IO are 5V tolerant.

Note2: Please connect to AVDD33 with a 2kΩ resistor ($\pm 1\%$).

Note3: Please tie to ground.

Buffer Type Abbreviation:

N: Normal IO

FS-SOD: Failed Safe Pseudo open-drain output, Schmidt input

Sch: Schmidt input buffer

MIPI-PHY: front-end analog IO for CSI-2

HDMI-PHY: front-end analog IO for HDMI

3.2. Pin Summary

Table 3-2 Pin Count Summary – TC358749XBG

Group Name	Pin Count	Notes
SYSTEM	5	-
CSI-2 TX	11	Include Power pins
HDMI RX	13	Include Power, External (Misc) Resistor pins.
DDC	2	-
CEC	1	-
Audio	7	-
I ² C	2	-
IR	1	-
HPD	2	-
APLL	4	Audio PLL – Include Power pin
POWER	7	IO, Core, eFuse
GROUND	25	IO, Core, Analog
TOTAL	80	-

3.3. Pin Layout

Top View (through the die)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10
AVDD12	REXT	VDDC2	BIASDA	DAOUT	PFIL	VSS	VDD_PLL11	CSID3N	CSID3P
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10
AVDD33	VSS	VSS	VSS	VSS	VSS	PCKIN	VSS	CSID2N	CSID2P
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
HDMICP	HDMICN							CSICN	CSICP
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10
HDMID0P	HDMID0N		VSS	VSS	VSS	VSS		VSS	VDD_MIPI
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10
HDMID1P	HDMID1N		VSS	VSS	VSS	VSS		CSID1N	CSID1P
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10
HDMID2P	HDMID2N		VSS	VSS	VSS	VSS		CSID0N	CSID0P
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10
AVDD33	VSS		VPGM	TEST	VSS	VSS		VSS	A_OSCK
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10
AVDD12	CEC							A_SD_0	A_WFS
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10
DDC_SCL	DDC_SDA	HPDO	INT	I2C_SCL	IR	REFCLK	VSS	A_SCK	A_SD_1
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10
VDDC1	VDDIO1	HPDI	STBY	I2C_SDA	RESETN	VDDIO2	A_SD_3	A_SD_2	VDDC2

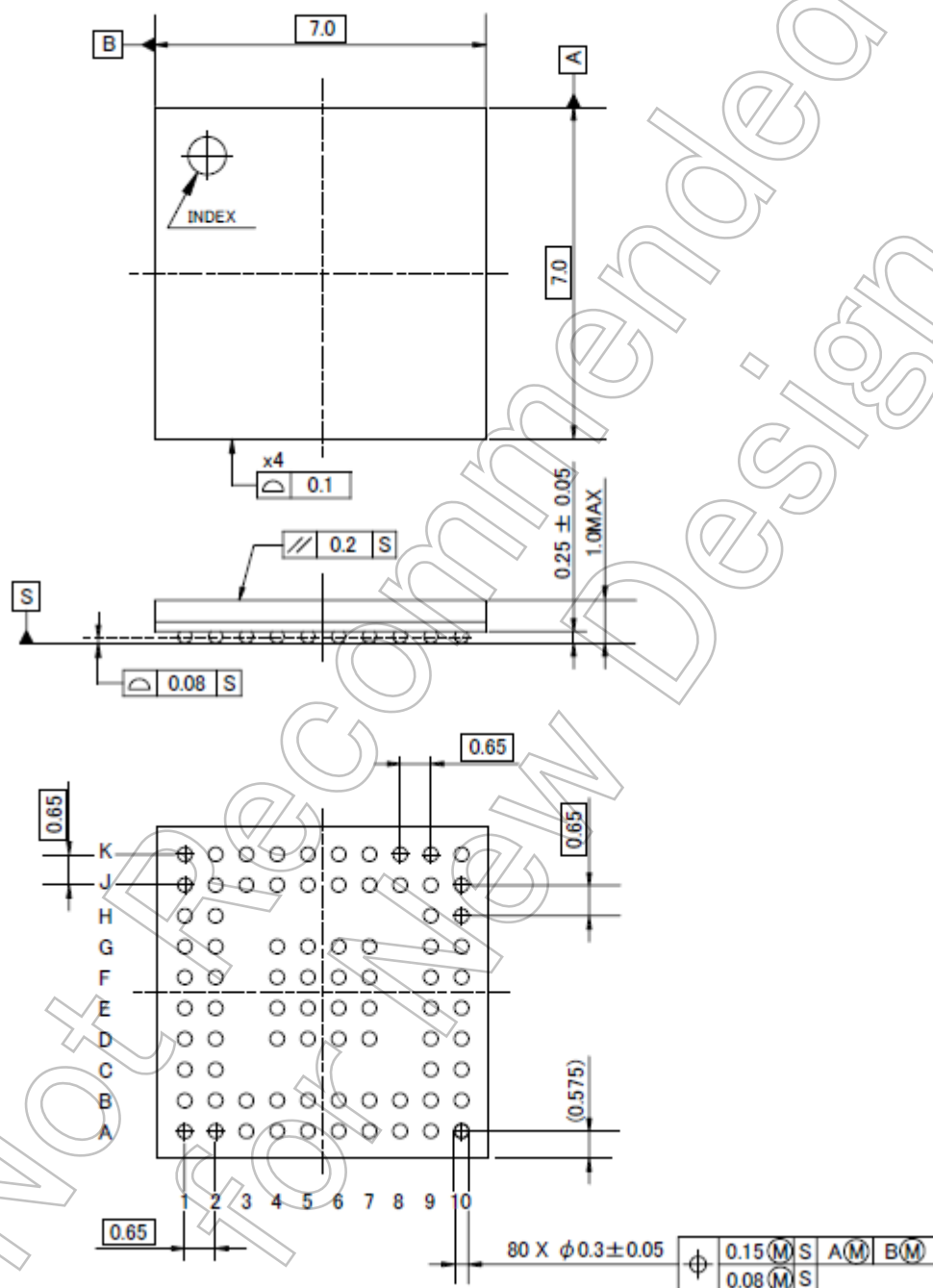
Figure 3.1 TC358749XBG 80-Pin Layout Package (Top View)

4. Package

4.1. TC358749XBG Package (80-pin, P-VFBGA80-0707-0.65-001)

P-VFBGA80-0707-0.65-001

"Unit:mm"



Weight: 77 mg (Typ.)

Table 4-1 Mechanical Dimension for TC358749XBG

Dimension	Min	Typ.	Max
Solder ball pitch	-	0.65 mm	-
Package dimension	-	7.0 x 7.0 mm ²	-
Package height	-	-	1.0 mm

5. Electrical Characteristics

5.1. Absolute Maximum Ratings

VSS= 0V reference

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V - Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V - Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V - MIPI CSI-2 PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (3.3V - HDMIRX Phy)	AVDD33	-0.3 to +3.9	V
Supply voltage (1.2V - HDMIRX Phy)	AVDD12	-0.3 to +1.8	V
Input voltage (CSI-2 IO)	VIN_CSI-2	-0.3 to VDD_MIPI+0.3	V
Output voltage (CSI-2 IO)	VOUT_CSI-2	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	VIN_IO	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	VOUT_IO	-0.3 to VDDIO+0.3	V
Junction temperature	Tj	125	°C
Storage temperature	Tstg	-40 to +125	°C

5.2. Operating Condition

VSS= 0V reference

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8/3.3V - Digital IO)	VDDIO2	1.65	1.8	3.6	V
Supply voltage (3.3V - HDMI Digital IO)	VDDIO1	3.0	3.3	3.6	V
Supply voltage (1.2V - Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (3.3V - HDMIRX PHY)	AVDD33	3.135	3.3	3.465	V
Supply voltage (1.2V - HDMIRX PHY)	AVDD12	1.15	1.2	1.25	V
Supply voltage (1.2V - MIPI CSI-2 PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating temperature (ambient temperature with voltage applied)	Ta	-30	+25	+70	°C
Supply Noise Voltage	V _{SN}	-	-	100	mV _{pp}

6. Revision History

Table 6-1 Revision History

Revision	Date	Description
0.8321	2015-12-18	Newly released
0.8322	2016-02-04	• Delete TC358747XBG's descriptions • Typo Init(O) DAOUT pin in External Pins
0.85	2016-09-13	Added comment to De-Interlace function.
0.87	2016-11-02	Deleted comment in part of Features.
1.0	2017-10-10	Added comment to HDCP. Changed header, footer and the last page. Changed corporate name.
1.1	2017-11-13	Modified values in Table 2-1.

Not Recommended
for New Design

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