TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62D612FTG

24-Channel Constant-Current LED Driver of the 3.3-V and 5-V Power Supply Voltage Operation

The TB62D612FTG is a constant-current driver designed for LED and LED display lighting.

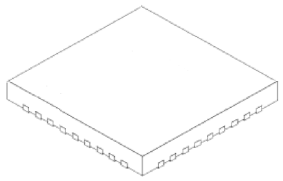
The TB62D612FTG incorporates twenty-four channels of seven-bit PWM dimming controllers and constant-current drivers. Twenty-four constant-current drivers are divided into three blocks, each consisting of three drivers, and the output current of each can be independently adjusted by the relevant external resistor.

The TB62D612FTG is controlled using the SDA and SCLK input signals, and capable of high-speed data transfers.

The TB62D612FTG can be set address with ID terminal. (Up to 64 address)

High-speed processing is capable by applying Bi-CMOS process.

The TB62D612FTG operates with a supply voltage of 3.3 V or 5 V.



P-WQFN36-0606-0.50-001

Weight: 0.083 g (typ.)

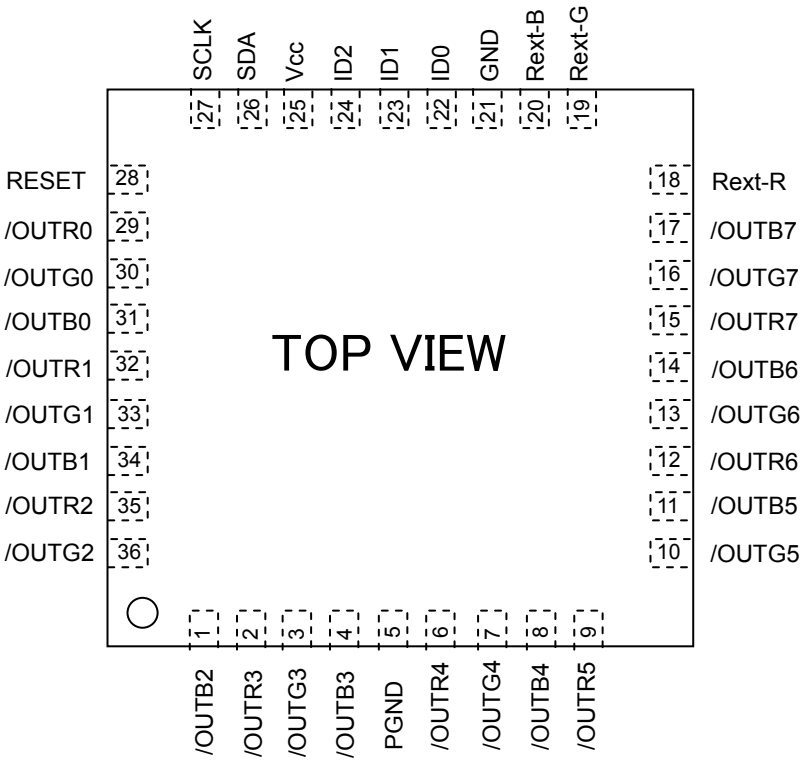
1. Features

- Power supply voltages: V_{CC} = 3.3 V/5 V
- Output drive capability and output count: 80 mA (max)× 24 channels
- Constant-current output range: 5 to 40 mA
- Voltage applied to constant-current output terminals: 0.4 V(min) (I_{OUT} = 5 to 40 mA)
- Designed for common-anode LEDs
- The input interface is controlled by the SDA and SCLK signal lines
- Thermal shutdown (TSD)
- Logical Input signal voltage level: 3.3-V and 5-V CMOS interfaces (Schmitt trigger input)
- Maximum output voltage: 28 V
- Incorporating PWM control circuitry: Provides seven-bit PWM control.
- Driver identification: Up to 64 drivers can be controlled individually.
- Operating temperature range: T_{opr} = −40 to 85 °C
- Package: P-WQFN36-0606-0.50-001

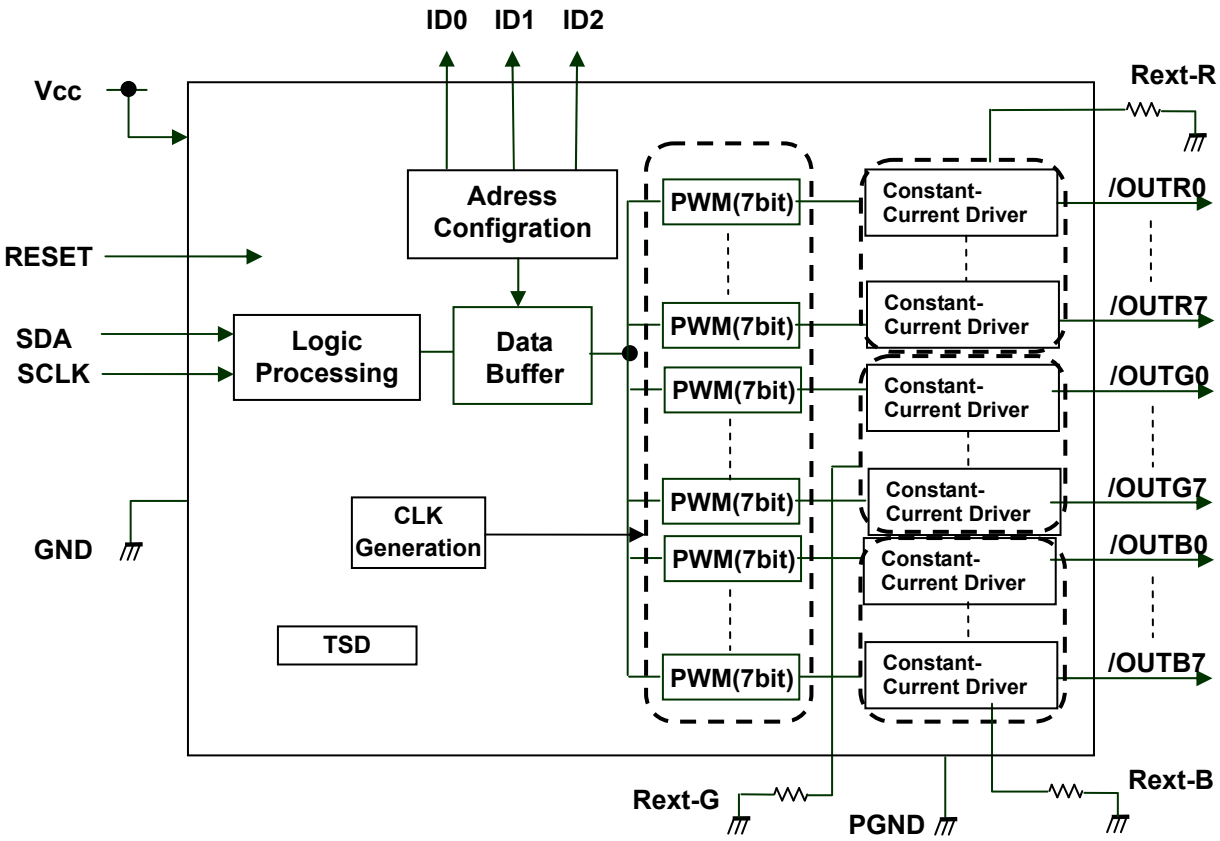
- Constant-current accuracy

Output Voltage	Current Accuracy Between Channels	Current Accuracy Between ICs	Output Current
0.4 V	±3.0%	±6.0%	15 mA

2. Pin Assignment (top view)



3. Block Diagram



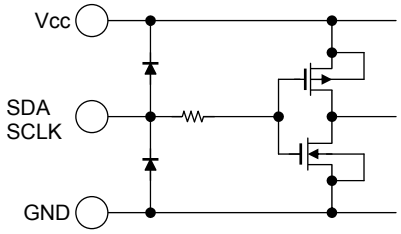
4. Terminal Description

Pin No	Symbol	Function
1	/OUTB2	Constant-current output terminal (Open-collector type)
2	/OUTR3	Constant-current output terminal (Open-collector type)
3	/OUTG3	Constant-current output terminal (Open-collector type)
4	/OUTB3	Constant-current output terminal (Open-collector type)
5	PGND	Power Ground pin
6	/OUTR4	Constant-current output terminal (Open-collector type)
7	/OUTG4	Constant-current output terminal (Open-collector type)
8	/OUTB4	Constant-current output terminal (Open-collector type)
9	/OUTR5	Constant-current output terminal (Open-collector type)
10	/OUTG5	Constant-current output terminal (Open-collector type)
11	/OUTB5	Constant-current output terminal (Open-collector type)
12	/OUTR6	Constant-current output terminal (Open-collector type)
13	/OUTG6	Constant-current output terminal (Open-collector type)
14	/OUTB6	Constant-current output terminal (Open-collector type)
15	/OUTR7	Constant-current output terminal (Open-collector type)
16	/OUTG7	Constant-current output terminal (Open-collector type)
17	/OUTB7	Constant-current output terminal (Open-collector type)
18	Rext-R	External resistor pin for output current configuration (/OUTR0 to /OUTR7)
19	Rext-G	External resistor pin for output current configuration (/OUTG0 to /OUTG7)
20	Rext-B	External resistor pin for output current configuration (/OUTB0 to /OUTB7)
21	GND	Ground pin
22	ID0	ID configuration pin (Note 1)
23	ID1	ID configuration pin (Note 1)
24	ID2	ID configuration pin (Note 1)
25	Vcc	Power supply terminal
26	SDA	Serial data input terminal
27	SCLK	Serial clock input terminal
28	RESET	Reset signal input. (Setting this pin High resets internal data.) (Note 1)
29	/OUTR0	Constant-current output terminal (Open-collector type)
30	/OUTG0	Constant-current output terminal (Open-collector type)
31	/OUTB0	Constant-current output terminal (Open-collector type)
32	/OUTR1	Constant-current output terminal (Open-collector type)
33	/OUTG1	Constant-current output terminal (Open-collector type)
34	/OUTB1	Constant-current output terminal (Open-collector type)
35	/OUTR2	Constant-current output terminal (Open-collector type)
36	/OUTG2	Constant-current output terminal (Open-collector type)

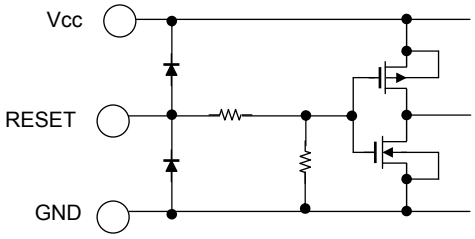
Note 1: After the reset is released, it should be ensured that IDs (slave addresses) are properly configured.

5. Equivalent Circuits for Inputs and Outputs

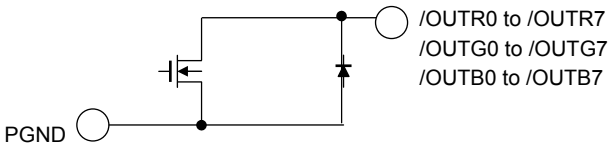
SDA and SCLK Terminals



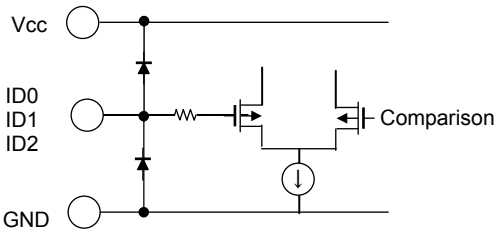
RESET Terminals



Constant-Current Output Terminals



ID0, ID1, and ID2 Terminals



6. Programming the TB62D612FTG

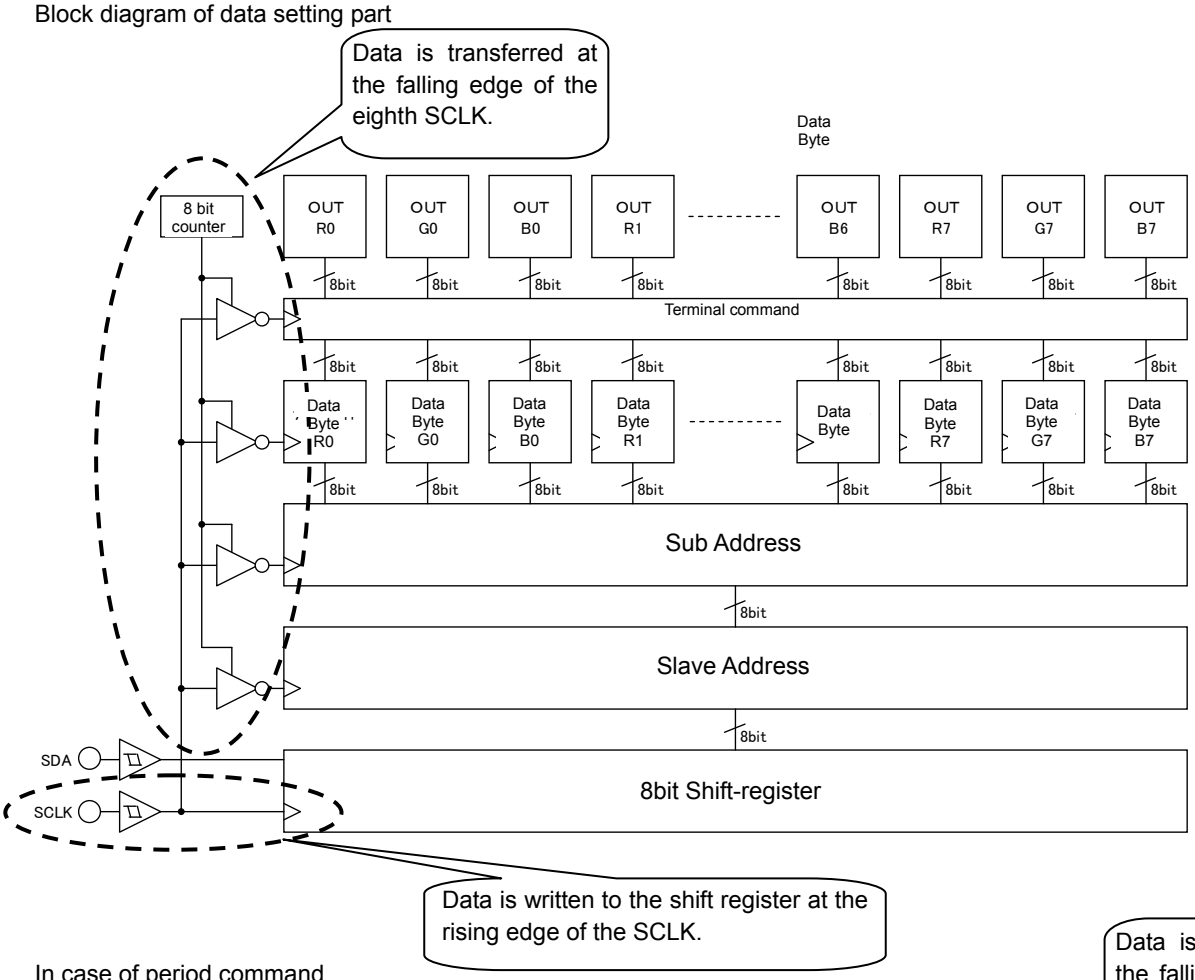
The TB62D612FTG can be programmed by the SDA and SCLK signals.
The TB62D612FTG should be programmed using one of the following formats: (1) Serial Packet Format in Normal Programming Mode or (3) Serial Packet Format in Special Mode.

(1) Serial Packet Format in Normal programming Mode
【Typical】

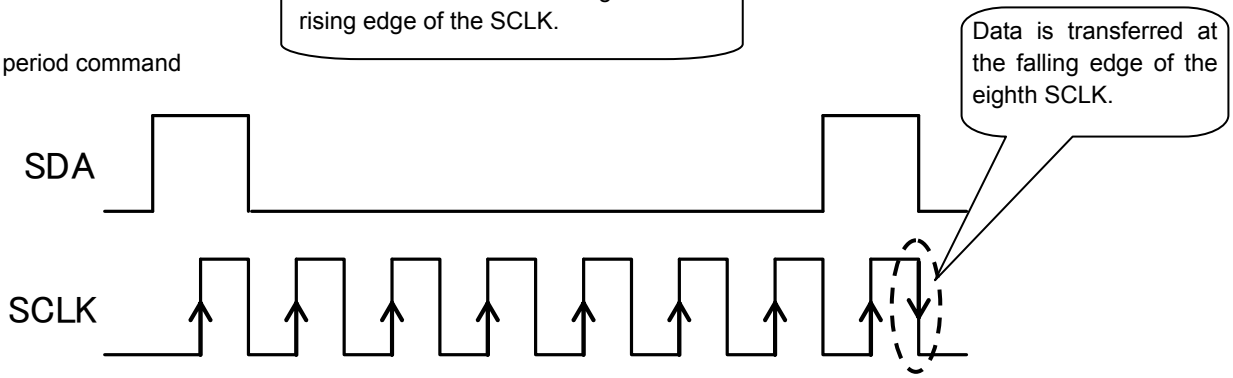
Start Command [11111111]	Slave address 8 bits	Sub-address (Channel select) 8 bits	Data byte (PWM configuration) 8 bits	Period Command [10000001]

・Normal programming Mode should be set as the following flow.
"Start Command" → "Slave address" → "Sub-address" → "Data byte" → "Period Command"
As for example of data input, refer to Page8.
・Input data from SDA signal is written to the shift register at the rising edge of SCLK every 8 bit.
This data is transferred at the falling edge of the eighth CLK. So, at the eighth CLK, data should be inputted to the falling edge.

Block diagram of data setting part



In case of period command



(2) Data Settings

a) Slave Addresses

Input voltages and logic states of the ID0, ID1 and ID2 pins are determined as follows.

(High order bit = 0. Low order bit = 0 (Except of all selection))

Vcc =”11”, 2/3Vcc =”10”, 1/3Vcc = "01”, GND =”00”

Slave Addresses	ID2	ID1	ID0
00000000	GND	GND	GND
00000010	GND	GND	1/3Vcc
00000100	GND	GND	2/3Vcc
00000110	GND	GND	Vcc
00001000	GND	1/3Vcc	GND
00001010	GND	1/3Vcc	1/3Vcc
00001100	GND	1/3Vcc	2/3Vcc
00001110	GND	1/3Vcc	Vcc
00010000	GND	2/3Vcc	GND
00010010	GND	2/3Vcc	1/3Vcc
00010100	GND	2/3Vcc	2/3Vcc
00010110	GND	2/3Vcc	Vcc
00011000	GND	Vcc	GND
00011010	GND	Vcc	1/3Vcc
00011100	GND	Vcc	2/3Vcc
00011110	GND	Vcc	Vcc
00100000	1/3Vcc	GND	GND
00100010	1/3Vcc	GND	1/3Vcc
00100100	1/3Vcc	GND	2/3Vcc
00100110	1/3Vcc	GND	Vcc
00101000	1/3Vcc	1/3Vcc	GND
00101010	1/3Vcc	1/3Vcc	1/3Vcc
00101100	1/3Vcc	1/3Vcc	2/3Vcc
00101110	1/3Vcc	1/3Vcc	Vcc
00110000	1/3Vcc	2/3Vcc	GND
00110010	1/3Vcc	2/3Vcc	1/3Vcc
00110100	1/3Vcc	2/3Vcc	2/3Vcc
00110110	1/3Vcc	2/3Vcc	Vcc
00111000	1/3Vcc	Vcc	GND
00111010	1/3Vcc	Vcc	1/3Vcc
00111100	1/3Vcc	Vcc	2/3Vcc
00111110	1/3Vcc	Vcc	Vcc
01000000	2/3Vcc	GND	GND
01000010	2/3Vcc	GND	1/3Vcc
01000100	2/3Vcc	GND	2/3Vcc
01000110	2/3Vcc	GND	Vcc
01001000	2/3Vcc	1/3Vcc	GND
01001010	2/3Vcc	1/3Vcc	1/3Vcc
01001100	2/3Vcc	1/3Vcc	2/3Vcc
01001110	2/3Vcc	1/3Vcc	Vcc
01010000	2/3Vcc	2/3Vcc	GND
01010010	2/3Vcc	2/3Vcc	1/3Vcc
01010100	2/3Vcc	2/3Vcc	2/3Vcc
01010110	2/3Vcc	2/3Vcc	Vcc
01011000	2/3Vcc	Vcc	GND
01011010	2/3Vcc	Vcc	1/3Vcc
01011100	2/3Vcc	Vcc	2/3Vcc
01011110	2/3Vcc	Vcc	Vcc
01100000	Vcc	GND	GND
01100010	Vcc	GND	1/3Vcc
01100100	Vcc	GND	2/3Vcc

01100110	Vcc	GND	Vcc
01101000	Vcc	1/3Vcc	GND
01101010	Vcc	1/3Vcc	1/3Vcc
01101100	Vcc	1/3Vcc	2/3Vcc
01101110	Vcc	1/3Vcc	Vcc
01110000	Vcc	2/3Vcc	GND
01110010	Vcc	2/3Vcc	1/3Vcc
01110100	Vcc	2/3Vcc	2/3Vcc
01110110	Vcc	2/3Vcc	Vcc
01111000	Vcc	Vcc	GND
01111010	Vcc	Vcc	1/3Vcc
01111100	Vcc	Vcc	2/3Vcc
01111110	Vcc	Vcc	Vcc
0XXXXXX1	All Select		

b) Sub-Addresses

Output channel set / All channels set / Special mode set

In output channel set, a channel which defines PWM configuration is selected. In all channels set, PWM is configured for all channels. Special mode sets this mode according to the description in page 8.

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	Ch set
0	0	0	0	0	0	1	0	/OUTR0
0	0	0	0	0	1	0	0	/OUTG0
0	0	0	0	0	1	1	0	/OUTB0
0	0	0	0	1	0	0	0	/OUTR1
0	0	0	0	1	0	1	0	/OUTG1
0	0	0	0	1	1	0	0	/OUTB1
0	0	0	0	1	1	1	0	/OUTR2
0	0	0	1	0	0	0	0	/OUTG2
0	0	0	1	0	0	1	0	/OUTB2
0	0	0	1	0	1	0	0	/OUTR3
0	0	0	1	0	1	1	0	/OUTG3
0	0	0	1	1	0	0	0	/OUTB3
0	0	0	1	1	0	1	0	/OUTR4
0	0	0	1	1	1	0	0	/OUTG4
0	0	0	1	1	1	1	0	/OUTB4
0	0	1	0	0	0	0	0	/OUTR5
0	0	1	0	0	0	1	0	/OUTG5
0	0	1	0	0	1	0	0	/OUTB5
0	0	1	0	0	1	1	0	/OUTR6
0	0	1	0	1	0	0	0	/OUTG6
0	0	1	0	1	0	1	0	/OUTB6
0	0	1	0	1	1	0	0	/OUTR7
0	0	1	0	1	1	1	0	/OUTG7
0	0	1	1	0	0	0	0	/OUTB7
0	1	0	0	0	0	0	0	All channel select
0	1	1	0	0	0	0	0	Special mode

(Bits of high order and low order must be zero.)

c) Data Bytes (PWM configuration)

Data bytes set PWM diming. (Low order bit must be zero.)

7bit	6bit	5bit	4bit	3bit	2bit	1bit	0bit	PWM Dimming (for reference only)
0	0	0	0	0	0	0	0	OFF(Default)
0	0	0	0	0	0	1	0	1/127
0	0	0	0	0	1	0	0	2/127
								・・・
1	1	1	1	1	1	0	0	126/127
1	1	1	1	1	1	1	0	127/127

Note: Any data other than those specified above must not be programmed.

(3) Serial Packet Format in Special Mode

When data of 01100000 is input to the sub address, the operation moves to the special mode where all channels are selected in order. Data of 24 channels should be input.
(If data of more than 24 channels are provided, the 25th and subsequent data are treated as invalid. If data of less than 24 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.)
To return to the normal mode, input data from the start command (ALL"H"8bit). In case of using this mode configuration, volume of data can be omitted.

Start Condition [11111111]	Slave Addresses	Sub-address (Special mode set) [01100000]	Data OUTR0	Data OUTG0	Data OUTB0	Data OUTR1	-----	Data OUTB6	Data OUTR7	Data OUTG7	Data OUTB7	Period Command [10000001]

(4) Input example of data set

a) In case 127 PWM clocks/127(100% ON) are configured to all channels of slave address 00h.

Start command (11111111)	Slave address (00000000)	Sub address(R0) (00000010)	Data bytes (11111110)	Sub address(G0) (00000100)	Data bytes (11111110)	Sub address(B0) (00000110)	Data bytes (11111110)

Sub address(R1) (00001000)	Data bytes (11111110)	Sub address(G1) (00001010)	Data bytes (11111110)	Sub address(B1) (00001100)	Data bytes (11111110)	----------	Sub address(R7) (00101100)	Data bytes (11111110)

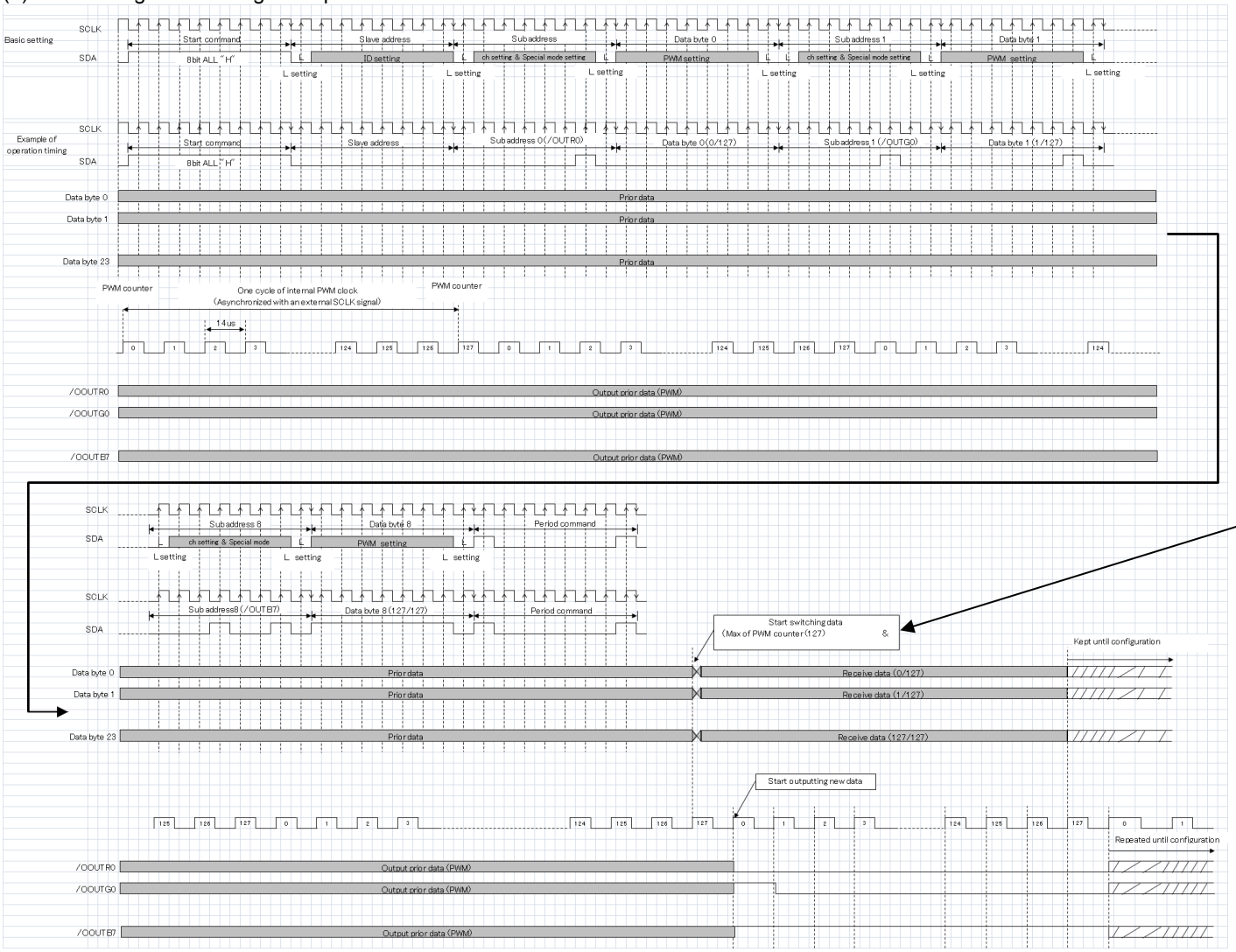
Sub address(G7) (00101110)	Data bytes (11111110)	Sub address(B7) (00110000)	Data bytes (11111110)	Period command (10000001)

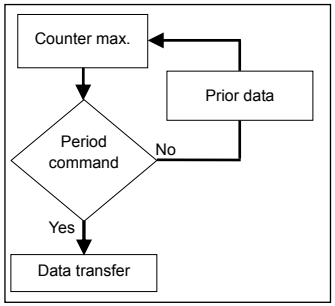
b) In case 127 PWM clocks/127(100% ON) are configured to only /OUTR0 pin and /OUTB7 pin of slave address 02h.

Start command (11111111)	Slave Addresses (00000010)	Sub-address (R0) (00000010)	Data bytes (11111110)	Sub-address (B7) (00110000)	Data bytes (11111110)	Period Command (10000001)

As for other than /OUTR0 and /OUTB7 terminals in above configuration, output pins which have already outputted data continue to output prior data. (In case of changing only outputting data which is required to be changed, this configuration is valid.)

(5) Data settings and Timing of outputs

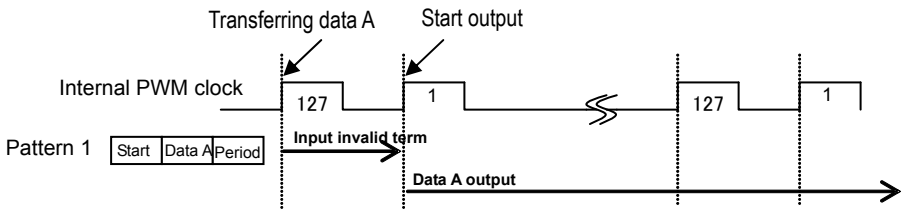




Note) Data is transferred by synchronizing period command (10000001) with the internal PWM counter (MAX). So, if data is inputted after the period command is inputted and before the internal PWM counter counts its maximum, data which is inputted after period input is not accepted. In order to set data to the same ID (IC), next data should be inputted after 3 ms which corresponds to 128 internal PWM clocks is passed since the period command is inputted. However, in order to set data to the different ID, terminal of 3 ms which corresponds to 128 internal PWM clocks should not be taken. Data is written to the shift register at the rising edge of SCLK every 8 bits, and is transferred at the falling edge of eighth CLK. So, data should be inputted to the falling edge at the eighth CLK.

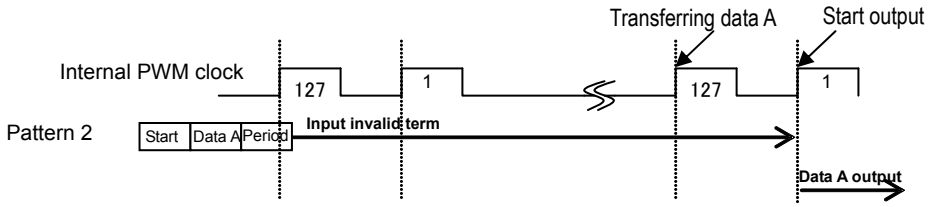
(6) Example of data input to the same ID

a) In case data A is inputted up to the rising edge of 127 internal PWM clocks.



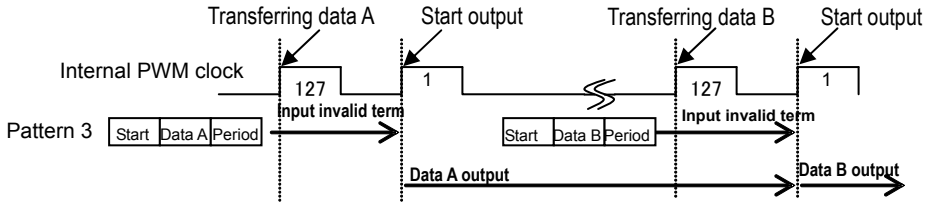
Outputting data A starts at the rising edge of one internal PWM clock.
Inputting is invalid from the rising edge of 127 internal PWM clocks to the rising edge of one internal PWM clock which is just after these 127 PWM clocks.

b) In case data A is inputted after the rising edge of 127 internal PWM clocks.



Outputting data A does not start at the rising edge of one internal PWM clock just after the data A is inputted. It starts at the next rising edge of one internal PWM clock.
Inputting is invalid from the data A (period) input to the rising edge of after the next one internal PWM clock.

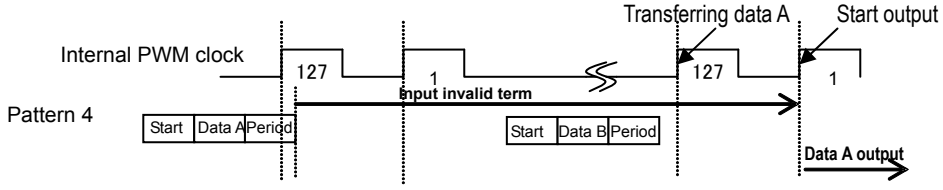
c) In case data B is inputted after data of pattern 1 starts outputting.



Outputting data A starts at the rising edge of one internal PWM clock just after the data A is inputted. Outputting data B starts at the rising edge of one internal PWM clock which is just after the data B input.
Inputting is invalid in the following term.
From the rising edge of 127 internal PWM clocks which are just after the data A is inputted to the rising edge of one internal PWM clock which is just after these 127 clocks.
From the rising edge of 127 internal PWM clocks which is just after the data B input to the rising edge of one internal PWM clock which is just after these 127 clocks.

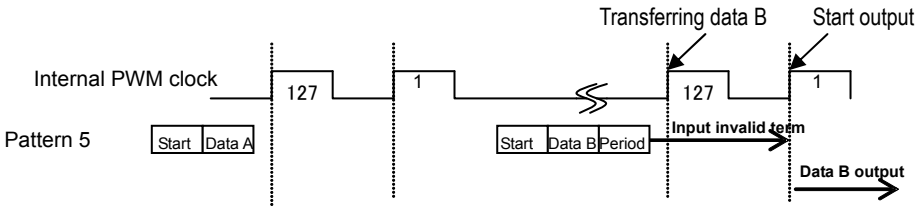
Pay attention that the IC does not operate according to the configuration while the following patterns (patterns 4 and 5) are inputted.

d) In case data B is inputted by the time the output of pattern 2 starts.



Inputting is invalid from the data A (period) input to the rising edge of the second internal clock. So, data B is invalid and data A is outputted.

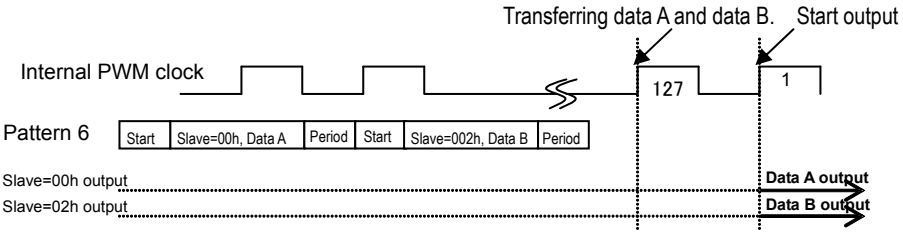
e) In case the period command mistakes.



Outputting data A does not start at the rising edge of one internal clock which is just after the data A input. Outputting data B starts at the rising edge of one internal PWM clock which is just after the data B input.

(7) Example of data input to the different ID.

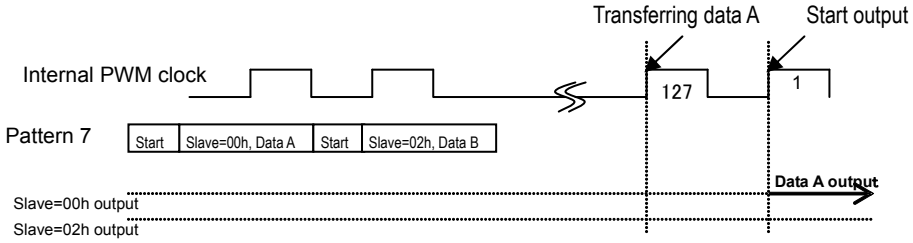
a) In case the data B is inputted to slave (= 02h) just after the data A is inputted to slave (= 00h).



Both data A and data B are outputted at the rising edge of one internal PWM clock which is just after the data A and the data B inputs.

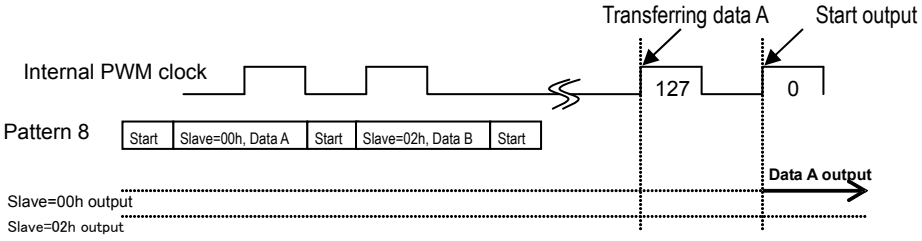
Pay attention that the IC does not operate according to the configuration while following patterns (patterns 7 and 8) are inputted.

b) In case period command after inputting data A to the slave (=00h) is missed or omitted or in case period command after inputting data B to the slave (=02h) is missed or omitted.



Data A is outputted. Data B is not outputted.

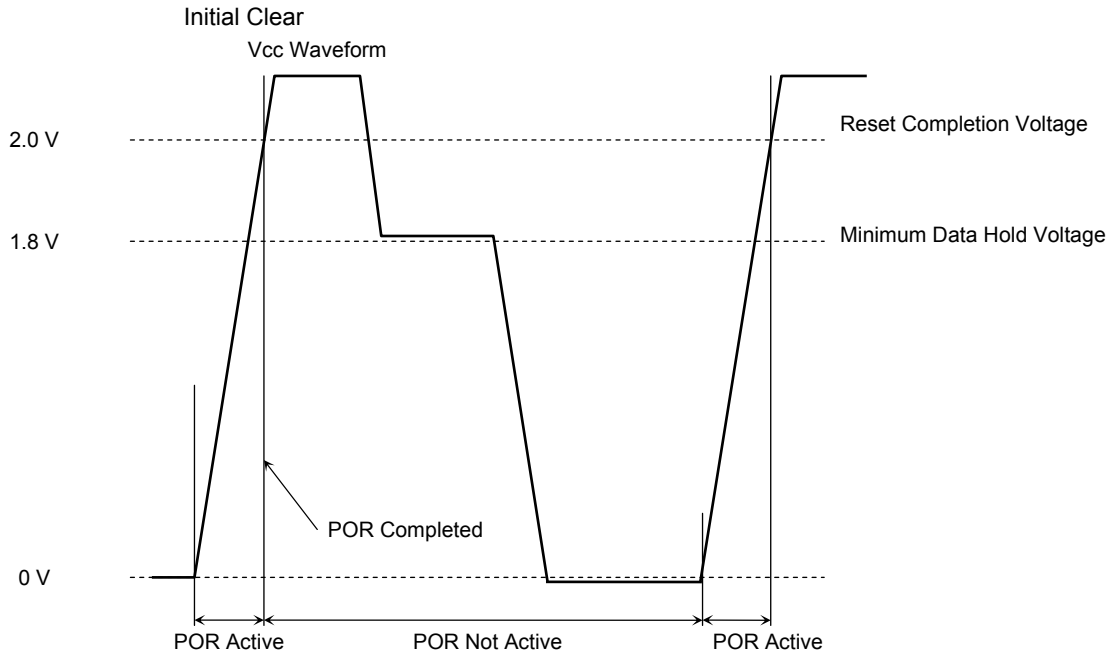
c) In case start command is inputted after data B of pattern 7 is inputted.



Data A is outputted. Data B is not outputted.

7. Power-ON Reset (POR)

The POR circuitry resets all the internal data to the default values upon powering up the TB62D612FTG in order to ensure proper device operation.
The POR circuitry is only activated when Vcc rises from 0 V. To reactivate POR, Vcc must be powered down to 0 V. The internal data hold voltage is guaranteed after Vcc has once reached or exceeded 3.0 V.



8. Thermal Shutdown (TSD)

When the die temperature reaches 150 °C , the thermal shutdown circuit is tripped, switching the constant-current outputs to off. The constant-current outputs are automatically turned on when the temperature cools past the shutdown threshold.

TSD trip temperature: 150 °C to 180 °C
TSD recovery temperature: 30 °C below the TSD trip temperature

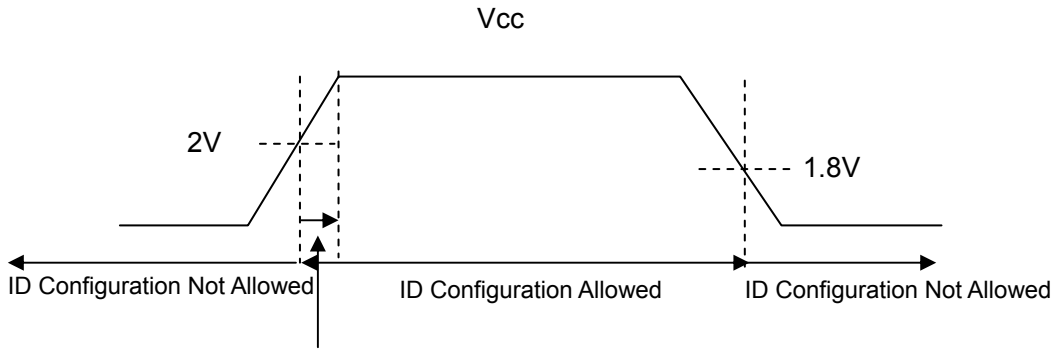
*Please avoid positively using TSD because TSD is a detecting function of the product.

9. Points to Note when Setting Up the TB62D612FTG

1. External resistors for specifying the LED driving current (Rext-R, Rext-G, Rext-B)
   External resistors should be separately connected to the Rext-R, Rext-G and Rext-B pins. Three resistors must not be collectively connected to a single pin. If they are connected to a single pin, current error is generated in each RBG.

2. External resistors for ID configuration
   The total resistance value of three external resistors used for specifying a device ID (which are connected between Vcc and GND) should be about 30 kΩ or lower.

3. ID configuration sequence
   ID configuration can be performed after POR is released upon powering on. However, to avoid false operation of the ID configuration, transient input signals of less than two clock cycles of the reference clock for the internal oscillator are not accepted.



Care should be taken during the period between the POR released timing and the timing when power supply has reached the rated Vcc voltage.

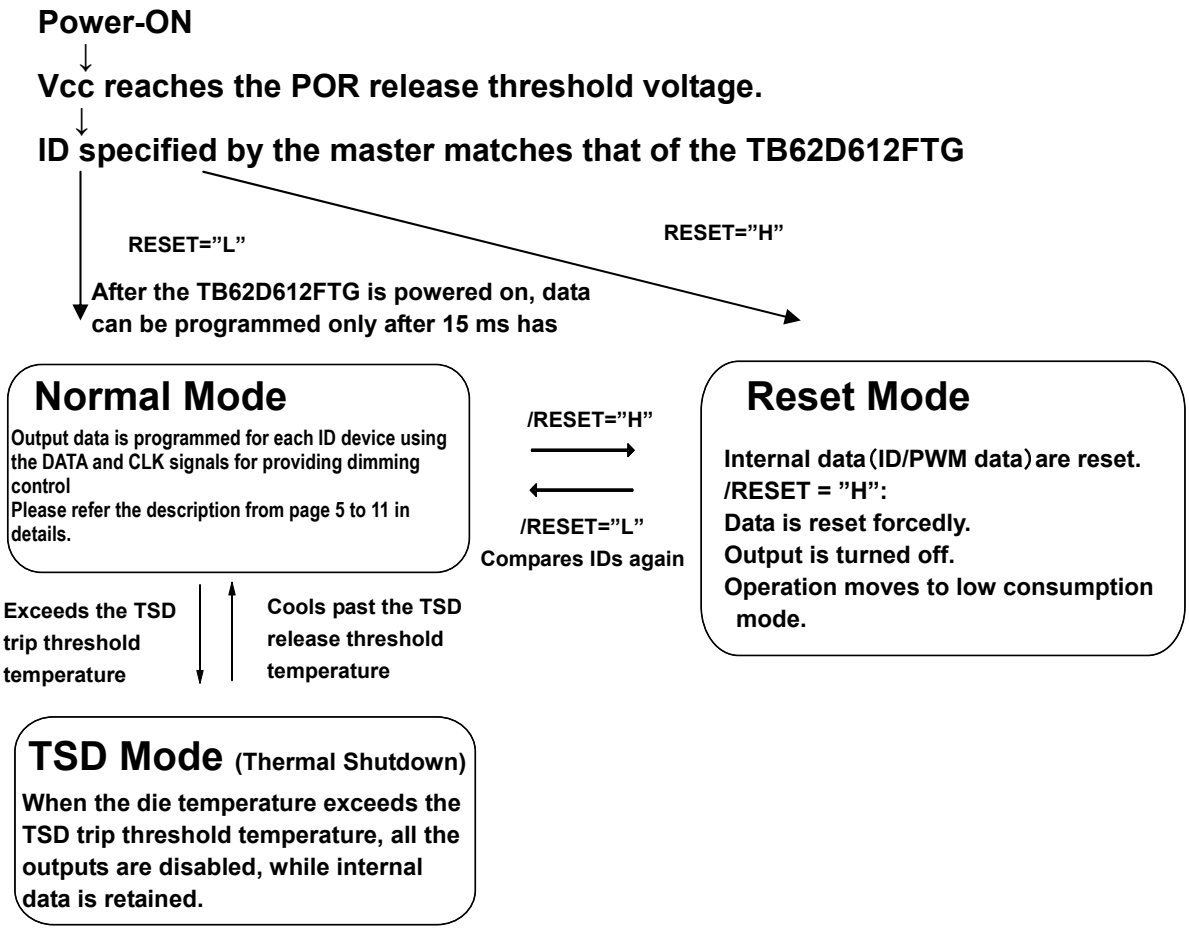
4. ID configuration
   Make sure to set IDs after releasing reset condition.

5. Data configuration
   Do not input the data which is not on the list of the data configuration table in page 6 and 7.
   Data is written to the shift resister at the rising edge of SCLK every 8 bits. And data is transferred at the falling edge of the eighth clock. So, input data to the falling edge at the eighth clock.

6. Special mode
   Data which corresponds to 24 channels should be inputted. If data of more than 24 channels are provided, the 25th and subsequent data are treated as invalid. If data of less than 24 channels are provided, those data are written to the channels in order and the remaining channels retain the previous data.

7. Timing of data configuration
   In order to set data to the same slave address, next data should be inputted after 3 ms which corresponds to 127 internal PWM clocks is passed since the period command is inputted. However, in order to set data to the different slave address, terminal of 3 ms which corresponds to 127 internal PWM clocks should not be taken.

10. State Transition Diagram



11. Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	6.0	V
Input voltage	V_{IN}	-0.3 to Vcc + 0.3 (Note 1)	V
Output current	I_{OUT}	85	mA/ch
Output voltage	V_{OUT}	-0.3 to 29	V
Power dissipation	P_d	4.3 (Notes 2 and 3)	W
Thermal resistance	$R_{th\ (j\text{-}a)}$	29 (Note 2)	°C /W
Operating temperature range	T_{opr}	-40 to 85	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Maximum junction temperature	T_j	150	°C

Note 1: However, do not exceed 6.0 V.

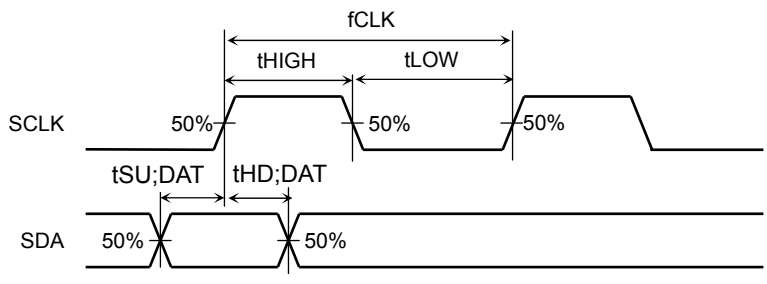
Note 2: When mounted on a PCB (76.2 × 114.3 × 1.6 mm; Cu = 30%; 35-μm-thick; SEMI-compliant)

Note 3: Power dissipation is reduced by $1/R_{th\ (j\text{-}a)}$ for each °C above 25°C ambient.

12. Operating Ranges (Ta = 40°C to 85°C, unless otherwise specified)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	—	3	—	5.5	V
Output voltage	$V_{OUT\ (ON)}$	All Output	0.4	—	4	V
Output current	I_{OUT}	All Output	5	—	40	mA/ch
Input voltage	V_{IH}	SDA, SCLK, RESET	0.7 × Vcc	—	Vcc	V
	V_{IL}		GND	—	0.3 × Vcc	
	V_{ID0}	ID0, ID1, ID2	0	—	0.3	
	V_{ID1}		1/3Vcc -0.3	1/3 Vcc	1/3Vcc +0.3	
	V_{ID2}		2/3Vcc -0.3	2/3 Vcc	2/3Vcc +0.3	
	V_{ID3}		Vcc − 0.3	—	Vcc	
SCLK clock frequency	fCLK	SCLK (Note. 4)	—	—	10	MHz
Data setup time	tSU;DAT	SDA-SCLK (Note. 4)	10	—	—	ns
Data hold time	tHD;DAT	SCLK-SDA (Note. 4)	10	—	—	
“L” term of SCLK clock	tLOW	SCLK (Note. 4)	50	—	—	
“H” term of SCLK clock	tHIGH	SCLK (Note. 4)	50	—	—	

Note. 4: Please refer to below timing chart.



13. Electrical Characteristics (Ta = 25℃, VCC = 4.5 to 5.5 V, unless otherwise specified)

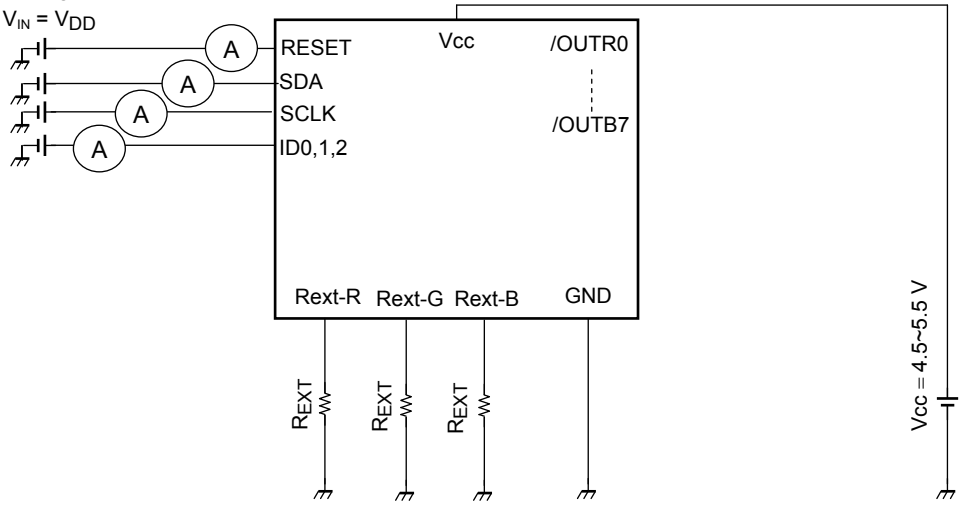
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output current	I_{OUT1}	4	V_{OUT} = 0.4 V, R-EXT = 1.2kΩ Vcc = 5 V,	12.69	13.5	14.31	mA
Output current accuracy between channels	ΔI_{OUT2}	4	V_{OUT} = 0.4 V, R-EXT =1.2kΩ All ch ON Vcc = 5 V,	—	—	±3.0	%
Output leakage current	I_{OZ}	4	V_{OUT} = 28 V	—	—	1	μA
Input current	I_{IH}	1	SDA, SCLK	—	—	1	μA
			RESET(Vcc=5V)	25	50	75	
	I_{IL}	2	SDA, SCLK, RESET	—	—	-1	
	I_{ID}	1,2	ID0, ID1, ID2	—	—	±0.1	
Changes in constant output current dependent on V_{CC}	%/Vcc	4	Vcc = 4.5 V to 5.5 V	—	1	2	%
Supply current	Icc_1	3	R-EXT=1.2 kΩ ,V_{OUT} =0.4 V, RESET=L	—	9	14	mA
	Icc_2	3	R-EXT = OPEN, V_{OUT} = 28.0 V	—	3	5	
Current consumption in Reset mode	$Icc_{(PS)}$	3	R-EXT = 1.2 kΩ , V_{OUT} = 0.4 V, RESET = H (The input current of the RESET pin is excluded.)	—	—	1	μA
Time required for a mode transition from Reset mode to Normal mode	tON2 (*1)	—	Time between a High to Low transition on RESET and the timing when an output current is generated after input data is applied.	—	—	3	ms

(*1): Internal data is reset forcedly by RESET command. In order to turn on the output current, data should be inputted again. Pay attention that the output current flows after PWM counter counts its maximum (128 PWM CLKs) though data is inputted again.

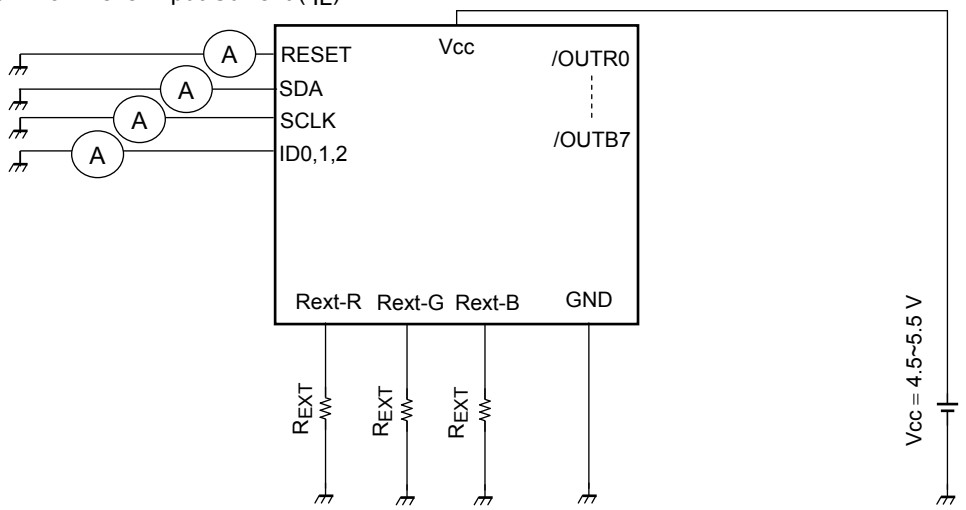
RESET recovery time: 3ms (MAX) ←In case the voltage is inputted until the PWM counter counts one cycle after RESET release. (After RESET release, PWM counter starts from zero.)

14. Test Circuits

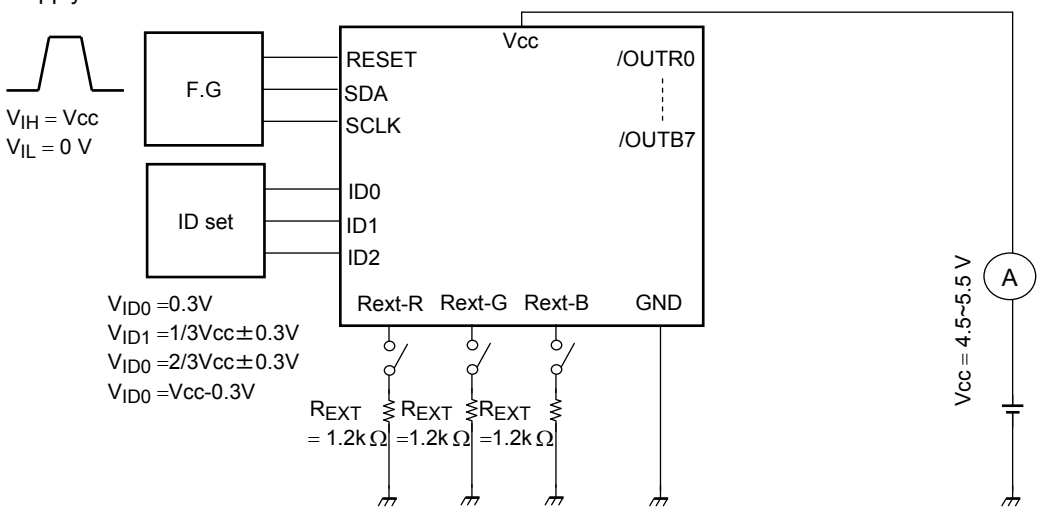
Test Circuit 1: High-Level Input Current (I_{IH})



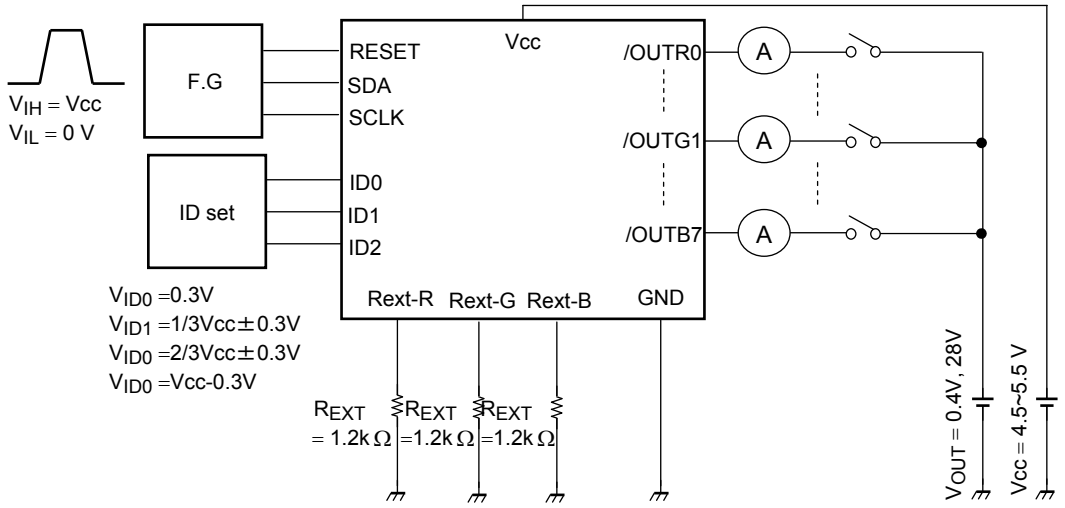
Test Circuit 2: Low-Level Input Current (I_{IL})



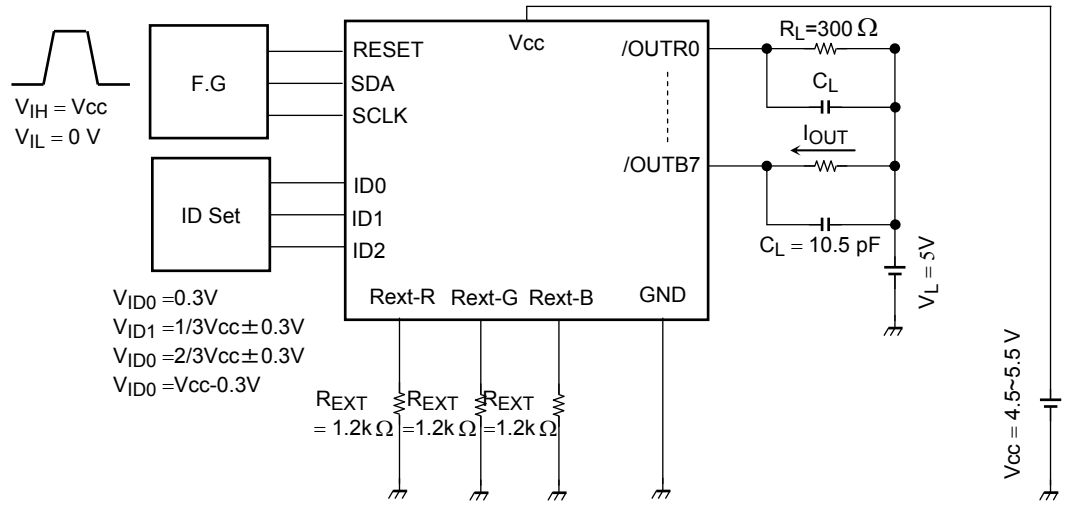
Test Circuit 3: Supply Current



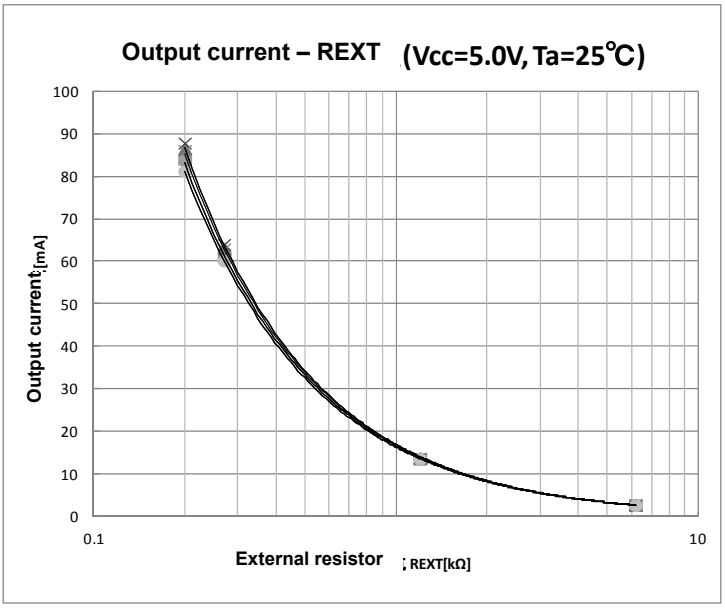
Test Circuit 4: Output Current, Output Leakage Current, Output current accuracy, Changes in constant output current dependent on V_{CC}



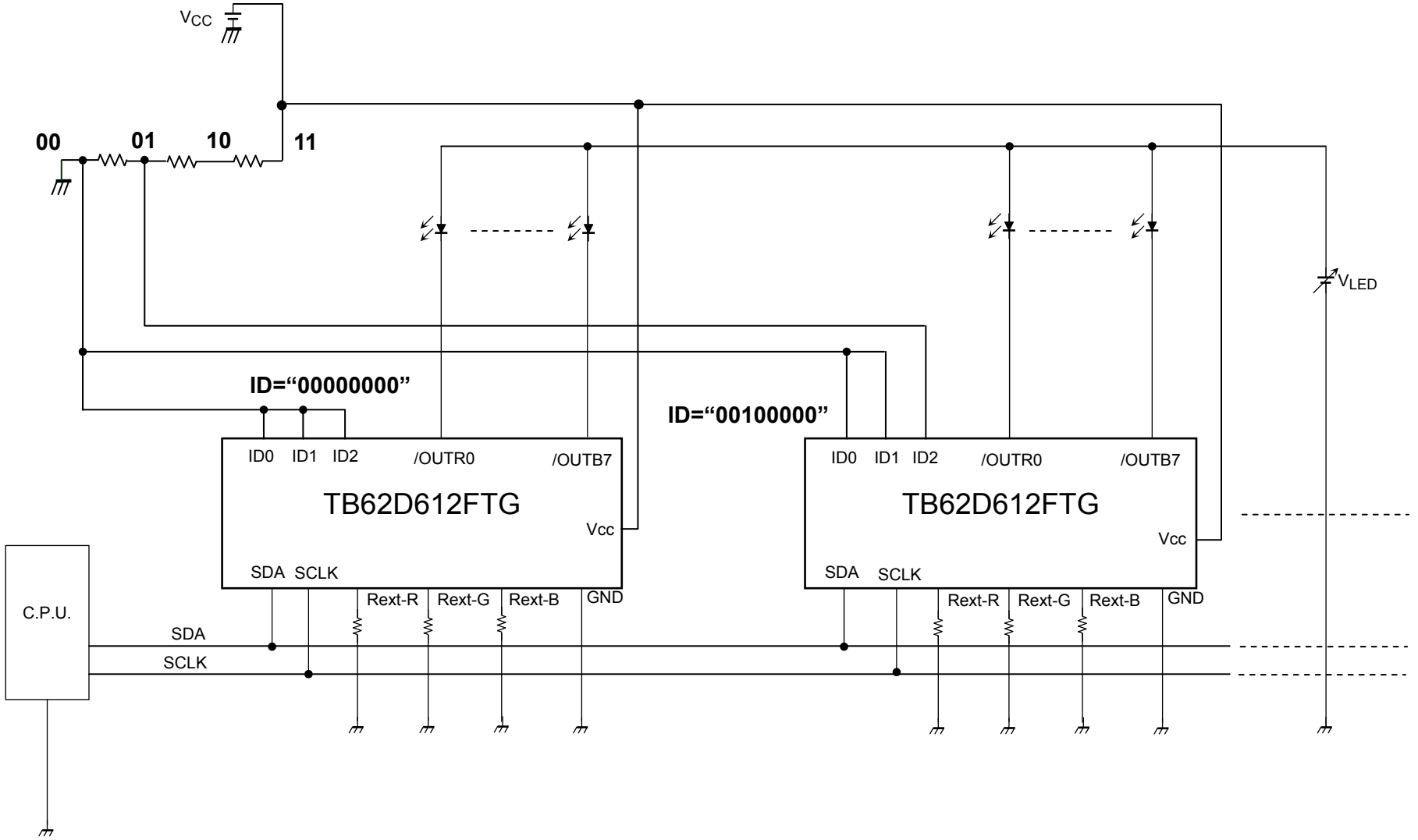
Test Circuit 5: Switching Characteristics



15. Characteristics of Output Current vs. External resistor (For reference)

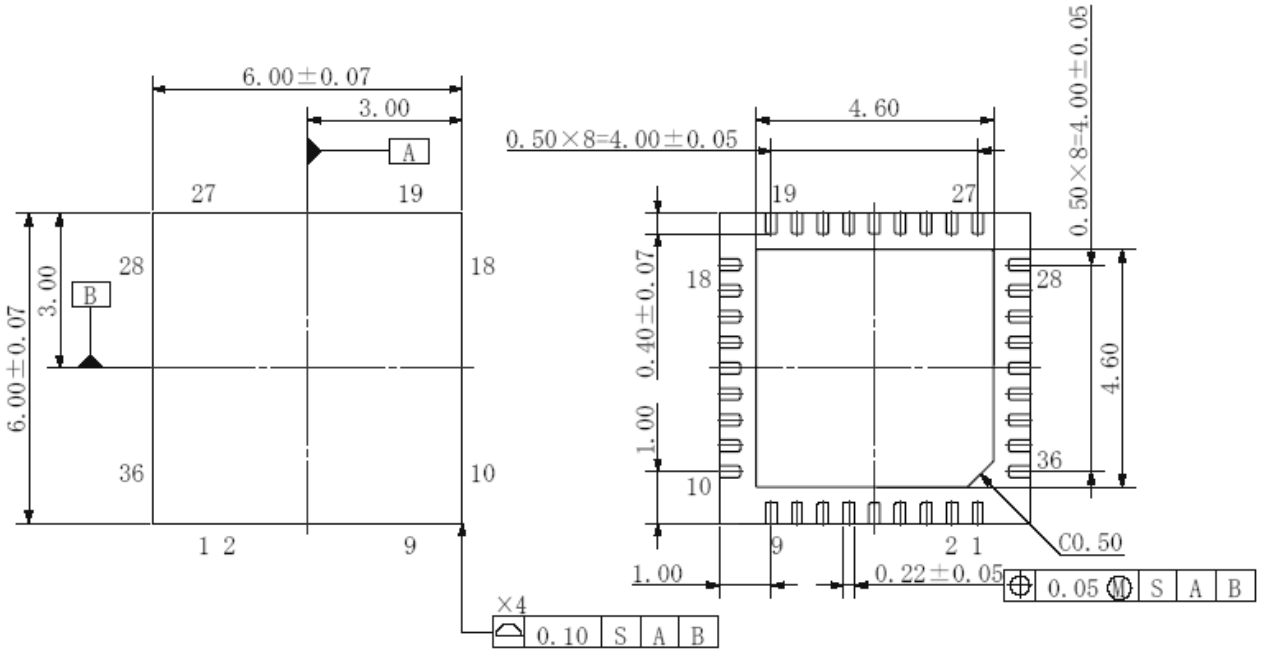


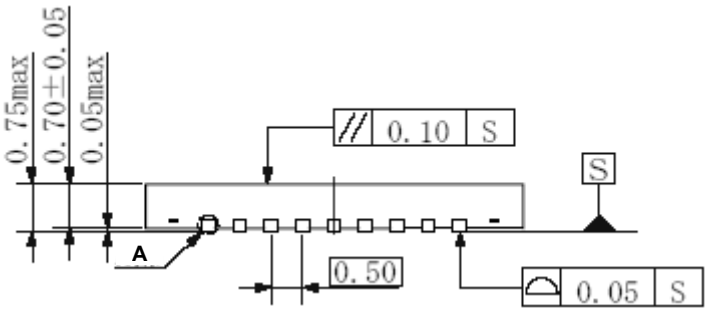
16. Application Circuit Example

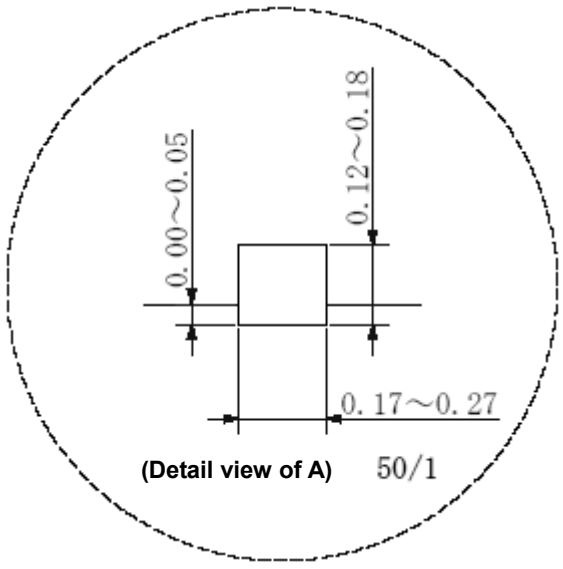


Package Dimensions

P-WQFN36-0606-0.50-001 **Unit: mm**







Weight: 0.083 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Examples

The application examples provided in this data sheet are provided for reference only. Thorough evaluation and testing should be implemented when designing your application's mass production design.
In providing these application examples, Toshiba does not grant the use of any industrial property rights.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause breakdown, damage or deterioration of the device, and may result in injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the event of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly, or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow. Such a breakdown can lead to smoke or ignition. To minimize effects of a large current flow in the event of breakdown, fuse capacity, fusing time, insertion circuit location, and other such suitable settings are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current caused by inrush current at power ON or the negative current caused by the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
For ICs with built-in protection functions, use a stable power supply. An unstable power supply may cause the protection function to not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices incorrectly or in the wrong orientation.
Make sure that the positive and negative terminals of power supplies are connected properly.
Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause breakdown, damage or deterioration of the device, which may result in injury by explosion or combustion.
In addition, do not use any device that has had current applied to it while inserted incorrectly or in the wrong orientation even once.

(5) Carefully select power amp, regulator, or other external components (such as inputs and negative feedback capacitors) and load components (such as speakers),.

If there is a large amount of leakage current such as input or negative feedback capacitors, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to remember on handling of ICs

(1) Heat Dissipation Design

In using an IC with large current flow such as a power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time or under any condition. These ICs generate heat even during normal use. An inadequate IC heat dissipation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat dissipation on peripheral components.

(2) Back-EMF

When a motor rotates in the reverse direction, stops, or slows down abruptly, a current flows back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in your system design.

(3) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

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