# 12W I²S Input Class-D Amplifier with Digital Audio Processor and DirectPath™ HP / Line Driver

**Check for Samples: TAS5729MD**

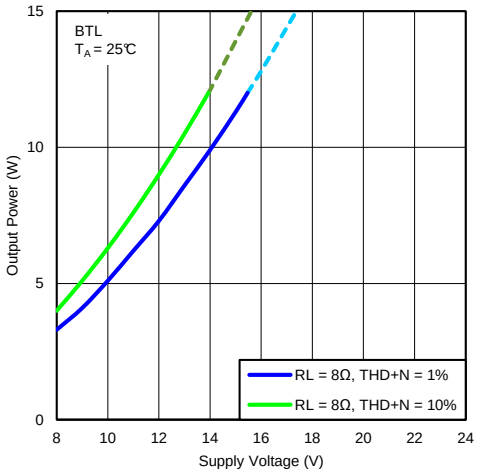
## FEATURES

- **Audio I/O Configuration:**
  - **Single Stereo I²S Input**
  - **Stereo BTL or Mono PBTL Operation**
  - **8 to 48 kHz Sample Rates**
  - **Headphone Amplifier / Line Driver**
- **Audio Digital Signal Processing:**
  - **Digital Equalization**
  - **Two-band Automatic Gain Limiting**
  - **Coarse and Fine Volume Control**
  - **PWM Level Meter**
- **General Operational Features:**
  - **I²C Software Control with Programmable I²C Address (1010100[R/W] or 1010101[R/W])**
  - **AD, BD, Ternary Modulation**
  - **Overtemp, Undervoltage, Clock, and Overcurrent Protection**
- **Audio Performance (PVDD = 18 V, $R_{LOAD}$ = 8 Ω)**
  - **Idle Channel Noise = 56 µVrms**
  - **THD+N at 1 W, 1 kHz, = 0.15 %**
  - **SNR = 105 dB (ref. to 0dBFS)**

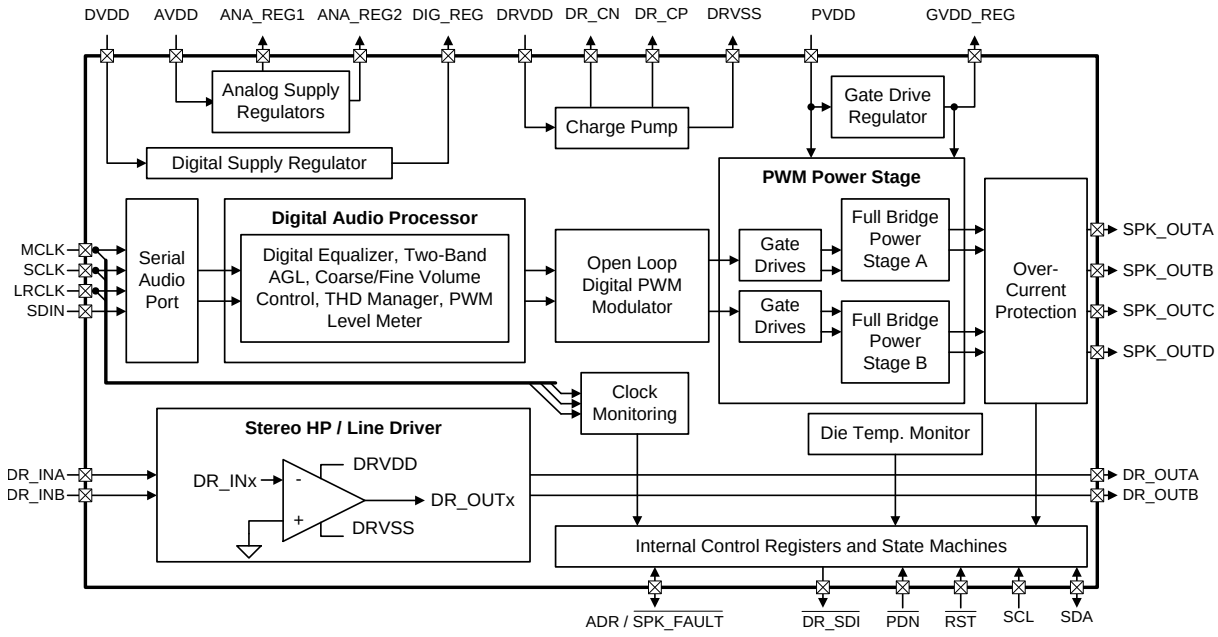
## APPLICATIONS

- **LCD/LED TV and Multi-Purpose Monitors**
- **Sound Bars, Docking Stations, PC Audio**
- **Consumer Audio Equipment**

**Power at 10% THD+N vs PVDD**




**NOTE: Dashed lines represent thermally limited region.**

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION

The TAS5729MD is a stereo I²S input device which includes a digital auto processor with two-band automatic gain limiting (AGL), digital equalization, course and fine volume control, and PWM Level meter. The AGL is an enhanced dymanic range compression (DRC) function. The device can operate from a wide PVDD power supply range to enable use in a multitude of applications. The TAS5729MD operates with a nominal supply voltage from 4.5 to 24 VDC. It is controlled by an (I²C) control port.The device has an integrated DirectPath™ headphone amplifier / line driver to increase system level integration and reduce total solution costs.

An optimal mix of thermal performance and device cost is provided in the 200 mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 48-Pin TSSOP provides excellent operation in the elevated ambient temperatures found in today's modern consumer electronic devices.

The entire TAS5729xx family is pin to pin compatible allowing a single hardware solution to be used across several end application platforms. Additionally, the I²C register map in all of the TAS5729xx family is identical, to ensure low development overhead to choose between devices based upon system level requirements.

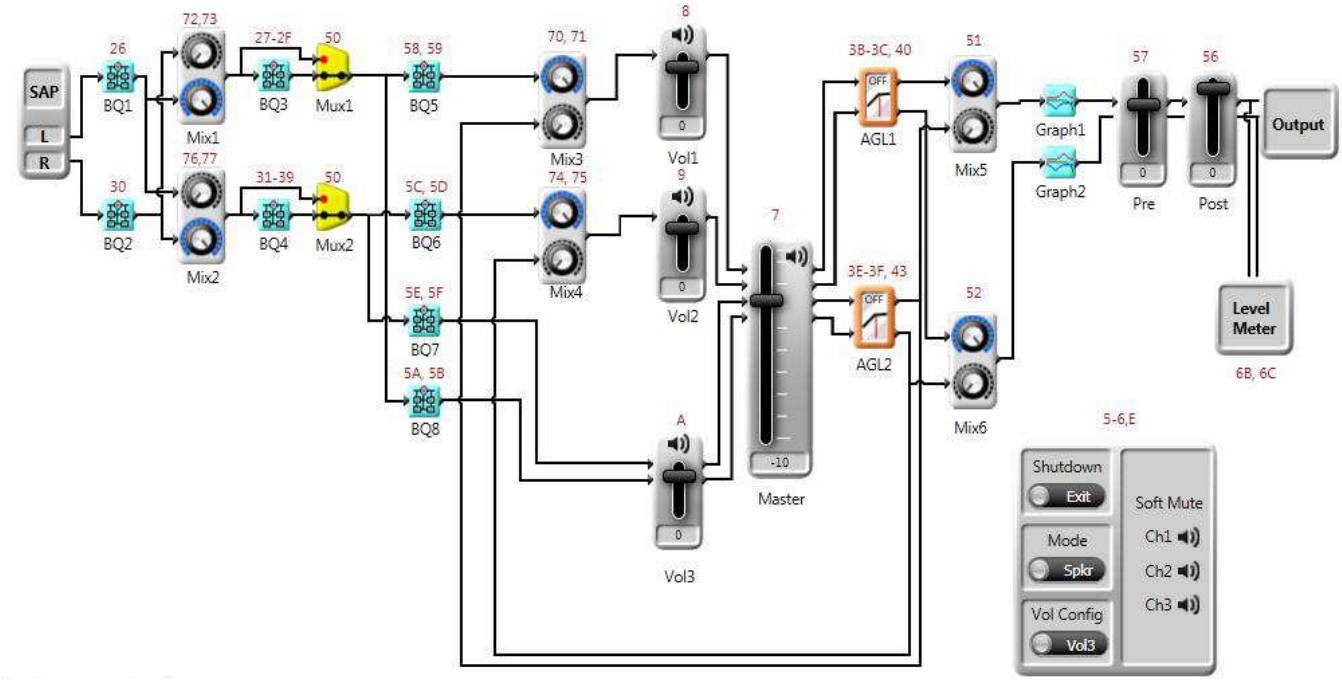
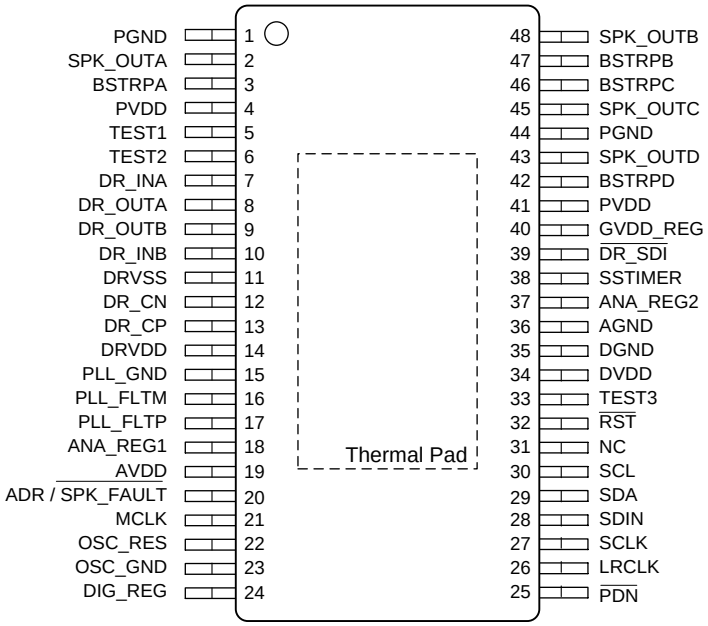



**Figure 1. TAS5729MD Signal Processing Flow**

## PINOUT AND PIN DESCRIPTIONS

**TSSOP PACKAGE**
**DCA-48**
**(TOP VIEW)**




### TAS5729MD Pin Out

| PIN | | TYPE[1] | TERMINATION | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| ADR/SPK_FAULT | 20 | DI/DO | - | Dual function terminal which sets the LSB of the 7-bit I²C address to 0 if pulled to GND, 1 if pulled to DVDD. If configured to be a fault output via the System Control Register 2 (0x05), this terminal is pulled low when an internal fault with the speaker amplifier occurs. A pull-up or pull-down resistor is required, as is shown in the Typical Application Circuit Diagrams. |
| AGND | 36 | P | - | Ground for analog circuitry[2] |
| AVDD | 19 | P | - | Power supply for internal analog circuitry |
| ANA_REG1 | 18 | P | - | Linear voltage regulator output derived from AVDD supply which is used for internal analog circuitry. Nominal 1.8 V output.[3] |
| ANA_REG2 | 37 | P | - | Linear voltage regulator output derived from AVDD supply which is used for internal analog circuitry. Nominal 3.3 V output.[3] |
| BSTRPx | 3, 42, 46, 47 | P | - | Connection points for the bootstrap capacitors, which are used to create a power supply for the high-side gate drive of the device |
| DGND | 35 | P | - | Ground for digital circuitry[2] |
| DIG_REG | 24 | P | - | Linear voltage regulator output derived from DVDD supply which is used for internal digital circuitry[3] |
| DR_CN | 12 | P | - | Negative terminal for capacitor connection used in headphone amplifier and line driver charge pump |
| DR_CP | 13 | P | - | Positive terminal for capacitor connection used in headphone amplifier and line driver charge pump |
| DR_INx | 7, 10 | AI | - | Input for channel A or B of headphone amplifier or line driver |
| DR_OUTx | 8, 9 | AO | - | Output for channel A or B of headphone amplifier or line driver |
| DR_SDI | 39 | DI | - | Places the headphone amplifier/line driver in shutdown when pulled low. |
| DRVSS | 11 | P | - | Negative supply generated by charge pump for ground centered headphone and line driver output |
| DRVDD | 14 | P | - | Power supply for internal headphone and line driver circuitry |

(1) TYPE: AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, P = Power, G = Ground (0V)
(2) This terminal should be connected to the system ground
(3) This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.

## TAS5729MD Pin Out (continued)

| | | | | |
|---|---|---|---|---|
| DVDD | 34 | P | - | Power supply for the internal digital circuitry |
| GVDD_REG | 40 | P | - | Voltage regulator derived from PVDD supply(3) |
| LRCLK | 26 | DI | Pulldown | Word select clock of the serial audio port. |
| MCLK | 21 | DI | Pulldown | Master clock used for internal clock tree and sub-circuit and state machine clocking |
| NC | 31 | - | - | Not connected inside the device (all NC terminals should be connected to ground for optimal thermal performance) |
| OSC_GND | 23 | P | - | Ground for oscillator circuitry (this terminal should be connected to the system ground) |
| OSC_RES | 22 | AO | - | Connection point for oscillator trim resistor |
| $\overline{\text{PDN}}$ | 25 | DI | Pullup | Quick powerdown of the device that is used upon an unexpected loss of PVDD or DVDD power supply in order to quickly transition the outputs of the speaker amplifier to hi-Z. This quick powerdown feature avoids the audible anamolies that would occur as a result of loss of either of the supplies. |
| PGND | 1, 44 | P | - | Ground for power device circuitry(2) |
| PLL_FLTM | 16 | AI/AO | - | Negative connection point for the PLL loop filter components |
| PLL_FLTP | 17 | AI/AO | - | Positive connection point for the PLL loop filter components |
| PLL_GND | 15 | P | - | Ground for PLL circuitry (this terminal should be connected to the system ground) |
| PowerPAD™ | - | P | - | Thermal and ground pad that provides both an electrical connection to the ground plane and a thermal path to the PCB for heat dissipation. This pad must be grounded to the system ground. (4) |
| PVDD | 4, 41 | P | - | Power supply for internal power circuitry |
| $\overline{\text{RST}}$ | 32 | DI | Pullup | Places the device in reset when pulled low |
| SCL | 30 | DI | - | I²C serial control port clock |
| SCLK | 27 | DI | Pulldown | Bit clock of the serial audio port |
| SDA | 29 | DI/DO | - | I²C serial control port data |
| SDIN | 28 | DI | Pulldown | Data line to the serial data port |
| SPK_OUTx | 2, 43, 45, 48 | AO | - | Speaker amplifier outputs |
| SSTIMER | 38 | AI | - | Controls ramp time of SPK_OUTx to minimize pop. Leave this pin floating for BD mode. Requires capacitor to GND in AD mode, as is shown in the Typical Application Circuit Diagrams. The capacitor determines the ramp time. |
| TEST1 | 5 | DO | - | Used for testing during device production (this terminal must be left floating) |
| TEST2 | 6 | DO | - | Used for testing during device production (this terminal must be left floating) |
| TEST3 | 33 | DI | - | Used for testing during device production (this terminal must be connected to GND) |

(4) This terminal should be connected to the system ground

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Temperature | Ambient Operating Temperature, $T_A$ | 0 | 85 | °C |
| | Ambient Storage Temperature, $T_S$ | -40 | 125 | °C |
| Supply voltage | DVDD, DRVDD, AVDD | -0.3 | 4.2 | V |
| | PVDD | -0.3 | 30 | V |
| Input voltage | DVDD Referenced Digital Inputs | -0.5 | DVDD + 0.5 | V |
| | 5-V tolerant digital inputs (2) | -0.5 | DVDD + 2.5(3) | V |
| | DR_INx | DRVSS - 0.3 | DRVDD + 0.3 | V |
| HP Load | $R_{LOAD}$(HP) | 12.8 | N/A | Ω |
| Line Driver Load | $R_{LOAD}$(LD) | 600 | N/A | Ω |
| Voltage at speaker output pins | SPK_OUTx | -0.03 | 32 | V |
| Voltage at BSTRPx pins | BSTRPx | -0.03 | 39 | V |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 5-V tolerant inputs are PDN, RESET, SCLK, LRCLK, MCLK, SDIN, SDA, and SCL.
(3) Maximum pin voltage should not exceed 6 V.

## THERMAL CHARACTERISTICS

| THERMAL METRIC(1) | | TAS5729MD | | UNIT |
|---|---|---|---|---|
| | | 48 Pin DCA (2) | 48 Pin DCA(3) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 62.6 | 32.6 | °C/W |
| $\theta_{JC(bottom)}$ | Junction-to-case (bottom) thermal resistance | 17.9 | 16.2 | °C/W |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 11.9 | 14.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | 0.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 13.5 | 14.3 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case (top) thermal resistance | 1.5 | 1.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) JEDEC Standard 2 Layer Board
(3) JEDEC Standard 4 Layer Board

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | | 0 | - | 85 | °C |
| VDD | DVDD, DRVDD and AVDD Supply | | 2.97 | - | 3.63 | V |
| PVDD | PVDD Supply | | 4.5 | - | 26.4(1) | V |
| $V_{IH}$ | Input Logic High | | 2 | - | - | V |
| $V_{IL}$ | Input Logic Low | | - | - | 0.8 | V |
| $R_{HP}$ | Minimum HP Load | | 16 | - | - | Ω |
| $R_{LD}$ | Minimum Line Driver Load | | 600 | - | - | Ω |
| $R_{SPK(BTL)}$ | Minimum Speaker Load in BTL Mode | | 8 | - | - | Ω |
| $R_{SPK(PBTL)}$ | Minimum Speaker Load in Post-Filter PBTL Mode | | 4 | - | - | Ω |
| $L_{FILT}$ | Minimum output inductance under short-circuit condition | | 10 | - | - | µH |

(1) For operation at PVDD levels greater than 18 V, the modulation limit must be set to 93.8% via the control port register 0x10.

# ELECTRICAL SPECIFICATIONS AND CHARACTERISTICS

## DIGITAL I/O PINS

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\|I_{IH}\|$ | Input Logic "High" Current Level | All digital pins | - | - | 75 | µA |
| $V_{IH}$ | Input Logic "High" threshold for DVDD Referenced Digital Inputs | All digital pins | 2 | - | - | V |
| $\|I_{IL}\|$ | Input Logic "Low" Current Level | All digital pins | - | - | 75 | µA |
| $V_{IL}$ | Input Logic "Low" threshold for DVDD Referenced Digital Inputs | All digital pins | - | - | 0.8 | V |
| $V_{OH}$ | Output Logic "High" Voltage Level | $I_{OH}$ = 4 mA, VDD = 3V | 2.4 | - | - | V |
| $V_{OL}$ | Output Logic "Low" Voltage Level | $I_{OH}$ = -4 mA, VDD = 3V | - | - | 0.5 | V |

## MASTER CLOCK

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $D_{MCLK}$ | Allowable MCLK Duty Cycle | | 40 | 50 | 60 | % |
| $f_{MCLK}$ | Supported MCLK Frequencies | | 2.8224 | - | 24.576 | MHz |
| $t_r$ $t_f$ | Rise and fall time for MCLK | | - | - | 5 | ns |

## SERIAL AUDIO PORT

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCLK}$ | Supported SCLK Frequencies | Values include 32, 48, and 64 | 32 | - | 64 | x $f_S$ |
| $D_{SCLK}$ | Allowable SCLK Duty Cycle | | 40 | 50 | 60 | % |
| $t_{su2}$ | Required SDIN Setup Time before SCLK Rising Edge | | 10 | - | - | ns |
| $t_{h2}$ | Required SDIN Hold Time after SCLK Rising Edge | | 10 | - | - | ns |
| $f_S$ | Supported Input Sample Rates | | 8 | - | 48 | kHz |
| $D_{LRCLK}$ | Allowable LRCLK Duty Cycle | | 40 | 50 | 60 | % |
| $t_{su1}$ | Required LRCLK to SCLK Rising Edge | | 10 | - | - | ns |
| $t_{h1}$ | Required LRCLK to SCLK Rising Edge | | 10 | - | - | ns |
| $t_r$ $t_f$ | Rise and fall time for SCLK and LRCLK | | - | - | 8 | ns |
| | Allowable LRCLK drift before LRCLK reset | | - | - | 4 | MCLKs |

## PROTECTION CIRCUITRY

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $OCE_{THRES}$ | Overcurrent Threshold for each BTL Output | PVDD = 15V, $T_A$ = 25°C | - | 4.5 | - | A |
| $UVE_{THRES(PVDD)}$ | Undervoltage Error (UVE) Threshold | PVDD falling | - | 4 | - | V |
| $UVE_{THRES(AVDD)}$ | Undervoltage Error (UVE) Threshold | AVDD falling | - | 4.1 | - | V |
| $UVE_{HYST(PVDD)}$ | UVE Recovery Threshold | PVDD rising | - | 4.5 | - | V |
| $UVE_{HYST(AVDD)}$ | UVE Recovery Threshold | AVDD rising | - | 2.7 | - | V |
| $OTE_{THRES}$ | Overtemperature Error (OTE) Threshold | | - | 150 | - | °C |
| $OTE_{HYST}$ | OTE Recovery Threshold | | - | 30 | - | °C |

## SPEAKER AMPLIFIER IN ALL MODES

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SPK\_AMP}$ | Speaker Amplifier Switching Frequency | 11.025/22.05/44.1-kHz data rate ±2% | - | 352.8 | - | kHz |
| | | 48/24/12/8/16/32-kHz data rate ±2% | - | 384 | - | kHz |
| $R_{DS(ON)}$ | On Resistance of Output Mosfet (both high-side and low-side) | PVDD = 15 V, TA = 25 °C, Die Only | - | 200 | - | mΩ |
| | | PVDD= 15V, TA = 25 °C, Includes: Die, Bond Wires, Leadframe | - | 240 | - | mΩ |
| $R_{PD}$ | Internal Pulldown Resistor at Output of each Half-Bridge Making up the Full Bridge Outputs | Connected when drivers are tri-stated to provide bootstrap capacitor charge | - | 3 | - | kΩ |

## SPEAKER AMPLIFIER IN STEREO BRIDGE TIED LOAD (BTL) MODE

$T_A$ = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal = 1 kHz sine wave, BTL, AD mode, $f_S$ = 48 kHz, RSPK = 8 Ω, AES17 filter, $f_{PWM}$ = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $ICN_{(SPK)}$ | Idle Channel Noise | PVDD = 18 V, A-Weighted | - | 56 | - | µVrms |
| $Po_{(SPK)}$ | Maximum Continuous Output Power Per. Ch. | PVDD = 13 V, 10% THD, 1-kHz input signal | - | 10.5 | - | W |
| | | PVDD = 8 V, 10% THD, 1-kHz input signal | - | 4 | - | W |
| | | PVDD = 18 V, 10% THD, 1-kHz input signal | - | 12 | - | W |
| $SNR_{(SPK)}$ | Signal to Noise Ratio (Referenced to 0dBFS Input Signal) | PVDD = 18V, A-weighted, f = 1 kHz, maximum power at THD < 1% | - | 105 | - | dB |
| $THD+N_{(SPK)}$ | Total Harmonic Distortion and Noise | PVDD = 18 V; $P_O$ = 1 W | - | 0.15 | - | % |
| | | PVDD = 13 V; $P_O$ = 1 W | - | 0.13 | - | % |
| | | PVDD = 8 V; $P_O$ = 1 W | - | 0.2 | - | % |
| $X\text{-}Talk_{(SPK)}$ | Cross-talk (worst case between LtoR and RtoL coupling) | $P_O$ = 1 W, f = 1 kHz (BD mode) | - | –70 | - | dB |
| | | $P_O$ = 1 W, f = 1 kHz (AD mode) | - | –48 | - | dB |

## SPEAKER AMPLIFIER IN STEREO POST-FILTER PARALLEL BRIDGE TIED LOAD (POST-FILTER PBTL) MODE

$T_A$ = 25°C, PVDD = 18 V, AVDD = DRVDD = DVDD = 3.3 V, audio input signal = 1 kHz sine wave, BTL, AD mode, $f_S$ = 48 kHz, RSPK = 4 Ω, AES17 filter, $f_{PWM}$ = 384 kHz, external components per Typical Application Circuit diagrams, and in accordance with recommended operating conditions (unless otherwise specified).

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $ICN_{(SPK)}$ | Idle Channel Noise | PVDD = 18 V, A-Weighted | - | 42 | - | µVrms |
| $Po_{(SPK)}$ | Maximum Continuous Output Power Per. Ch. | PVDD = 13 V, 10% THD, 1-kHz input signal | - | 18.9 | - | W |
| | | PVDD = 8 V, 10% THD, 1-kHz input signal | - | 7.2 | - | W |
| | | PVDD = 18 V, 10% THD, 1-kHz input signal | - | 24 | - | W |
| $SNR_{(SPK)}$ | Signal to Noise Ratio (Referenced to 0dBFS Input Signal) | PVDD = 18V, A-weighted, f = 1 kHz, maximum power at THD < 1% | - | 105 | - | dB |
| $THD+N_{(SPK)}$ | Total Harmonic Distortion and Noise | PVDD = 18 V; $P_O$ = 1 W | - | 0.06 | - | % |
| | | PVDD = 13 V; $P_O$ = 1 W | - | 0.03 | - | % |
| | | PVDD = 8 V; $P_O$ = 1 W | - | 0.15 | - | % |

## HEADPHONE AMPLIFIER / LINE DRIVER

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CP}$ | Charge Pump Switching Frequency | | 200 | 300 | 400 | kHz |
| $Po_{(HP)}$ | Headphone Amplifier Output Power | $R_{LOAD}$(HP) = 32Ω, THD+N = 1%, Outputs in Phase | - | 55 | - | mW |
| $SNR_{(HP)}$ | Signal to Noise Ratio | (Referenced to 55mW Output Signal), $R_{LOAD}$(HP) = 32Ω, A-Weighted | - | 101 | - | dB |
| $SNR_{(LD)}$ | Signal to Noise Ratio | (Referenced to 2Vrms Output Signal), $R_{LOAD}$(LD) = 10kΩ, A-Weighted | - | 105 | - | dB |

## RESET TIMING

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(RESET)}$ | Pulse duration required to reset the device | | 100 | - | - | µs |

## I²C CONTROL PORT

over operating free-air temperature range (unless otherwise noted)

| Parameter | | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $C_{L(I^2C)}$ | Allowable Load Capacitance for Each I²C Line | | - | - | 400 | pF |
| $f_{SCL}$ | Supported SCL frequency | No Wait States | 100 | - | 400 | kHz |
| $t_{buf}$ | Bus Free time between stop and start conditions | | 1.3 | - | - | µs |
| $t_{f(I^2C)}$ | Rise Time, SCL and SDA | | - | - | 300 | ns |
| $t_{h1(I^2C)}$ | Hold Time, SCL to SDA | | 0 | - | - | ns |
| $t_{h2(I^2C)}$ | Hold Time, start condition to SCL | | 0.6 | - | - | µs |
| $t_{I^2C(start)}$ | I²C Startup Time | Time to enable I²C from release RST | - | - | 12 | ms |
| $t_{r(I^2C)}$ | Rise Time, SCL and SDA | | - | - | 300 | ns |
| $t_{su1(I^2C)}$ | Setup Time, SDA to SCL | | 100 | - | - | ns |
| $t_{su2(I^2C)}$ | Setup Time, SCL to start condition | | 0.6 | - | - | µs |
| $t_{su3(I^2C)}$ | Setup Time, SCL to stop condition | | 0.6 | - | - | µs |
| $T_{w(H)}$ | Required Pulse Duration, SCL High | | 0.6 | - | - | µs |
| $T_{w(L)}$ | Required Pulse Duration, SCL Low | | 1.3 | - | - | µs |

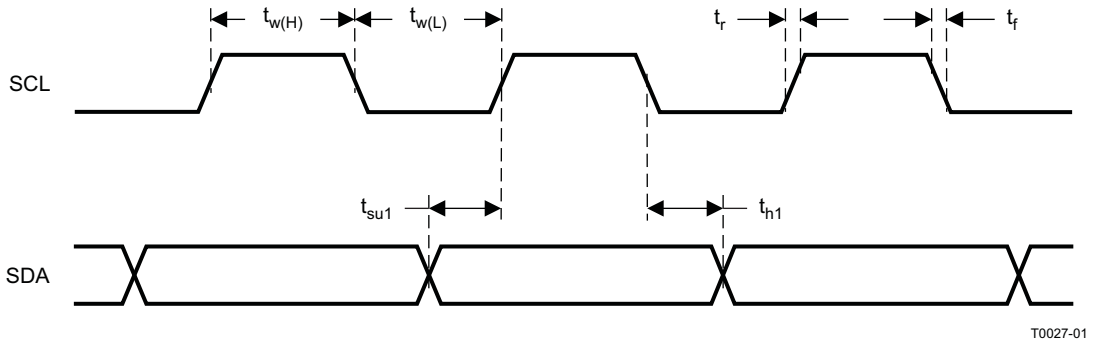



**Figure 2. SCL and SDA Timing for I²C Control Port**

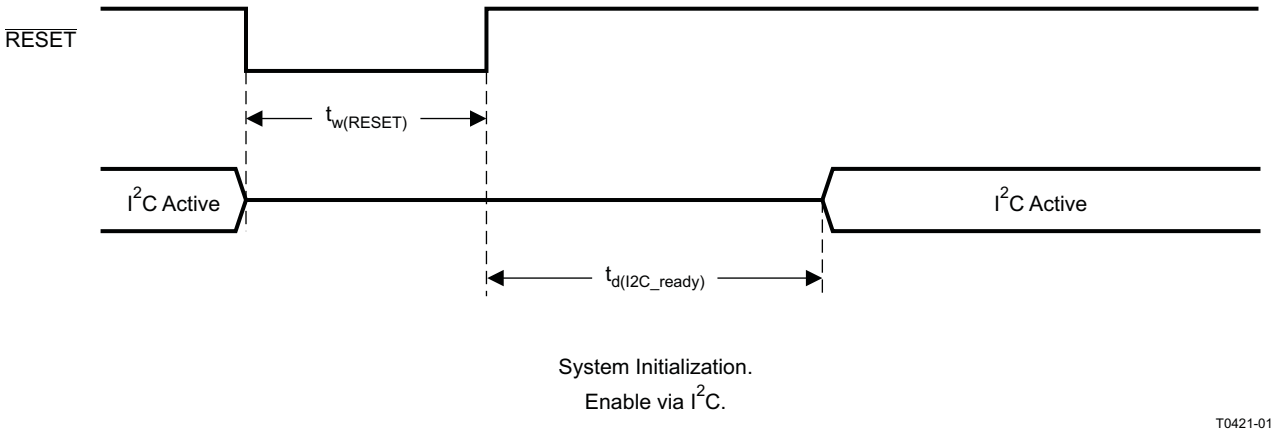


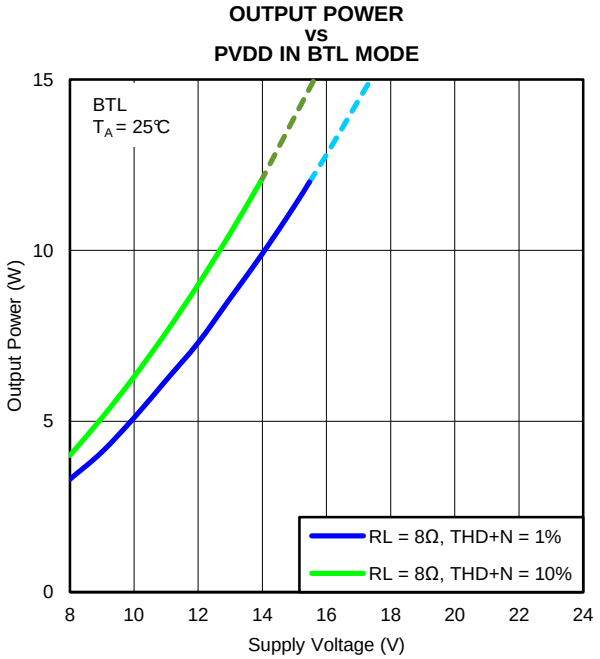

**Figure 3. Start and Stop Timing Conditions**

## TYPICAL ELECTRICAL POWER CONSUMPTION

over operating free-air temperature range (unless otherwise noted), with DVDD = DRVDD = 3.3 V and AVDD = PVDD, external components as specified on the EVM.

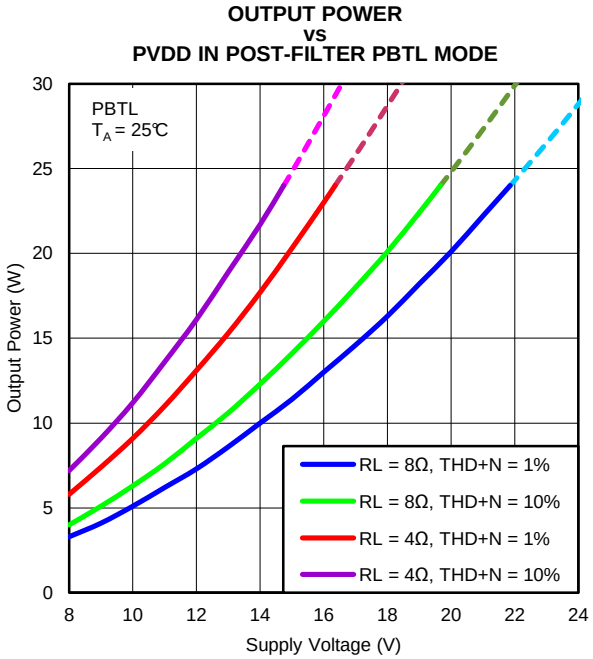
| Speaker Amplifier State | | Configuration Settings | $V_{PVDD}$ [V] | $I_{PVDD}$ [mA] | $I_{VDD}$ [mA] | $P_{DISS}$ (From all Supplies) [W] |
|---|---|---|---|---|---|---|
| $f_{SPK\_AMP}$ | Operational State | | | | | |
| 384kHz | Idle | $\overline{RST}$ pulled high, speaker amplifer outputs at 50/50 mute | 18 | 20 | 48 | 0.51 |
| | Reset | $\overline{RST}$ pulled low, $\overline{PDN}$ pulled high | | 5 | 21 | 0.16 |

## SPEAKER AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS




NOTE: Dashed lines represent thermally limited region.

**Figure 4.**




NOTE: Dashed lines represent thermally limited region.

**Figure 5.**

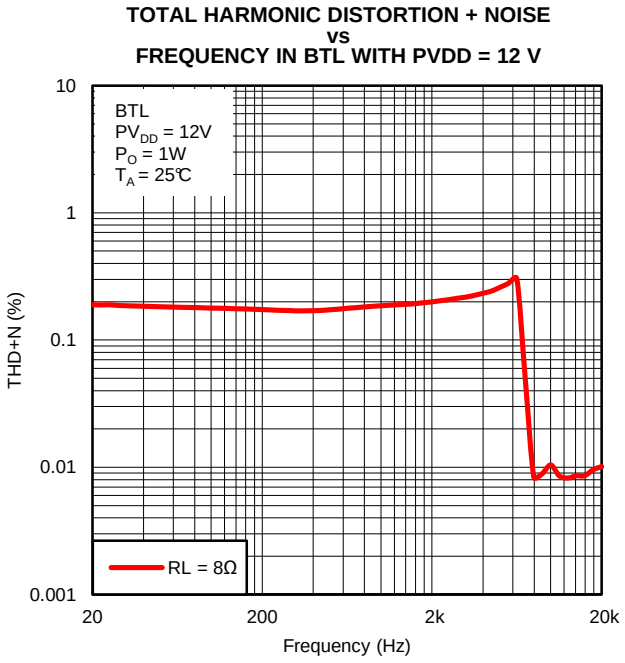



**Figure 6.**

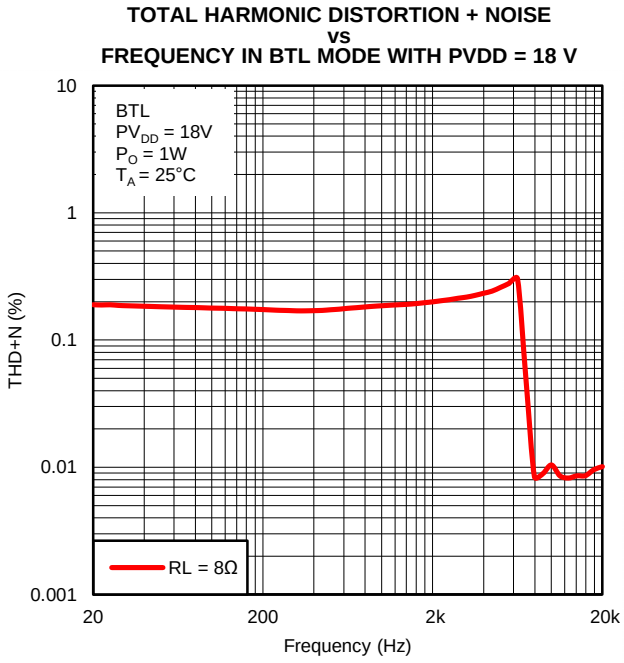



**Figure 7.**

## SPEAKER AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN BTL MODE WITH PVDD = 24 V**

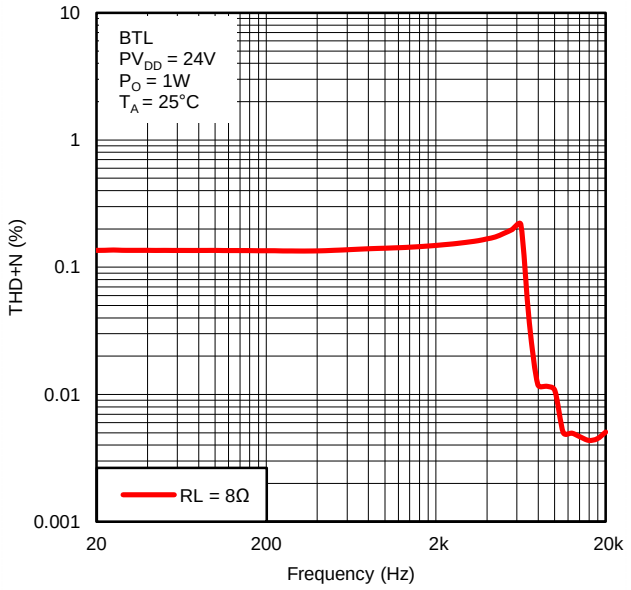



**Figure 8.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN POST-FILTER PBTL MODE WITH PVDD = 12 V**

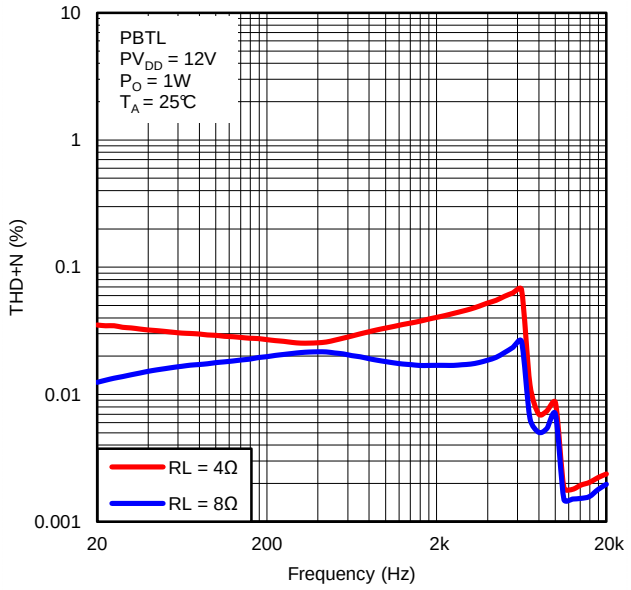



**Figure 9.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN POST-FILTER PBTL MODE WITH PVDD = 18 V**

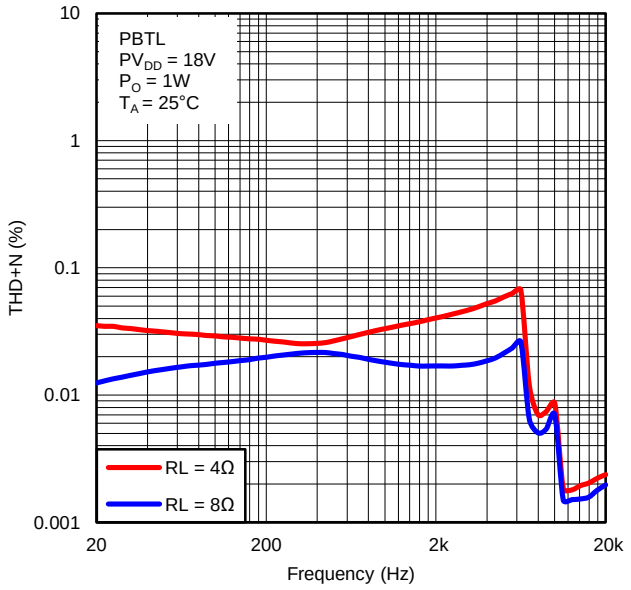



**Figure 10.**

**TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY IN POST-FILTER PBTL MODE WITH PVDD = 24 V**

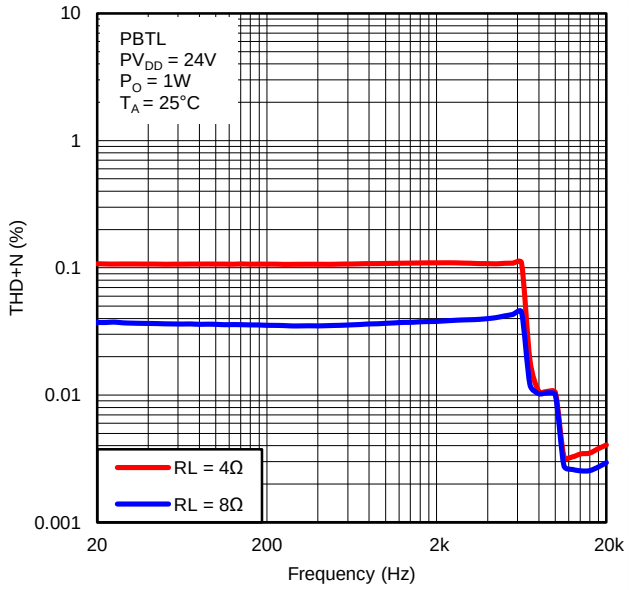



**Figure 11.**

## SPEAKER AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**STEREO BTL IDLE CHANNEL NOISE vs PVDD**

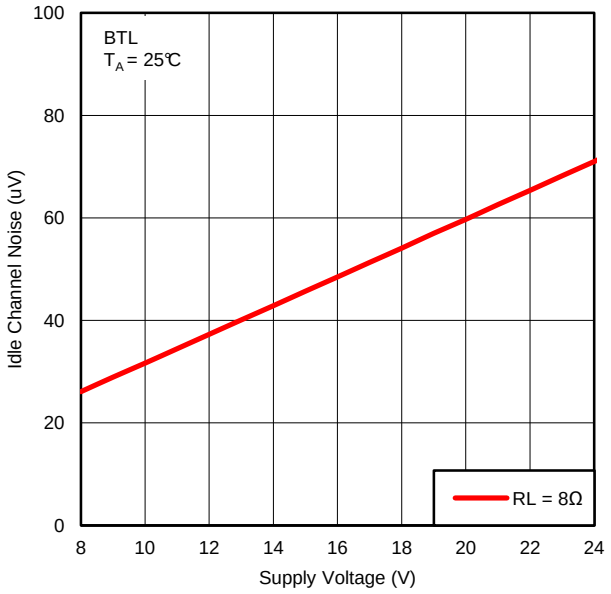



**Figure 12.**

**POST-FILTER PBTL IDLE CHANNEL NOISE vs PVDD**

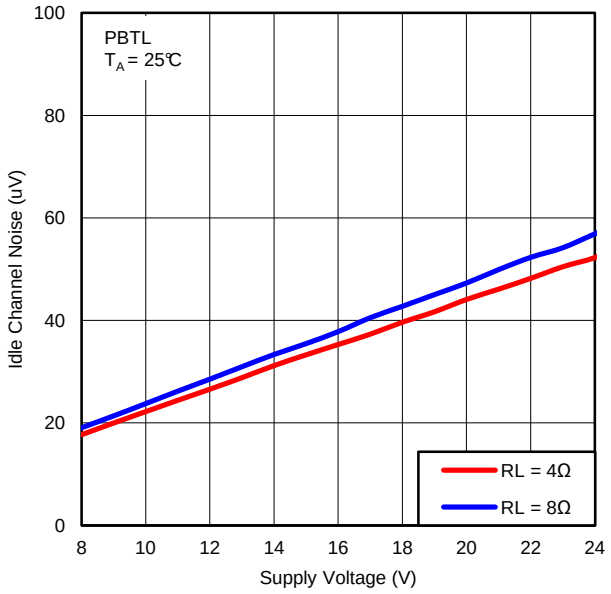



**Figure 13.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN BTL MODE WITH PVDD = 12 V**

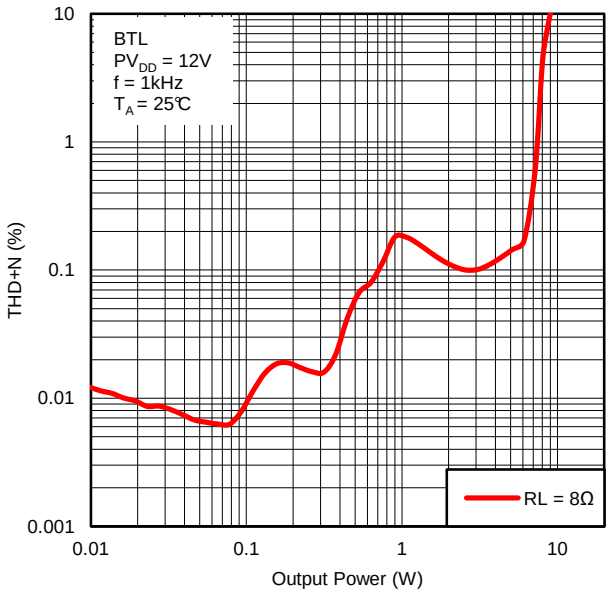



**Figure 14.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN BTL MODE WITH PVDD = 18 V**

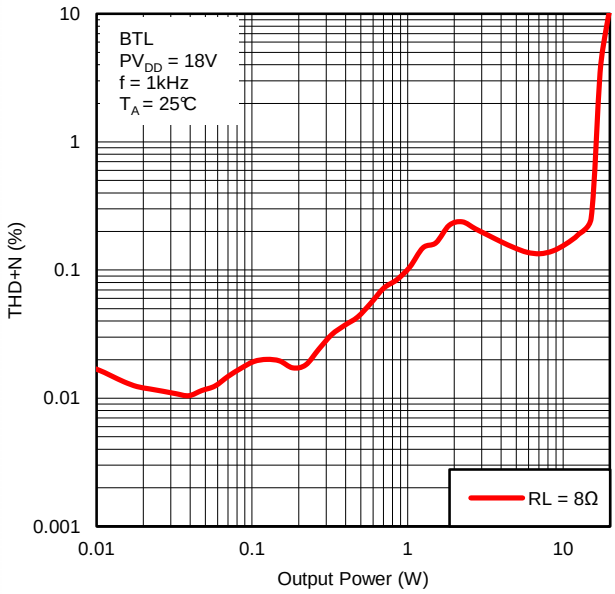



**Figure 15.**

## SPEAKER AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS (continued)

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN BTL MODE WITH PVDD = 24 V**

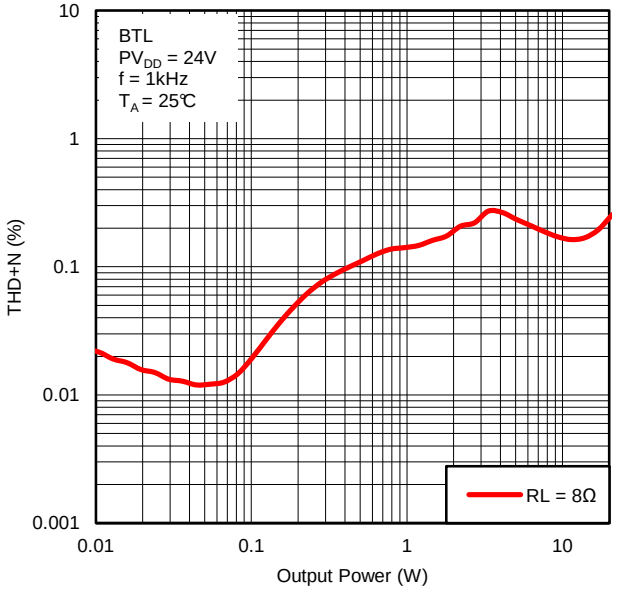



**Figure 16.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN POST-FILTER PBTL MODE WITH PVDD = 12 V**

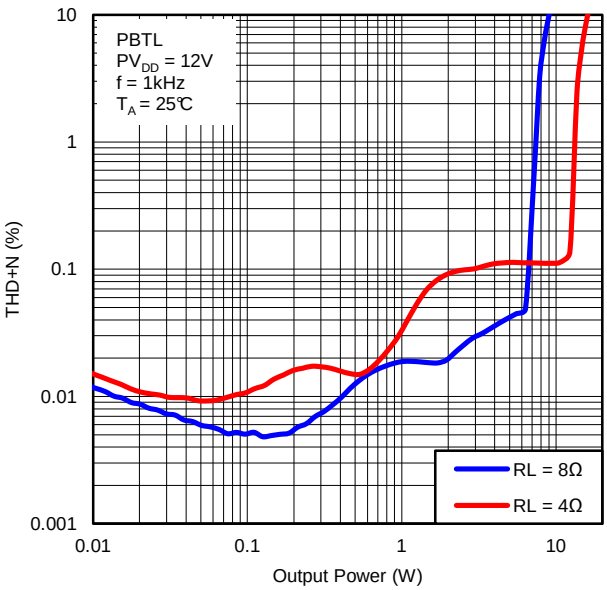



**Figure 17.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN POST-FILTER PBTL MODE WITH PVDD = 18 V**

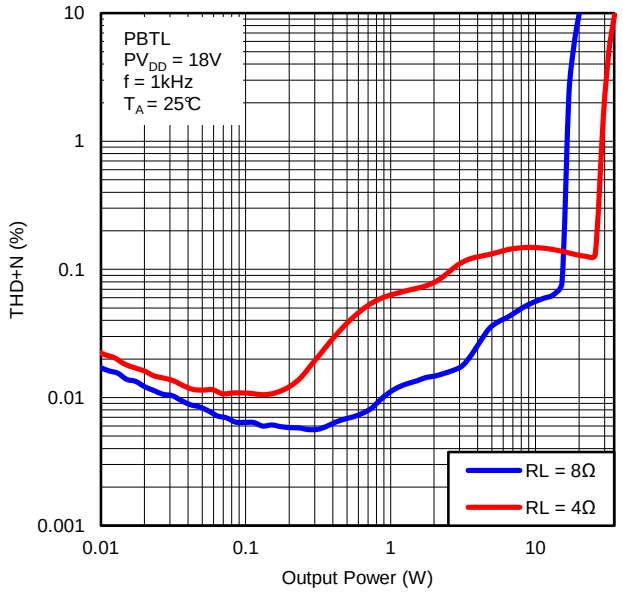



**Figure 18.**

**TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER IN POST-FILTER PBTL MODE WITH PVDD = 24 V**

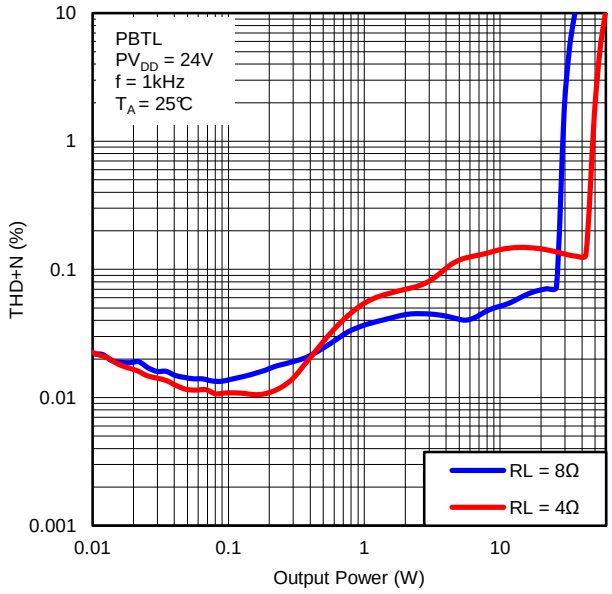
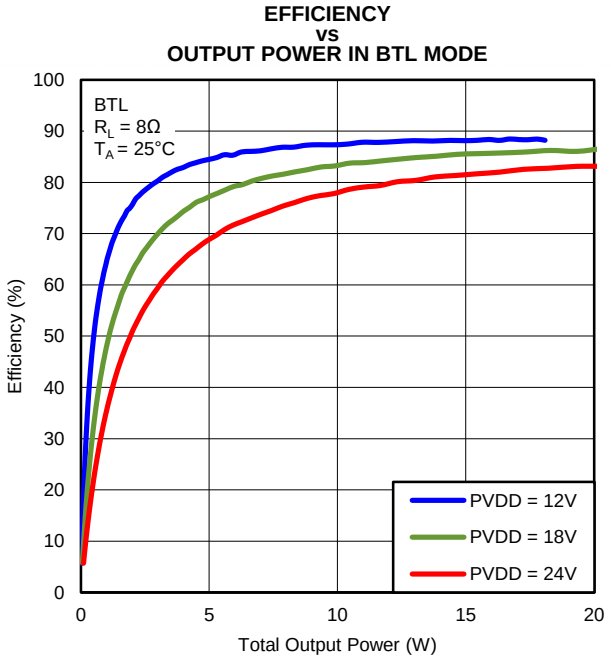


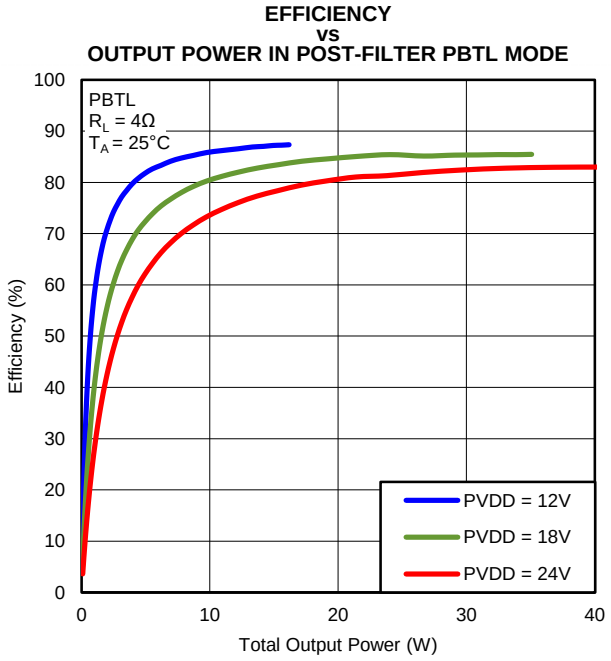

**Figure 19.**

## SPEAKER AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS (continued)




All channels driven

**Figure 20.**




All channels driven

**Figure 21.**

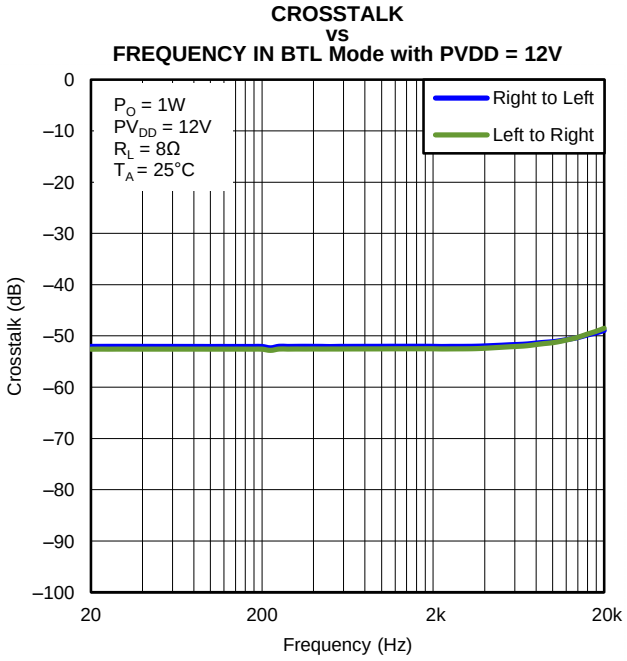



**Figure 22.**

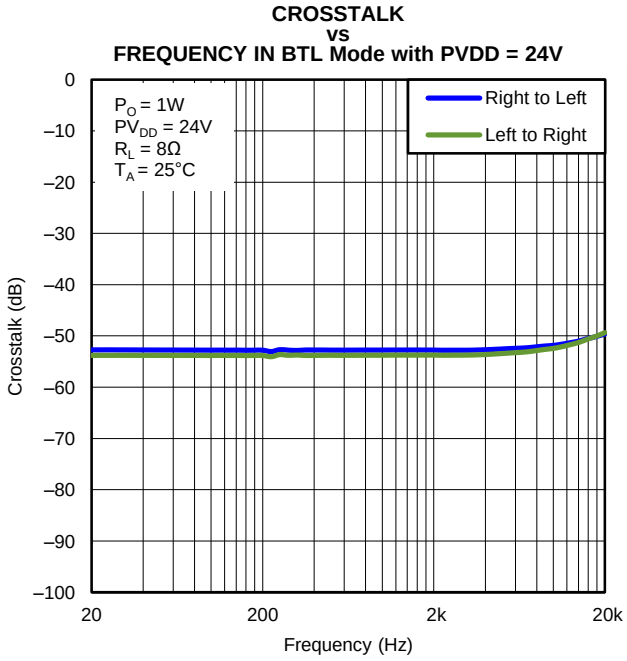



**Figure 23.**

## HEADPHONE AMPLIFIER TYPICAL PERFORMANCE CHARACTERISTICS

**HEADPHONE TOTAL HARMONIC DISTORTION + NOISE VS FREQUENCY WITH DRVDD = 3.3 V**

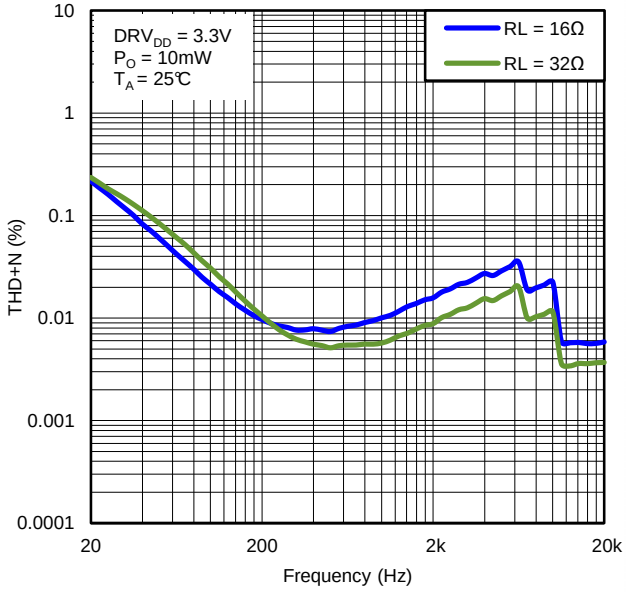



**Figure 24.**

**HEADPHONE TOTAL HARMONIC DISTORTION + NOISE VS POWER WITH DRVDD = 3.3 V**

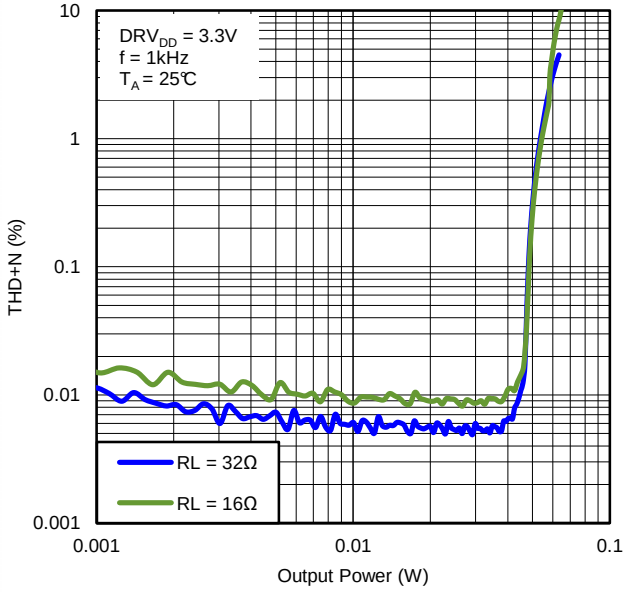



**Figure 25.**

**HEADPHONE CROSS TALK VS FREQUENCY WITH DRVDD = 3.3 V AND $R_{HP}$ = 16 Ω**

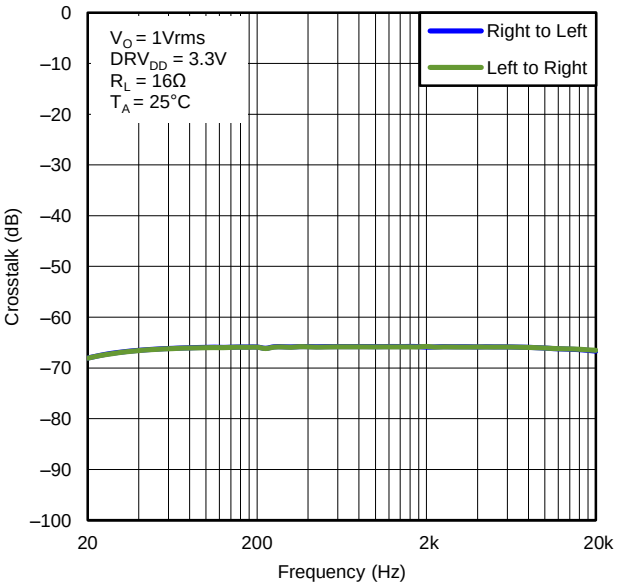



**Figure 26.**

**HEADPHONE CROSS TALK VS FREQUENCY WITH DRVDD = 3.3 V AND $R_{HP}$ = 32 Ω**

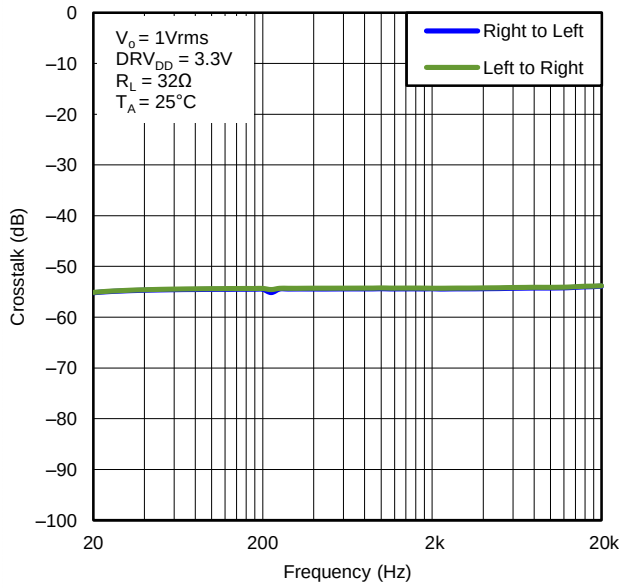



**Figure 27.**

## LINE DRIVER TYPICAL PERFORMANCECHARACTERISTICS

**LINE DRIVER TOTAL HARMONIC DISTORTION + NOISE VS FREQUENCY WITH DRVDD = 3.3 V**

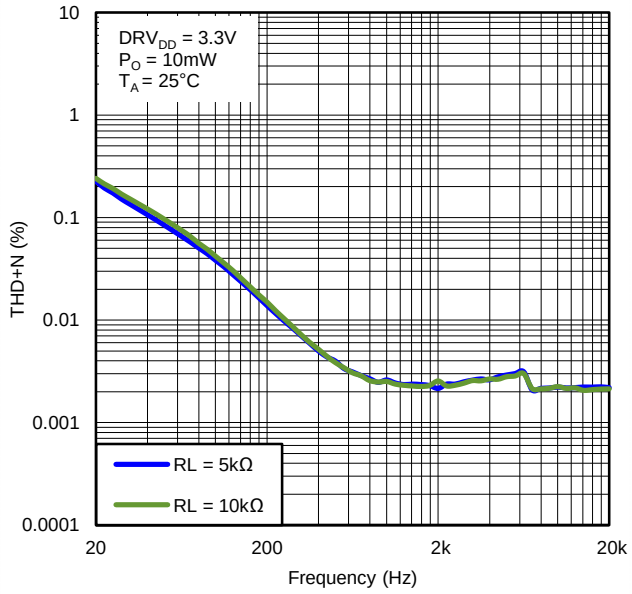



**Figure 28.**

**LINE DRIVER THD+N VS OUTPUT VOLTAGE WITH DRVDD = 3.3 V**

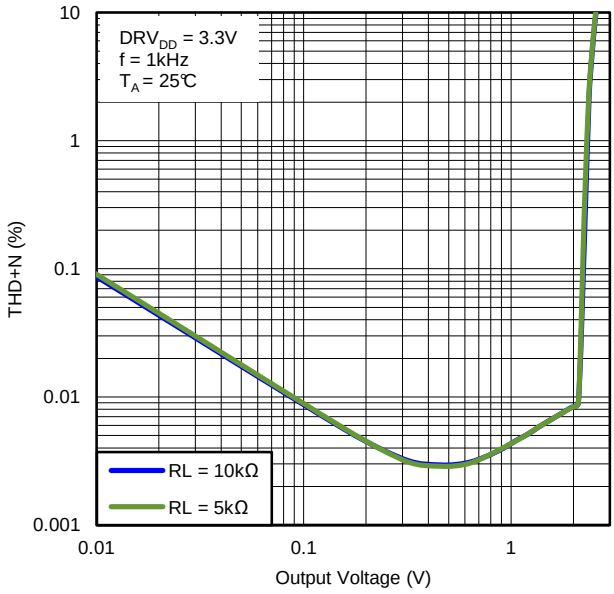



**Figure 29.**

**LINE DRIVER CROSSTALK VS FREQUENCY WITH DRVDD = 3.3 V**

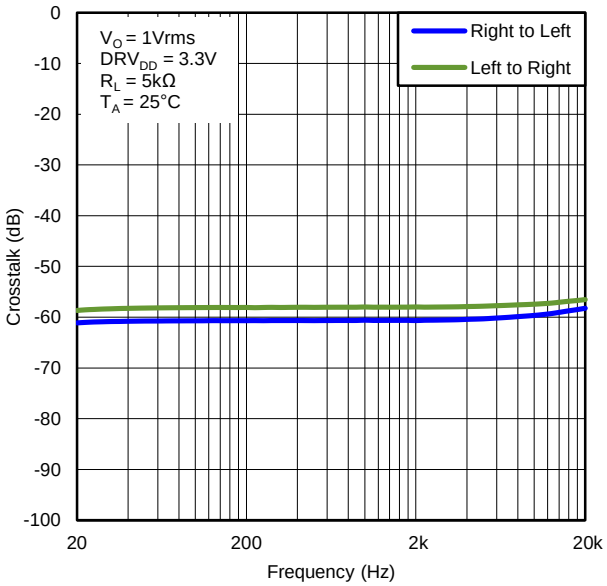



**Figure 30.**

## Theory of Operation and Detailed Description

### POWER SUPPLY

To facilitate system design, the TAS5729MD needs only a single low-voltage DVDD supply in addition to the higher-voltage PVDD power supply. An internal voltage regulator provides suitable voltage levels for the gate drive circuitry. Additionally, all circuitry requiring a floating voltage supply, e.g., the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only a few external capacitors.

In order to provide good electrical and acoustical characteristics, the PWM signal path for the output stage is designed as identical, independent half-bridges which operate in pairs to produce the full-bridge outputs capable of driving BTL loads. For this reason, each half-bridge has separate bootstrap pins (BSTRPx) and power-stage supply pins (PVDD). The gate drive voltage (GVDD_REG) is derived from the PVDD voltage. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power-supply pins and decoupling capacitors must be avoided.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSTRPx) to the power-stage output pin (SPK_OUTx). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive regulator output pin (GVDD_REG) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each pair of half-bridges has independent power-stage supply pins (PVDD). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD pin is decoupled with a ceramic capacitor placed as close as possible to each supply pin, as shown in the typical application circuits.

### ADR/$\overline{\text{SPK\_FAULT}}$

The ADR/$\overline{\text{SPK\_FAULT}}$ pin is an input pin during power up. It can be pulled high or low through a pull-up or pull-down resistor, as shown in the typical application circuit. HIGH sets an I²C address of 1010101[R/W] , and LOW an address of 1010100[R/W] . Additionally, via the control port, it can be configured to serve as the fault indicator for the speaker amplifier.

### DEVICE PROTECTION SYSTEM

#### Overcurrent (OC) Protection With Current Limiting

The device has independent, fast-reacting current detectors on all high-side and low-side power-stage FETs. The detector outputs are closely monitored by a protection system. If a high-current condition persists, that is, the power stage is being overloaded, a protection system triggers a shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state. The device retries to start-up based on the retry time set in the BKDN_ERR register and returns to normal operation once the fault condition (that is, a short circuit on the output) is removed. Current limiting and overcurrent protection are not independent for half-bridges. That is, if the bridge-tied load between half-bridges A and B causes an overcurrent fault, half-bridges A, B, C, and D are shut down. An overcurrent fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the SYSTEM CONTROL register.

#### Overtemperature Protection

The TAS5729MD has an overtemperature-protection system. If the device junction temperature exceeds the amount specified by $OTE_{THRES}$ in the Protection Circuitry Electrical Characteristics table, the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state. The TAS5729MD recovers automatically once the temperature drops by the amount specified by $OTE_{HYST}$. An overtemperature fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the SYSTEM CONTROL register.

### Undervoltage Error (UVE) and Power-On Reset (POR)

The UVE and POR circuits of the TAS5729MD fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit ensures that all circuits are fully operational when the PVDD and AVDD supply voltages reach their respective $UVE_{THRES}$ levels as specified in the Protection Circuitry Electrical Characteristics table. Although PVDD and AVDD are independently monitored, a supply voltage drop below the UVE threshold for AVDD or either of the PVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state. An undervoltage fault error is reported in the ERROR STATUS register, and a fault error signal can be monitored on the SPK_FAULT pin if configured in the SYSTEM CONTROL register.

## CLOCK, AUTO DETECTION, AND PLL

The TAS5729MD is an $I^2S$ slave device that needs a valid Master Clock (MCLK), Bit Clock (SCLK) and Word Clock (LRCLK) to play audio. The digital audio processor (DAP) supports all the sample rates and MCLK rates that are defined in the clock control register . The TAS5729MD checks to verify that SCLK is a specific value of 32 $f_S$, 48 $f_S$, or 64 $f_S$. The DAP only supports a 1 × $f_S$ LRCLK.

The device has robust clock error handling that uses a built-in auto detect block to quickly detect changes/errors. When the system detects a clock change/error, it mutes the audio (through a single-step mute) and forces PLL to limp, where output PWM's continue to switch in idle but the device cannot play audio. Once the clocks are valid and stable, the system auto detects the new rate and reverts to normal operation. During this process, the volume is restored in a single step (also called hard unmute). The ramp process can be programmed to ramp back slowly (also called soft unmute) as defined in volume register (0x0E).

The table below shows the valid MCLK rates across different $f_S$ rates. Note that for 44.1kHz/48kHz $f_S$ rates, a 64 x $f_S$ MCLK rate is supported. If a 64 x $f_S$ SCLK rate is used, a common 64 x $f_S$ clock can be used for both MCLK and SCLK.

**Table 1. Supported LRCLK, SCLK, and MCLK Ratios in the TAS5729MD**

| LRCLK Rate [kHz] | MCLK Rate [ x $f_S$] | | | | | |
|---|---|---|---|---|---|---|
| | 64 | 128 | 192 | 256 | 384 | 512 |
| 8 | — | — | — | — | Y | Y |
| 11.025/12 | — | — | — | Y | Y | Y |
| 16 | — | — | — | Y | Y | Y |
| 22.05/24 | — | — | — | Y | Y | Y |
| 32 | — | — | Y | Y | Y | Y |
| 44.1/48 | Y | Y | Y | Y | Y | Y |

## SERIAL DATA INTERFACE

Serial data is input on SDIN. The PWM outputs are derived from SDIN. The TAS5729MD DAP accepts serial data in 16-, 20-, or 24-bit left-justified, right-justified, or $I^2S$ serial data format.

### PWM Section

The TAS5729MD DAP device uses noise-shaping and sophisticated nonlinear correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The DAP uses a fourth-order noise shaper to increase dynamic range and SNR in the audio band. The PWM section accepts 24-bit PCM data from the DAP and outputs two BTL PWM audio output channels.

The PWM section has internal dc-blocking filters that can be enabled and disabled using SYSTEM CONTROL REGISTER 1. The controls for the DC-Blocking filters are ganged together and enabling or disabling will affect both channels simultaneously. The filter cutoff frequency is less than 1 Hz. Individual-channel de-emphasis filters for 44.1- and 48-kHz are included and can be enabled and disabled.

Finally, the PWM section has an adjustable maximum modulation limit of 93.8% to 99.2%.

## I²C COMPATIBLE SERIAL CONTROL INTERFACE

The TAS5729MD DAP has an I²C serial control slave interface to receive commands from a system controller. The serial control interface supports both normal-speed (100-kHz) and high-speed (400-kHz) operations without wait states. As an added feature, this interface operates even if MCLK is absent.

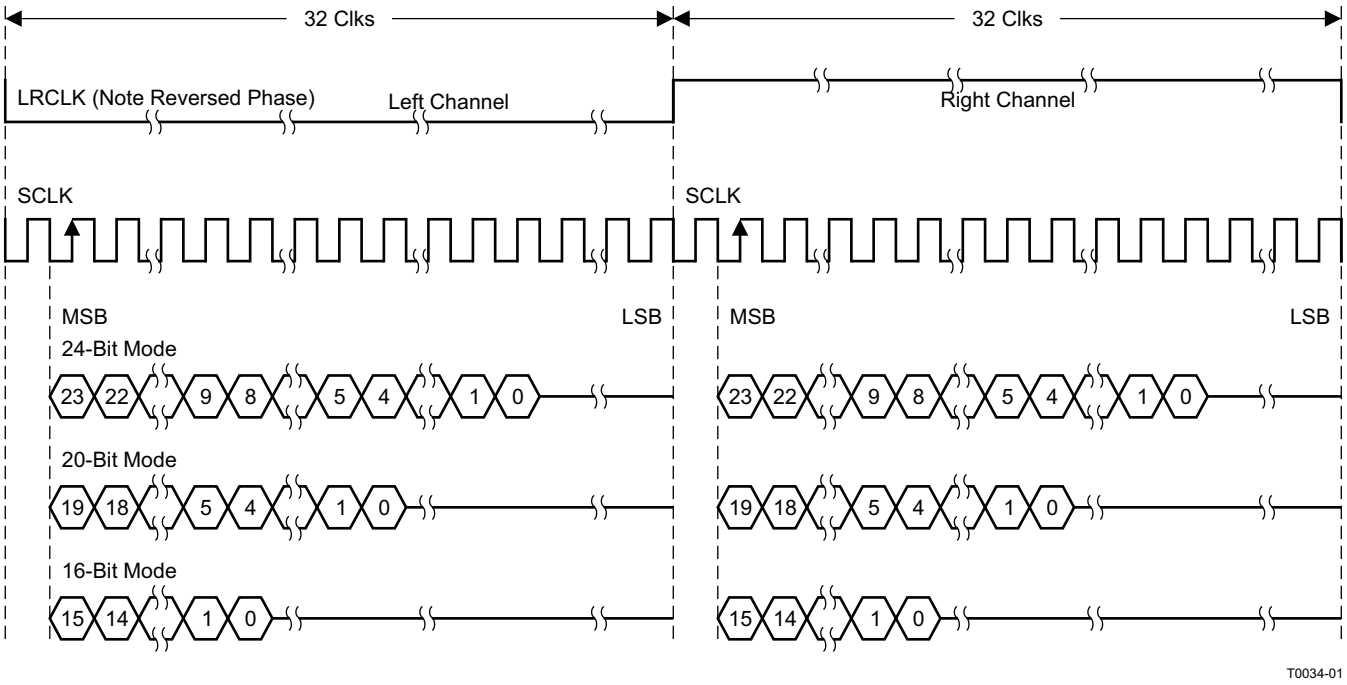
The serial control interface supports both single-byte and multiple-byte read and write operations for status registers and the general control registers associated with the PWM.

## SERIAL INTERFACE CONTROL AND TIMING

### I²S Timing

I²S timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is low for the left channel and high for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written msB-first and is valid on the rising edge of bit clock. The DAP masks unused trailing data-bit positions.

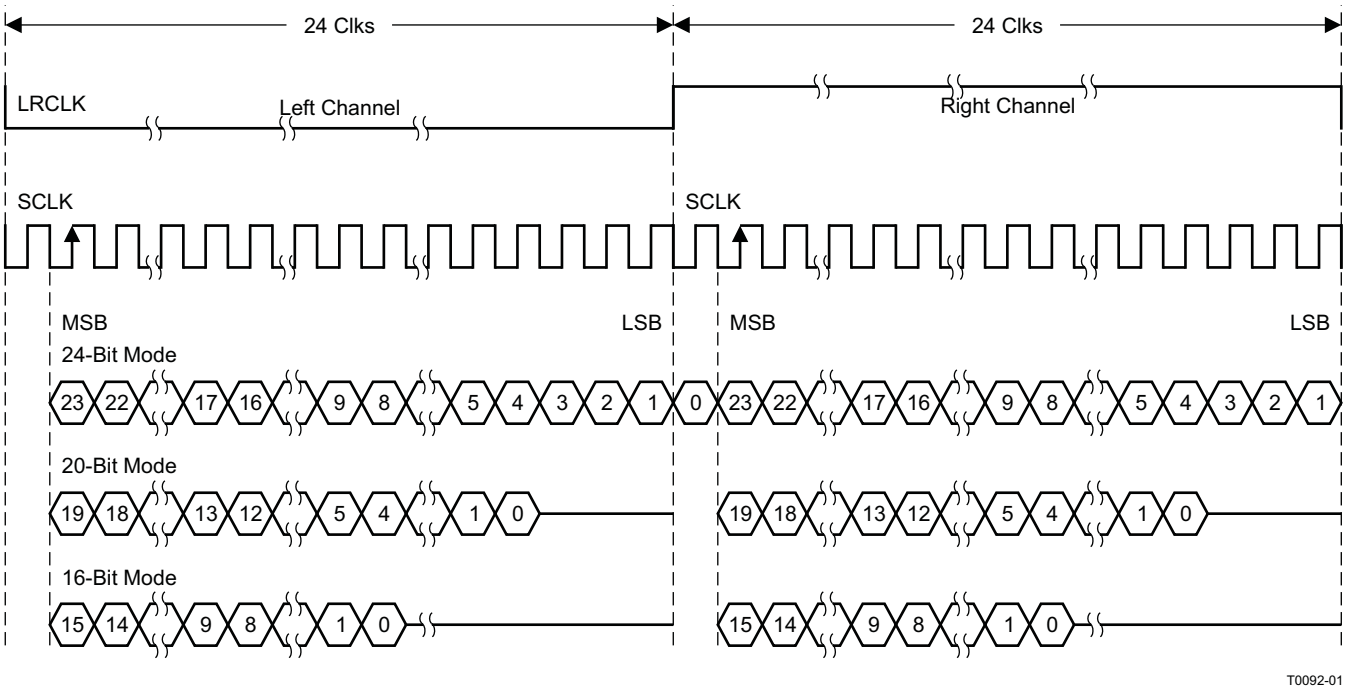
2-Channel $I^2S$ (Philips Format) Stereo Input




NOTE: All data presented in 2s-complement form with msB first.

**Figure 31. I²S 64-$f_S$ Format**

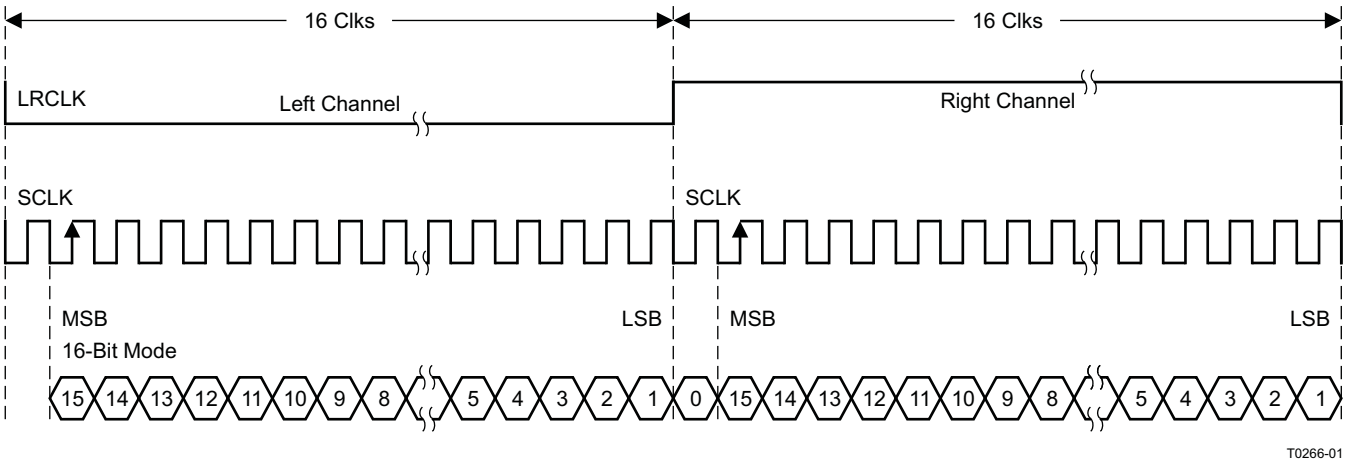
2-Channel I²S (Philips Format) Stereo Input/Output (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with msB first.

**Figure 32. I²S 48-$f_S$ Format**

2-Channel I²S (Philips Format) Stereo Input



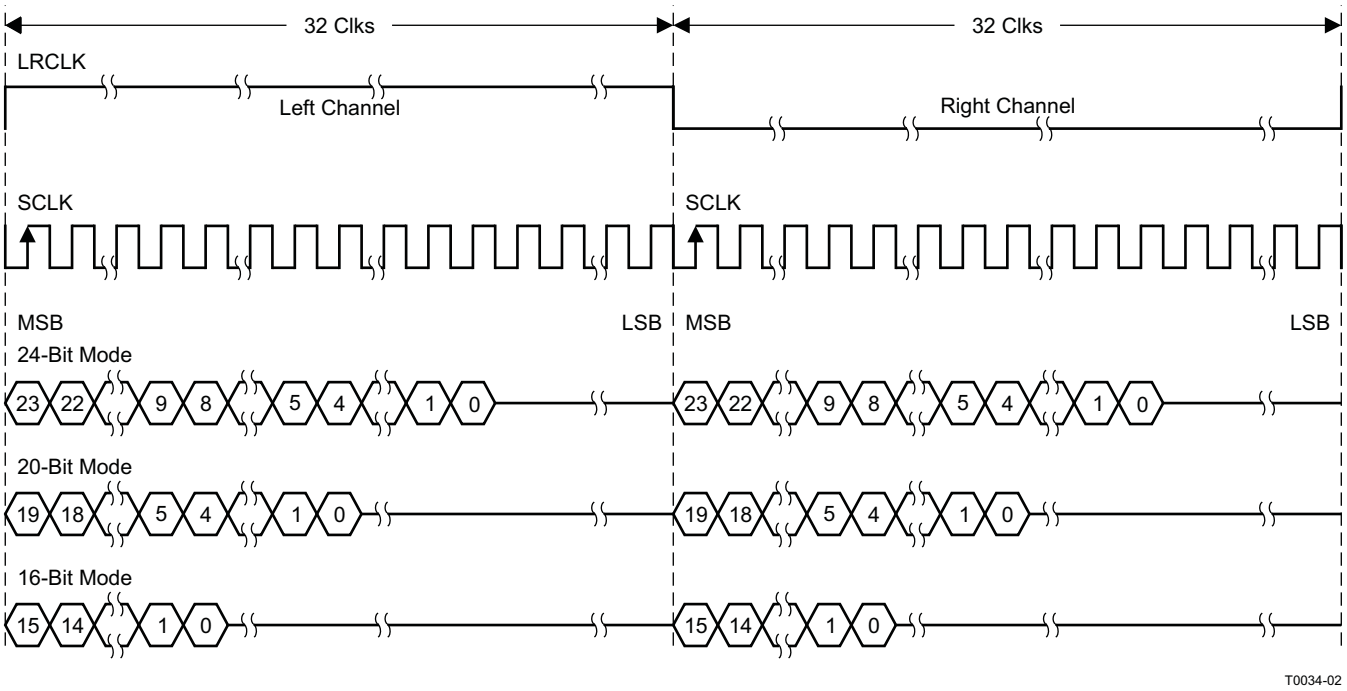

NOTE: All data presented in 2s-complement form with msB first.

**Figure 33. I²S 32-$f_S$ Format**

### Left-Justified

Left-justified (LJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data lines at the same time LRCLK toggles. The data is written msB-first and is valid on the rising edge of the bit clock. The DAP masks unused trailing data-bit positions.

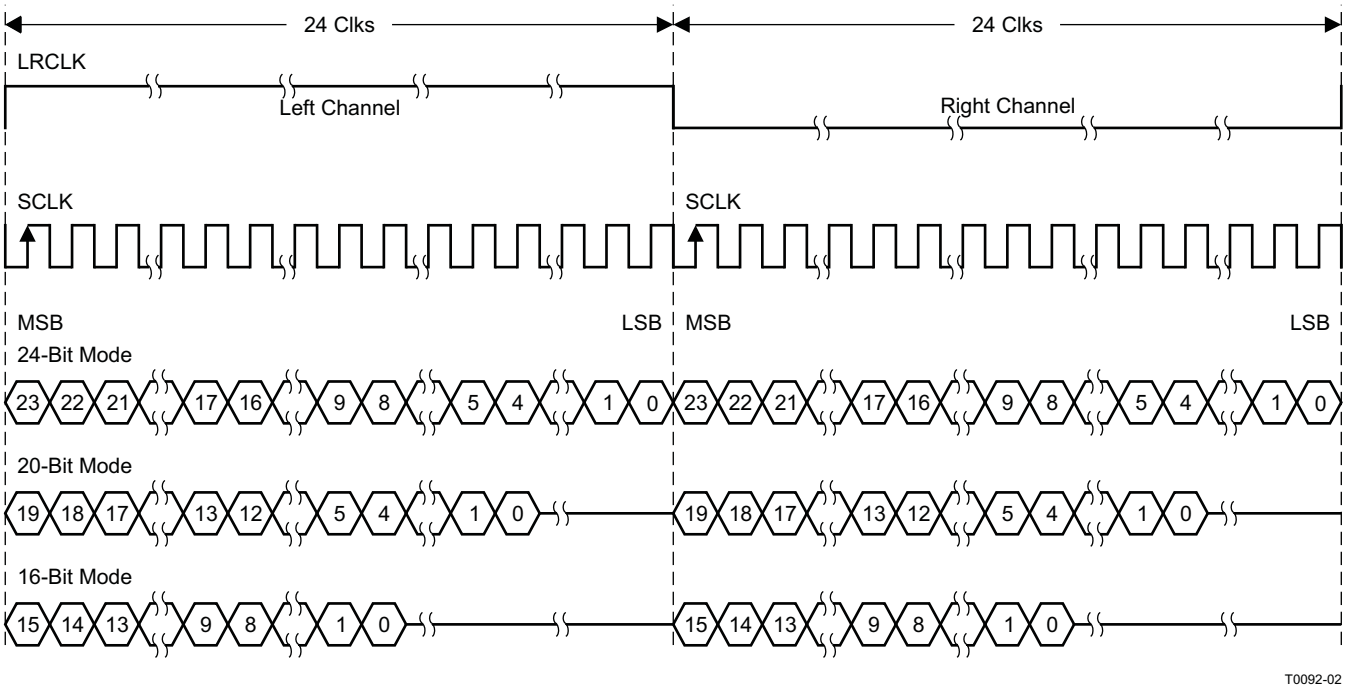
2-Channel Left-Justified Stereo Input




NOTE: All data presented in 2s-complement form with msB first.

**Figure 34. Left-Justified 64-$f_S$ Format**

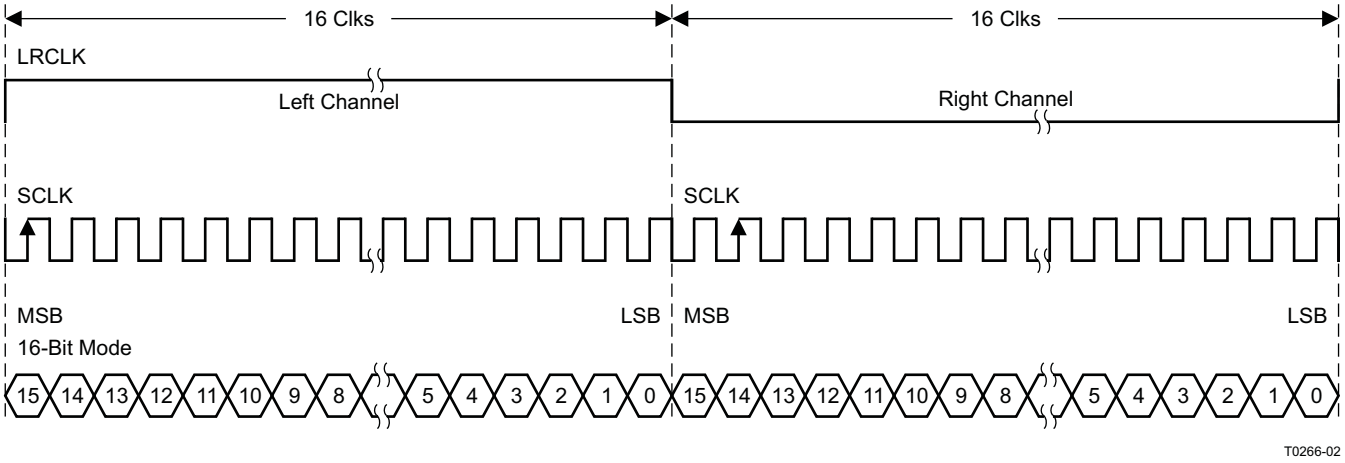
2-Channel Left-Justified Stereo Input (24-Bit Transfer Word Size)




NOTE: All data presented in 2s-complement form with msB first.

**Figure 35. Left-Justified 48-$f_S$ Format**

2-Channel Left-Justified Stereo Input




NOTE: All data presented in 2s-complement form with msB first.

**Figure 36. Left-Justified 32-$f_S$ Format**

### Right-Justified

Right-justified (RJ) timing uses LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCLK is high for the left channel and low for the right channel. A bit clock running at 32, 48, or 64 × $f_S$ is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCLK transitions. The data is written msB-first and is valid on the rising edge of bit clock. The DAP masks unused leading data-bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input

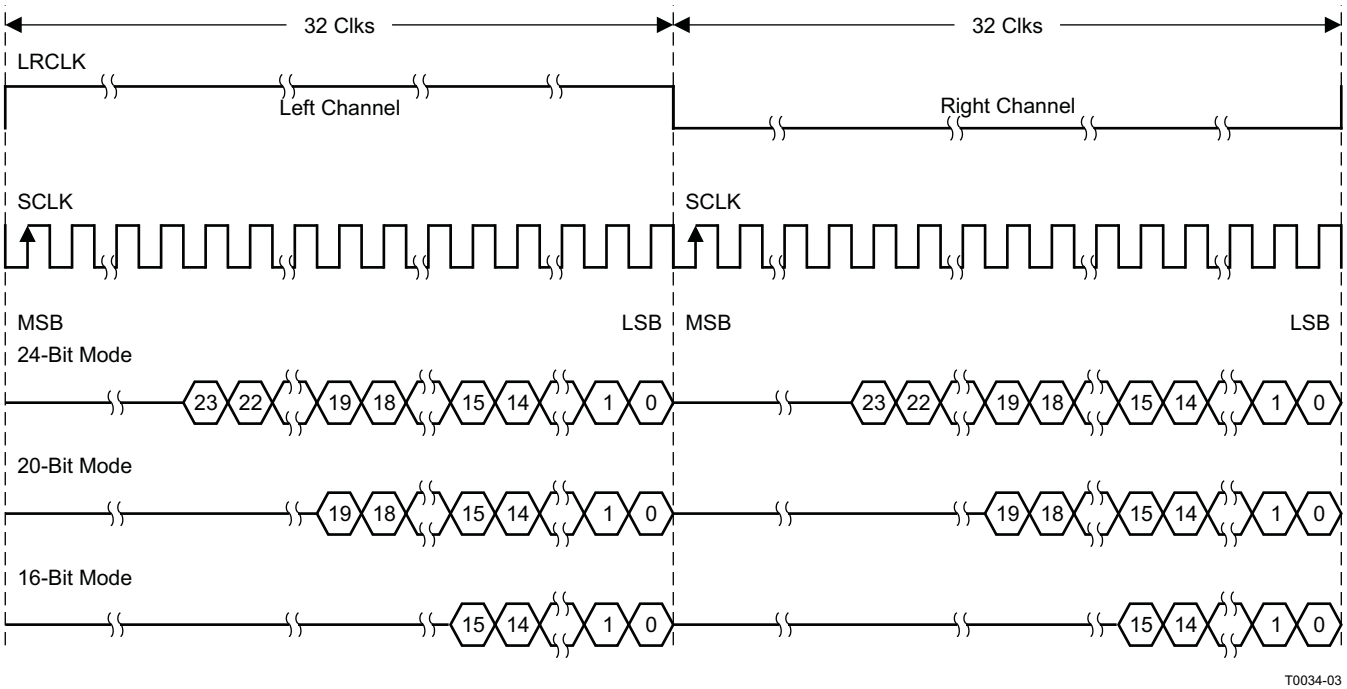



**Figure 37. Right-Justified 64-$f_S$ Format**

2-Channel Right-Justified Stereo Input (24-Bit Transfer Word Size)

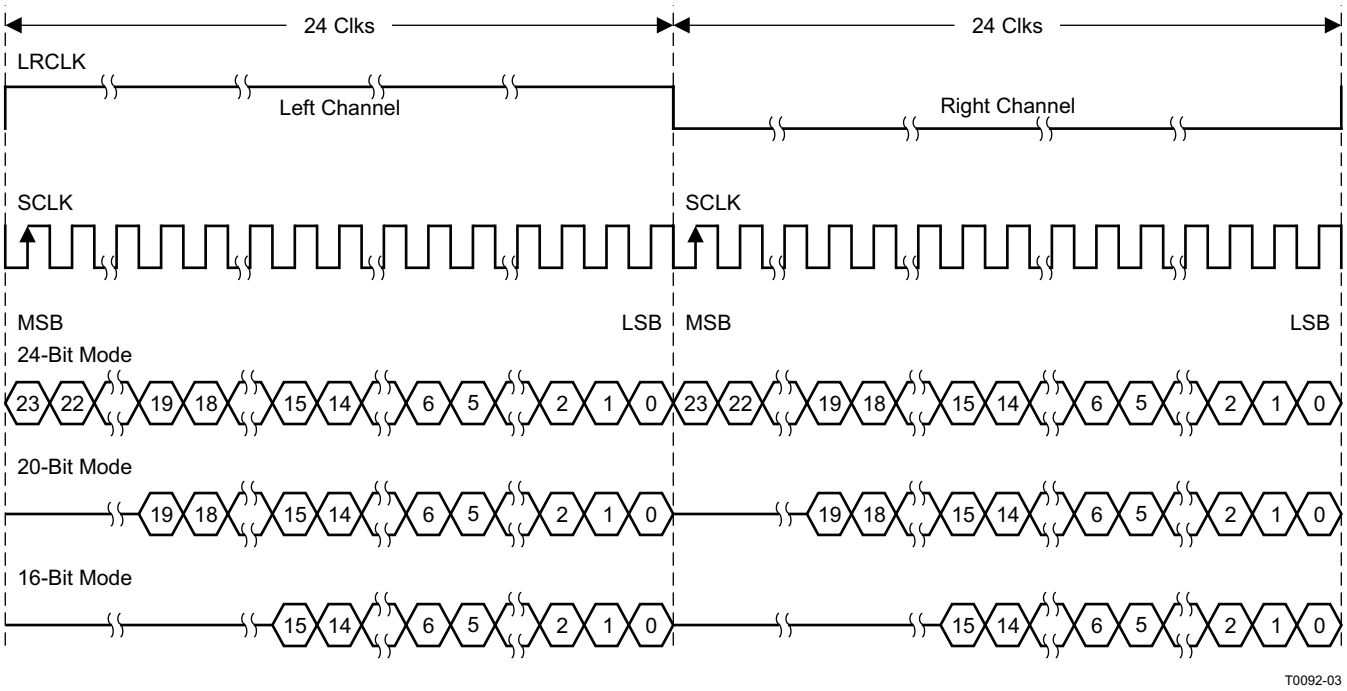



**Figure 38. Right-Justified 48-$f_S$ Format**

2-Channel Right-Justified (Sony Format) Stereo Input

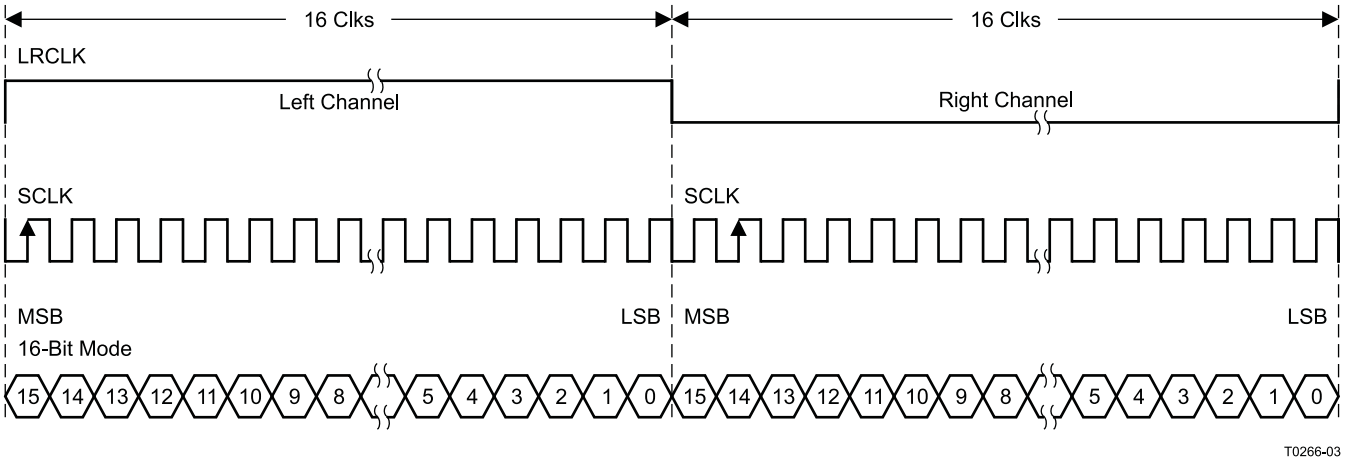



**Figure 39. Right-Justified 32-$f_S$ Format**

## I²C SERIAL CONTROL INTERFACE

The TAS5729MD DAP has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates for single- and multiple-byte write and read operations. This is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The DAP supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The DAP performs all I²C operations without I²C wait cycles.

### General I²C Operation

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (msB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 40. The master generates the 7-bit slave address and the read/write (R/$\overline{W}$) bit to open communication with another device and then waits for an acknowledge condition. The TAS5729MD holds SDA low during the acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/$\overline{W}$ bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

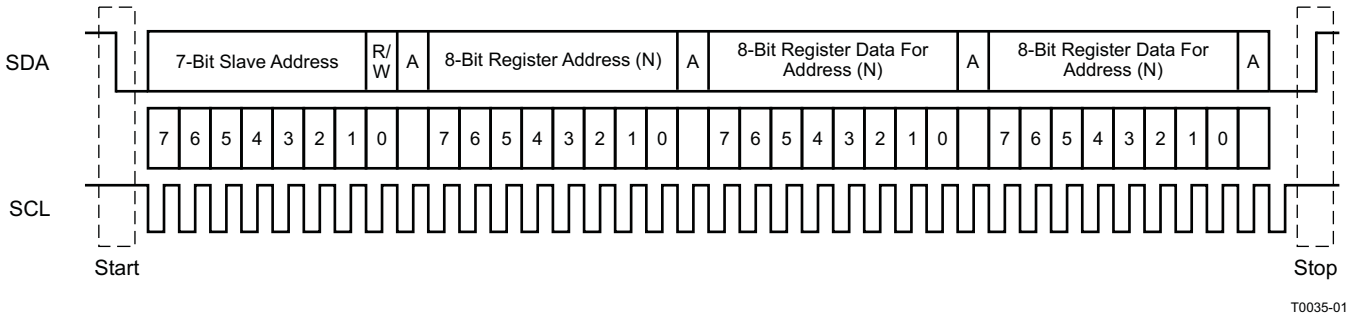



**Figure 40. Typical I²C Sequence**

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 40.

### Single- and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for subaddresses 0x00 to 0x1F. However, for the subaddresses 0x20 to 0xFF, the serial control interface supports only multiple-byte read/write operations (in multiples of 4 bytes).

During multiple-byte read operations, the DAP responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple-byte write operations, the DAP compares the number of bytes transmitted to the number of bytes that are required for each specific subaddress. For example, if a write command is received for a biquad subaddress, the DAP expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5729MD also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the 15 subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5729MD. For I²C sequential write transactions, the subaddress then serves as the start address, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; only the incomplete data is discarded.

### Single-Byte Write

As shown in Figure 41, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a data-write transfer, the read/write bit is 0. After receiving the correct I²C device address and the read/write bit, the DAP responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5729MD internal memory address being accessed. After receiving the address byte, the TAS5729MD again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5729MD again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

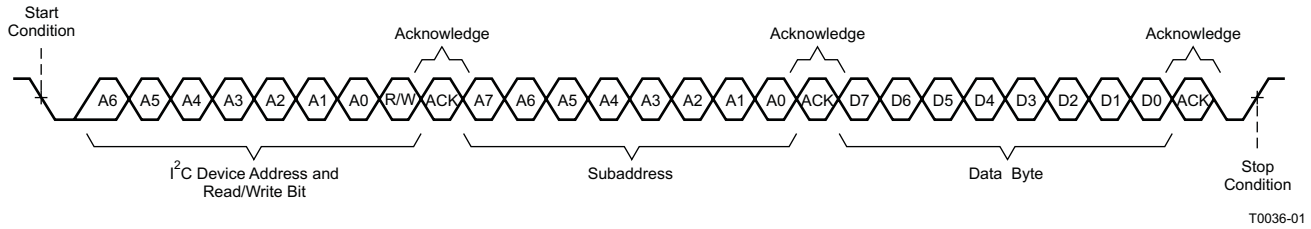



**Figure 41. Single-Byte Write Transfer**

### Multiple-Byte Write

A multiple-byte data-write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the DAP as shown in Figure 42. After receiving each data byte, the TAS5729MD responds with an acknowledge bit.

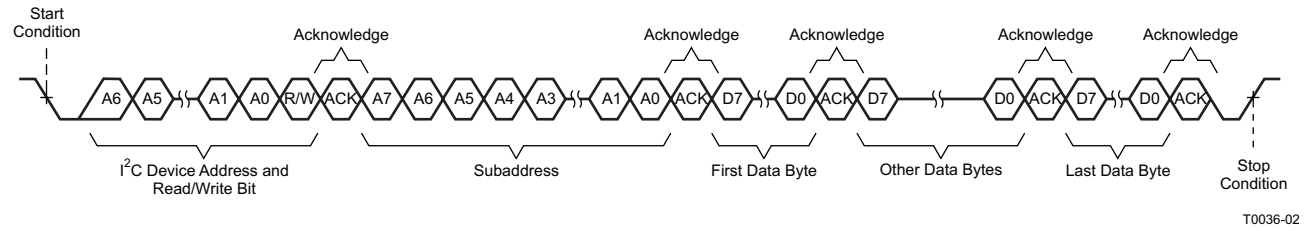



**Figure 42. Multiple-Byte Write Transfer**

### Single-Byte Read

As shown in Figure 43, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit becomes a 0. After receiving the TAS5729MD address and the read/write bit, TAS5729MD responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5729MD address and the read/write bit again. This time the read/write bit becomes a 1, indicating a read transfer. After receiving the address and the read/write bit, the TAS5729MD again responds with an acknowledge bit. Next, the TAS5729MD transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

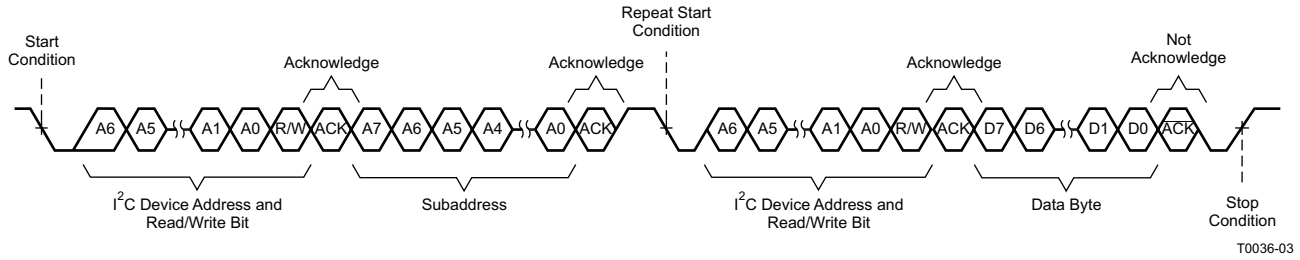



**Figure 43. Single-Byte Read Transfer**

### Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS5729MD to the master device as shown in Figure 44. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

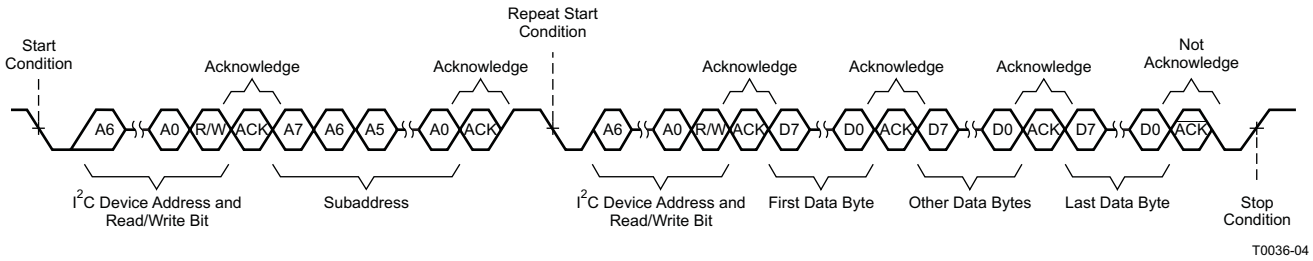
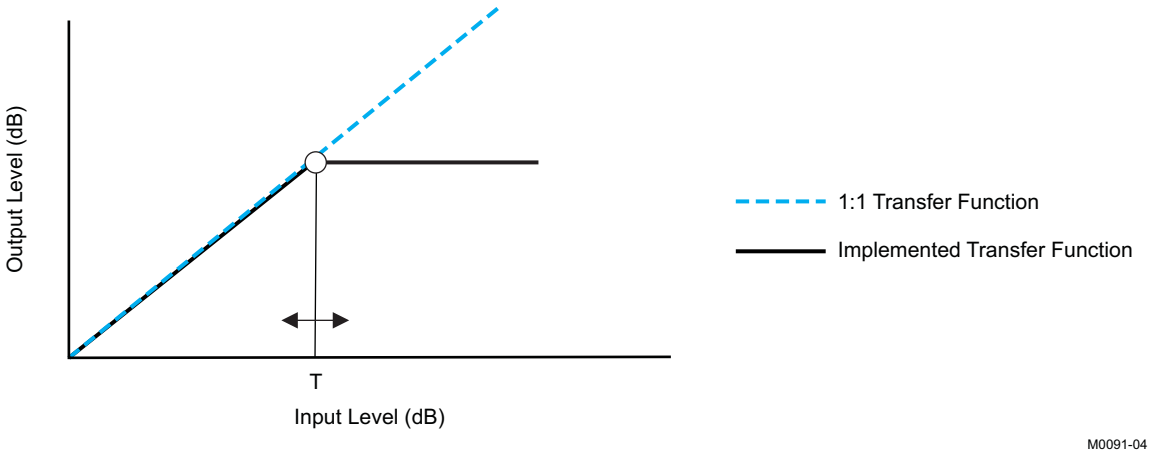



**Figure 44. Multiple-Byte Read Transfer**

## Automatic Gain Limiting (AGL)

The AGL scheme has two AGL blocks. There is one ganged AGL for the high-band left/right channels and one AGL for the low-band left/right channels.

The AGL input/output diagram is shown in Figure 45.

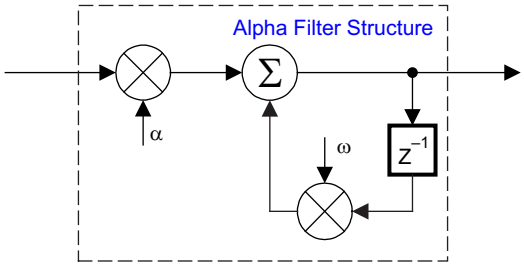



Professional-quality dynamic range compression automatically adjusts volume to flatten volume level.

- Each AGL has adjustable threshold levels.
- Programmable attack and release rate
- *Transparent compression*: compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

**Figure 45. Automatic Gain Limiting**

| | α, ω | T | $\alpha_a$, $\omega_a$ / $\alpha_d$, $\varphi_d$ |
|---|---|---|---|
| AGL1 | 0x3B | 0x40 | 0x3C |
| AGL2 | 0x3E | 0x43 | 0x3F |




T = 9.23 format, all other AGL coefficients are 3.23 format

**Figure 46. AGL Structure**

## PWM LEVEL METER

The structure in Figure 47 shows the PWM level meter that can be used to study the power profile.

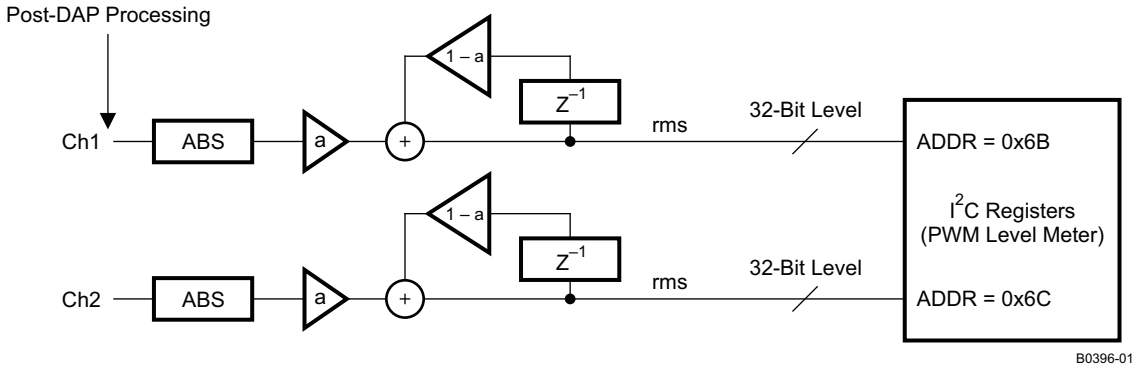



**Figure 47. PWM Level Meter Structure**

## 26-Bit 3.23 Number Format

All mixer gain coefficients are 26-bit coefficients using a 3.23 number format. Numbers formatted as 3.23 numbers means that there are 3 bits to the left of the binary point and 23 bits to the right of the binary point. This is shown in Figure 48 .

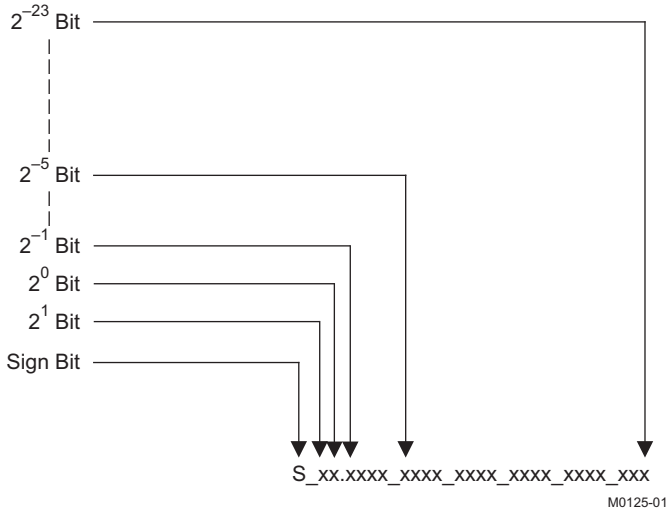



**Figure 48. 3.23 Format**

The decimal value of a 3.23 format number can be found by following the weighting shown in Figure 48. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 49 applied to obtain the magnitude of the negative number.

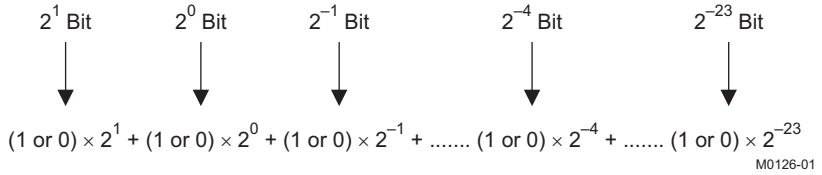



**Figure 49. Conversion Weighting Factors—3.23 Format to Floating Point**

Gain coefficients, entered via the I²C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 50

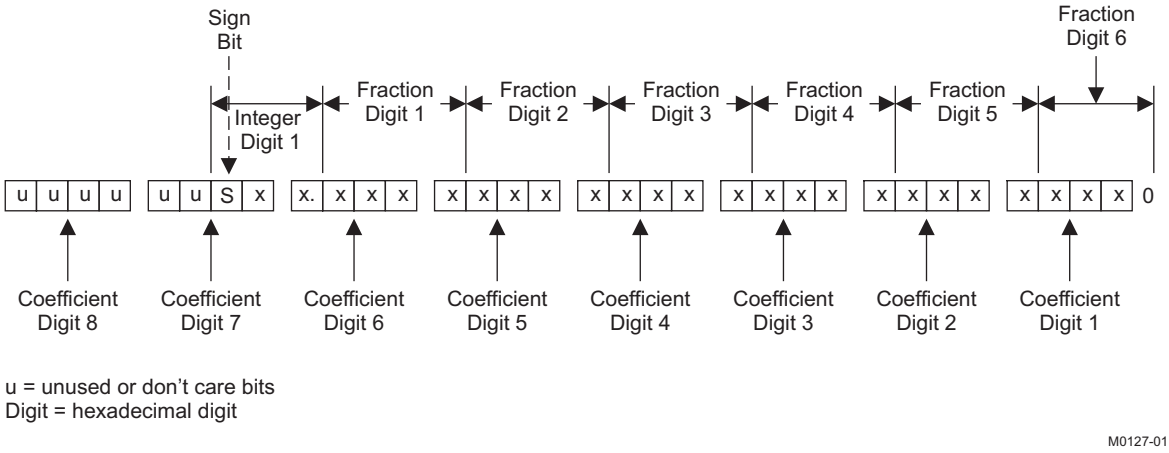



**Figure 50. Alignment of 3.23 Coefficient in 32-Bit I²C Word**

**Table 2. Sample Calculation for 3.23 Format**

| dB | Linear | Decimal | Hex (3.23 Format) |
|---|---|---|---|
| 0 | 1 | 8,388,608 | 80 0000 |
| 5 | 1.77 | 14,917,288 | 00E3 9EA8 |
| –5 | 0.56 | 4,717,260 | 0047 FACC |
| X | $L = 10^{(X/20)}$ | D = 8388608 × L | H = dec2hex (D, 8) |

**Table 3. Sample Calculation for 9.17 Format**

| dB | Linear | Decimal | Hex (9.17 Format) |
|---|---|---|---|
| 0 | 1 | 131,072 | 20 000 |
| 5 | 1.77 | 231,997 | 38 A3D |
| –5 | 0.56 | 73,400 | 11 EB8 |
| X | $L = 10^{(X/20)}$ | D = 131,072 × L | H = dec2hex (D, 8) |

## Control Port Detailed Register Description

**Table 4. Serial Control Interface Register Summary**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | DEFAULT VALUE |
|---|---|---|---|---|
| | | | A u indicates unused bits. | |
| 0x00 | Clock control register | 1 | Description shown in subsequent section | 0x6C |
| 0x01 | Device ID register | 1 | Description shown in subsequent section | 0xC1 |
| 0x02 | Error status register | 1 | Description shown in subsequent section | 0x00 |
| 0x03 | System control register 1 | 1 | Description shown in subsequent section | 0xA0 |
| 0x04 | Serial data interface register | 1 | Description shown in subsequent section | 0x05 |
| 0x05 | System control register 2 | 1 | Description shown in subsequent section | 0x40 |
| 0x06 | Soft mute register | 1 | Description shown in subsequent section | 0x00 |
| 0x07 | Master volume | 2 | Description shown in subsequent section | 0x03FF (mute) |
| 0x08 | Channel 1 vol | 2 | Description shown in subsequent section | 0x00C0 (0 dB) |
| 0x09 | Channel 2 vol | 2 | Description shown in subsequent section | 0x00C0 (0 dB) |
| 0x0A | Channel 3 vol | 2 | Description shown in subsequent section | 0x00C0 (0 dB) |
| 0x0B–0x0D | | 1 | Reserved(1) | |
| 0x0E | Volume configuration register | 1 | Description shown in subsequent section | 0xF0 |
| 0x0F | | 1 | Reserved(1) | |
| 0x10 | Modulation limit register | 1 | Description shown in subsequent section | 0x01 |
| 0x11 | IC delay channel 1 | 1 | Description shown in subsequent section | 0xAC |
| 0x12 | IC delay channel 2 | 1 | Description shown in subsequent section | 0x54 |
| 0x13 | IC delay channel 3 | 1 | Description shown in subsequent section | 0xAC |
| 0x14 | IC delay channel 4 | 1 | Description shown in subsequent section | 0x54 |
| 0x15–0x18 | | 1 | Reserved(1) | |
| 0x19 | PWM Shutdown Group Register | 1 | Description shown in subsequent section | 0x30 |
| 0x1A | Start/stop period register | 1 | | 0x68 |
| 0x1B | Oscillator trim register | 1 | | 0x82 |
| 0x1C | BKND_ERR register | 1 | | 0x57 |
| 0x1D–0x1F | | 1 | Reserved(1) | |
| 0x20 | Input MUX register | 4 | Description shown in subsequent section | 0x0001 7772 |
| 0x21 | Ch 4 source select register | 4 | Description shown in subsequent section | 0x0000 4303 |
| 0x22–0x24 | | 4 | Reserved(1) | |
| 0x25 | PWM MUX register | 4 | Description shown in subsequent section | 0x0102 1345 |
| 0x26 | ch1_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x27 | ch1_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x28 | ch1_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

(1) Reserved registers should not be accessed.

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | DEFAULT VALUE |
|---|---|---|---|---|
| 0x29 | ch1_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2A | ch1_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2B | ch1_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2C | ch1_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2D | ch1_bq[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2E | ch1_bq[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x2F | ch1_bq[9] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x30 | ch2_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x31 | ch2_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | DEFAULT VALUE |
|---|---|---|---|---|
| 0x32 | ch2_bq[2] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x33 | ch2_bq[3] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x34 | ch2_bq[4] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x35 | ch2_bq[5] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x36 | ch2_bq[6] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x37 | ch2_bq[7] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x38 | ch2_bq[8] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x39 | ch2_bq[9] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x3A | | 4 | Reserved(2) | |
| 0x3B | AGL1 softening filter alpha | 8 | u[31:26], ae[25:0] | 0x0008 0000 |
| | AGL1 softening filter omega | | u[31:26], oe[25:0] | 0x0078 0000 |
| 0x3C | AGL1 attack rate | 8 | | 0x0000 0100 |
| | AGL1 release rate | | | 0xFFFF FF00 |

(2) Reserved registers should not be accessed.

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | DEFAULT VALUE |
|---|---|---|---|---|
| 0x3D | | 8 | Reserved(3) | |
| 0x3E | AGL2 softening filter alpha | 8 | u[31:26], ae[25:0] | 0x0008 0000 |
| | AGL2 softening filter omega | | u[31:26], oe[25:0] | 0x0078 0000 |
| 0x3F | AGL2 attack rate | 8 | u[31:26], at[25:0] | 0x0008 0000 |
| | AGL2 release rate | | u[31:26], rt[25:0] | 0xFFF8 0000 |
| 0x40 | AGL1 attack threshold | 4 | T1[31:0] (9.23 format) | 0x0800 0000 |
| 0x41–0x42 | | 4 | Reserved(3) | |
| 0x43 | AGL2 attack threshold | 4 | T2[31:0] (9.23 format) | 0x0074 0000 |
| 0x44–0x45 | | 4 | Reserved(3) | |
| 0x46 | AGL control | 4 | Description shown in subsequent section | 0x0002 0000 |
| 0x47–0x4E | | 4 | Reserved(3) | |
| 0x4F | PWM switching rate control | 4 | u[31:4], src[3:0] | 0x0000 0008 |
| 0x50 | EQ control | 4 | Description shown in subsequent section | 0x0F70 8000 |
| 0x51 | Ch 1 output mixer | 8 | Ch 1 output mix1[1] | 0x0080 0000 |
| | | | Ch 1 output mix1[0] | 0x0000 0000 |
| 0x52 | Ch 2 output mixer | 8 | Ch 2 output mix2[1] | 0x0080 0000 |
| | | | Ch 2 output mix2[0] | 0x0000 0000 |
| 0x53 | | 16 | Reserved(3) | |
| 0x54 | | 16 | Reserved(3) | |
| 0x56 | Output post-scale | 4 | u[31:26], post[25:0] | 0x0080 0000 |
| 0x57 | Output pre-scale | 4 | u[31:26], pre[25:0] (9.17 format) | 0x0002 0000 |
| 0x58 | ch1_bq[10] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x59 | ch1_bq[11] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5A | ch4_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5B | ch4_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |

(3) Reserved registers should not be accessed.

**Table 4. Serial Control Interface Register Summary (continued)**

| SUBADDRESS | REGISTER NAME | NO. OF BYTES | CONTENTS | DEFAULT VALUE |
|---|---|---|---|---|
| 0x5C | ch2_bq[10] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5D | ch2_bq[11] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5E | ch3_bq[0] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x5F | ch3_bq[1] | 20 | u[31:26], b0[25:0] | 0x0080 0000 |
| | | | u[31:26], b1[25:0] | 0x0000 0000 |
| | | | u[31:26], b2[25:0] | 0x0000 0000 |
| | | | u[31:26], a1[25:0] | 0x0000 0000 |
| | | | u[31:26], a2[25:0] | 0x0000 0000 |
| 0x60–0x61 | | 4 | Reserved(4) | |
| 0x62 | IDF post scale | 4 | | 0x0000 0080 |
| 0x63–0x6A | | | Reserved(4) | |
| 0x6B | Left channel PWM level meter | 4 | Data[31:0] | 0x0000 0000 |
| 0x6C | Right channel PWM level meter | 4 | Data[31:0] | 0x0000 0000 |
| 0x6D–0x6F | | | Reserved(4) | |
| 0x70 | ch1 inline mixer | 4 | u[31:26], in_mix1[25:0] | 0x0080 0000 |
| 0x71 | inline_AGL_en_mixer_ch1 | 4 | u[31:26], in_mixAGL_1[25:0] | 0x0000 0000 |
| 0x72 | ch1 right_channel mixer | 4 | u[31:26], right_mix1[25:0] | 0x0000 0000 |
| 0x73 | ch1 left_channel_mixer | 4 | u[31:26], left_mix_1[25:0] | 0x0080 0000 |
| 0x74 | ch2 inline mixer | 4 | u[31:26], in_mix2[25:0] | 0x0080 0000 |
| 0x75 | inline_AGL_en_mixer_ch2 | 4 | u[31:26], in_mixAGL_2[25:0] | 0x0000 0000 |
| 0x76 | ch2 left_chanel mixer | 4 | u[31:26], left_mix1[25:0] | 0x0000 0000 |
| 0x77 | ch2 right_channel_mixer | 4 | u[31:26], right_mix_1[25:0] | 0x0080 0000 |
| 0x78–0xF7 | | | Reserved(4) | |
| 0xF8 | Update dev address key | 4 | Dev Id Update Key[31:0] (Key = 0xF9A5A5A5) | 0x0000 0000 |
| 0xF9 | Update dev address reg | 4 | u[31:8],New Dev Id[7:0] (New Dev Id = 0x38 for TAS5729MD) | 0x0000 0056 |
| 0xFA–0xFF | | 4 | Reserved(4) | |

(4) Reserved registers should not be accessed.

All DAP coefficients are 3.23 format unless specified otherwise.

Registers 0x3B through 0x46 should be altered only during the initialization phase.

## CLOCK CONTROL REGISTER (0x00)

The clocks and data rates are automatically determined by the TAS5729MD. The clock control register contains the autodetected clock status. Bits D7–D5 reflect the sample rate. Bits D4–D2 reflect the MCLK frequency.

**Table 5. Clock Control Register (0x00)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | – | – | – | – | – | $f_S$ = 32-kHz sample rate |
| 0 | 0 | 1 | – | – | – | – | – | Reserved |
| 0 | 1 | 0 | – | – | – | – | – | Reserved |
| **0** | **1** | **1** | **–** | **–** | **–** | **–** | **–** | **$f_S$ = 44.1/48-kHz sample rate**(1) |
| 1 | 0 | 0 | – | – | – | – | – | $f_S$ = 16-kHz sample rate |
| 1 | 0 | 1 | – | – | – | – | – | $f_S$ = 22.05/24-kHz sample rate |
| 1 | 1 | 0 | – | – | – | – | – | $f_S$ = 8-kHz sample rate |
| 1 | 1 | 1 | – | – | – | – | – | $f_S$ = 11.025/12-kHz sample rate |
| – | – | – | 0 | 0 | 0 | – | – | MCLK frequency = 64 × $f_S$(2) |
| – | – | – | 0 | 0 | 1 | – | – | MCLK frequency = 128 × $f_S$(2) |
| – | – | – | 0 | 1 | 0 | – | – | MCLK frequency = 192 × $f_S$(3) |
| **–** | **–** | **–** | **0** | **1** | **1** | **–** | **–** | **MCLK frequency = 256 × $f_S$** (1)(4) |
| – | – | – | 1 | 0 | 0 | – | – | MCLK frequency = 384 × $f_S$ |
| – | – | – | 1 | 0 | 1 | – | – | MCLK frequency = 512 × $f_S$ |
| – | – | – | 1 | 1 | 0 | – | – | Reserved |
| – | – | – | 1 | 1 | 1 | – | – | Reserved |
| **–** | – | – | – | – | – | **0** | – | **Reserved**(1) |
| **–** | **–** | **–** | – | **–** | **–** | **–** | **0** | **Reserved**(1) |

(1) Default values are in **bold**.
(2) Only available for 44.1-kHz and 48-kHz rates
(3) Rate only available for 32/44.1/48-KHz sample rates
(4) Not available at 8 kHz

## DEVICE ID REGISTER (0x01)

The device ID register contains the ID code for the firmware revision.

**Table 6. General Status Register (0x01)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | **1** | 0 | 0 | 0 | 0 | 0 | **1** | **Identification code**(1) |

(1) Default values are in **bold**.

## ERROR STATUS REGISTER (0x02)

The error bits are sticky and are not cleared by the hardware. This means that the software must clear the register (write zeroes) and then read them to determine if they are persistent errors.

Error definitions:

- MCLK error: MCLK frequency is changing. The number of MCLKs per LRCLK is changing.
- SCLK error: The number of SCLKs per LRCLK is changing.
- LRCLK error: LRCLK frequency is changing.
- Frame slip: LRCLK phase is drifting with respect to internal frame sync.

**Table 7. Error Status Register (0x02)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 1 | – | – | – | – | – | – | – | MCLK error |
| – | 1 | – | – | – | – | – | – | PLL autolock error |
| – | – | 1 | – | – | – | – | – | SCLK error |
| – | – | – | 1 | – | – | – | – | LRCLK error |
| – | – | – | – | 1 | – | – | – | Frame slip |
| – | – | – | – | – | 1 | – | – | Clip indicator |
| – | – | – | – | – | – | 1 | – | Overcurrent, overtemperature, overvoltage, or Undervoltage error |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reserved |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **No errors** (1) |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 1 (0x03)

System control register 1 has several functions:

Bit D7: If 0, the dc-blocking filter for each channel is disabled.
If 1, the dc-blocking filter (–3 dB cutoff <1 Hz) for each channel is enabled.

Bit D5: If 0, use soft unmute on recovery from a clock error. This is a slow recovery. Unmute takes the same time as the volume ramp defined in register 0x0E.
If 1, use hard unmute on recovery from clock error. This is a fast recovery, a single-step volume ramp.

Bits D1–D0: Select de-emphasis

**Table 8. System Control Register 1 (0x03)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | – | – | – | – | – | – | – | PWM high-pass (dc blocking) disabled |
| **1** | – | – | – | – | – | – | – | **PWM high-pass (dc blocking) enabled** (1) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **0** | – | – | – | – | – | **Soft unmute on recovery from clock error or exit all channel shutdown.**(1) |
| – | – | 1 | – | – | – | – | – | Hard unmute on recovery from clock error or exit all channel shutdown. |
| – | – | – | **0** | – | – | – | – | **Reserved**(1) |
| – | – | – | – | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | **0** | **0** | **No de-emphasis**(1) |
| – | – | – | – | – | – | 0 | 1 | De-emphasis for $f_S$ = 32 kHz |
| – | – | – | – | – | – | 1 | 0 | De-emphasis for $f_S$ = 44.1 kHz |
| – | – | – | – | – | – | 1 | 1 | De-emphasis for $f_S$ = 48 kHz |

(1) Default values are in **bold**.

## SERIAL DATA INTERFACE REGISTER (0x04)

As shown in Table 9, the TAS5729MD supports nine serial data modes. The default is 24-bit, I²S mode.

**Table 9. Serial Data Interface Control Register (0x04) Format**

| RECEIVE SERIAL DATA INTERFACE FORMAT | WORD LENGTH | D7–D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|
| Right-justified | 16 | 0000 | 0 | 0 | 0 | 0 |
| Right-justified | 20 | 0000 | 0 | 0 | 0 | 1 |
| Right-justified | 24 | 0000 | 0 | 0 | 1 | 0 |
| I²S | 16 | 000 | 0 | 0 | 1 | 1 |
| I²S | 20 | 0000 | 0 | 1 | 0 | 0 |
| **I²S**(1) | **24** | **0000** | **0** | **1** | **0** | **1** |
| Left-justified | 16 | 0000 | 0 | 1 | 1 | 0 |
| Left-justified | 20 | 0000 | 0 | 1 | 1 | 1 |
| Left-justified | 24 | 0000 | 1 | 0 | 0 | 0 |
| Reserved | | 0000 | 1 | 0 | 0 | 1 |
| Reserved | | 0000 | 1 | 0 | 1 | 0 |
| Reserved | | 0000 | 1 | 0 | 1 | 1 |
| Reserved | | 0000 | 1 | 1 | 0 | 0 |
| Reserved | | 0000 | 1 | 1 | 0 | 1 |
| Reserved | | 0000 | 1 | 1 | 1 | 0 |
| Reserved | | 0000 | 1 | 1 | 1 | 1 |

(1) Default values are in **bold**.

## SYSTEM CONTROL REGISTER 2 (0x05)

When bit D6 is set low, the system exits all-channel shutdown and starts playing audio; otherwise, the outputs are shut down (hard mute).

**Table 10. System Control Register 2 (0x05)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | **–** | **–** | **–** | **–** | **–** | – | **Reserved**(1) |
| – | 0 | – | – | – | – | – | – | Exit all-channel shutdown (normal operation)(2) |
| – | **1** | – | – | – | – | – | – | **Enter all-channel shutdown (hard mute)(1)** |
| – | – | **0** | **--** | **–** | **–** | **–** | – | **Reserved** (1) |
| – | – | – | **0** | **–** | **–** | **–** | **–** | **Reserved** (1) |
| – | – | – | – | 1 | – | – | **–** | In speaker mode, a value of 1 means device is in ternary modulation. |
| – | – | – | – | **0** | – | – | **–** | **In speaker mode, a value of 0 means device is in not in ternary modulation (AD or BD as defined in register 0x25).** (1) |
| – | – | – | – | – | **0** | – | – | **Reserved** (1) |
| – | – | – | – | – | – | **0** | – | ADR/$\overline{\text{SPK\_FAULT}}$ configured as input for address select. |
| – | – | – | – | – | – | 1 | – | ADR/$\overline{\text{SPK\_FAULT}}$ configured as output for $\overline{\text{SPK\_FAULT}}$ |
| .– | – | – | – | – | – | – | **0** | **Reserved(1)** |

(1) Default values are in **bold**.
(2) When exiting all-channel shutdown, a soft or hard unmute is determined by register 0x03, bit 5.

## SOFT MUTE REGISTER (0x06)

Writing a 1 to any of the following bits sets the output of the respective channel to 50% duty cycle (soft mute).

**Table 11. Soft Mute Register (0x06)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | 1 | – | – | Soft mute channel 3 |
| – | – | – | – | – | **0** | – | – | **Soft unmute channel 3**(1) |
| – | – | – | – | – | – | 1 | – | Soft mute channel 2 |
| – | – | – | – | – | – | **0** | – | **Soft unmute channel 2**(1) |
| – | – | – | – | – | – | – | 1 | Soft mute channel 1 |
| – | – | – | – | – | – | – | **0** | **Soft unmute channel 1**(1) |

(1) Default values are in **bold**.

## VOLUME REGISTERS (0x07, 0x08, 0x09)

Step size is 0.125 dB and volume registers are 2 bytes.

| | |
|---|---|
| Master volume | – 0x07 (default is mute) |
| Channel-1 volume | – 0x08 (default is 0 dB) |
| Channel-2 volume | – 0x09 (default is 0 dB) |

Volume Range: +24dB to -103.75dB

Step-Size: 0.125dB

Formula:

Target Volume Level (dB) = 'V'

- Step-1: Calculate (24-V)/0.125
- Step-2: Convert calculated decimal value to 2-byte hexadecimal to get the register hex-value

Examples:

Target Volume = 12dB

- (24-12)/0.125 = 96
- Converting decimal value 96 to 2-byte hexadecimal gives x0060

Target Volume = 0dB

- (24-0)/0.125 = 192
- Converting decimal value 192 to 2-byte hexadecimal gives x00C0

Target Volume = -12dB

- (24-(-12)/0.125 = 36/0.125 = 288
- Converting decimal value 288 to 2-byte hexadecimal gives x0120

## VOLUME CONFIGURATION REGISTER (0x0E)

Bits D2–D0: Volume slew rate (used to control volume change and MUTE ramp rates). These bits control the number of steps in a volume ramp. Volume steps occur at a rate that depends on the sample rate of the I²S data as follows:

| Sample rate (kHz) | Approximate ramp rate |
|---|---|
| 8/16/32 | 125 µs/step |
| 11.025/22.05/44.1 | 90.7 µs/step |
| 12/24/48 | 83.3 µs/step |

**Table 12. Volume Configuration Register (0x0E)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | 1 | 1 | **1** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | **0** | **0** | **Volume slew 512 steps (43 ms volume ramp time at 48 kHz)**(1) |
| – | – | – | – | – | 0 | 0 | 1 | Volume slew 1024 steps (85-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 0 | 1 | 0 | Volume slew 2048 steps (171-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 0 | 1 | 1 | Volume slew 256 steps (21-ms volume ramp time at 48 kHz) |
| – | – | – | – | – | 1 | X | X | Reserved |

(1) Default values are in **bold**.

## MODULATION LIMIT REGISTER (0x10)

**Table 13. Modulation Limit Register (0x10)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | MODULATION LIMIT |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | – | – | – | Reserved |
| – | – | – | – | – | 0 | 0 | 0 | 99.2% |
| – | – | – | – | – | **0** | **0** | **1** | **98.4%** (1) |
| – | – | – | – | – | 0 | 1 | 0 | 97.7% |
| – | – | – | – | – | 0 | 1 | 1 | 96.9% |
| – | – | – | – | – | 1 | 0 | 0 | 96.1% |
| – | – | – | – | – | 1 | 0 | 1 | 95.3% |
| – | – | – | – | – | 1 | 1 | 0 | 94.5% |
| – | – | – | – | – | 1 | 1 | 1 | 93.8% |

(1) Default values are in **bold**.

## INTERCHANNEL DELAY REGISTERS (0x11, 0x12, 0x13, and 0x14)

Internal PWM channels 1, 2, $\overline{1}$, and $\overline{2}$ are mapped into registers 0x11, 0x12, 0x13, and 0x14.

**Table 14. Channel Interchannel Delay Register Format**

| BITS DEFINITION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | – | – | Minimum absolute delay, 0 DCLK cycles |
| | 0 | 1 | 1 | 1 | 1 | 1 | – | – | Maximum positive delay, 31 × 4 DCLK cycles |
| | 1 | 0 | 0 | 0 | 0 | 0 | – | – | Maximum negative delay, –32 × 4 DCLK cycles |
| | | | | | | | 0 | 0 | Reserved |
| **SUBADDRESS** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **Delay = (value) × 4 DCLKs** |
| **0x11** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for channel 1**(1) |
| **0x12** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for channel 2**(1) |
| **0x13** | **1** | **0** | **1** | **0** | **1** | **1** | – | – | **Default value for $\overline{\text{channel 1}}$**(1) |
| **0x14** | **0** | **1** | **0** | **1** | **0** | **1** | – | – | **Default value for $\overline{\text{channel 2}}$**(1) |

(1) Default values are in **bold**.

ICD settings have high impact on audio performance (e.g., dynamic range, THD, crosstalk, etc.) Therefore, appropriate ICD settings must be used. By default, the device has ICD settings for the AD mode. If used in BD mode, then update these registers before coming out of all-channel shutdown.

| MODE | AD MODE | BD MODE |
|---|---|---|
| 0x11 | AC | B8 |
| 0x12 | 54 | 60 |
| 0x13 | AC | A0 |
| 0x14 | 54 | 48 |

## PWM SHUTDOWN GROUP REGISTER (0x19)

Settings of this register determine which PWM channels are active. The value should be 0x30 for BTL mode and 0x3A for post-filter PBTL mode. The default value of this register is 0x30. The functionality of this register is tied to the state of bit D5 in the system control register.

This register defines which channels belong to the shutdown group (SDG). If a 1 is set in the shutdown group register, that particular channel is **not** started following an exit *out of all-channel shutdown* command (if bit D5 is set to 0 in system control register 2, 0x05).

**Table 15. PWM Shutdown Group Register (0x19)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | – | – | – | – | – | – | – | **Reserved**(1) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **1** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | **1** | – | – | – | – | **Reserved**(1) |
| – | – | – | – | **0** | – | – | – | **PWM channel 4 does not belong to shutdown group.**(1) |
| – | – | – | – | 1 | – | – | – | PWM channel 4 belongs to shutdown group. |
| – | – | – | – | – | **0** | – | – | **PWM channel 3 does not belong to shutdown group.**(1) |
| – | – | – | – | – | 1 | – | – | PWM channel 3 belongs to shutdown group. |
| – | – | – | – | – | – | **0** | – | **PWM channel 2 does not belong to shutdown group.**(1) |
| – | – | – | – | – | – | 1 | – | PWM channel 2 belongs to shutdown group. |
| – | – | – | – | – | – | – | **0** | **PWM channel 1 does not belong to shutdown group.**(1) |
| – | – | – | – | – | – | – | 1 | PWM channel 1 belongs to shutdown group. |

(1) Default values are in **bold**.

## START/STOP PERIOD REGISTER (0x1A)

This register is used to control the soft-start and soft-stop period following an enter/exit all-channel shutdown command or change in the PDN state. This helps reduce pops and clicks at start-up and shutdown. The times are only approximate and vary depending on device activity level and I²S clock stability.

**Table 16. Start/Stop Period Register (0x1A)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **–** | **–** | – | – | – | – | – | **SSTIMER enabled**(1) |
| 1 | – | – | – | – | – | – | – | SSTIMER disabled |
| – | **1** | **1** | – | – | – | – | – | **Reserved**(1) |
| – | – | – | 0 | 0 | – | – | – | No 50% duty cycle start/stop period |
| – | – | – | **0** | **1** | **0** | **0** | **0** | **16.5-ms 50% duty cycle start/stop period**(1) |
| – | – | – | 0 | 1 | 0 | 0 | 1 | 23.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 0 | 31.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 0 | 1 | 1 | 40.4-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 0 | 53.9-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 0 | 1 | 70.3-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 0 | 94.2-ms 50% duty cycle start/stop period |
| – | – | – | 0 | 1 | 1 | 1 | 1 | 125.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 0 | 164.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 0 | 1 | 239.4-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 0 | 314.2-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 0 | 1 | 1 | 403.9-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 0 | 538.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 0 | 1 | 703.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 0 | 942.5-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 0 | 1 | 1 | 1 | 1256.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 0 | 1728.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 0 | 1 | 2513.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 0 | 3299.1-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 0 | 1 | 1 | 4241.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 0 | 5655.6-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 0 | 1 | 7383.7-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 0 | 9897.3-ms 50% duty cycle start/stop period |
| – | – | – | 1 | 1 | 1 | 1 | 1 | 13,196.4-ms 50% duty cycle start/stop period |

(1) Default values are in **bold**.

## OSCILLATOR TRIM REGISTER (0x1B)

The TAS5729MD PWM processor contains an internal oscillator to support autodetect of I²S clock rates. This reduces system cost because an external reference is not required. Currently, TI recommends a reference resistor value of 18.2 kΩ (1%). This should be connected between OSC_RES and DVSSO.

Writing 0x00 to register 0x1B enables the trim that was programmed at the factory.

Note that trim must always be run following reset of the device.

**Table 17. Oscillator Trim Register (0x1B)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **1** | – | – | – | – | – | – | – | **Reserved**(1) |
| – | **0** | – | – | – | – | – | – | **Oscillator trim not done (read-only)**(1) |
| – | 1 | – | – | – | – | – | – | Oscillator trim done (read only) |
| – | – | **0** | **0** | **0** | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | 0 | – | Select factory trim (Write a 0 to select factory trim; default is 1.) |
| – | – | – | – | – | – | **1** | – | **Factory trim disabled**(1) |
| – | – | – | – | – | – | – | **0** | **Reserved**(1) |

(1) Default values are in **bold**.

## BKND_ERR REGISTER (0x1C)

When a back-end error signal is received from the internal power stage, the power stage is reset, stopping all PWM activity. Subsequently, the modulator waits approximately for the time listed in Table 18 before attempting to re-start the power stage.

**Table 18. BKND_ERR Register (0x1C)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **1** | **0** | **1** | – | – | – | – | **Reserved**(1) |
| – | – | – | – | 0 | 0 | 1 | 0 | Set back-end reset period to 299 ms |
| – | – | – | – | 0 | 0 | 1 | 1 | Set back-end reset period to 449 ms |
| – | – | – | – | 0 | 1 | 0 | 0 | Set back-end reset period to 598 ms |
| – | – | – | – | 0 | 1 | 0 | 1 | Set back-end reset period to 748 ms |
| – | – | – | – | 0 | 1 | 1 | 0 | Set back-end reset period to 898 ms |
| – | – | – | – | **0** | **1** | **1** | **1** | **Set back-end reset period to 1047 ms**(1) |
| – | – | – | – | 1 | 0 | 0 | 0 | Set back-end reset period to 1197 ms |
| – | – | – | – | 1 | 0 | 0 | 1 | Set back-end reset period to 1346 ms |
| – | – | – | – | 1 | 0 | 1 | X | Set back-end reset period to 1496 ms |
| – | – | – | – | 1 | 1 | X | X | Set back-end reset period to 1496 ms |

(1) Default values are in **bold**.

## INPUT MULTIPLEXER REGISTER (0x20)

This register controls the modulation scheme (AD or BD mode) as well as the routing of I²S audio to the internal channels.

**Table 19. Input Multiplexer Register (0x20)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| | | | | | | | | |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | – | – | – | – | – | – | – | **Channel-1 AD mode**(1) |
| 1 | – | – | – | – | – | – | – | Channel-1 BD mode |
| – | **0** | **0** | **0** | – | – | – | – | **SDIN-L to channel 1**(1) |
| – | 0 | 0 | 1 | – | – | – | – | SDIN-R to channel 1 |
| – | 0 | 1 | 0 | – | – | – | – | Reserved |
| – | 0 | 1 | 1 | – | – | – | – | Reserved |
| – | 1 | 0 | 0 | – | – | – | – | Reserved |
| – | 1 | 0 | 1 | – | – | – | – | Reserved |
| – | 1 | 1 | 0 | – | – | – | – | Ground (0) to channel 1 |
| – | 1 | 1 | 1 | – | – | – | – | Reserved |
| – | – | – | – | **0** | – | – | – | **Channel 2 AD mode**(1) |
| – | – | – | – | 1 | – | – | – | Channel 2 BD mode |
| – | – | – | – | – | 0 | 0 | 0 | SDIN-L to channel 2 |
| – | – | – | – | – | **0** | **0** | **1** | **SDIN-R to channel 2**(1) |
| – | – | – | – | – | 0 | 1 | 0 | Reserved |
| – | – | – | – | – | 0 | 1 | 1 | Reserved |
| – | – | – | – | – | 1 | 0 | 0 | Reserved |
| – | – | – | – | – | 1 | 0 | 1 | Reserved |
| – | – | – | – | – | 1 | 1 | 0 | Ground (0) to channel 2 |
| – | – | – | – | – | 1 | 1 | 1 | Reserved |
| | | | | | | | | |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **1** | **1** | **1** | **0** | **1** | **1** | **1** | **Reserved**(1) |
| | | | | | | | | |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **1** | **1** | **1** | **0** | **0** | **1** | **0** | **Reserved**(1) |

(1) Default values are in **bold**.

## CHANNEL 4 SOURCE SELECT REGISTER (0x21)

This register selects the channel 4 source.

**Table 20. Subchannel Control Register (0x21)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **1** | **0** | **0** | **0** | **0** | **1** | **–** | **Reserved**(1) |
| – | – | – | – | – | – | **–** | 0 | (L + R)/2 |
| – | – | – | – | – | – | – | **1** | **Left-channel post-BQ**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **Reserved**(1) |

(1) Default values are in **bold**.

## PWM OUTPUT MUX REGISTER (0x25)

This DAP output mux selects which internal PWM channel is output to the external pins. Any channel can be output to any external output pin.

Bits D21–D20: Selects which PWM channel is output to OUT_A

Bits D17–D16: Selects which PWM channel is output to OUT_B

Bits D13–D12: Selects which PWM channel is output to OUT_C

Bits D09–D08: Selects which PWM channel is output to OUT_D

Note that channels are encoded so that channel 1 = 0x00, channel 2 = 0x01, …, channel 4 = 0x03.

**Table 21. PWM Output Mux Register (0x25)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | – | – | – | – | – | – | **Reserved**(1) |
| **–** | **–** | **0** | **0** | – | – | – | – | **Multiplex channel 1 to OUT_A**(1) |
| – | – | 0 | 1 | – | – | – | – | Multiplex channel 2 to OUT_A |
| – | – | 1 | 0 | – | – | – | – | Multiplex $\overline{\text{channel 1}}$ to OUT_A |
| – | – | 1 | 1 | – | – | – | – | Multiplex $\overline{\text{channel 2}}$ to OUT_A |
| – | – | – | – | **0** | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | 0 | 0 | Multiplex channel 1 to OUT_B |
| – | – | – | – | – | – | 0 | 1 | Multiplex channel 2 to OUT_B |
| – | – | – | – | – | – | **1** | **0** | **Multiplex $\overline{\text{channel 1}}$ to OUT_B**(1) |
| – | – | – | – | – | – | 1 | 1 | Multiplex $\overline{\text{channel 2}}$ to OUT_B |

(1) Default values are in **bold**.

**Table 21. PWM Output Mux Register (0x25) (continued)**

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | – | – | – | – | – | – | **Reserved**(2) |
| – | – | 0 | 0 | – | – | – | – | Multiplex channel 1 to OUT_C |
| – | – | **0** | **1** | – | – | – | – | **Multiplex channel 2 to OUT_C**(2) |
| – | – | 1 | 0 | – | – | – | – | Multiplex $\overline{\text{channel 1}}$ to OUT_C |
| – | – | 1 | 1 | – | – | – | – | Multiplex $\overline{\text{channel 2}}$ to OUT_C |
| – | – | – | – | **0** | **0** | – | – | **Reserved**(2) |
| – | – | – | – | – | – | 0 | 0 | Multiplex channel 1 to OUT_D |
| – | – | – | – | – | – | 0 | 1 | Multiplex channel 2 to OUT_D |
| – | – | – | – | – | – | 1 | 0 | Multiplex $\overline{\text{channel 1}}$ to OUT_D |
| – | – | – | – | – | – | **1** | **1** | **Multiplex channel 2 to OUT_D**(2) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **Reserved**(2) |

(2) Default values are in **bold**.

## AGL CONTROL REGISTER (0x46)

**Table 22. AGL Control Register (0x46)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **Reserved**(1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | **0** | **–** | **–** | – | – | – | – | **Reserved**(1) |
| – | – | 0 | – | – | – | – | – | Reserved |
| – | – | 1 | – | – | – | – | – | Reserved |
| – | – | – | **0** | – | – | – | – | **Reserved**(1) |
| – | – | **–** | **–** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | – | – | **Reserved**(1) |
| – | – | – | – | – | – | **0** | – | **AGL2 turned OFF**(1) |
| – | – | – | – | – | – | 1 | – | AGL2 turned ON |
| – | – | – | – | – | – | – | **0** | **AGL1 turned OFF**(1) |
| – | – | – | – | – | – | – | 1 | AGL1 turned ON |

(1) Default values are in **bold**.

## PWM SWITCHING RATE CONTROL REGISTER (0x4F)

The output PWM switching frequency is configurable as a multiple of the input sample rate ($f_S$). The PWM frequency can be set to one of 6 x $f_S$, 7 x $f_S$, 8 x $f_S$ or 9 x $f_S$. PWM switching rate should be selected through the register 0x4F before coming out of all-channel shutdown.

**Table 23. PWM Switching Rate Control Register (0x4F)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| – | – | **0** | **0** | – | – | – | – | **Reserved**(1) |
| – | – | – | – | 0 | 1 | 1 | 0 | PWM SRC = 6 x $f_S$ |
| – | – | – | – | 0 | 1 | 1 | 1 | PWM SRC = 7 x $f_S$ |
| – | – | – | – | **1** | **0** | **0** | **0** | **PWM SRC = 8 x $f_S$**(1) |
| – | – | – | – | 1 | 0 | 0 | 1 | PWM SRC = 9 x $f_S$ |
| – | – | – | – | 1 | 0 | 1 | 0 | Reserved |
| – | – | – | – | 1 | 1 | – | – | Reserved |

(1) Default values are in **bold**.

## EQ CONTROL (0x50)

**Table 24. EQ Command (0x50)**

| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | **Reserved**(1) |
| **D23** | **D22** | **D21** | **D20** | **D19** | **D18** | **D17** | **D16** | **FUNCTION** |
| 0 | **1** | **1** | **1** | 0 | 0 | 0 | 0 | **Reserved**(1) |
| **D15** | **D14** | **D13** | **D12** | **D11** | **D10** | **D9** | **D8** | **FUNCTION** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **Reserved**(1) |
| **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **FUNCTION** |
| **0** | – | – | – | – | – | – | – | **EQ ON**(1) |
| 1 | – | – | – | – | – | – | – | EQ OFF (bypass BQ 0–7 of channels 1 and 2) |
| – | **0** | – | – | – | – | – | – | **Reserved**(1) |
| – | – | **0** | – | – | – | – | – | **Reserved**(1) |
| – | – | 1 | – | – | – | – | – | **Reserved**(1) |
| – | – | – | **0** | – | – | – | – | **L and R can be written independently.**(1) |
| – | – | – | 1 | – | – | – | – | L and R are ganged for EQ biquads; a write to the left-channel biquad is also written to the right-channel biquad. (0x29–0x2F is ganged to 0x30–0x36. Also, 0x58–0x5B is ganged to 0x5C–0x5F. |
| – | – | **–** | **–** | **0** | – | – | – | **Reserved**(1) |
| – | – | – | – | – | **0** | **0** | **0** | **Reserved**(1) |
| – | – | – | – | – | 0 | 0 | 1 | **Reserved** |
| – | – | – | – | – | 0 | 1 | X | Reserved |
| – | – | – | – | – | 1 | X | X | Reserved |

(1) Default values are in **bold**.

## APPLICATION INFORMATION

These typical connection diagrams highlight the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

### TAS5729MD Typical Application Circuit

These application circuits detail the recommended component selection and board configurations for the TAS5729MD device.

For further information regarding component selection, see SLOU367.

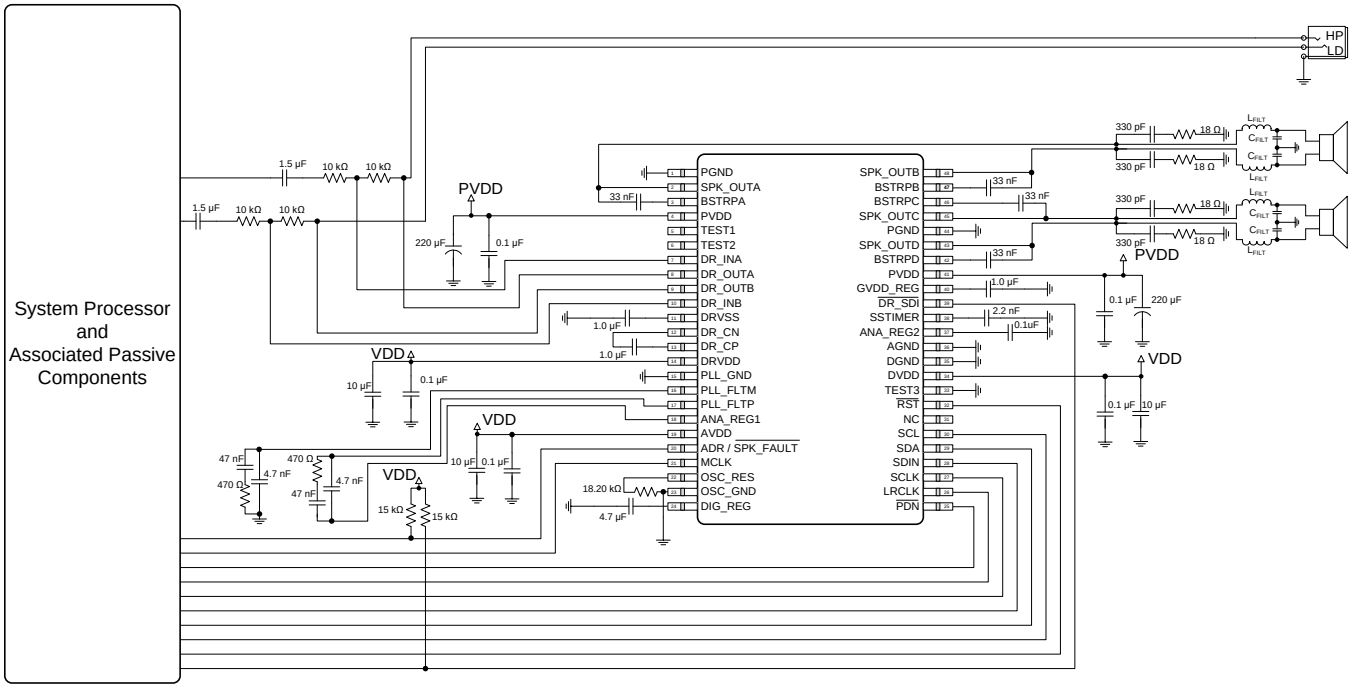



**Figure 51. Stereo BTL Configuration with Headphone / Line Driver Amplifier**

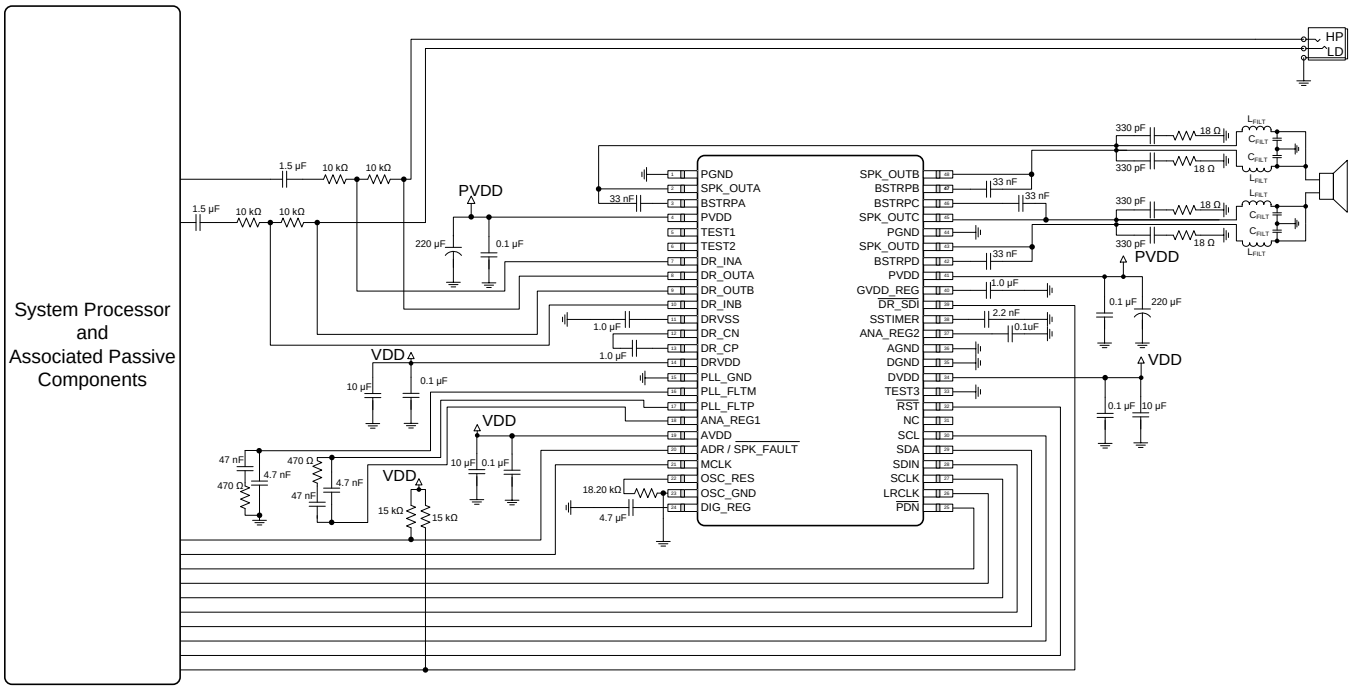



**Figure 52. Mono PBTL Configuration with Headphone / Line Driver Amplifier**

## REVISION HISTORY

| Changes from Original (May 2013) to Revision A | Page |
|---|---|
| • Changed the Product Preview data sheet | 1 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5729MDDCA | ACTIVE | HTSSOP | DCA | 48 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | TAS5729MD | Samples |
| TAS5729MDDCAR | ACTIVE | HTSSOP | DCA | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | TAS5729MD | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

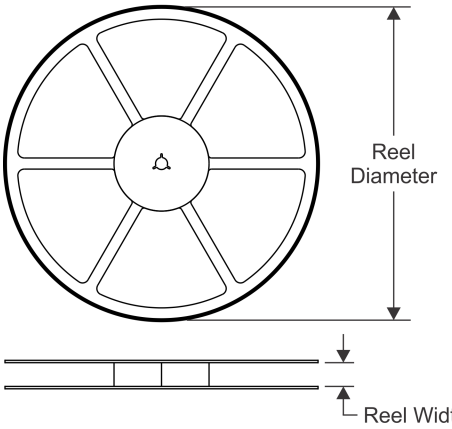
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

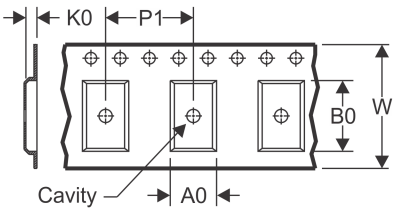
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

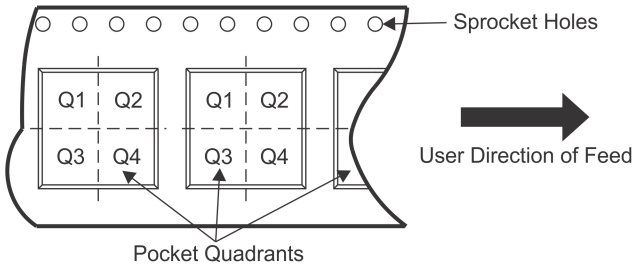



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

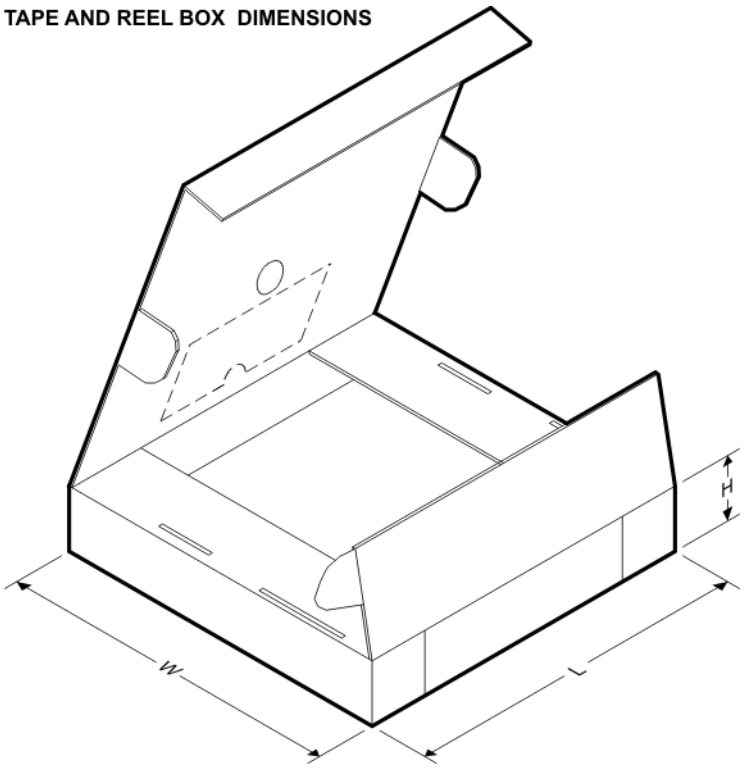
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TAS5729MDDCAR | HTSSOP | DCA | 48 | 2000 | 330.0 | 24.4 | 8.6 | 15.8 | 1.8 | 12.0 | 24.0 | Q1 |

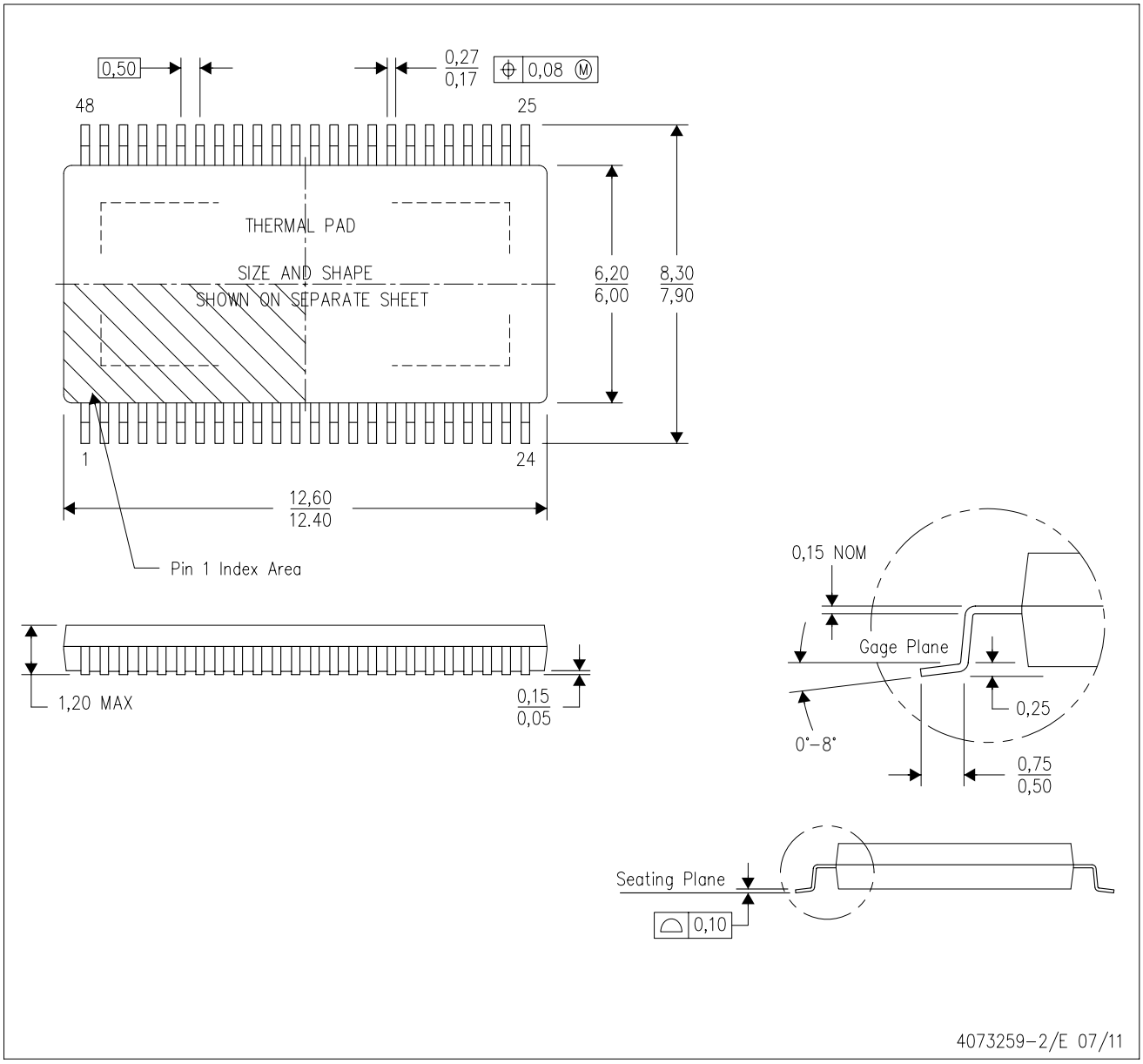
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TAS5729MDDCAR | HTSSOP | DCA | 48 | 2000 | 367.0 | 367.0 | 45.0 |

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

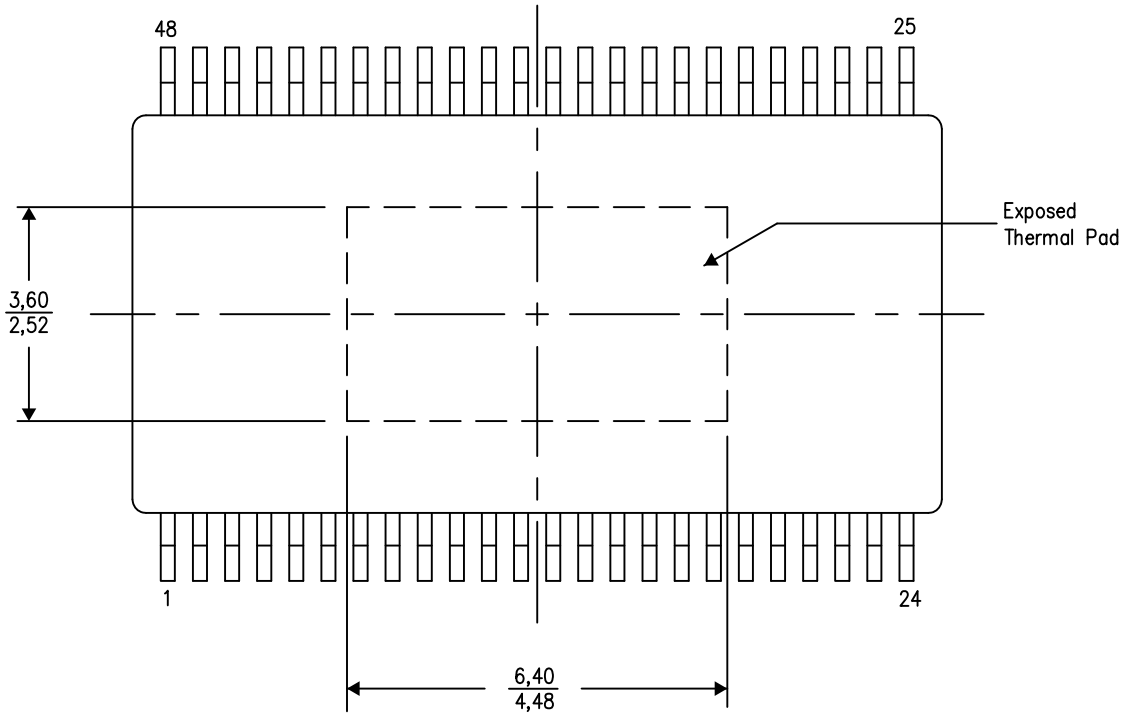
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

## THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

Exposed Thermal Pad Dimensions

4206320–4/R 03/13

NOTE: A. All linear dimensions are in millimeters

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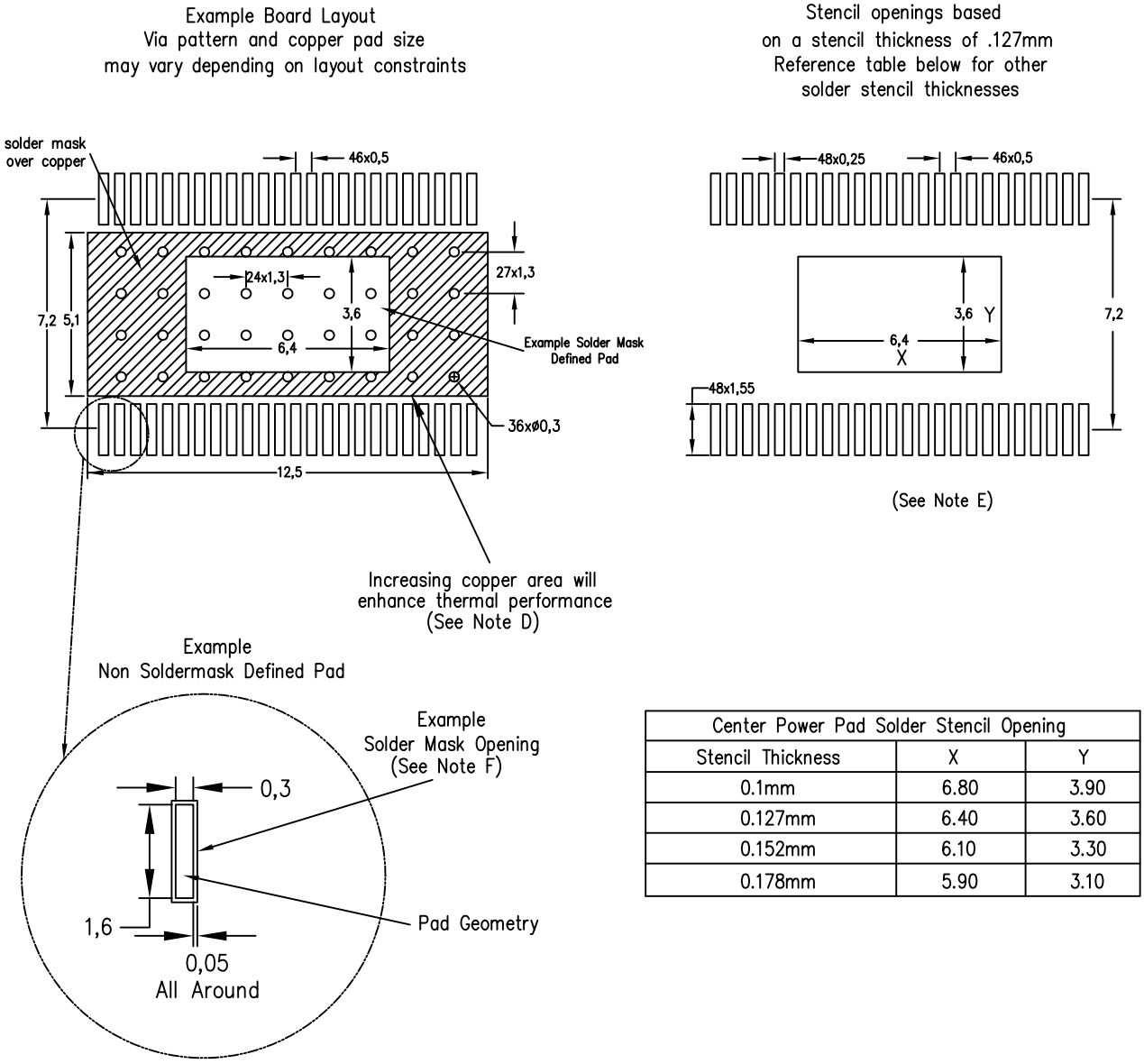
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 6.80 | 3.90 |
| 0.127mm | 6.40 | 3.60 |
| 0.152mm | 6.10 | 3.30 |
| 0.178mm | 5.90 | 3.10 |

4208546–3/G 12/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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