STY50N105DK5

N-channel 1050 V, 0.110 Ω typ., 46 A MDmesh™ DK5 Power MOSFET in a Max247 package

Datasheet - production data

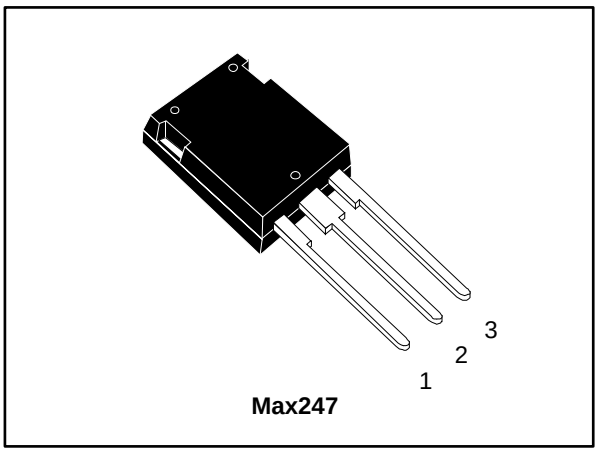
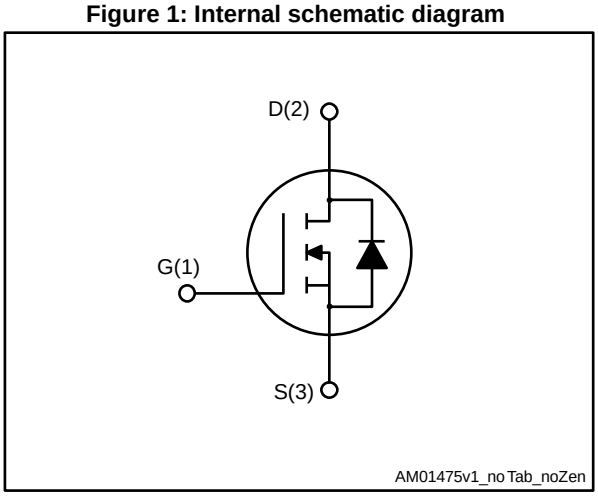


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STY50N105DK5	1050 V	0.120 Ω	46 A	625 W

- Fast-recovery body diode
- Best $R_{DS(on)}$ x area
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is part of the MDmesh™ DK5 fast recovery diode series. The MDmesh™ DK5 combines very low recovery charge (Q_{rr}) and recovery time (t_{rr}) with an excellent improvement in $R_{DS(on)}$ * area and one of the most effective switching behaviors, ideal for half bridge and full bridge converters.

Table 1: Device summary

Order code	Marking	Packages	Packaging
STY50N105DK5	50N105DK5	Max247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	46	A
	Drain current (continuous) at T_C = 100 °C	30	A
I_{DM} (1)	Drain current (pulsed)	184	A
P_{TOT}	Total dissipation at T_C = 25 °C	625	W
dv/dt (2)	Peak diode recovery voltage slope	50	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area

(2)I_{SD} ≤ 23 A, di/dt ≤ 400 A/µs; $V_{DS\ peak}$ ≤ $V_{(BR)DSS}$, V_{DD} = 525 V

(3)V_{DS} ≤ 840 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.2	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	30	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche energy (pulse width limited by T_{JMAX})	16	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25°C, I_D = I_{AS}, V_{DD} = 50 V)	1550	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	1050			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1050 V, V_{GS} = 0 V			1	µA
		V_{DS} = 1050 V, V_{GS} = 0 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 23 A		0.110	0.120	Ω

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	6675	-	pF
C_{oss}	Output capacitance		-	370	-	pF
C_{rss}	Reverse transfer capacitance		-	10	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0 V, V_{DS} = 0 to 840 V	-	630	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	219	-	
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 46 A, V_{GS} = 10 V (see *Figure 15: "Test circuit for gate charge behavior"*)	-	204	-	nC
Q_{gs}	Gate-source charge		-	36	-	nC
Q_{gd}	Gate-drain charge		-	133	-	nC

Notes:

(1)Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

(2)Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525 V, I_D = 23 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"* and *Figure 19: "Switching time waveform"*)	-	40.6	-	ns
t_r	Rise time		-	64.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	262	-	ns
t_f	Fall time		-	49.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		46	A
I_{SDM}	Source-drain current (pulsed)		-		184	A
V_{SD}(1)	Forward on voltage	I_{SD} = 46 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 46 A, V_{DD} = 60 V, di/dt = 100 A/µs (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	273		ns
Q_{rr}	Reverse recovery charge		-	3		µC
I_{RRM}	Reverse recovery current		-	23		A
t_{rr}	Reverse recovery time	I_{SD} = 46 A, V_{DD} = 60 V, di/dt = 100 A/µs, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	477		ns
Q_{rr}	Reverse recovery charge		-	10		µC
I_{RRM}	Reverse recovery current		-	42		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Forward bias safe operating area

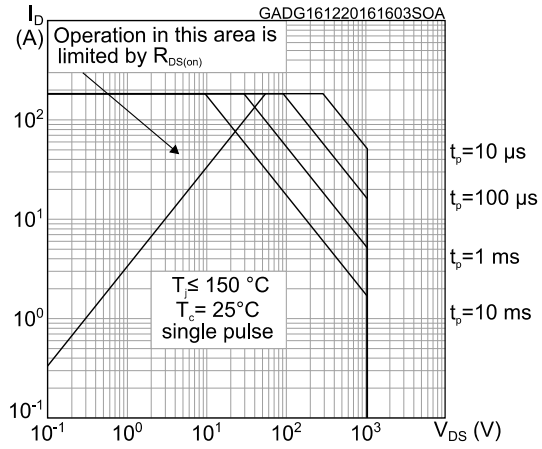


Figure 3: Thermal impedance

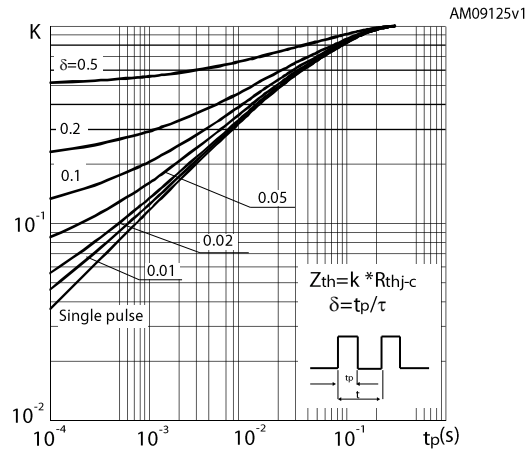


Figure 4: Output characteristics

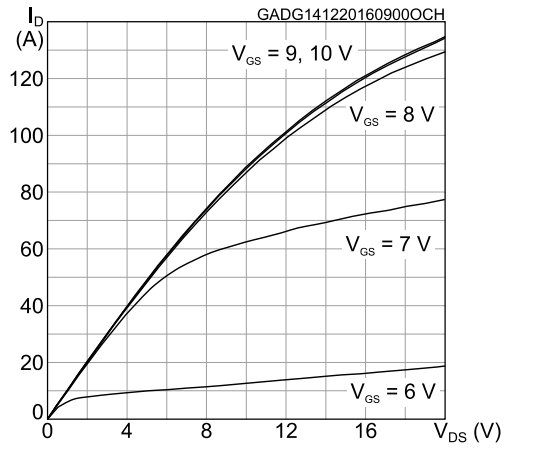


Figure 5: Transfer characteristics

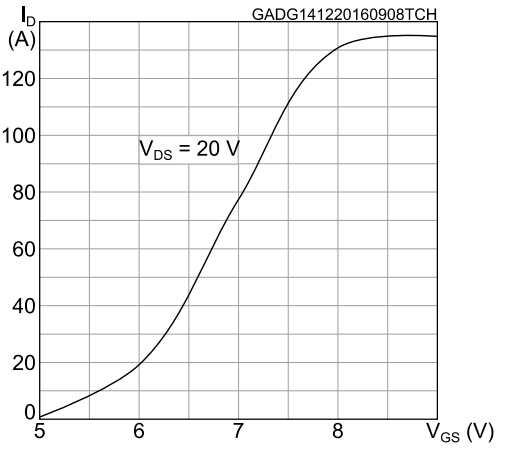


Figure 6: Gate charge vs gate-source voltage

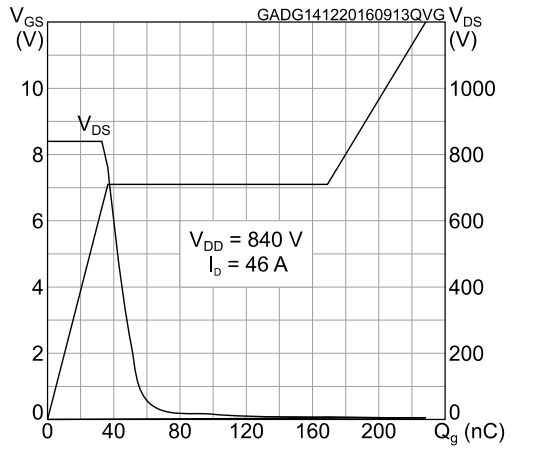


Figure 7: Static drain-source on-resistance

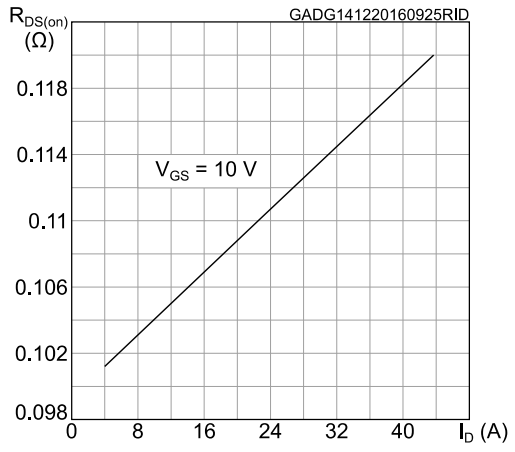


Figure 8: Capacitance variations

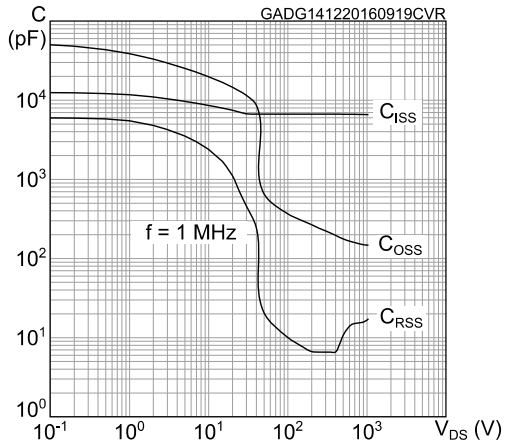


Figure 9: Normalized gate threshold voltage vs temperature

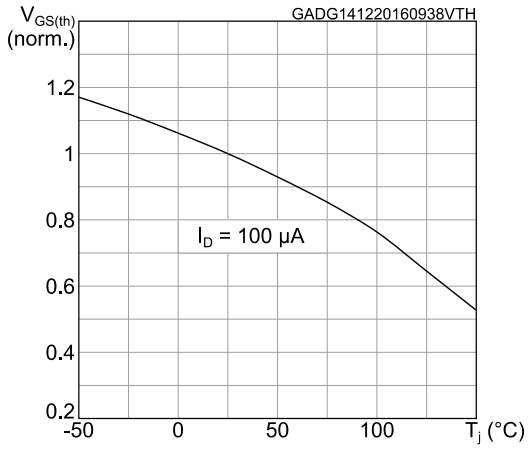


Figure 10: Normalized on-resistance vs temperature

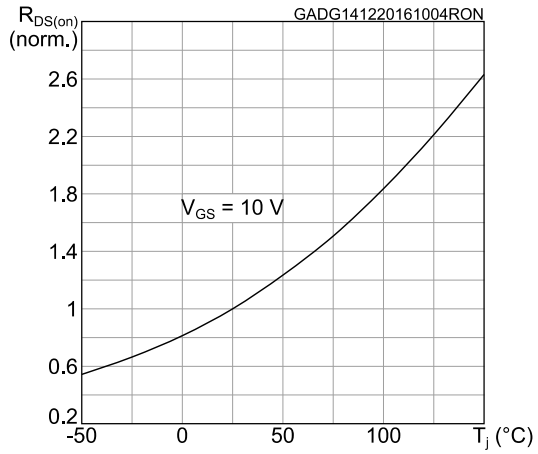


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

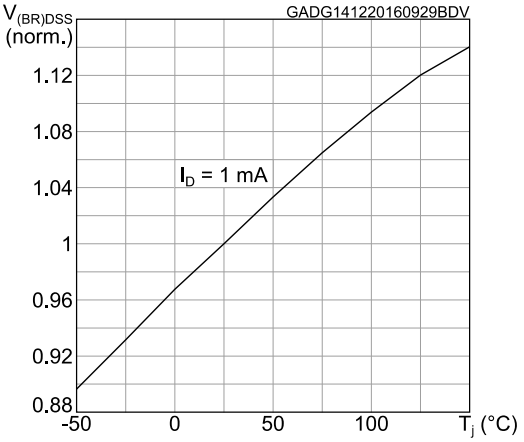


Figure 12: Source-drain diode forward characteristics

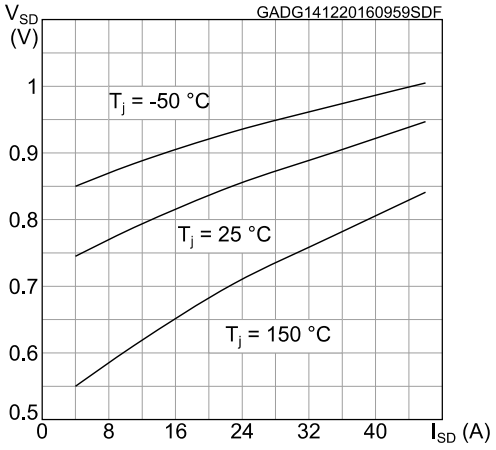
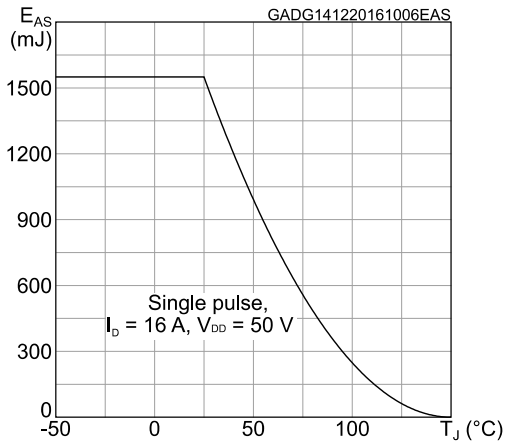


Figure 13: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 14: Test circuit for resistive load switching times

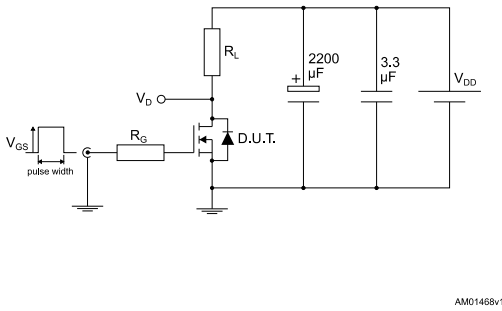


Figure 15: Test circuit for gate charge behavior

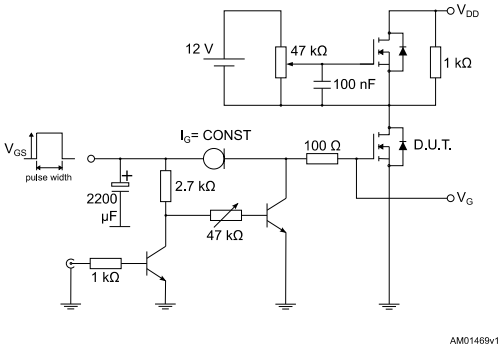


Figure 16: Test circuit for inductive load switching and diode recovery times

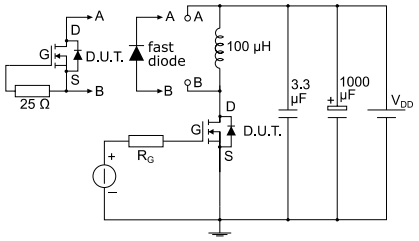


Figure 17: Unclamped inductive load test circuit

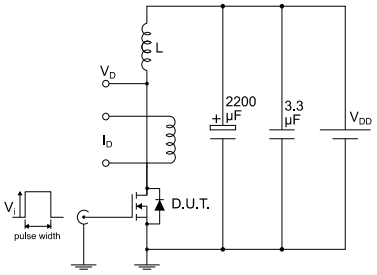


Figure 18: Unclamped inductive waveform

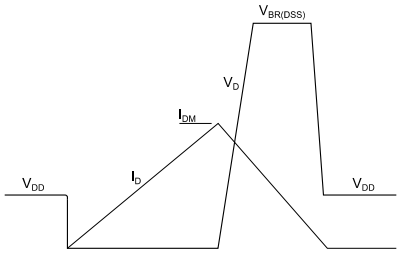
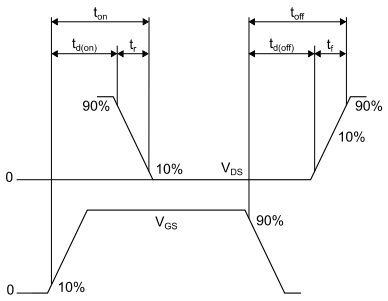


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 Max247 package information

Figure 20: Max247 package outline

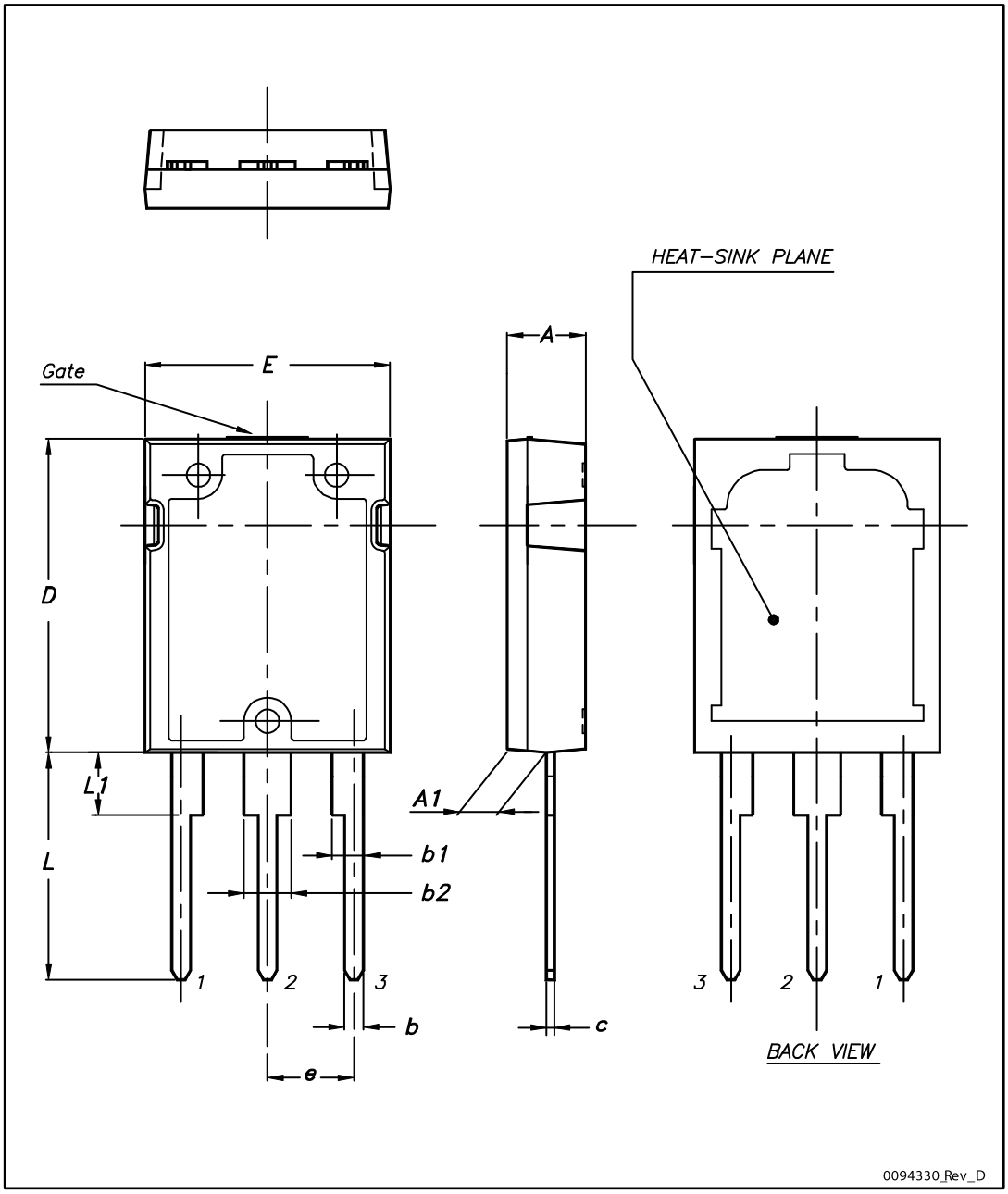


Table 9: Max247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70	-	5.30
A1	2.20	-	2.60
b	1.00	-	1.40
b1	2.00	-	2.40
b2	3.00	-	3.40
c	0.40	-	0.80
D	19.70	-	20.30
e	5.35	-	5.55
E	15.30	-	15.90
L	14.20	-	15.20
L1	3.70	-	4.30

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
24-Jan-2013	1	First release
19-Dec-2016	2	Datasheet status promoted from preliminary to production data. Updated features, description and internal schematic diagram on cover page. Updated *Section 1: "Electrical ratings"* and *Section 2: "Electrical characteristics"*. Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.