

## N-channel 950 V, 0.275 $\Omega$ , 17.5 A SuperMESH™ 5 Power MOSFET in TO-247 long leads package

Datasheet - preliminary data

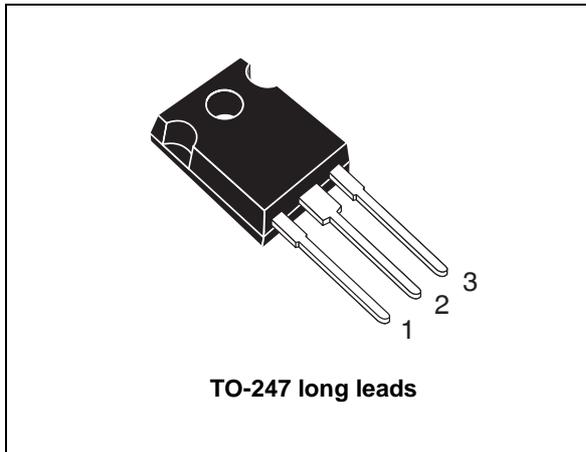
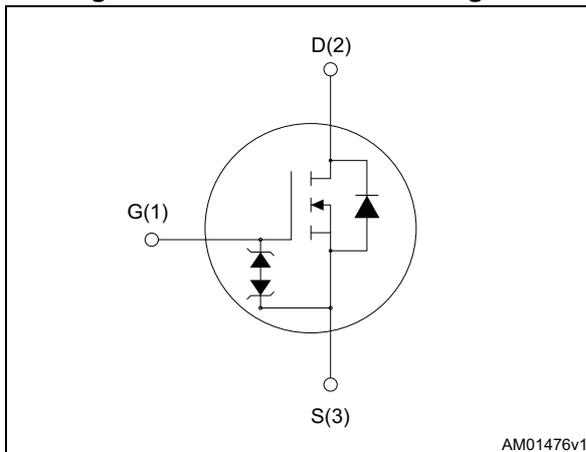


Figure 1. Internal schematic diagram



### Features

Order codes	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>W</sub>
STWA20N95K5	950 V	0.330 $\Omega$	17.5 A	250 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STWA20N95K5	20N95K5	TO-247 long leads	Tube

## Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17.5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(1)}$	Drain current (pulsed)	70	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	250	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{jmax}$ )	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	200	mJ
$E_{SD}$	Gate-source human body model ( $R = 1,5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	2	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	6	V/ns
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 17.5\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.5	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal resistance junction-amb max	50	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	950			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 950\text{ V}$ , $V_{DS} = 950\text{ V}$ , $T_c = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$		0.275	0.330	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1500	-	pF
$C_{oss}$	Output capacitance		-	80	-	pF
$C_{rss}$	Reverse transfer capacitance		-	5	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }760\text{ V}$	-	170	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	65	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}$ , $I_D = 9\text{ A}$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	40	-	nC
$Q_{gs}$	Gate-source charge		-	8	-	nC
$Q_{gd}$	Gate-drain charge		-	25	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475 \text{ V}$ , $I_D = 9 \text{ A}$ , $R_G = 4.7 \text{ } \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 17</a> )	-	17	-	ns
$t_r$	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
$t_f$	Fall time		-	20	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		17.5	A
$I_{SDM}$	Source-drain current (pulsed)		-		70	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 17.5 \text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , (see <a href="#">Figure 16</a> )	-	530		ns
$Q_{rr}$	Reverse recovery charge		-	12		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	44		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17.5 \text{ A}$ , $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$ , $T_J = 150 \text{ } ^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	650		ns
$Q_{rr}$	Reverse recovery charge		-	14		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	77		A

1. Pulsed: pulse duration =  $300 \mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0$	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

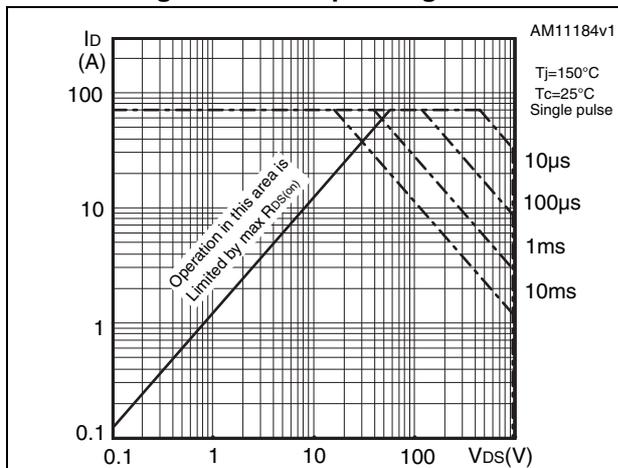


Figure 3. Thermal impedance

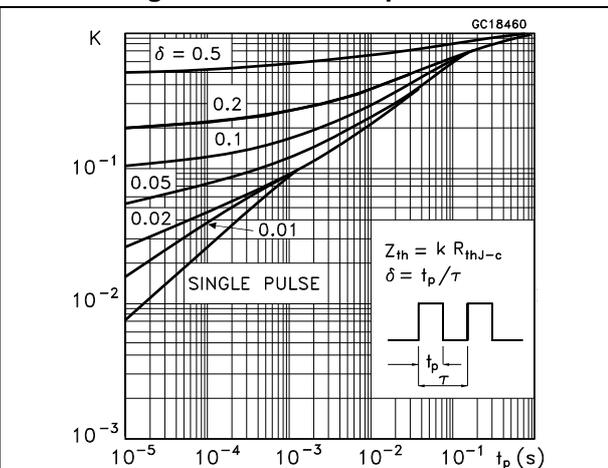


Figure 4. Output characteristics

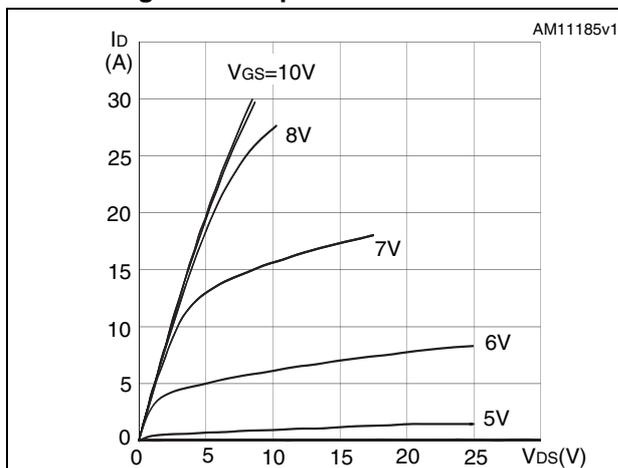


Figure 5. Transfer characteristics

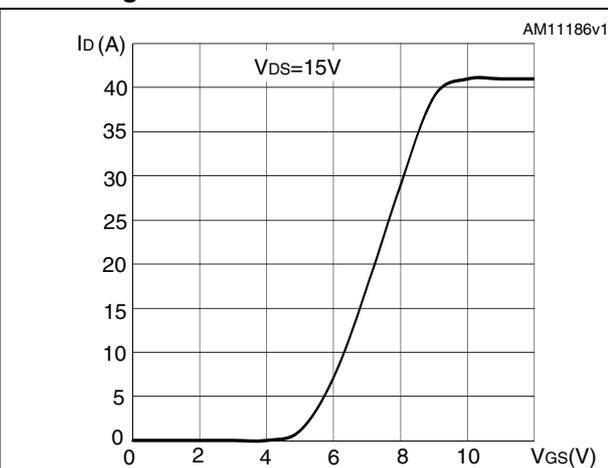


Figure 6. Gate charge vs gate-source voltage

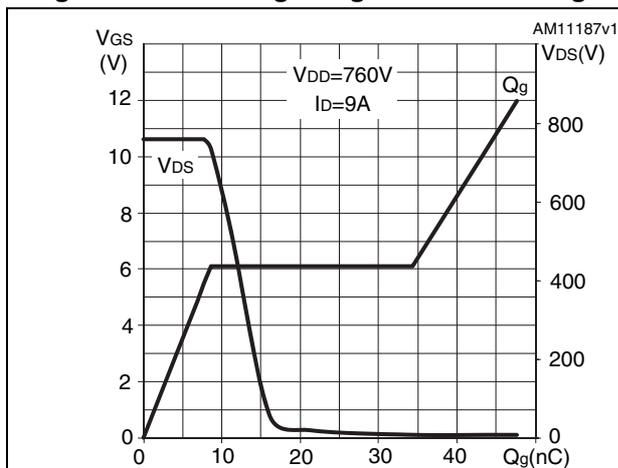


Figure 7. Static drain-source on-resistance

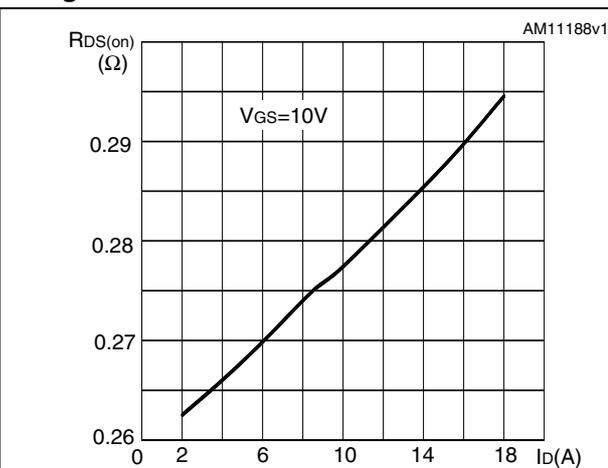


Figure 8. Capacitance variations

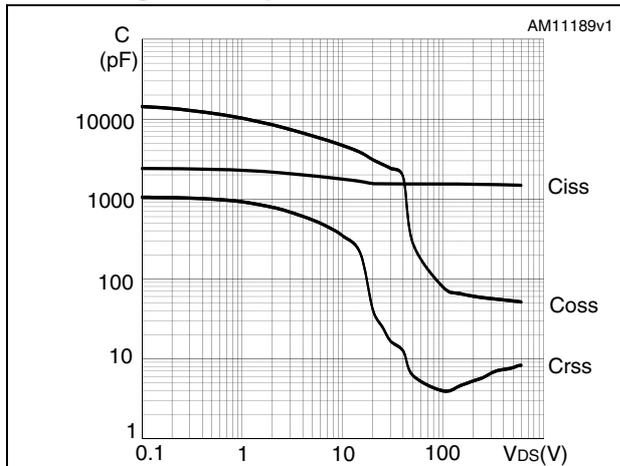


Figure 9. Output capacitance stored energy

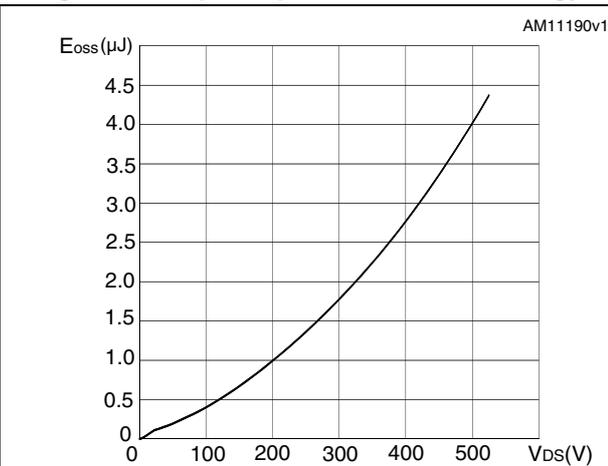


Figure 10. Normalized gate threshold voltage vs temperature

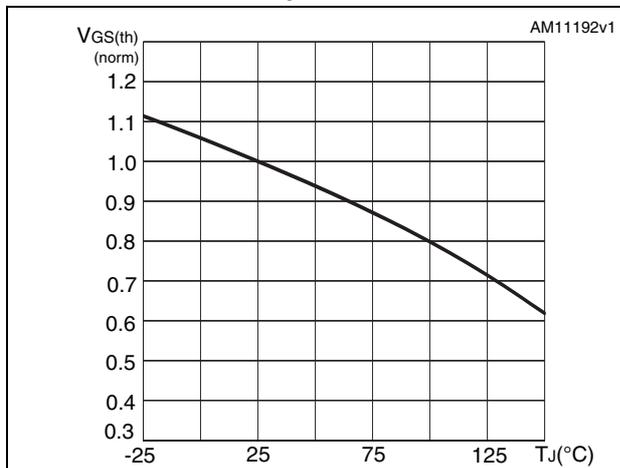


Figure 11. Normalized on-resistance vs temperature

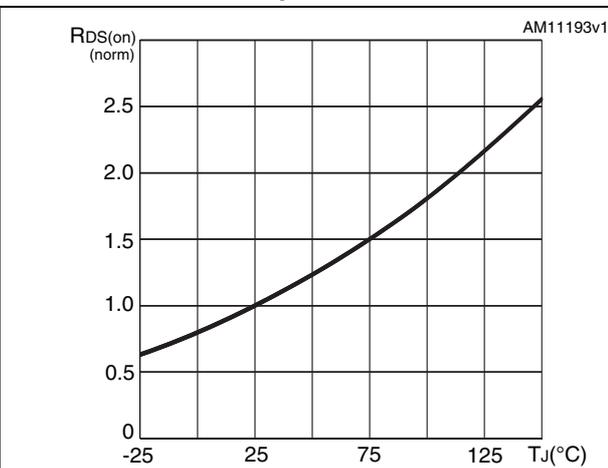


Figure 12. Maximum avalanche energy vs starting Tj

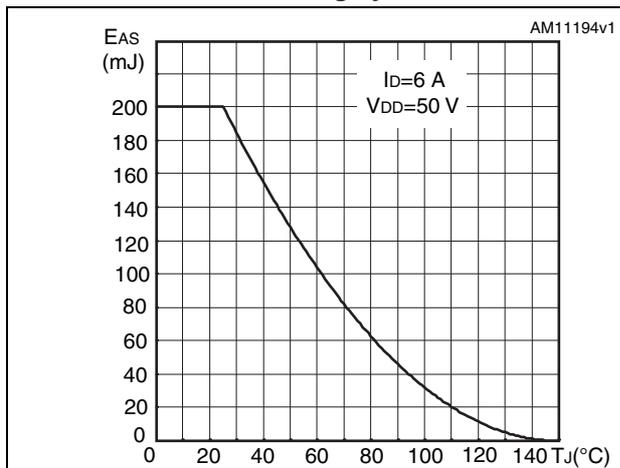
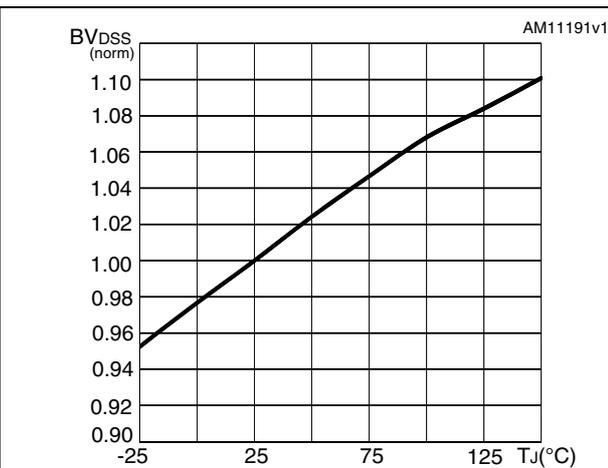


Figure 13. Normalized B<sub>VDS</sub> vs temperature



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load

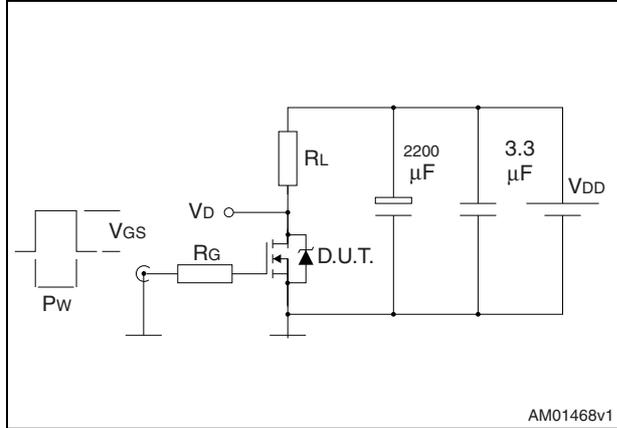


Figure 15. Gate charge test circuit

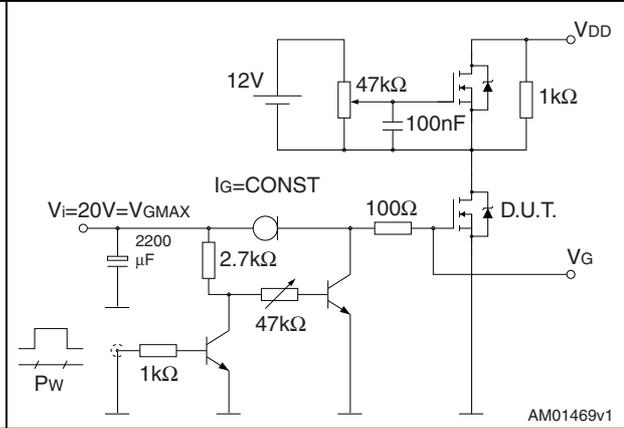


Figure 16. Test circuit for inductive load switching and diode recovery times

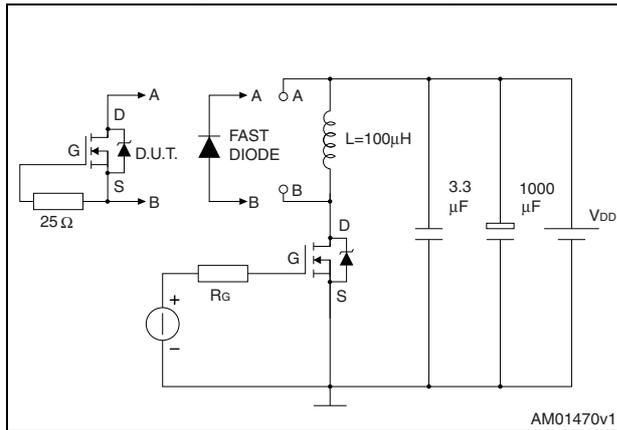


Figure 17. Unclamped inductive load test circuit

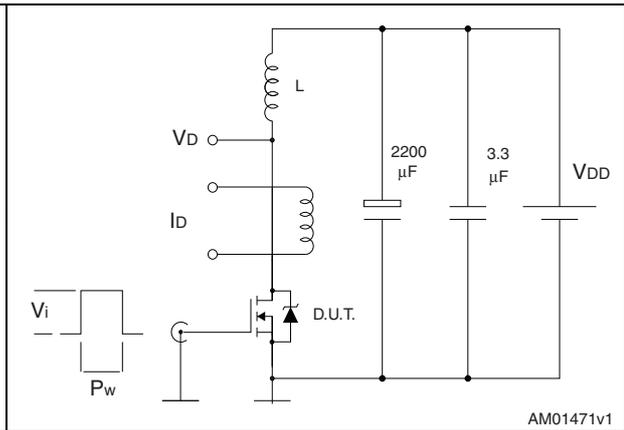


Figure 18. Unclamped inductive waveform

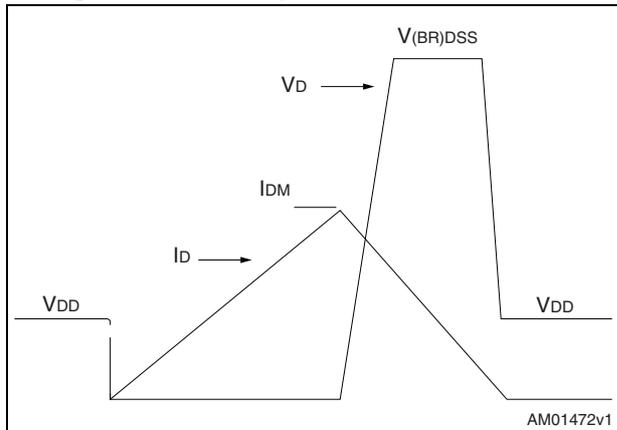
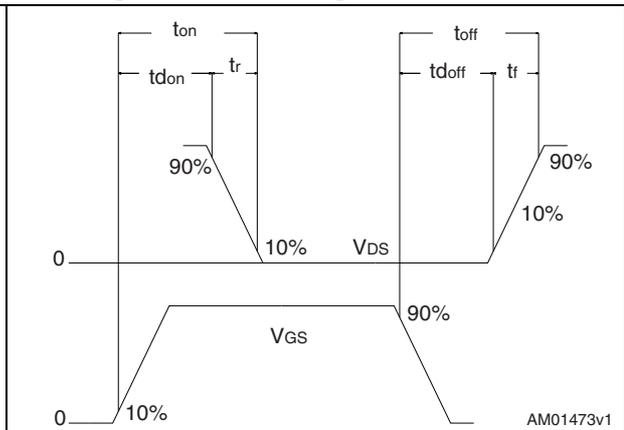


Figure 19. Switching time waveform



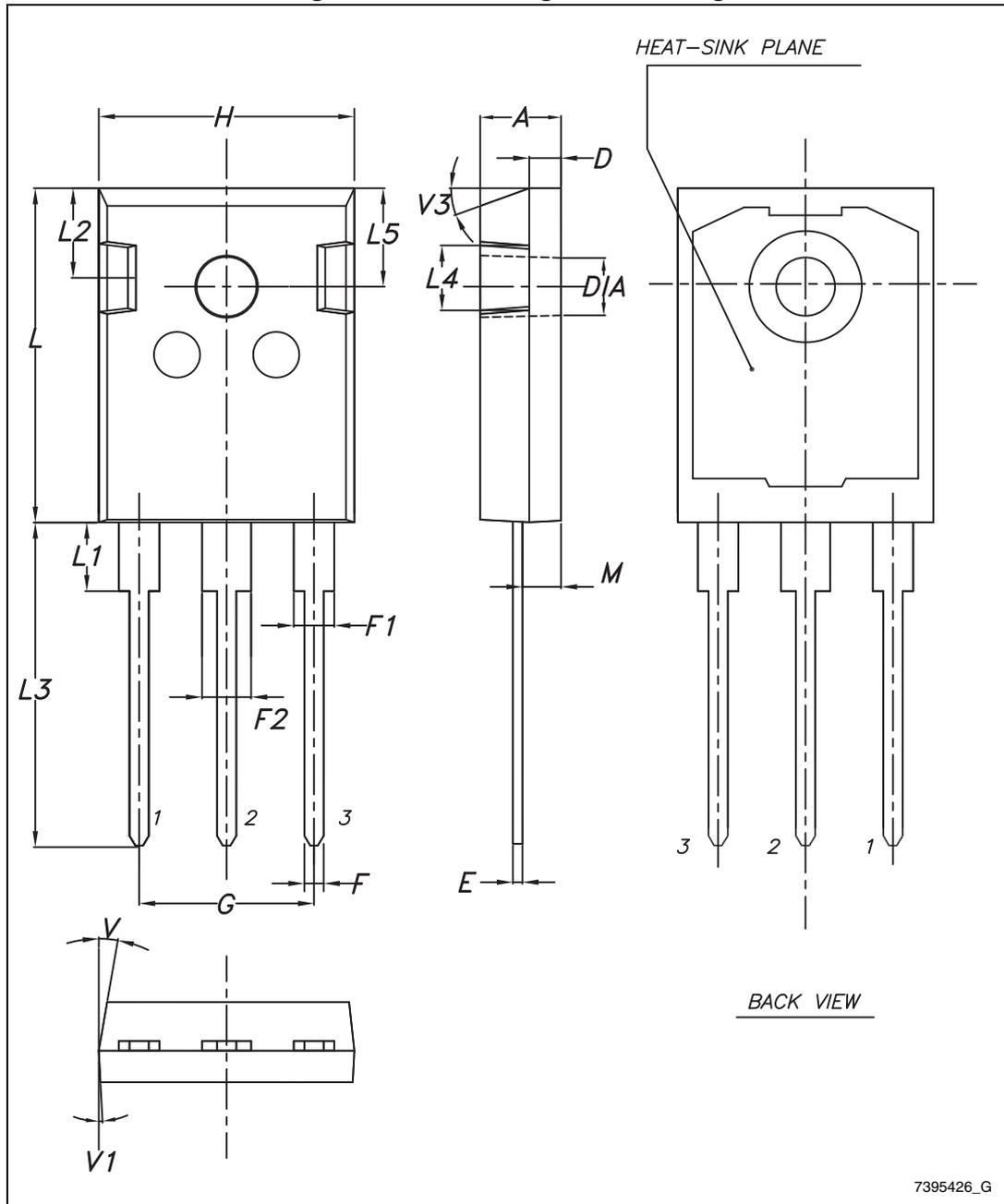
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 9. TO-247 long leads mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G	10.90 BSC		
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
Dia.	3.55		3.66

Figure 20. TO-247 long leads drawing



## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Nov-2013	1	First release.

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