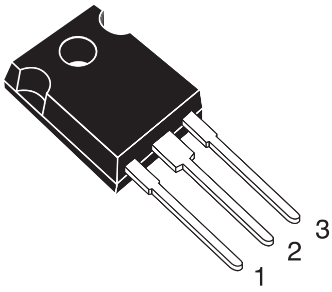
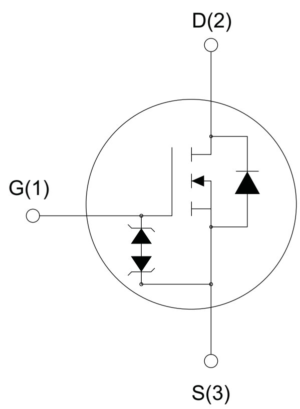
N-channel 950 V, 0.275 Ω, 17.5 A SuperMESH™ 5 Power MOSFET in TO-247 long leads package

Datasheet - preliminary data



TO-247 long leads

Figure 1. Internal schematic diagram



Features

Order codes	V_{DSS}	$R_{DS(on)}$ max	I_D	P_W
STWA20N95K5	950 V	0.330 Ω	17.5 A	250 W

- Worldwide best FOM (figure of merit)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using SuperMESH™ 5 technology. This revolutionary, avalanche-rugged, high voltage Power MOSFET technology is based on an innovative proprietary vertical structure. The result is a drastic reduction in on-resistance and ultra low gate charge for applications which require superior power density and high efficiency.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STWA20N95K5	20N95K5	TO-247 long leads	Tube

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	17.5	A
I_D	Drain current (continuous) at T_C = 100 °C	11	A
I_{DM} (1)	Drain current (pulsed)	70	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	200	mJ
E_{SD}	Gate-source human body model (R= 1,5 kΩ, C = 100 pF)	2	kV
dv/dt (2)	Peak diode recovery voltage slope	6	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq$ 17.5 A, di/dt $\leq$ 100 A/μs, $V_{Peak} \leq V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.5	°C/W
Rthj-amb	Thermal resistance junction-amb max	50	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	950			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 950 V, V_{DS} = 950 V, Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 9 A		0.275	0.330	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =100 V, f=1 MHz, V_{GS}=0	-	1500	-	pF
C_{oss}	Output capacitance		-	80	-	pF
C_{rss}	Reverse transfer capacitance		-	5	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 760 V	-	170	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	65	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	3.5	-	Ω
Q_g	Total gate charge	V_{DD} = 760 V, I_D = 9 A V_{GS} =10 V *(see Figure 15)*	-	40	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 475 V, I_D = 9 A, R_G=4.7 Ω, V_{GS}=10 V (see *Figure 17*)	-	17	-	ns
t_r	Rise time		-	12	-	ns
$t_{d(off)}$	Turn-off delay time		-	70	-	ns
t_f	Fall time		-	20	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		17.5	A
I_{SDM}	Source-drain current (pulsed)		-		70	A
V_{SD}(1)	Forward on voltage	I_{SD}= 17.5 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}= 17.5 A, V_{DD}= 60 V di/dt = 100 A/μs, (see *Figure 16*)	-	530		ns
Q_{rr}	Reverse recovery charge		-	12		μC
I_{RRM}	Reverse recovery current		-	44		A
t_{rr}	Reverse recovery time	I_{SD}= 17.5 A,V_{DD}= 60 V di/dt=100 A/μs, Tj=150 °C (see *Figure 16*)	-	650		ns
Q_{rr}	Reverse recovery charge		-	14		μC
I_{RRM}	Reverse recovery current		-	77		A

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D= 0	30	-	-	V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

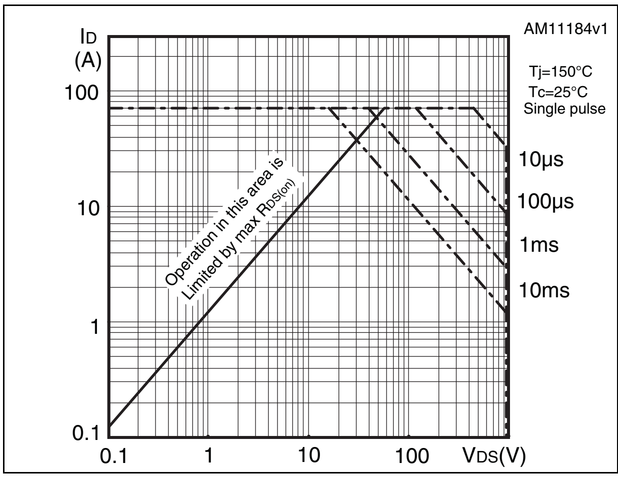


Figure 3. Thermal impedance

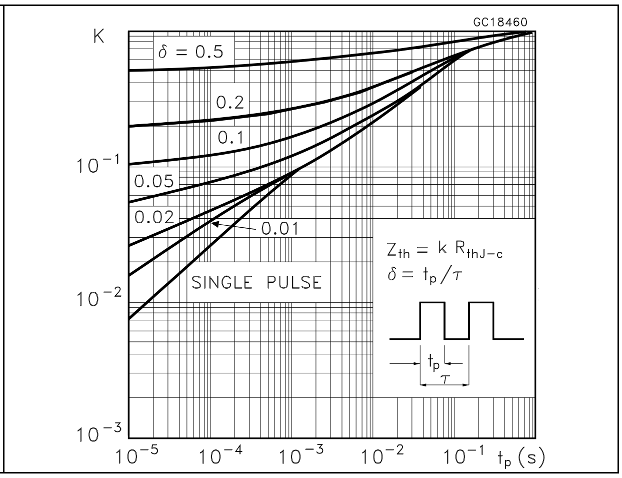


Figure 4. Output characteristics

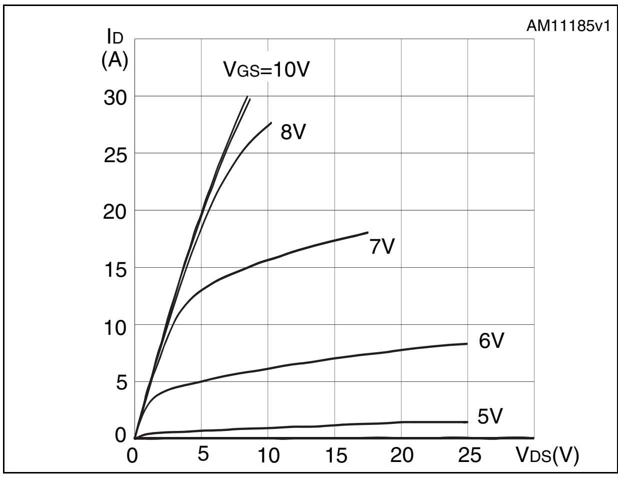


Figure 5. Transfer characteristics

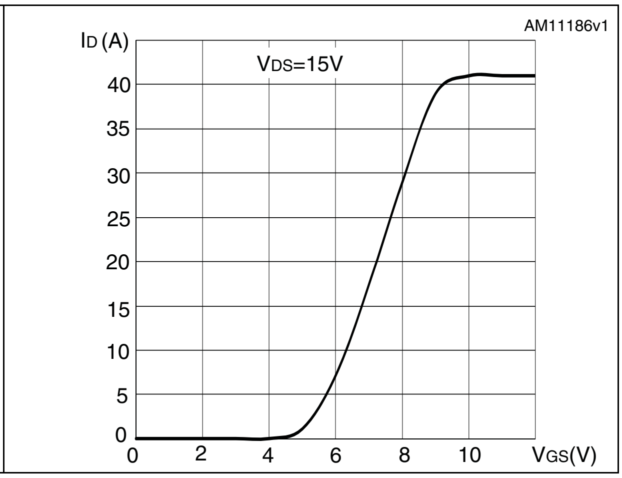


Figure 6. Gate charge vs gate-source voltage

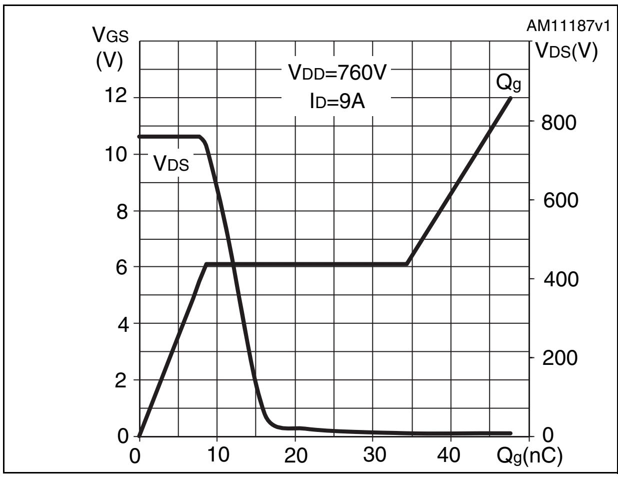


Figure 7. Static drain-source on-resistance

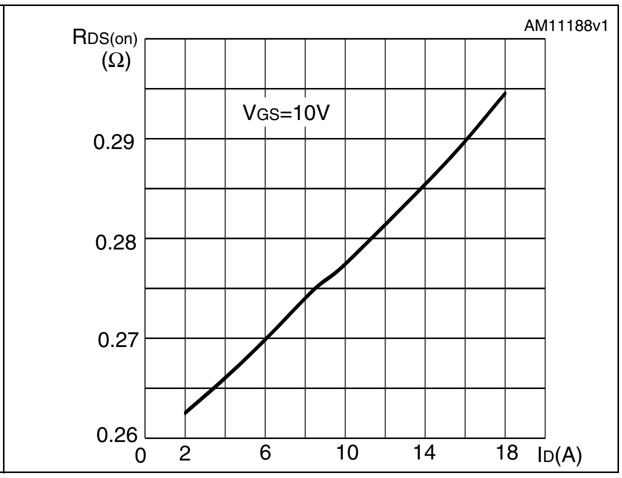


Figure 8. Capacitance variations

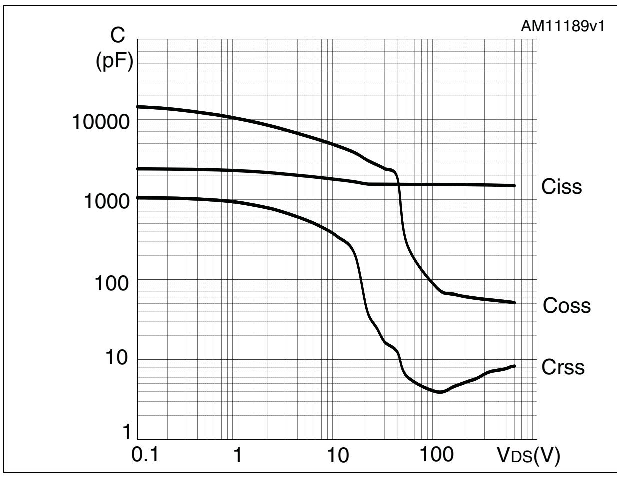


Figure 9. Output capacitance stored energy

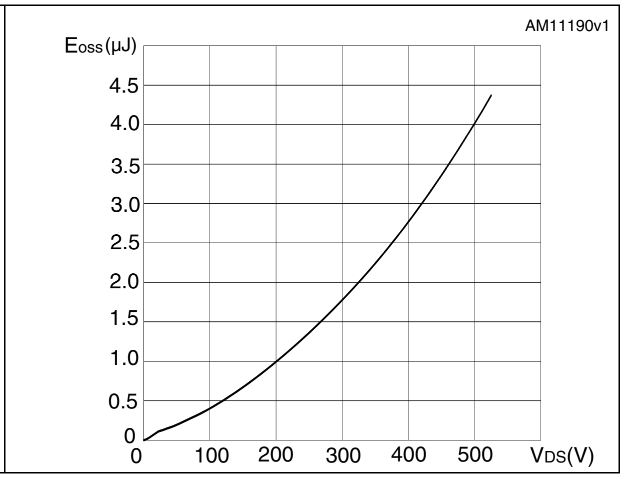


Figure 10. Normalized gate threshold voltage vs temperature

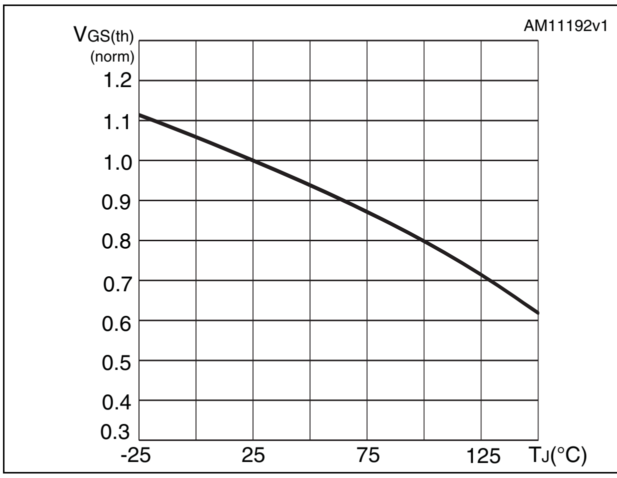


Figure 11. Normalized on-resistance vs temperature

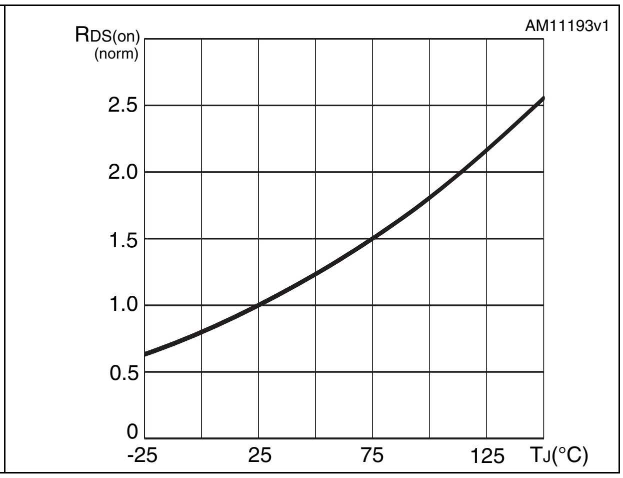


Figure 12. Maximum avalanche energy vs starting Tj

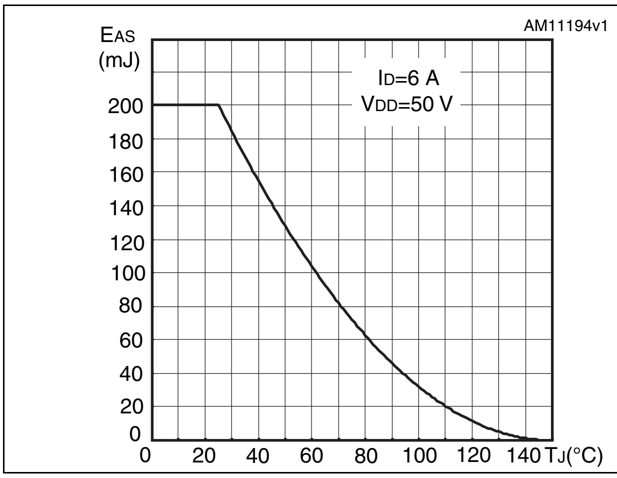
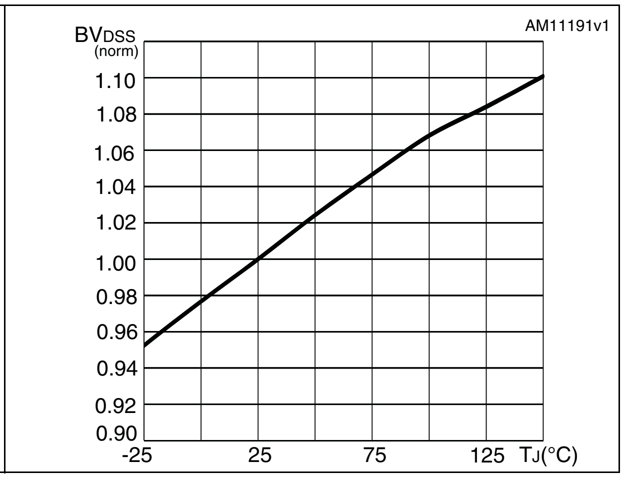


Figure 13. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

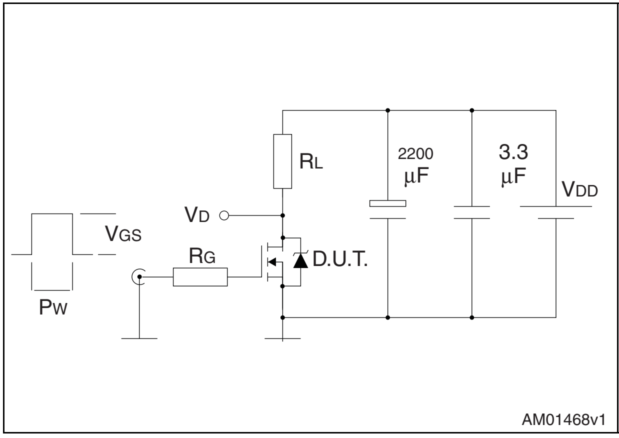


Figure 15. Gate charge test circuit

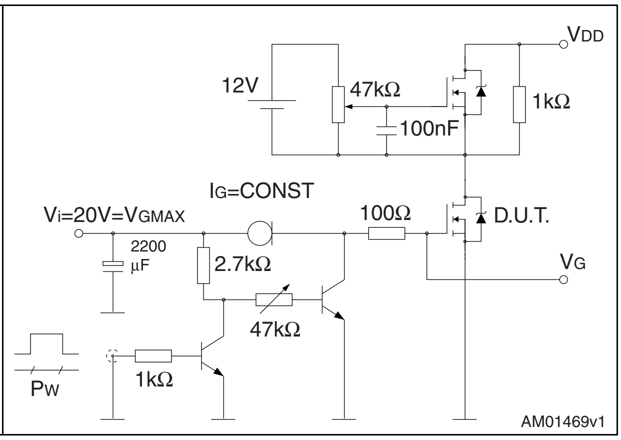


Figure 16. Test circuit for inductive load switching and diode recovery times

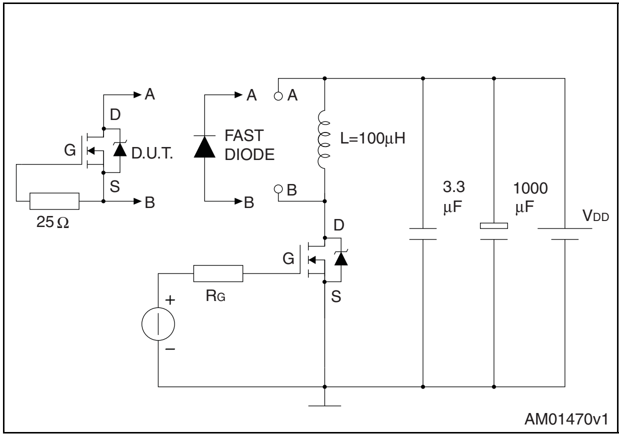


Figure 17. Unclamped inductive load test circuit

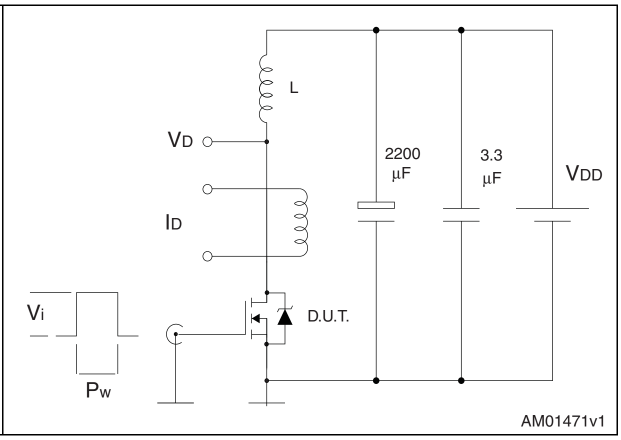


Figure 18. Unclamped inductive waveform

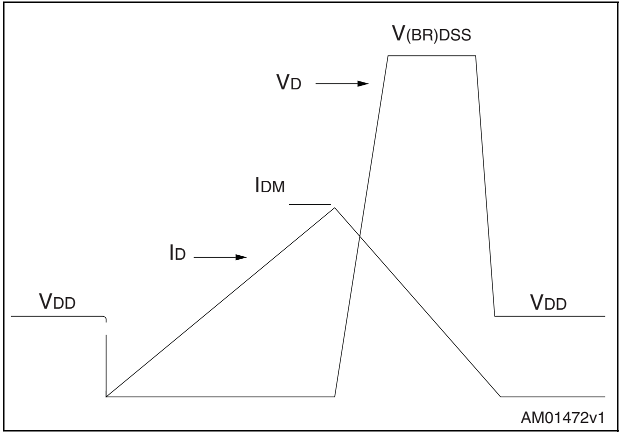
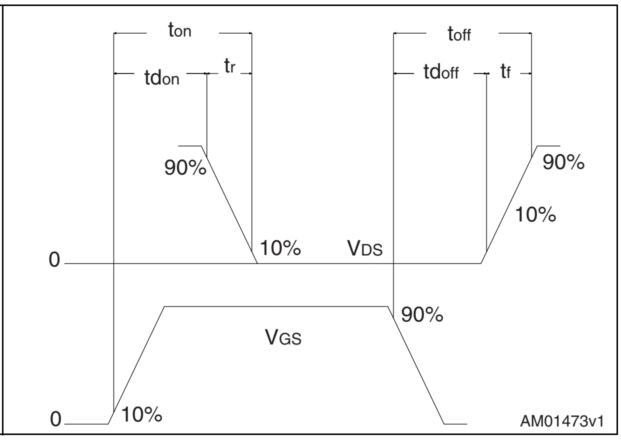


Figure 19. Switching time waveform



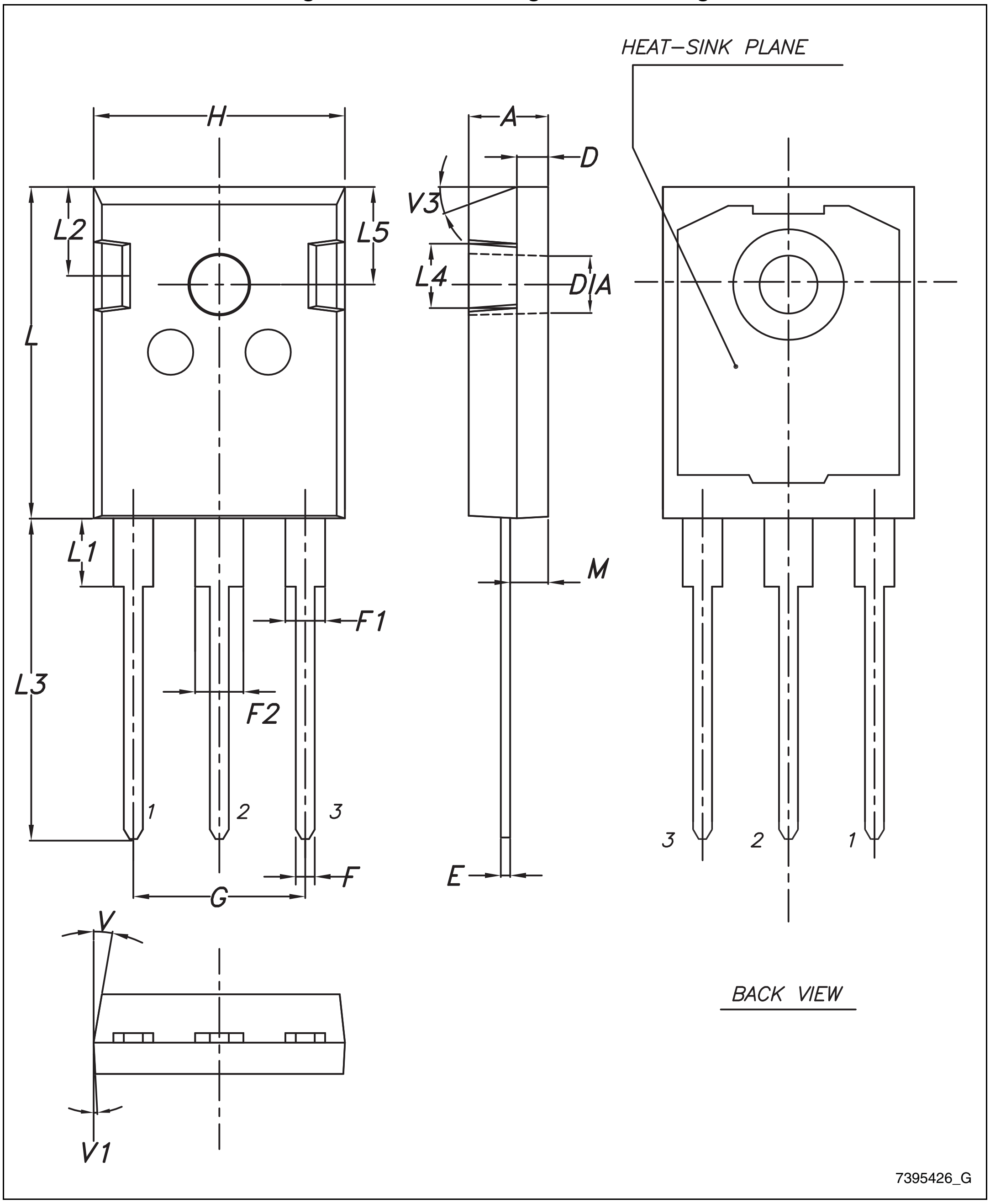
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. TO-247 long leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90		5.15
D	1.85		2.10
E	0.55		0.67
F	1.07		1.32
F1	1.90		2.38
F2	2.87		3.38
G		10.90 BSC	
H	15.77		16.02
L	20.82		21.07
L1	4.16		4.47
L2	5.49		5.74
L3	20.05		20.30
L4	3.68		3.93
L5	6.04		6.29
M	2.25		2.55
V		10°	
V1		3°	
V3		20°	
Dia.	3.55		3.66

Figure 20. TO-247 long leads drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Nov-2013	1	First release.