



STN3N40K3

N-channel 400 V, 3 Ω , 1.8 A SOT-223
SuperMESH3™ Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D	P _W
STN3N40K3	400 V	< 3.4 Ω	1.8 A	3.3 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Application

- Switching applications

Description

The device is made using the SuperMESH3™ Power MOSFET technology that is obtained via improvements applied to STMicroelectronics' SuperMESH3™ technology combined with a new optimized vertical structure. The resulting product has an extremely low on resistance, superior dynamic performance and high avalanche capability, making it especially suitable for the most demanding applications.

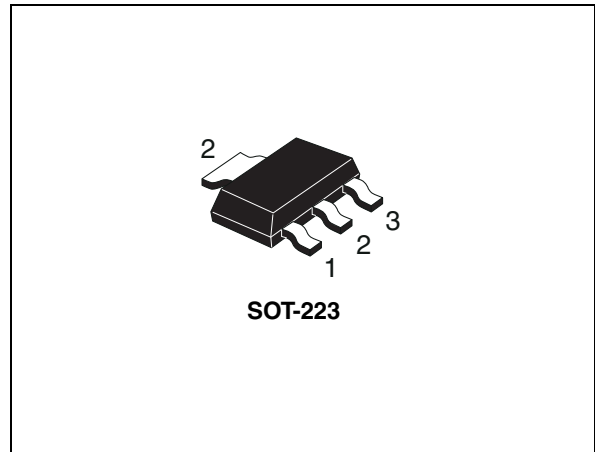


Figure 1. Internal schematic diagram

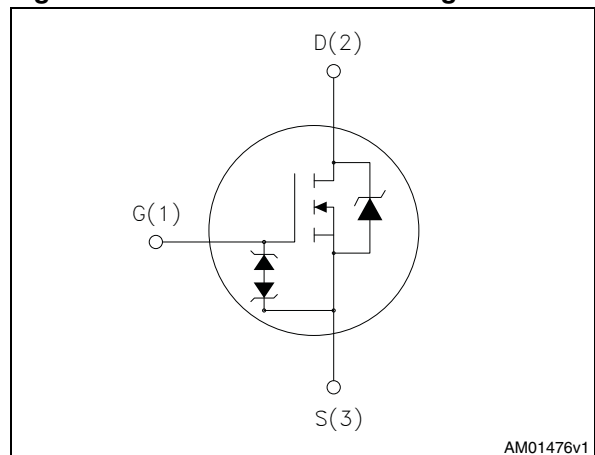


Table 1. Device summary

Order code	Marking	Package	Packaging
STN3N40K3	3N40K3	SOT-223	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain source voltage	400	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current continuous $T_C = 25\text{ }^{\circ}\text{C}$	1.8 ⁽¹⁾	A
I_D	Drain current continuous $T_C = 100\text{ }^{\circ}\text{C}$	1 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current pulsed	7.2	A
I_{AR} ⁽³⁾	Avalanche current, repetetive or not repetetive	0.6	A
E_{AS} ⁽⁴⁾	Single pulse avalanche energy	45	mJ
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	3.3	W
dv/dt ⁽⁵⁾	Peak diode recovery voltage slope	12	V/ns
$V_{esd-(g-s)}$	G-S ESD (HBM C 0 100 pF; R = 1.5 k Ω)	1000	V
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Drain current limited by maximum temperature allowed.
2. Pulse width limited by safe operating area.
3. Pulse width limited by T_{Jmax} .
4. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.
5. $I_{sd} \leq 1.8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	37.88	$^{\circ}\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-amb max.	60	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	260	$^{\circ}\text{C}$

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	400			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125 \text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{GS} = V_{DS}$, $I_D = 50 \text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}$, $I_D = 0.6 \text{ A}$		3	3.4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	165 17 3	-	pF pF pF
$C_{oss(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{DS} = 0 \text{ to } 320 \text{ V}$, $V_{GS} = 0$	-	9	-	pF
$C_{oss(tr)}^{(2)}$	Equivalent output capacitance time related		-	14	-	pF
R_g	Intrinsic gate resistance	$f = 1 \text{ MHz}$ open drain	-	10	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 320 \text{ V}$, $I_D = 1.8 \text{ A}$, $V_{GS} = 10 \text{ V}$ (see Figure 16)	-	11 2 7	-	nC nC nC

1. Is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

2. Is defined as a constant equivalent capacitance giving the same storage energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn on delay time	$V_{DD} = 200\text{ V}$, $I_D = 0.6$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	7	-	ns
t_r	Rise time			8		ns
$t_{d(off)}$	Turn off delay time			18		ns
t_f	Fall time			14		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1.8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				7.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 0.6\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	145		ns
Q_{rr}	Reverse recovery charge			490		nC
I_{RRM}	Reverse recovery current			7		A
t_{rr}	Reverse recovery time	$I_{SD} = 1.8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	166		ns
Q_{rr}	Reverse recovery charge			580		nC
I_{RRM}	Reverse recovery current			7		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics

Figure 2. Safe operating area

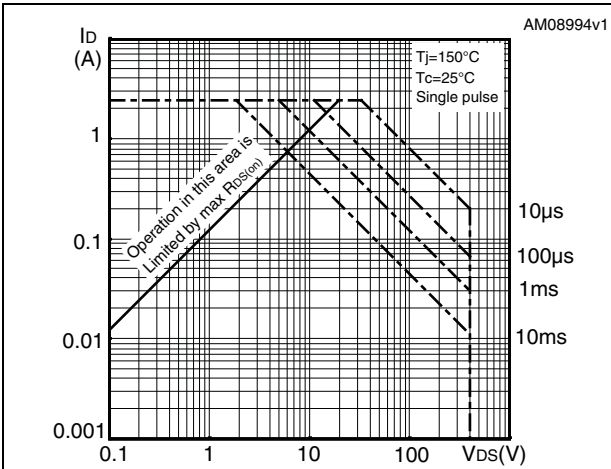


Figure 3. Thermal impedance

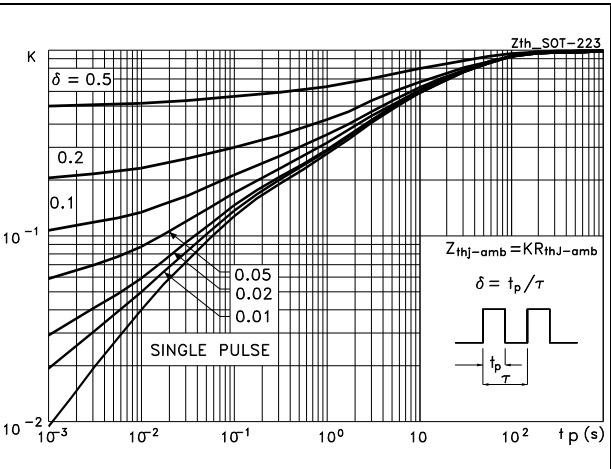


Figure 4. Output characteristics

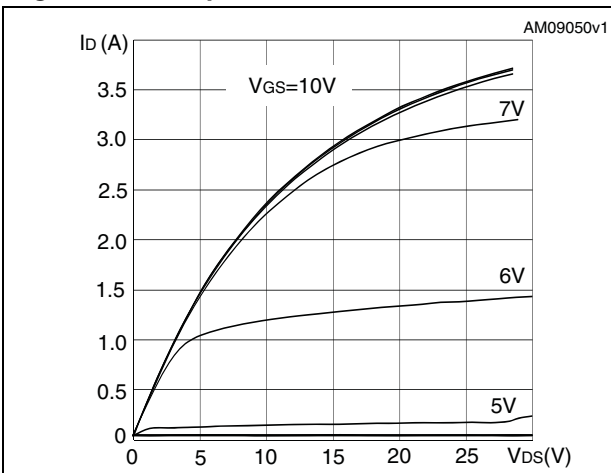


Figure 5. Transfer characteristics

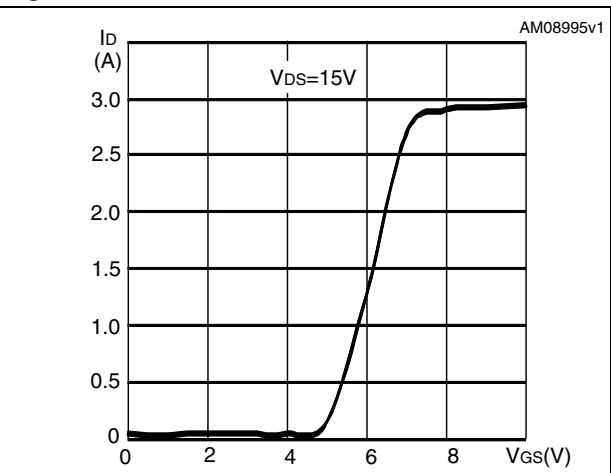


Figure 6. Gate charge vs gate-source voltage

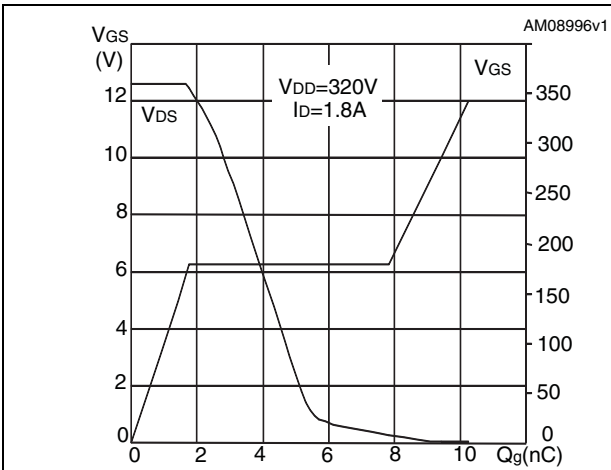


Figure 7. Static drain-source on resistance

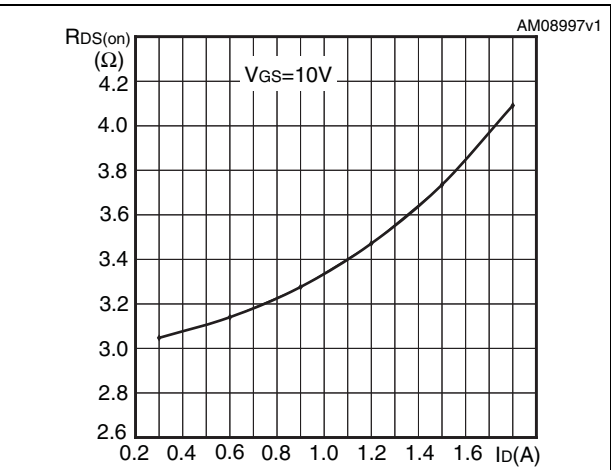


Figure 8. Capacitance variations

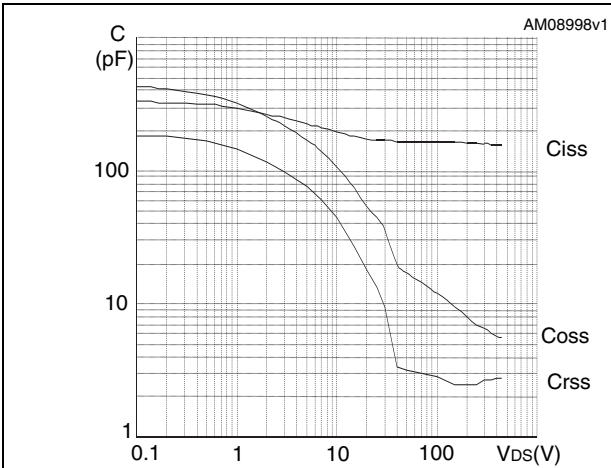


Figure 9. Output capacitance stored energy

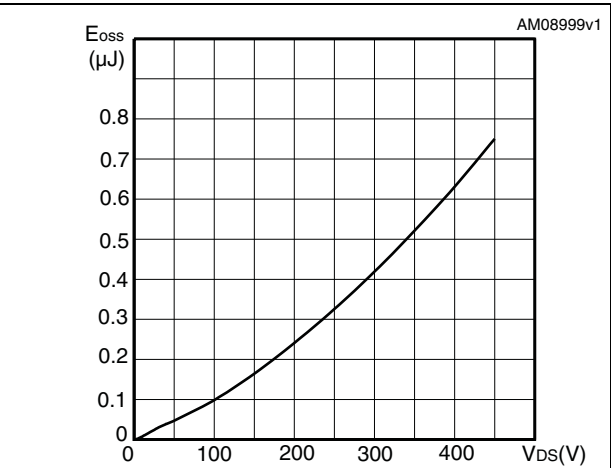


Figure 10. Normalized gate threshold voltage vs. temperature

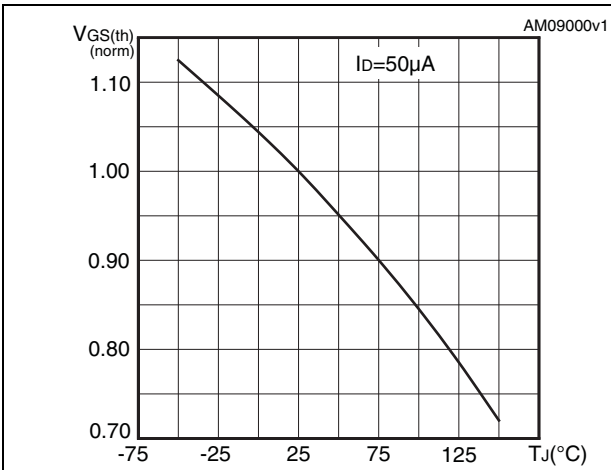


Figure 11. Normalized on resistance vs. temperature

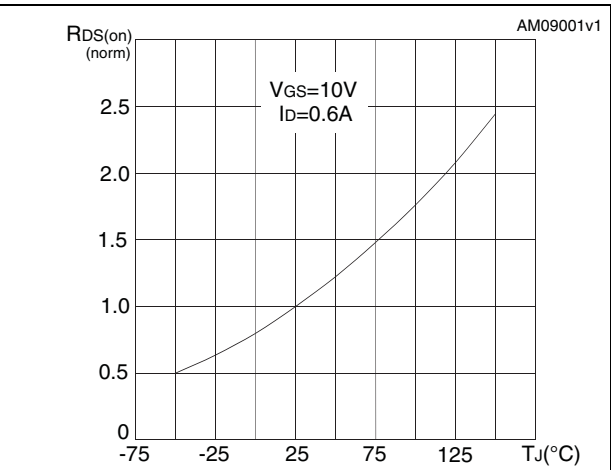


Figure 12. Source-drain diode forward characteristics

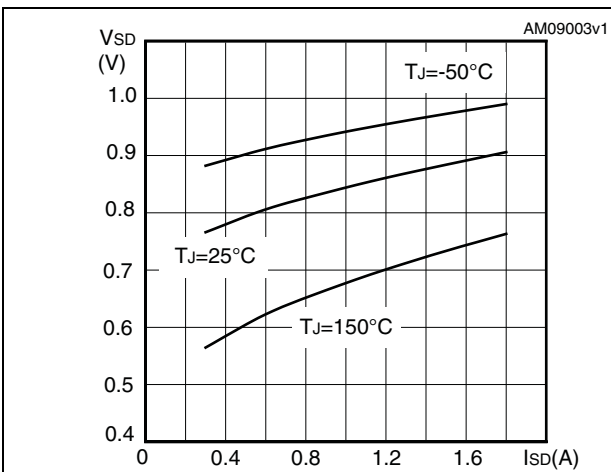


Figure 13. Normalized BVDS vs. temperature

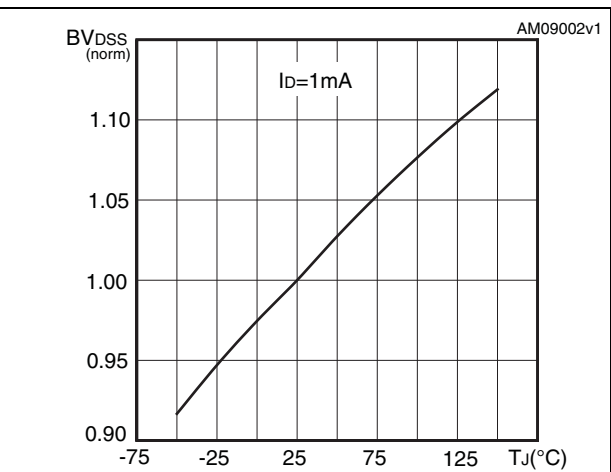
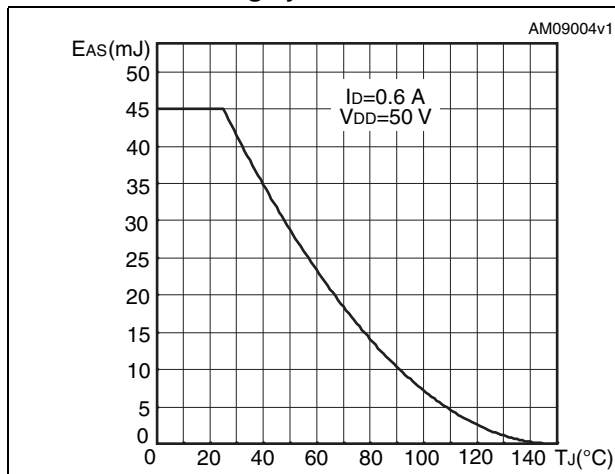


Figure 14. Maximum avalanche energy vs. starting T_J



3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times

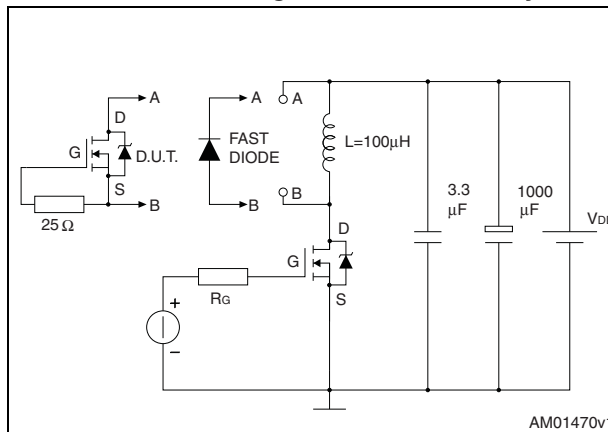


Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

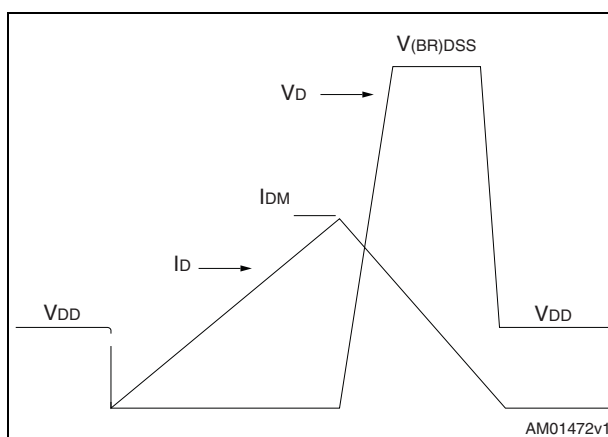
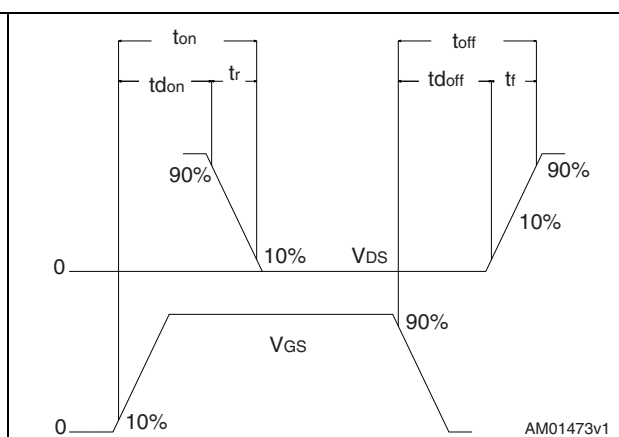


Figure 20. Switching time waveform



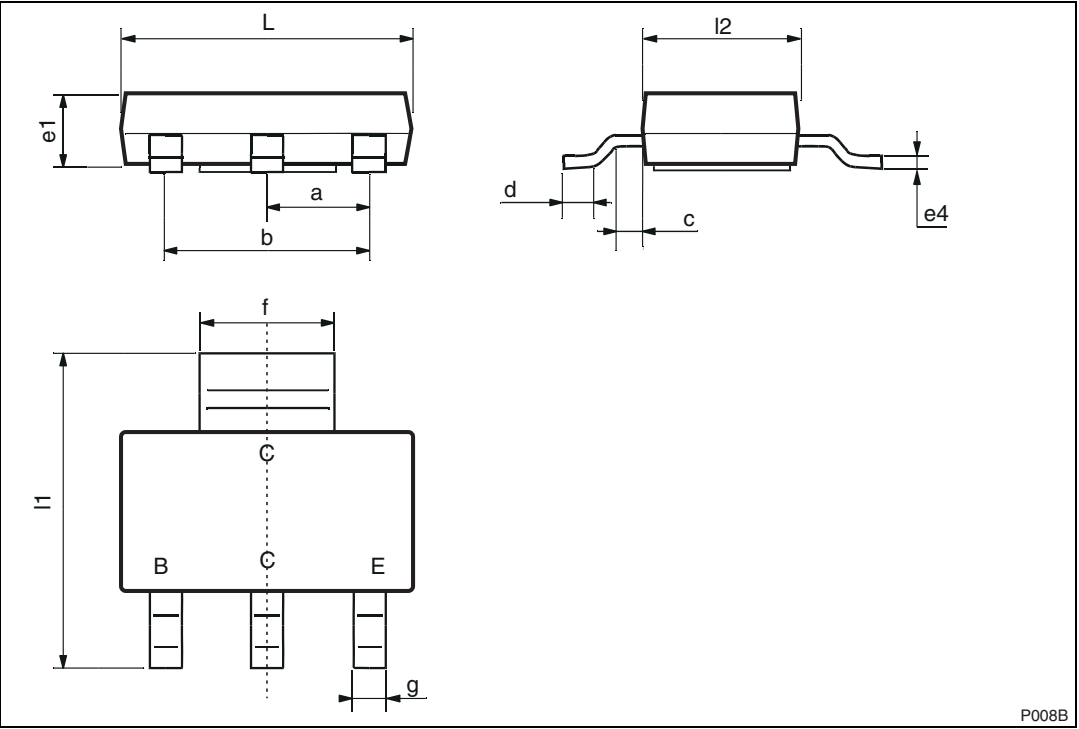
4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
a	2.27	2.3	2.33
b	4.57	4.6	4.63
c	0.2	0.4	0.6
d	0.63	0.65	0.67
e1	1.5	1.6	1.7
e4			0.32
f	2.9	3	3.1
g	0.67	0.7	0.73
l1	6.7	7	7.3
l2	3.5	3.5	3.7
L	6.3	6.5	6.7

Figure 21. SOT-223 mechanical data drawing



P008B

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jun-2010	1	First release.
08-Apr-2011	2	Document status promoted from preliminary data to datasheet.

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