Ordering number : ENA2252A

STK682-010-E

Thick Film Hybrid IC

2-phase Stepping Motor Driver

ON Semiconductor®

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Overview

The STK682-010-E is a hybrid IC for use as a Bipolar, 2-phase stepping motor driver with PWM current control.

Function

- Output on-resistance (High side 0.3 Ω, Low side 0.25 Ω, Total 0.55 Ω ; Ta = 25°C, I_O = 2.5A)
- VMmax=36V(DC), Iopmax=3.0A
- 2, 1-2, W1-2, 2W1-2, 4W1-2, 8W1-2, 16W1-2, 32W1-2 phase excitation are selectable
- With built-in automatic half current maintenance energizing function
- Over current protection circuit
- Thermal shutdown circuit
- Input pull down resistance
- With reset pin and enable pin

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VMmax		36.0	V
Peak output current	Iopmax		3.0	A
Logic input voltage	VINmax		6.0	V
VREF input voltage	VREFmax		6.0	V
Operating substrate temperature	Tc		–20 to +105	°C
Storage temperature	Tstg		–40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

Recommended Operating Conditions at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		9.0 to 32.0	V
Logic input voltage range	VIN		0 to 5.0	V
V_{CC} input voltage range	V_{CC}		0 to 5.0	V
VREF input voltage range	VREF		0 to 3.0	V
Output current1	Io1	1-2 Phase-ex, Tc ≤ 90°C	3.0	A
Output current2	Io2	1-2 Phase-ex, Tc=105°C	2.5	A
Output current3	Io3	2 Phase-ex, Tc=105°C	1.8	A

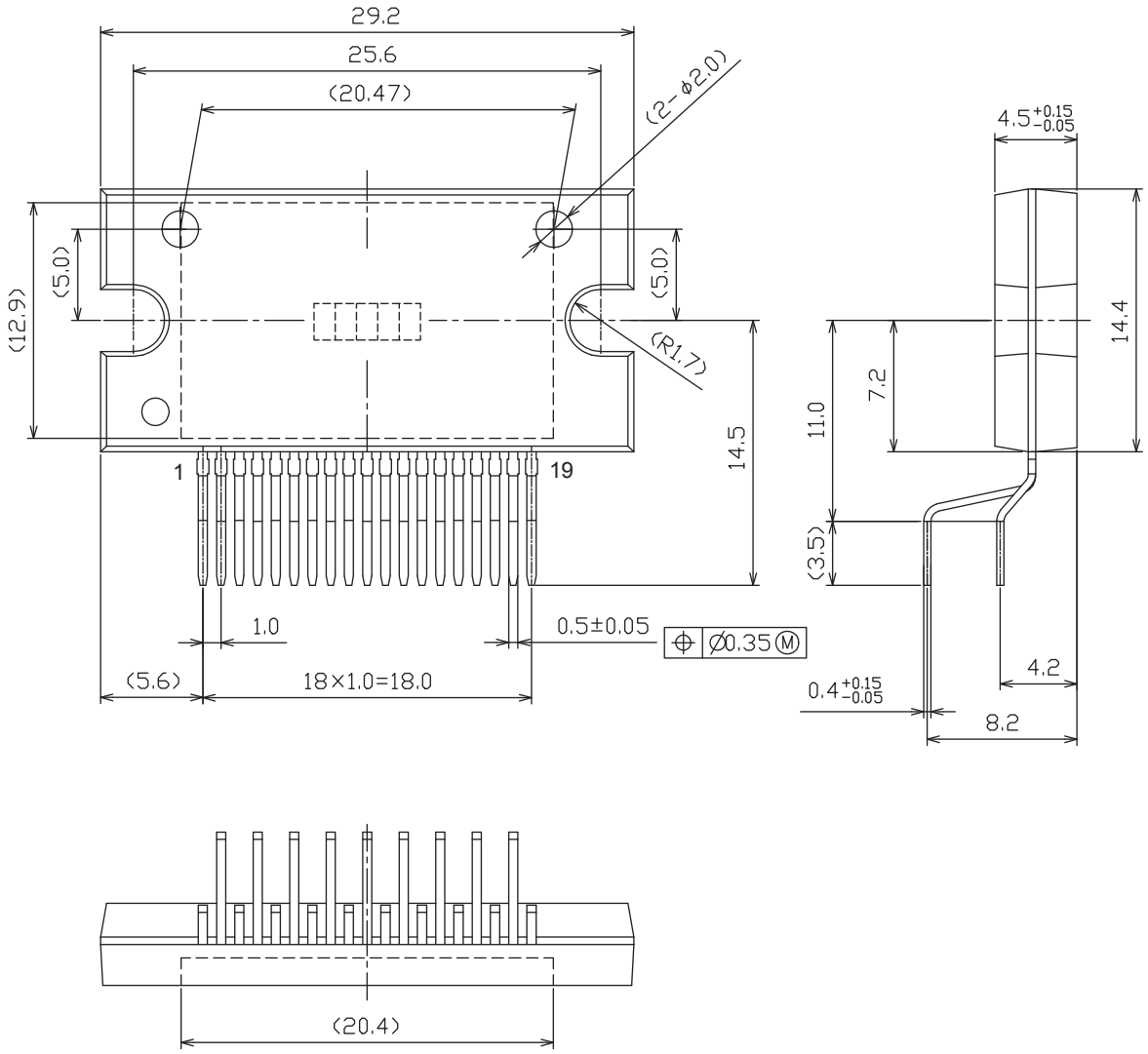
Electrical Characteristics at Tc = 25°C, V_{CC} = 5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	IMstn	VCC="L"		70	100	μA
Current drain	IM	VCC="H", ENABLE="H" No Load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	210	°C
Thermal hysteresis width	ΔTSD	Design guarantee		40		°C
Logic pin input current	IinL1	VIN=0.8V	3	8	15	μA
	IinH1	VIN=5V	30	50	70	μA
V_{CC} pin input current	V_{CC}	15pin=5V	51	83	115	μA
Logic input high-level voltage	Vinh	Pins 2,3,16,17,18,19	2.0			V
Logic input low-level voltage	Vinl	Pins 2,3,16,17,18,19			0.8	V
FDT pin high-level voltage	Vfdth	Pin 6	3.5			V
FDT pin middle-level voltage	Vfdtm	Pin 6	1.1		3.1	V
FDT pin low-level voltage	Vfdtl	Pin 6			0.8	V
Chopping frequency	Fch	C1=100pF	58	83	108	kHz
Chopping frequency	Iosc1			10		μA
Chopping oscillator circuit threshold voltage	Vtup1			1		V
	Vtdown1			0.5		V
VREF pin input voltage	Iref	VREF=1.5V, CLK=10kHz	−0.5			μA
DOWN output residual voltage	VolDO	Idown=1mA, CLK=Low		40		mV
Hold current switching frequency	Falert			1.6		Hz
Blanking time	Tb1			1		μs
Output block						
Output on-resistance	Ronu	I_O=2.0A, high-side ON resistance		0.30	0.42	Ω
	Rond	I_O=2.0A, low-side ON resistance		0.25	0.35	Ω
Output leakage current	Ioleak	VM=36V			50	μA
Diode forward voltage	VD	ID=−2.0A		1.1	1.4	V
Current setting reference voltage	VRF	VREF=1.5V, Current ratio 100%		300		mV
Output short-circuit protection block						
Timer latch time	Tscp			256		μs

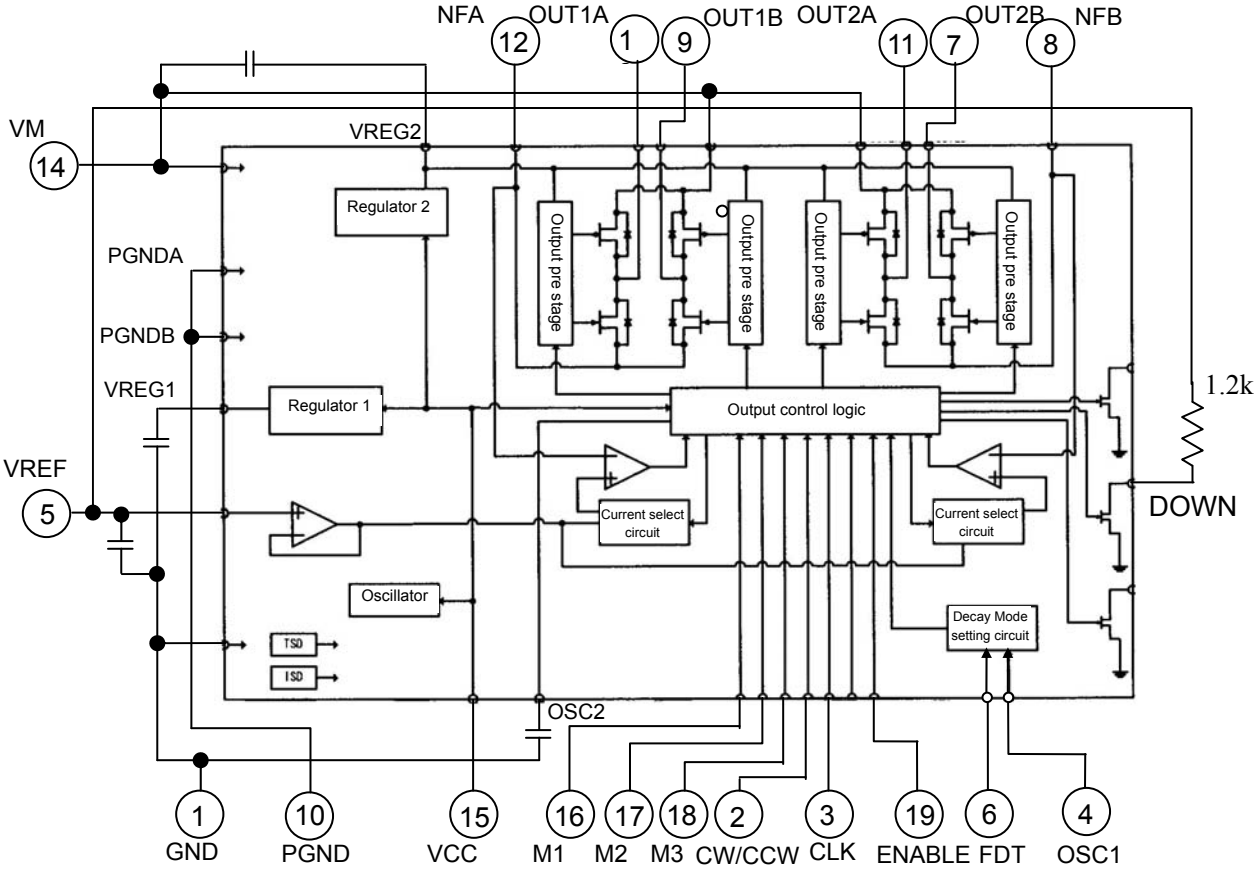
Package Dimensions

unit : mm

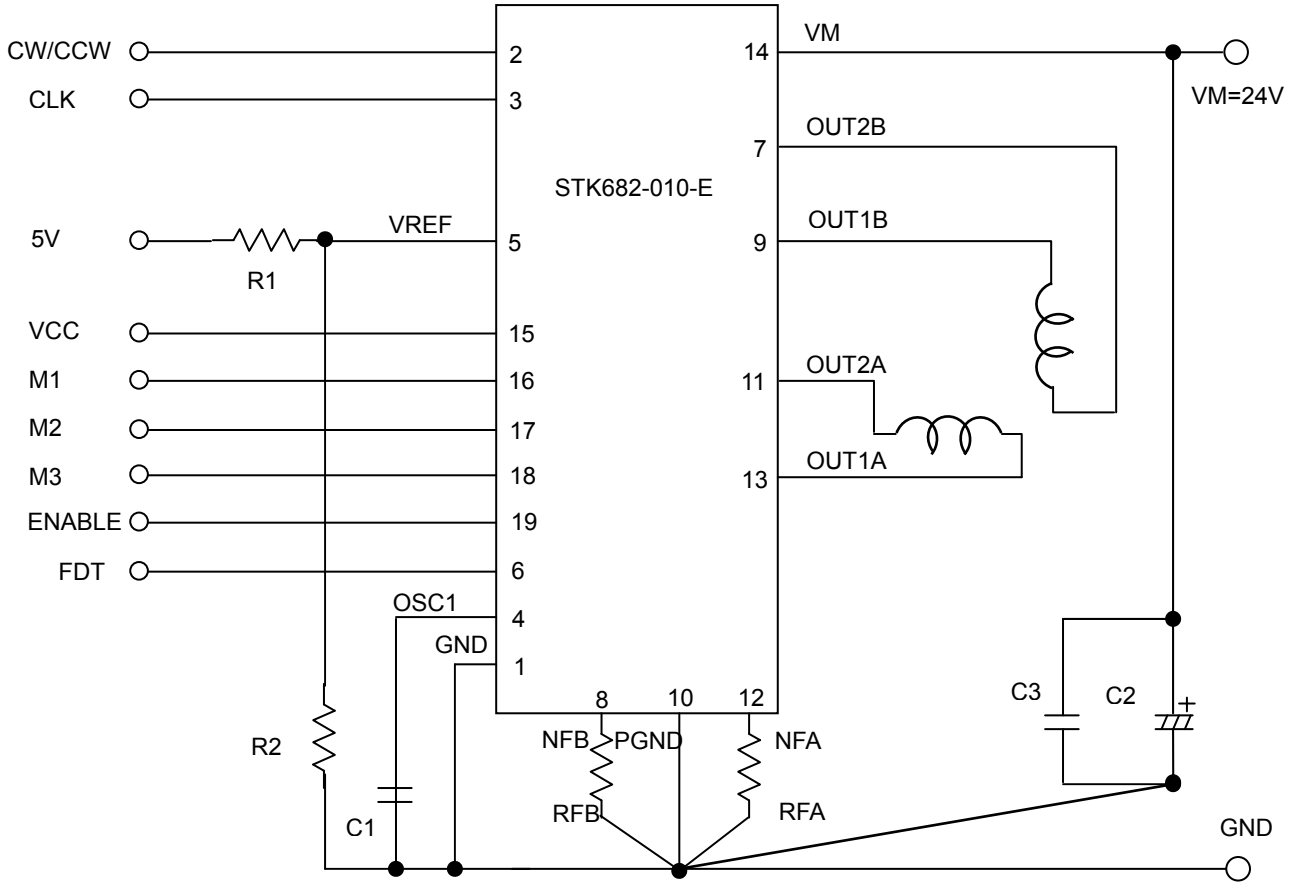
SIP19 29.2x14.4
CASE 127CF
ISSUE O



Block diagram



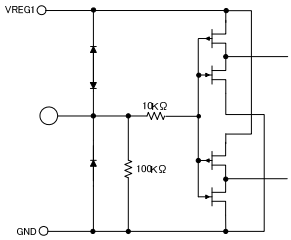
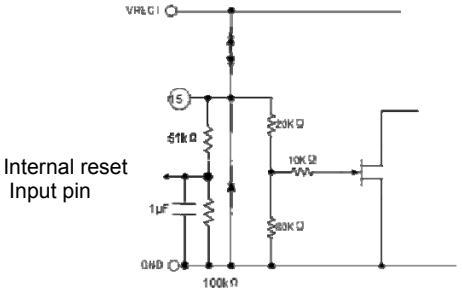
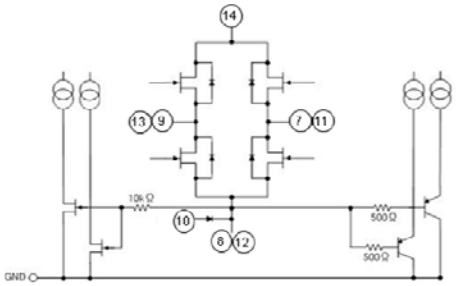
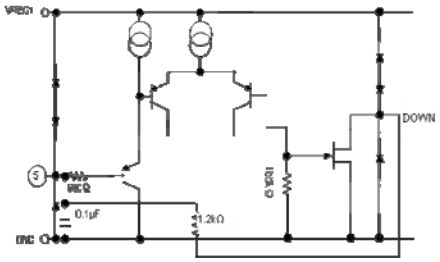
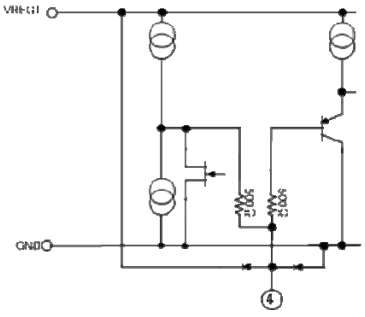
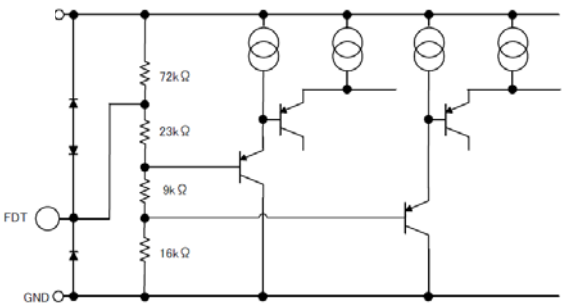
Application Circuit Example



Pin Functions

Pin No.	Pin symbol	Pin Functions
1	GND	Circuit GND
2	CW/CCW	Forward / Reverse signal input
3	CLK	Clock pulse signal input
4	OSC1	Chopping frequency setting capacitor connection
5	VREF	Constant-current control reference voltage input
6	FDT	Decay mode select voltage input
7	OUT2B	B phase OUTB output
8	NFB	B phase current sense resistance connection
9	OUT1B	B phase OUTA output
10	PGND	Power GND
11	OUT2A	A phase OUTB output
12	NFA	A phase current sense resistance connection
13	OUT1A	A phase OUTA output
14	VM	Motor supply connection
15	VCC	Chip enable input
16	M1	Excitation-mode switching pin
17	M2	
18	M3	
19	ENABLE	Output enable signal input

Equivalent circuit diagram

Pin No.	Pin type	Equivalent Circuit Diagram
3 2 19 18 17 16	CLK CW/CCW ENABLE M3 M2 M1	
15	VCC	
13 10 14 12 11 9 8 7	OUT1A PGND VM NFA OUT2A OUT1B NFB OUT2B	
5	VREF	
4	OSC1	
6	FDT	

Description of functions

(1) Excitation setting method

Set the excitation setting as shown in the following table by setting M1 pin, M2 pin and M3 pin

Input signal			MODE (Excitation)	Initial position	
M3	M2	M1		A phase current	B phase current
L	L	L	2 Phase	100%	−100%
L	L	H	1-2 Phase	100%	0%
L	H	L	W1-2 Phase	100%	0%
L	H	H	2W1-2 Phase	100%	0%
H	L	L	4W1-2 Phase	100%	0%
H	L	H	8W1-2 Phase	100%	0%
H	H	L	16W1-2 Phase	100%	0%
H	H	H	32W1-2 Phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode

(2) Output current setting

Output current is set as shown below by the VREF pin (applied voltage) and a resistance value between NFA (B) pin and GND.

I_{OUT} = (VREF / 5) / NFA (B) resistance

* The setting value above is a 100% output current in each excitation mode.

(Example) When VREF=1.5V and NFA (B) resistance is 0.3 Ω, the setting current is shown below.

I_{OUT} = (1.5 V / 5) / 0.3 Ω = 1.0 A

(3) Chip enable terminal/ VCC function

When Chip enable terminal/ V_{CC} pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.

When Chip enable terminal/ V_{CC} pin is at high levels, the stand-by mode is released

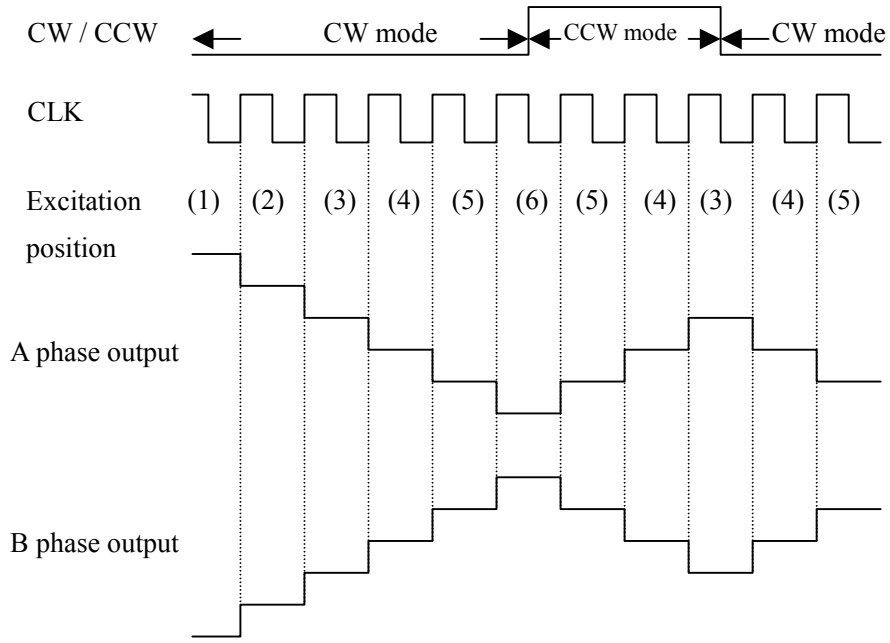
(4) Step pin function

CLK pin step signal input allows advancing excitation step

Input		Operation
V_{CC}	CLK	
L	*	Stand-by mode
H		Excitation step feed
H		Excitation step hold

(5) Forward / reverse switching function

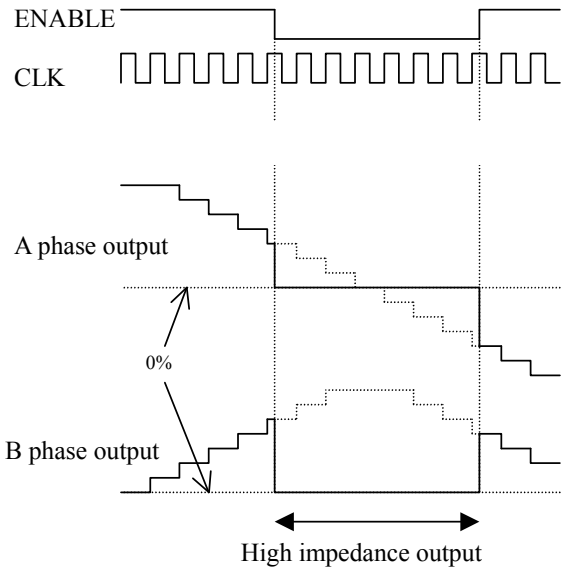
CW/CCW	Operation
L	CW
H	CCW



The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the CLK pin. In addition, CW and CCW mode are switched by CW and CCW pin setting.
In CW mode, the B phase current is delayed by 90° relative to the A phase current. In CCW mode, the B phase current is advanced by 90° relative to the A phase current.

(6) Output enable function

When the ENABLE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the CLK is input. Therefore, when ENABLE pin is returned to High, the output level conforms to the excitation position proceeded by the CLK input.



(7) DECAY mode

The DECAY mode of the output current becomes only MIXED DECAY.

FDT voltage	DECAY method
3.5V to	SLOW DECAY
1.1V to 3.1V or OPEN	MIXED DECAY
to 0.8V	FAST DECAY

(8) Chopping frequency setting function

Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$Fch = 1 / (C1+20pF / 10\times10^{-6})$ (Hz)

(Example) When Cosc1=100pF, the chopping frequency is shown below.

$Fch = 1 / ((20+ 100)\times10^{-12} / 10\times10^{-6})$ (Hz) = 83.3 (kHz)

Note

- The 20pF is a stray capacitance which is involved by the package of STK682-010-E.

(9) Output short-circuit protection circuit

Build-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected, short-circuit detection circuit starts the operating and output is once turned OFF. After the timer latch time (typ : 256μs), output is turned ON again. Still the output is at short state, the output is turned OFF and fixed in stand-by mode.

When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting Chip enable terminal/ V_{CC}="L"

(10) Internal DOWN pin

The DOWN pin is an open drain connection.

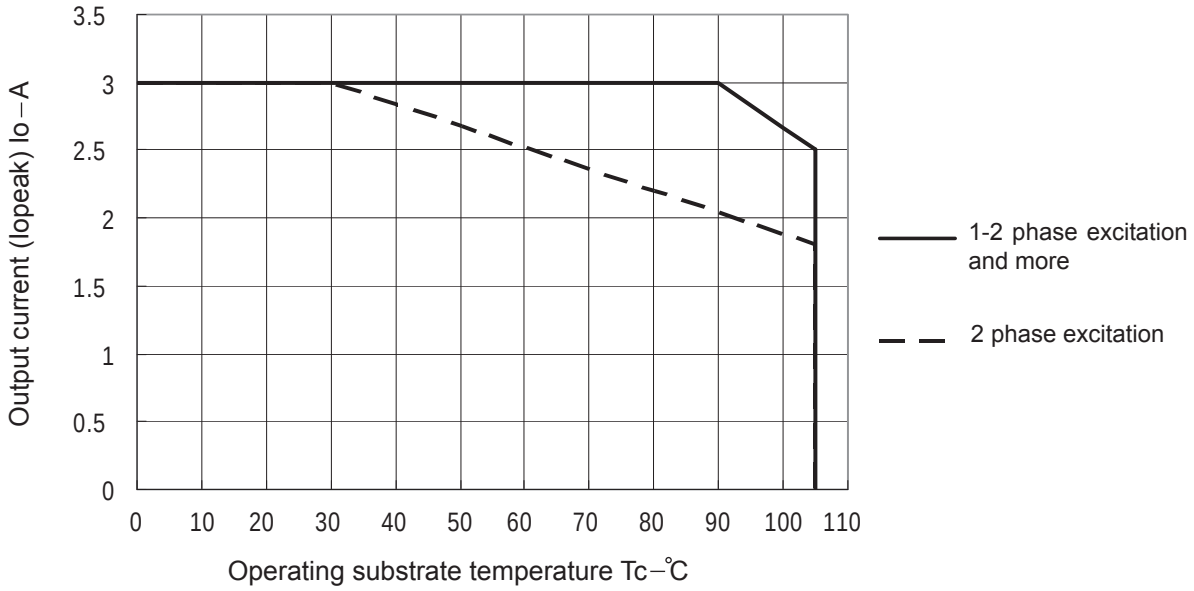
This pin is turned ON when no rising edge of CLK between the input signals while a period determined by a capacitor between OSC2 and GND, and outputs at low levels.

The DOWN pin output in once turned ON, is turned OFF at the next rising edge of CLK.

Holding current switching time (0.6sectyp) is set by an internal capacitor between OSC2 pin and GND.

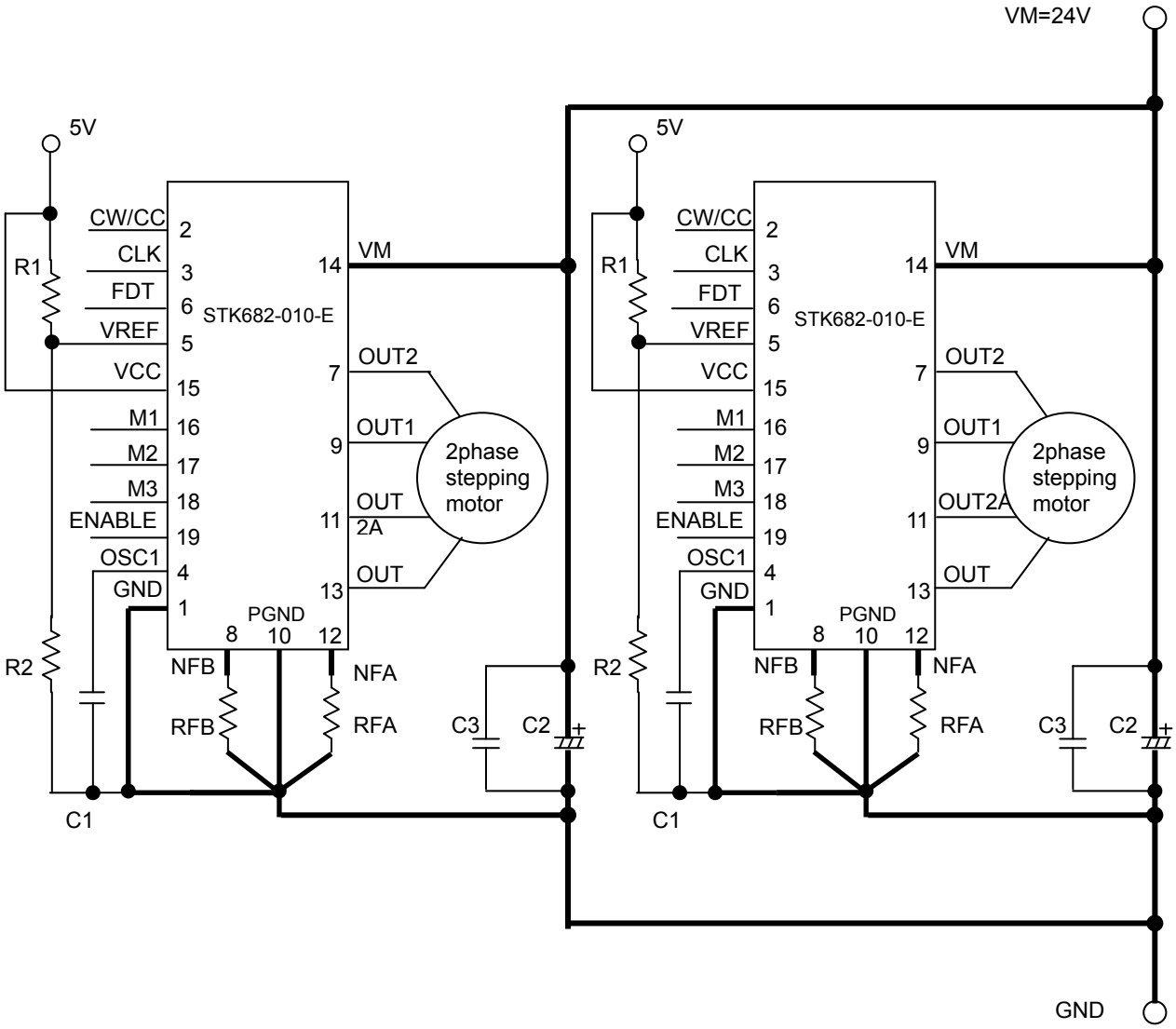
(11) Output current tolerance

STK682-010-E Output current tolerance Io－Tc

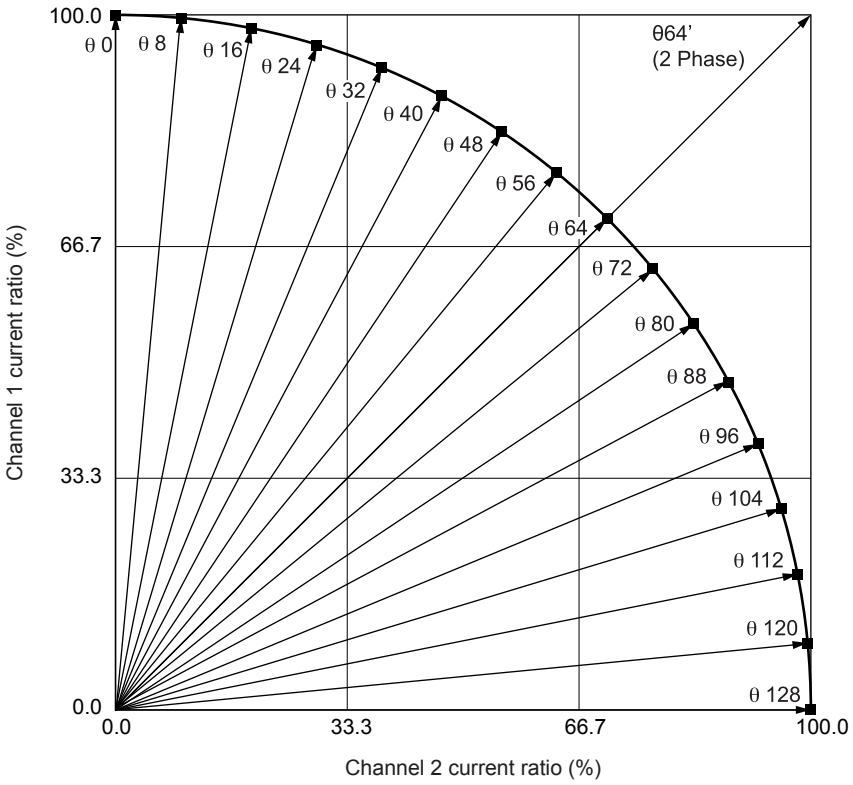


(12) When mounting multiple drivers on a single PC board

When mounting multiple drivers on a single PC board, the GND design should mount a VCC decoupling capacitor,C2 and C3, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.



(13) Output current vector locus (1 step normalized 90°)

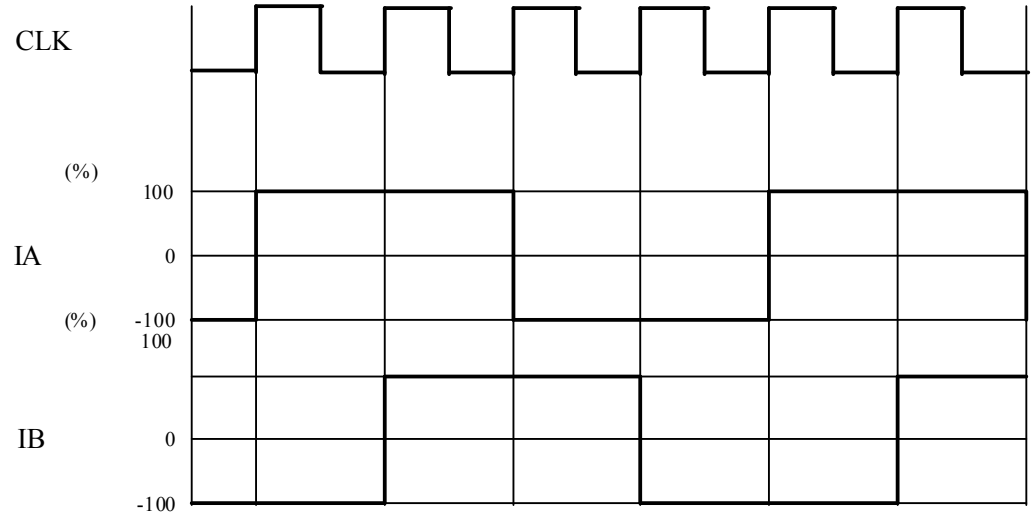


(14) Current setting ratio in each excitation mode

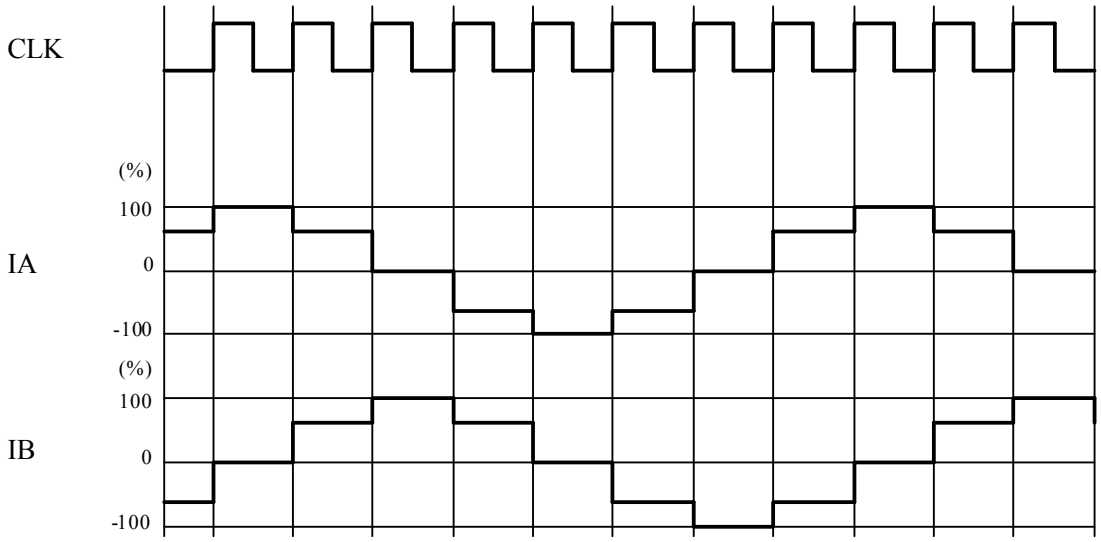
	32W1-2 phase(%		16W1-2 phase(%		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase(%)		W1-2 phase(%)		1-2 phase(%)		2 phase(%)			32W1-2 phase(%		16W1-2 phase(%		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase(%)		W1-2 phase(%)		1-2 phase(%)		2 phase(%)	
STEP	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	STEP	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch
θ0	100	0	100	0	100	0	100	0	100	0	100	0	100	0			θ65	70	72														
θ1	100	1															θ66	69	72	69	72												
θ2	100	2	100	2													θ67	68	73														
θ3	100	4															θ68	67	74	67	74	67	74										
θ4	100	5	100	5	100	5											θ69	66	75														
θ5	100	6															θ70	65	76	65	76												
θ6	100	7	100	7													θ71	64	77														
θ7	100	9															θ72	63	77	63	77	63	77	63	77								
θ8	100	10	100	10	100	10	100	10									θ73	62	78														
θ9	99	11															θ74	62	79	62	79												
θ10	99	12	99	12													θ75	61	80														
θ11	99	13															θ76	60	80	60	80	60	80										
θ12	99	15	99	15	99	15											θ77	59	81														
θ13	99	16															θ78	58	82	58	82												
θ14	99	17	99	17													θ79	57	82														
θ15	98	18															θ80	56	83	56	83	56	83	56	83	56	83						
θ16	98	20	98	20	98	20	98	20	98	20							θ81	55	84														
θ17	98	21															θ82	53	84	53	84												
θ18	98	22	98	22													θ83	52	85														
θ19	97	23															θ84	51	86	51	86	51	86										
θ20	97	24	97	24	97	24											θ85	50	86														
θ21	97	25															θ86	49	87	49	87												
θ22	96	27	96	27													θ87	48	88														
θ23	96	28															θ88	47	88	47	88	47	88	47	88								
θ24	96	29	96	29	96	29	96	29									θ89	46	89														
θ25	95	30															θ90	45	89	45	89												
θ26	95	31	95	31													θ91	44	90														
θ27	95	33															θ92	43	90	43	90	43	90										
θ28	94	34	94	34	94	34											θ93	42	91														
θ29	94	35															θ94	41	91	41	91												
θ30	93	36	93	36													θ95	39	92														
θ31	93	37															θ96	38	92	38	92	38	92	38	92	38	92						
θ32	92	38	92	38	92	38	92	38	92	38	92	38					θ97	37	93														
θ33	92	39															θ98	36	93	36	93												
θ34	91	41	91	41													θ99	35	94														
θ35	91	42															θ100	34	94	34	94	34	94										
θ36	90	43	90	43	90	43											θ101	33	95														
θ37	90	44															θ102	31	95	31	95												
θ38	89	45	89	45													θ103	30	95														
θ39	89	46															θ104	29	96	29	96	29	96	29	96								
θ40	88	47	88	47	88	47	88	47									θ105	28	96														
θ41	88	48															θ106	27	96	27	96												
θ42	87	49	87	49													θ107	25	97														
θ43	86	50															θ108	24	97	24	97	24	97										
θ44	86	51	86	51	86	51											θ109	23	97														
θ45	85	52															θ110	22	98	22	98												
θ46	84	53	84	53													θ111	21	98														
θ47	84	55															θ112	20	98	20	98	20	98	20	98	20	98						
θ48	83	56	83	56	83	56	83	56	83	56							θ113	18	98														
θ49	82	57															θ114	17	99	17	99												
θ50	82	58	82	58													θ115	16	99														
θ51	81	59															θ116	15	99	15	99	15	99										
θ52	80	60	80	60	80	60											θ117	13	99														
θ53	80	61															θ118	12	99	12	99												
θ54	79	62	79	62													θ119	11	99														
θ55	78	62															θ120	10	100	10	100	10	100	10	100								
θ56	77	63	77	63	77	63	77	63									θ121	9	100														
θ57	77	64															θ122	7	100	7	100												
θ58	76	65	76	65													θ123	6	100														
θ59	75	66															θ124	5	100	5	100	5	100										
θ60	74	67	74	67	74	67											θ125	4	100														
θ61	73	68															θ126	2	100	2	100												
θ62	72	69	72	69													θ127	1	100														
θ63	72	70															θ128	0	100	0	100	0	100	0	100	0	100	0	100				
θ64	71	71	71	71	71	71	71	71	71	71	71	71	71	71	100	100																

(15) Current wave example in each excitation mode (2 phase, 1-2 phase, W1-2 phase, 4W1-2 phase)

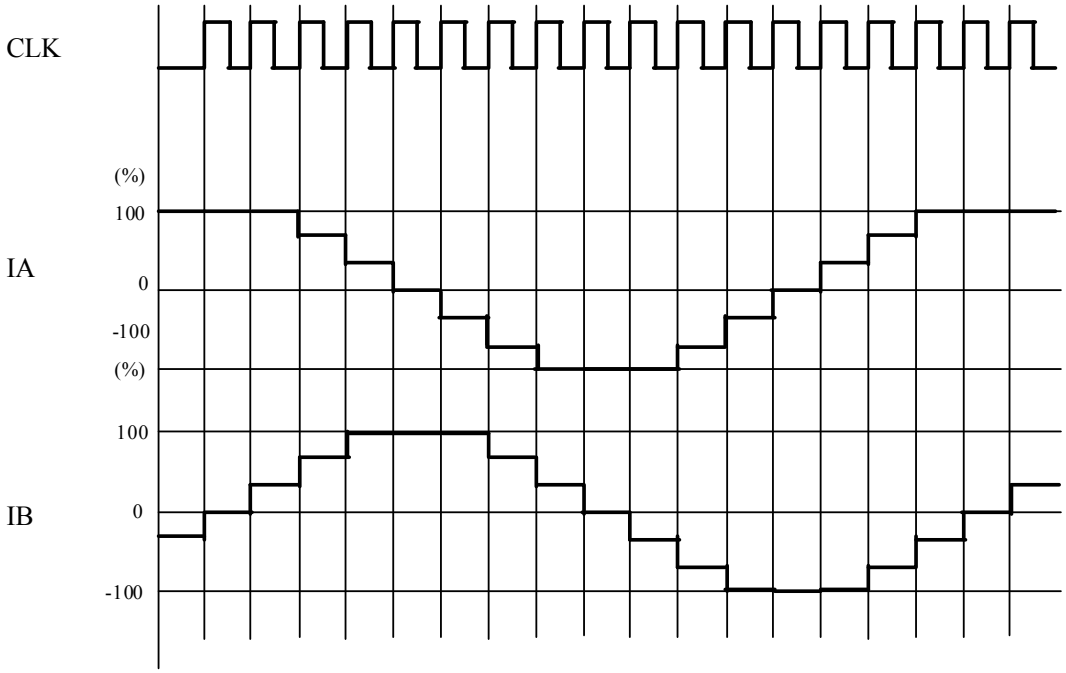
2 phase excitation (CW mode)



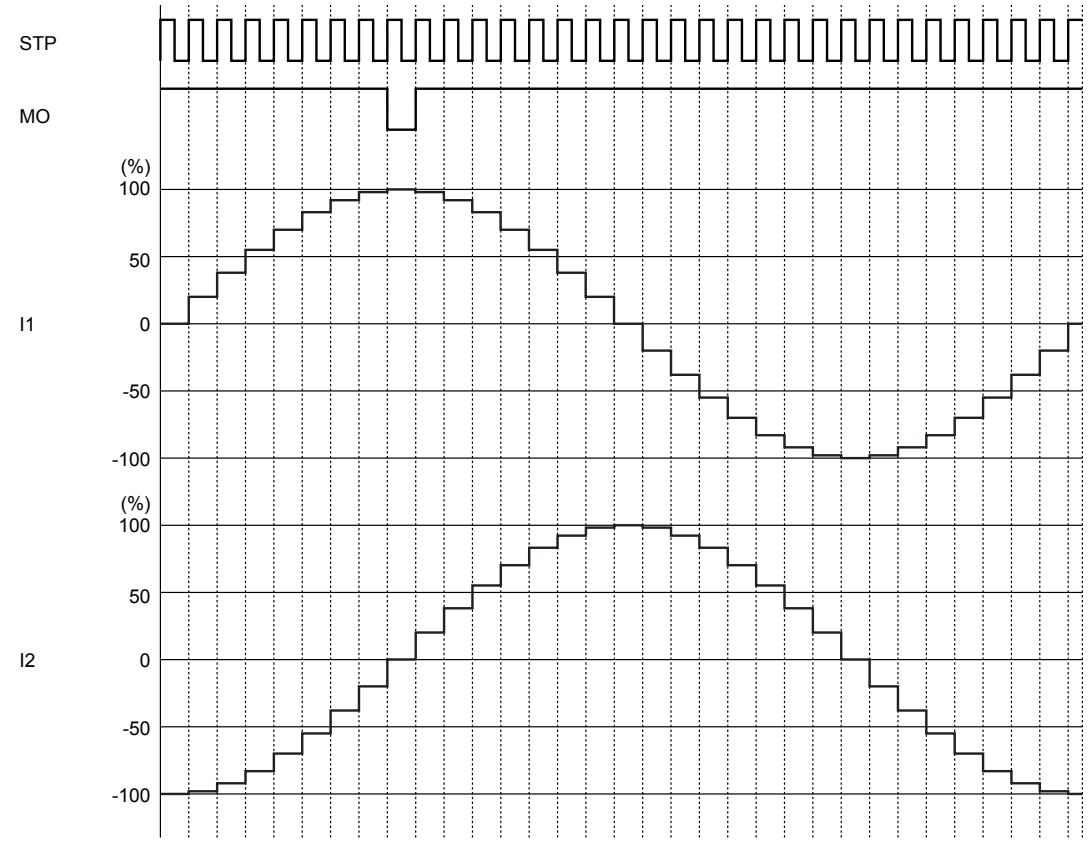
1-2 phase excitation (CW mode)



W1-2 phase excitation (CW mode)



4W1-2 phase excitation (CW mode)

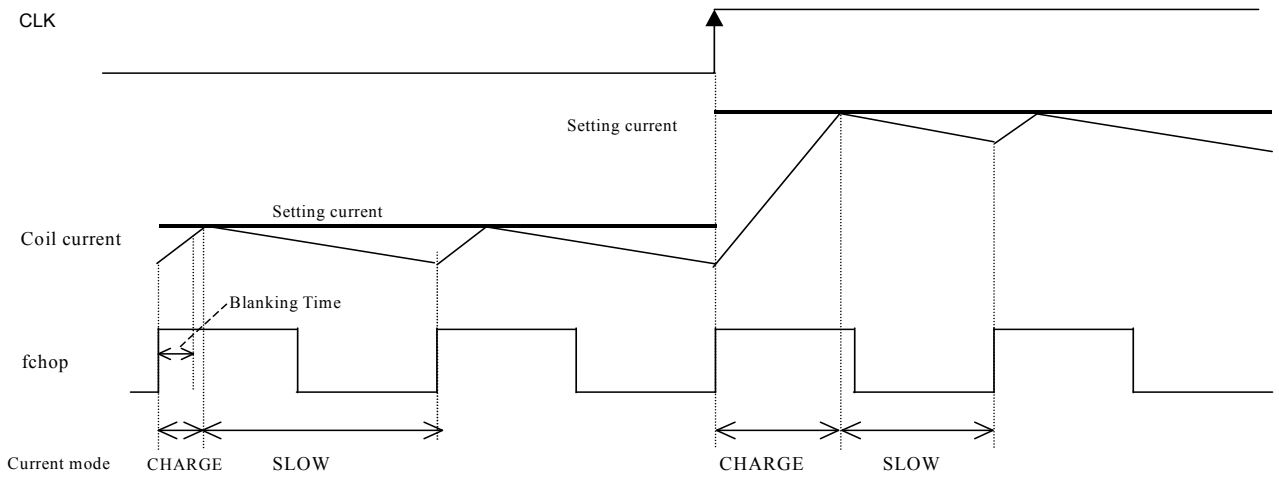


(16) Current control operation

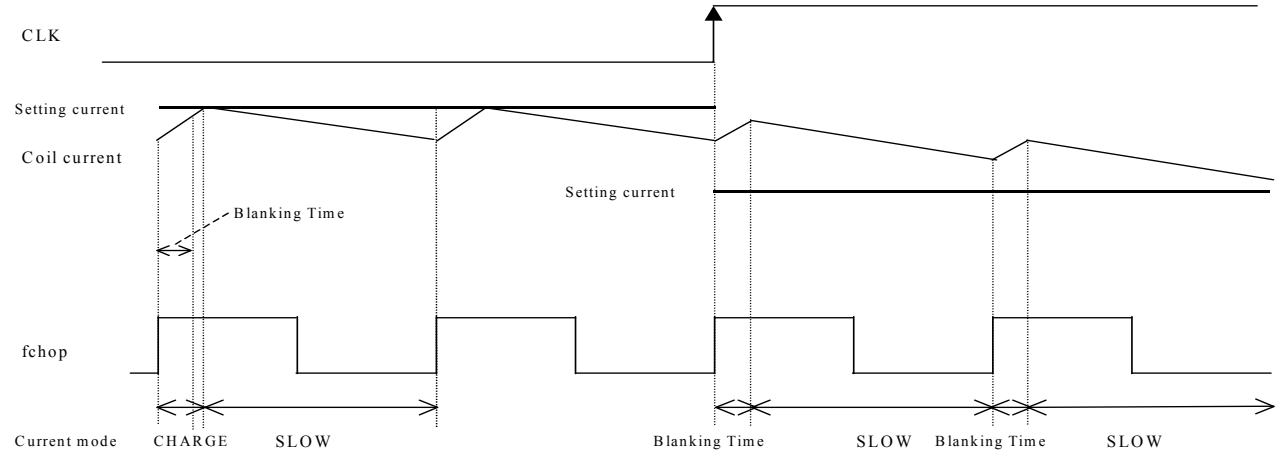
SLOW DECAY current control operation

When FDT pin voltage is a voltage over 3.5 V, the constant-current control is operated in SLOW DECAY mode.

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



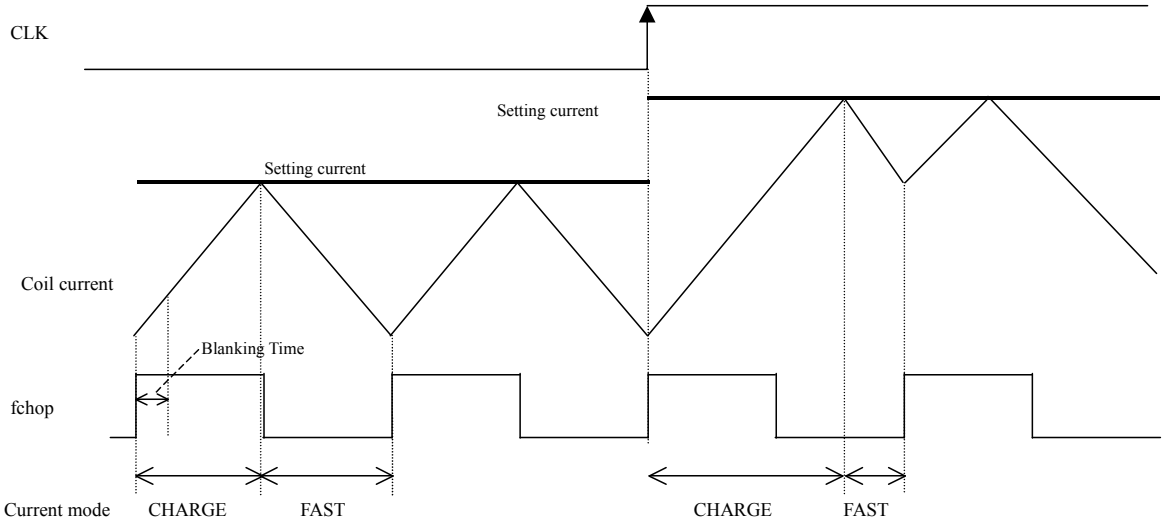
Each of current modes operates with the follow sequence.

- The IC enters CHARGE mode at a rising edge of the chopping oscillation.
  (A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1 μs, regardless of the current value of the coil current (ICOIL) and set current (IREF)).
- After the period of the blanking time, the IC operates in CHARGE mode until ICOIL ≥ IREF. After that, the mode switches to the SLOW DECAY mode and the coil current is attenuated until the end of a chopping period.
  At the constant-current control in SLOW DECAY mode, following to the setting current from the coil current may take time (or not follow) for the current delay attenuation.

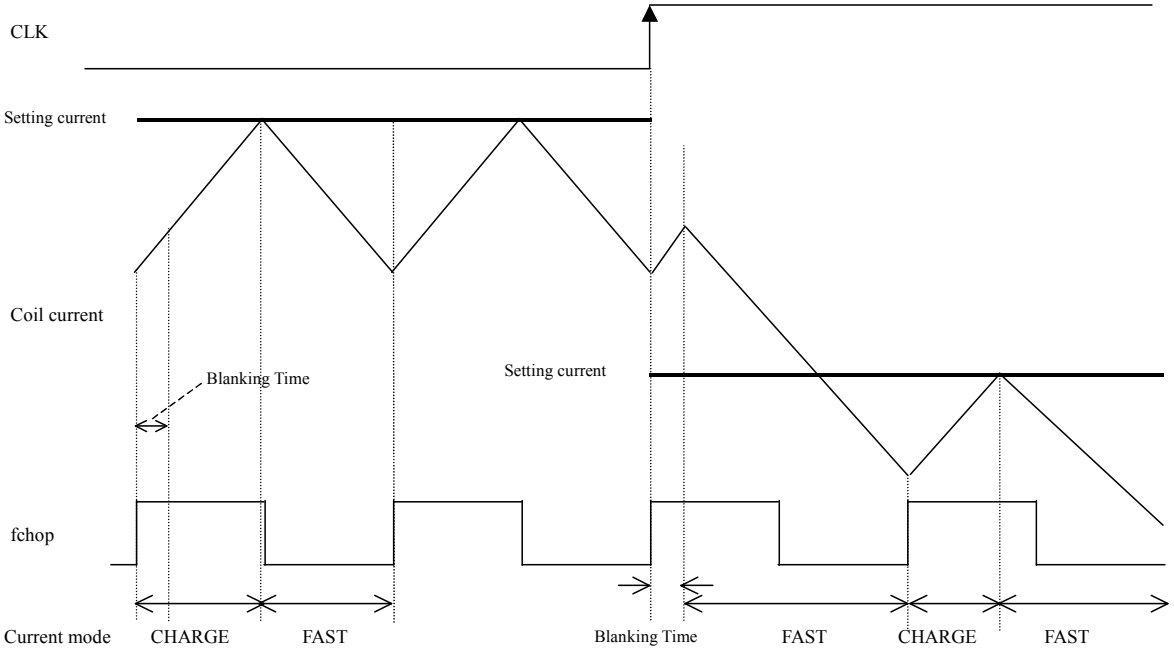
FAST DECAY current control operation

When FDT pin voltage is a voltage under 0.8V, the constant-current control is operated in FAST DECAY mode.

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



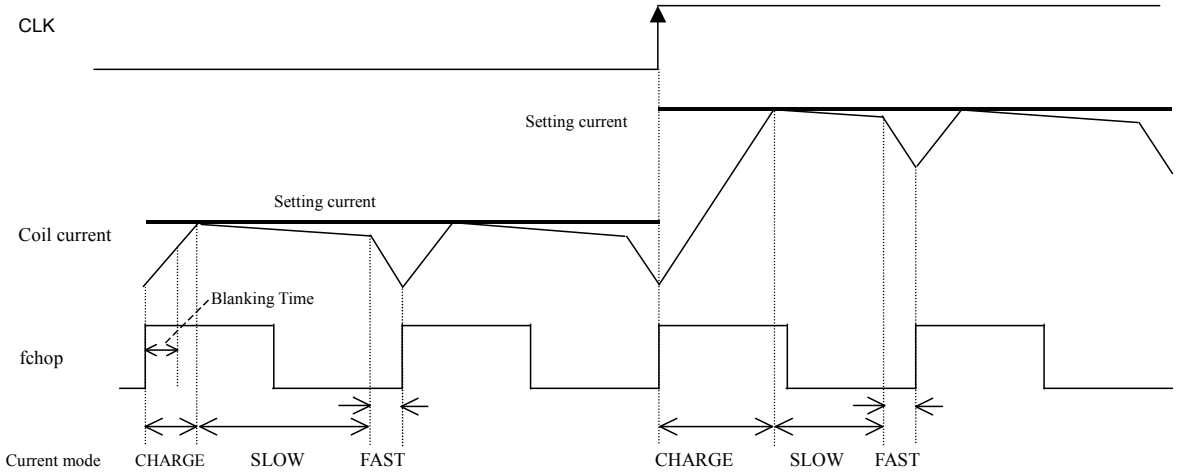
Each of current modes operates with the follow sequence.

The IC enters CHARGE mode at a rising edge of the chopping oscillation.
(A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1μs, regardless of the current value of the coil current (ICOIL) and set current (IREF)).

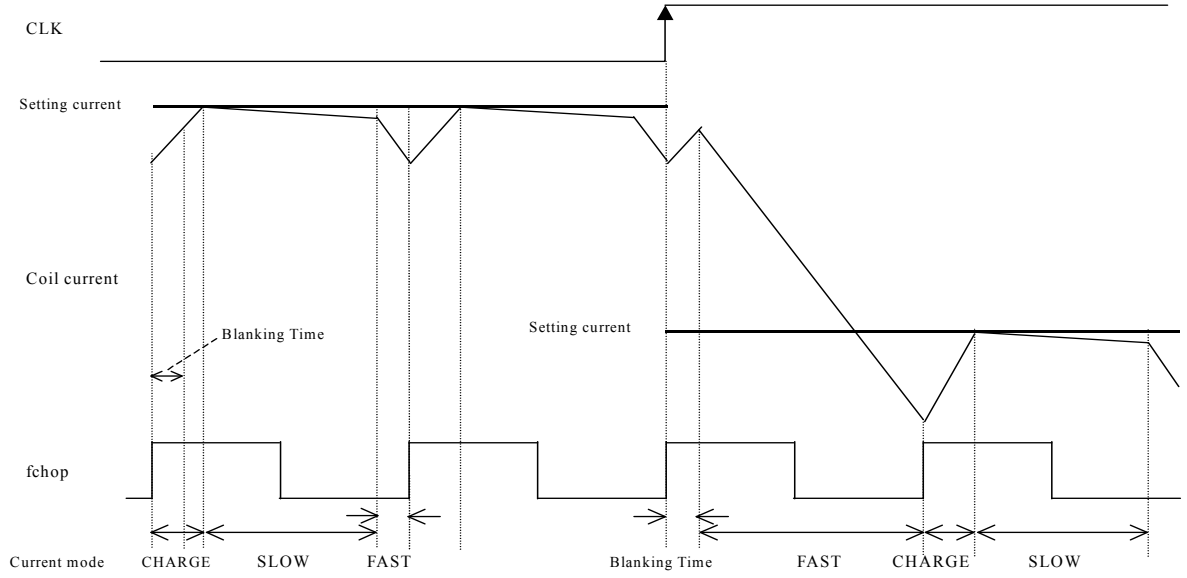
After the period of the blanking time, The IC operates in CHARGE mode until ICOIL ≥ IREF. After that, the mode switches to the FAST DECAY mode and the coil current is attenuated until the end of a chopping period. At the constant-current control in FAST DECAY mode, following to the setting current from the coil current takes short-time for the current fast attenuation, but, the current ripple value may be higher.

MIXED DECAY current control operation

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



Each of current modes operates with the follow sequence.
The IC enters CHARGE mode at a rising edge of the chopping oscillation.
(A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1 μs, regardless of the current value of the coil current (ICOIL) and set current (IREF)).
In a period of Blanking Time, the coil current (ICOIL) and the setting current (IREF) are compared.

If an ICOIL = IREF state exists during the charge period:

The IC operates in CHAGE mode until ICOIL ≥ IREF. After that, it switches to SLOW DECAY mode and then switches to FAST DECAY mode in the last approximately 1 μs of the period.

If no ICOIL = IREF state exists during the charge period:

The IC switches to FAST DECAY mode and the coil current is attenuated with the FAST DECAY operation until the end of a chopping period.
The above operation is repeated.
Normally, in the sine wave increasing direction the IC operates in SLOW (+FAST) DECAY mode, and in the sine wave decreasing direction the IC operates in FAST DECAY mode until the current is attenuated and reaches the set value and the IC operates in SLOW (+FAST) DECAY mode.

Power Dissipation

Power dissipation calculation of STK682-010-E following becomes.
2-phase excitation
$Pd=IOH\times(Ronu + Rond)^2$
1-2-phase excitation
$Pd=0.71\times IOH\times(Ronu + Rond)^2$

Please by substituting from electrical characteristic table value of Rond and Ronu.

Thermal design

[Operating range in which a heat sink is not used]
Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.
The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to "Calculating Internal HIC Loss for the STK672-640C-E in the specification document.
Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

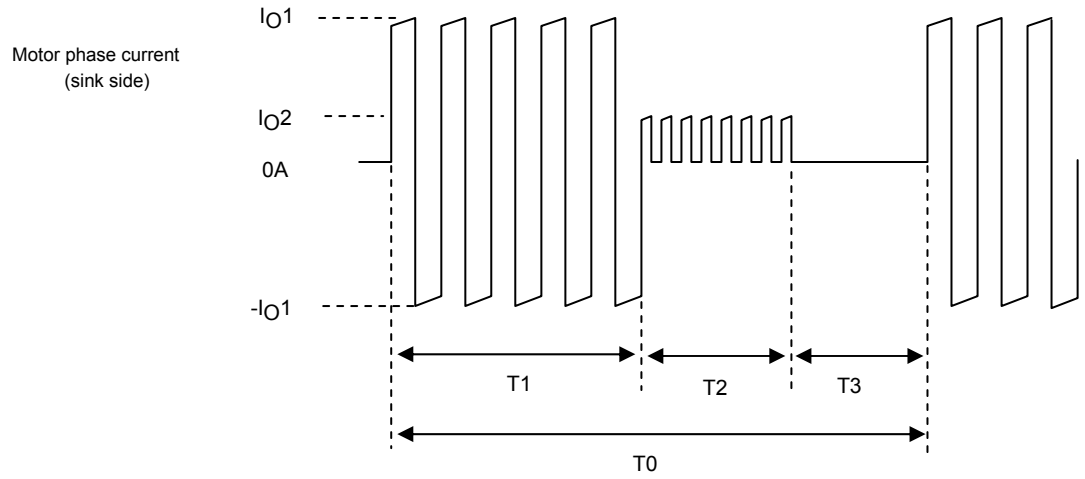


Figure 1 Motor Current Timing

T1 : Motor rotation operation time
T2 : Motor hold operation time
T3 : Motor current off time
T2 may be reduced, depending on the application.
T0 : Single repeated motor operating cycle
IO1 and IO2 : Motor current peak values
Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.
Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.
The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.
PdAV= (T1×P1+T2×P2+T3×0) · TO ---------- (I)
(Here, P1 is the PdAV for IO1 and P2 is the PdAV for IO2)
If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]
Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of c-a in Equation (II) below and the graph depicted in Figure 3.
c-a = (Tc max-Ta) · PdAV ---------- (II)
Tc max : Maximum operating substrate temperature =105°C
Ta : HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

Figure 2 Substrate temperature rise, ΔTc (no heat sink) - Internal average power dissipation, PdAV

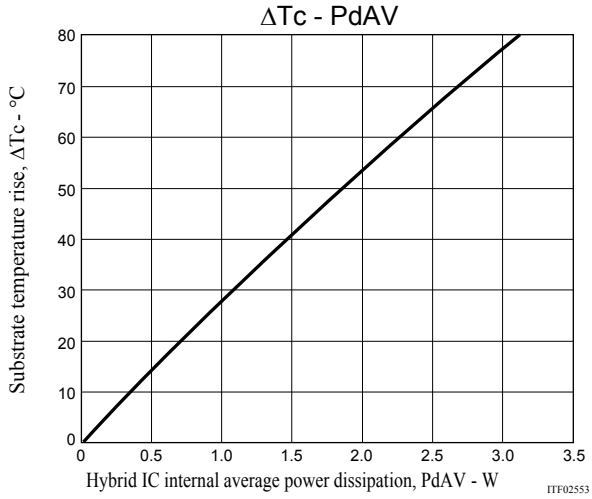
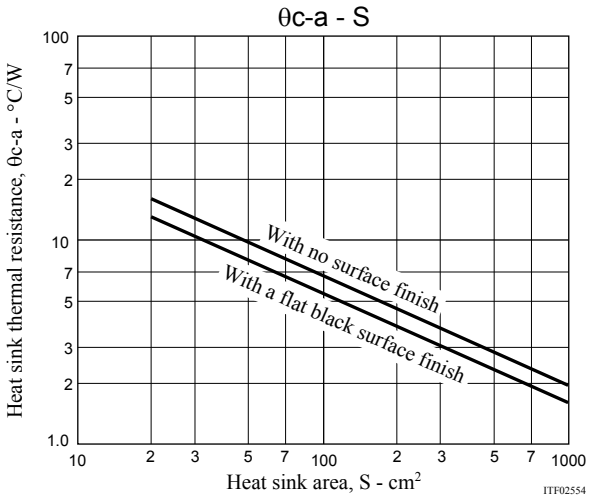
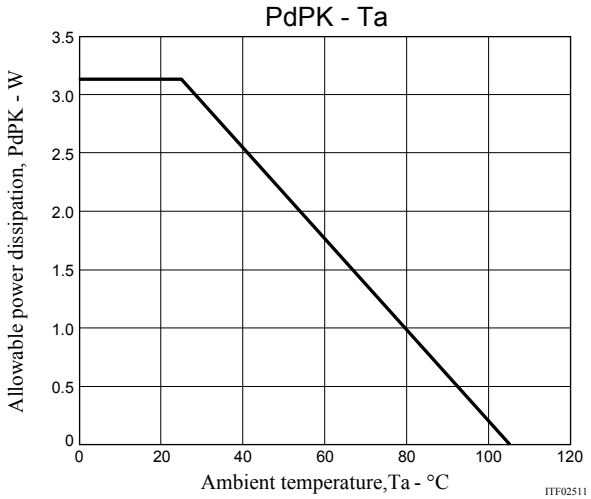


Figure 3 Heat sink area (Board thickness: 2mm) - θc-a



Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta
Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink.
The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta.
Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

Allowable power dissipation, PdPK(no heat sink) - Ambient temperature, Ta



ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK682-010-E	SIP-19 (Pb-Free)	15 / Tube