

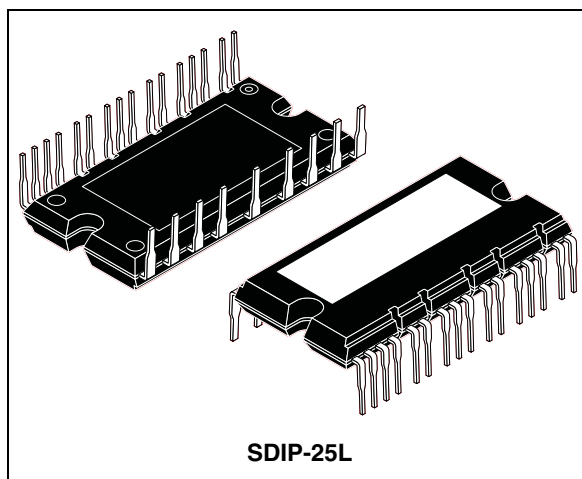


STGIPS20K60

IGBT intelligent power module (IPM)
17 A, 600 V, DBC isolated SDIP-25L molded

Features

- 17 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Internal bootstrap diode
- Interlocking function
- $V_{CE(sat)}$ negative temperature coefficient
- Short-circuit rugged IGBTs
- Undervoltage lockout
- Smart shutdown function
- Comparator for fault protection against over temperature and overcurrent
- DBC fully isolated package
- Isolation rating of 2500 Vrms/min



technology. Please refer to dedicated technical note TN0107 for mounting instructions.

Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners

Description

The STGIPS20K60 intelligent power module provides a compact, high performance AC motor drive for a simple and rugged design. It mainly targets low power inverters for applications such as home appliances and air conditioners. It combines ST proprietary control ICs with the most advanced short circuit rugged IGBT system

Table 1. Device summary

| Order code | Marking | Package | Packaging |
|-------------|-----------|----------|-----------|
| STGIPS20K60 | GIPS20K60 | SDIP-25L | Tube |

Contents

| | | |
|----------|---|-----------|
| 1 | Internal block diagram and pin configuration | 3 |
| 2 | Electrical ratings | 5 |
| 2.1 | Absolute maximum ratings | 5 |
| 2.2 | Thermal data | 6 |
| 3 | Electrical characteristics | 7 |
| 3.1 | Control part | 9 |
| 3.2 | Waveforms definitions | 12 |
| 4 | Smart shutdown function | 13 |
| 5 | Applications information | 14 |
| 5.1 | Recommendations | 15 |
| 6 | Package mechanical data | 16 |
| 7 | Revision history | 18 |

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

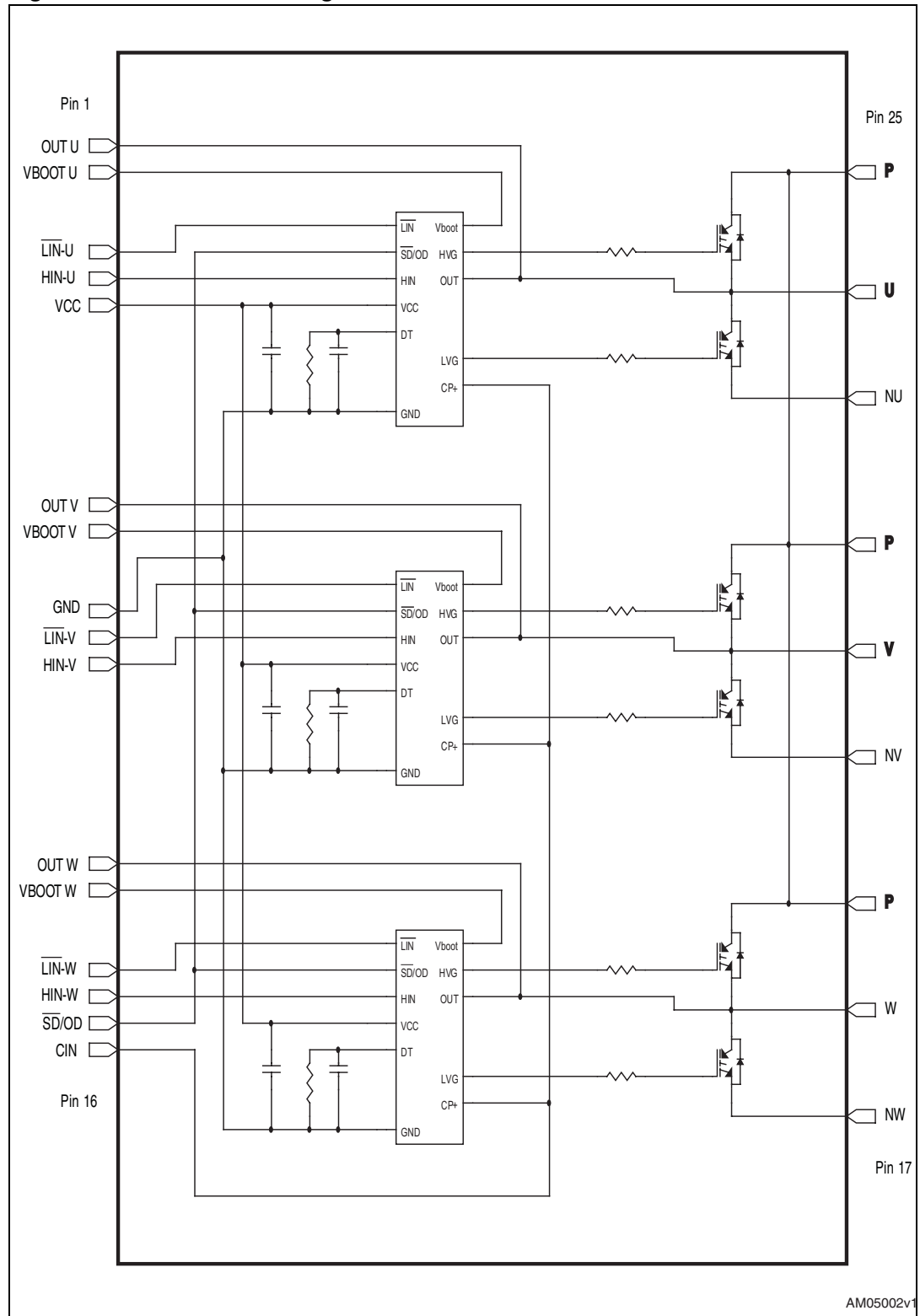
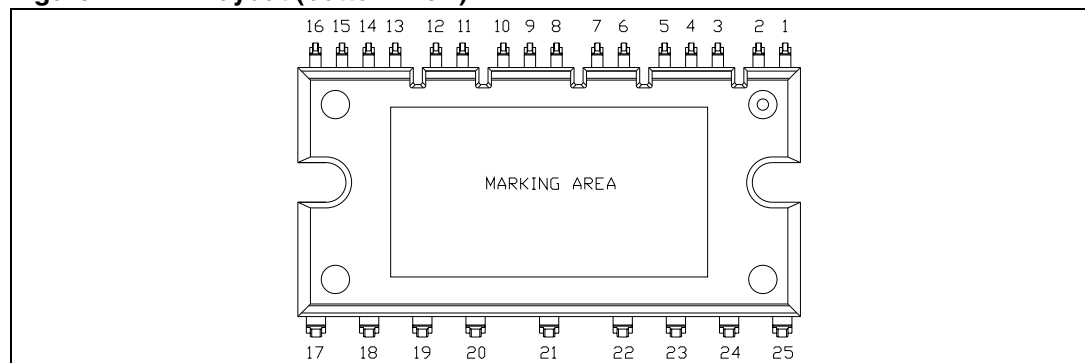


Table 2. Pin description

| Pin n° | Symbol | Description |
|--------|------------------------------------|--|
| 1 | OUT _U | High-side reference output for U phase |
| 2 | V _{bootU} | Bootstrap voltage for U phase |
| 3 | $\overline{\text{LIN}}_{\text{U}}$ | Low-side logic input for U phase |
| 4 | HIN _U | High-side logic input for U phase |
| 5 | V _{CC} | Low voltage power supply |
| 6 | OUT _V | High-side reference output for V phase |
| 7 | V _{boot V} | Bootstrap voltage for V phase |
| 8 | GND | Ground |
| 9 | $\overline{\text{LIN}}_{\text{V}}$ | Low-side logic input for V phase |
| 10 | HIN _V | High-side logic input for V phase |
| 11 | OUT _W | High-side reference output for W phase |
| 12 | V _{boot W} | Bootstrap voltage for W phase |
| 13 | $\overline{\text{LIN}}_{\text{W}}$ | Low-side logic input for W phase |
| 14 | HIN _W | High-side logic input for W phase |
| 15 | $\overline{\text{SD}} / \text{OD}$ | Shutdown logic input (active low) / open-drain (comparator output) |
| 16 | CIN | Comparator input |
| 17 | N _W | Negative DC input for W phase |
| 18 | W | W phase output |
| 19 | P | Positive DC input |
| 20 | N _V | Negative DC input for V phase |
| 21 | V | V phase output |
| 22 | P | Positive DC input |
| 23 | N _U | Negative DC input for U phase |
| 24 | U | U phase output |
| 25 | P | Positive DC input |

Figure 2. Pin layout (bottom view)

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3. Inverter part

| Symbol | Parameter | Value | Unit |
|--------------------|--|-------|---------------|
| V_{PN} | Supply voltage applied between P - N_U , N_V , N_W | 450 | V |
| $V_{PN(surge)}$ | Supply voltage (surge) applied between P - N_U , N_V , N_W | 500 | V |
| V_{CES} | Collector emitter voltage ($V_{IN}^{(1)} = 0$) | 600 | V |
| $\pm I_C^{(2)}$ | Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$ | 17 | A |
| $\pm I_{CP}^{(3)}$ | Each IGBT pulsed collector current | 40 | A |
| P_{TOT} | Each IGBT total dissipation at $T_C = 25^\circ\text{C}$ | 42 | W |
| t_{scw} | Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$ | 5 | μs |

1. Applied between HIN_i , $\overline{LIN_i}$ and GND for $i = U, V, W$

2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

| Symbol | Parameter | Value | Unit |
|---------------|---|-------------------------------------|------|
| V_{OUT} | Output voltage applied between OUT_U , OUT_V , OUT_W - GND | $V_{boot} - 21$ to $V_{boot} + 0.3$ | V |
| V_{CC} | Low voltage power supply | -0.3 to +21 | V |
| V_{CIN} | Comparator input voltage | -0.3 to $V_{CC} + 0.3$ | V |
| V_{boot} | Bootstrap voltage applied between $V_{boot\ i}$ - OUT_i for $i = U, V, W$ | -0.3 to 620 | V |
| V_{IN} | Logic input voltage applied between HIN , \overline{LIN} and GND | -0.3 to 15 | V |
| $V_{SD/OD}$ | Open drain voltage | -0.3 to 15 | V |
| dV_{OUT}/dt | Allowed output slew rate | 50 | V/ns |

Table 5. Total system

| Symbol | Parameter | Value | Unit |
|-----------|---|------------|------|
| V_{ISO} | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60$ sec.) | 2500 | V |
| T_J | Operating junction temperature | -40 to 125 | °C |

2.2 Thermal data

Table 6. Thermal data

| Symbol | Parameter | Value | Unit |
|------------|---|-------|------|
| R_{thJC} | Thermal resistance junction-case single IGBT | 2.4 | °C/W |
| | Thermal resistance junction-case single diode | 5 | °C/W |

3 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 7. Inverter part

| Symbol | Parameter | Test conditions | Value | | | Unit |
|---|--|--|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 12\text{ A}$ | - | 2.2 | 2.75 | V |
| | | $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 12\text{ A}$, $T_J = 125\text{ °C}$ | - | 1.8 | | |
| I_{CES} | Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state") | $V_{CE} = 600\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$ | - | | 100 | μA |
| V_F | Diode forward voltage | $V_{IN}^{(1)} = 0$ "logic state", $I_C = 12\text{ A}$ | - | | 3.8 | V |
| Inductive load switching time and energy | | | | | | |
| t_{on} | Turn-on time | $V_{PN} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 12\text{ A}$ (see Figure 3) | - | 300 | - | ns |
| $t_{c(on)}$ | Crossover time (on) | | - | 150 | - | |
| t_{off} | Turn-off time | | - | 730 | - | |
| $t_{c(off)}$ | Crossover time (off) | | - | 170 | - | |
| t_{rr} | Reverse recovery time | | - | 60 | - | |
| E_{on} | Turn-on switching losses | | - | 290 | - | μJ |
| E_{off} | Turn-off switching losses | | - | 250 | - | |

1. Applied between HIN_i , $\overline{LIN_i}$ and GND for $i = U, V, W$. (\overline{LIN} inputs are active-low).

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

Figure 3. Switching time test circuit

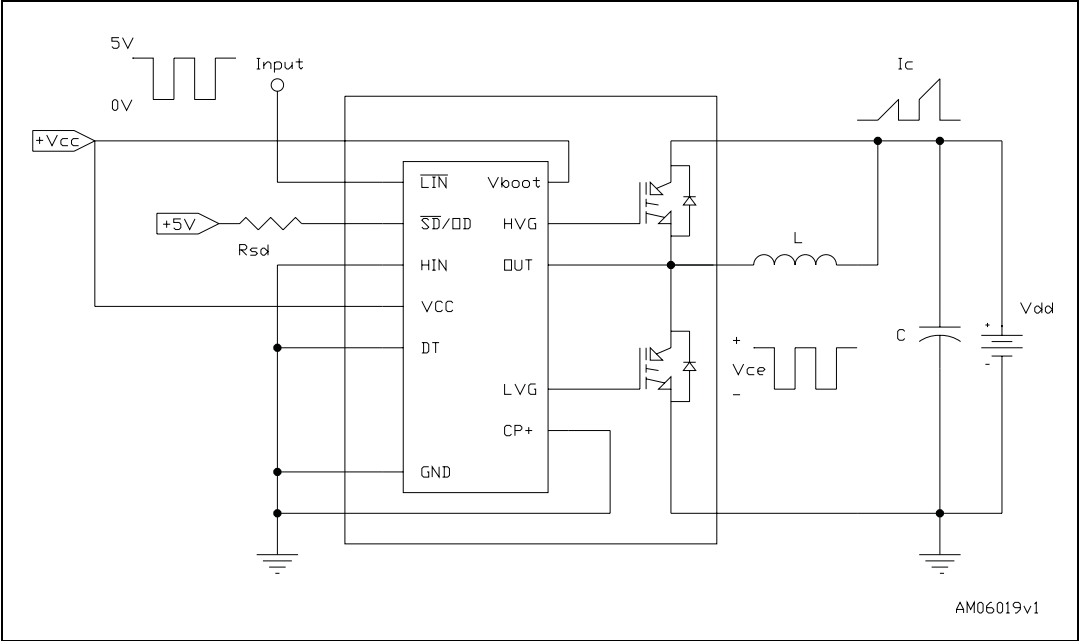
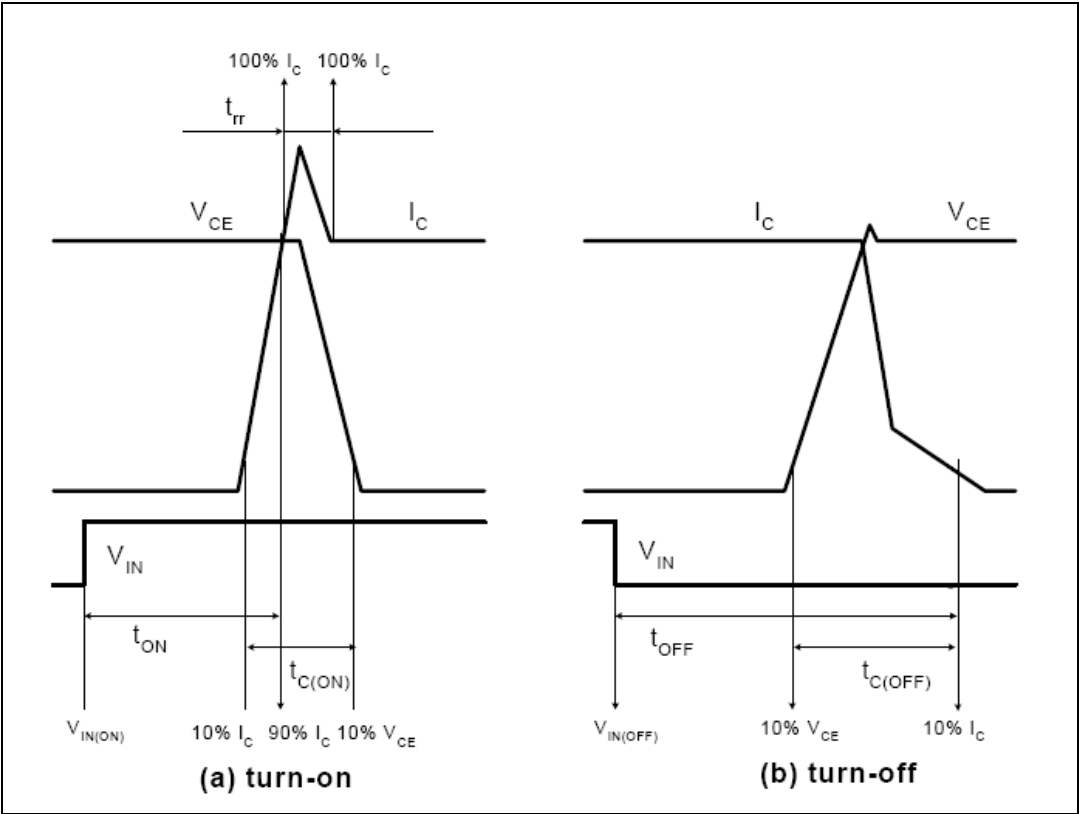


Figure 4. Switching time definition



3.1 Control part

Table 8. Low voltage power supply

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---|--|------|------|------|---------------|
| V_{CC_hys} | V_{CC} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{CC_thON} | V_{CC} UV turn ON threshold | | 11.5 | 12 | 12.5 | V |
| V_{CC_thOFF} | V_{CC} UV turn OFF threshold | | 10 | 10.5 | 11 | V |
| I_{qccu} | Undervoltage quiescent supply current | $V_{CC} = 10\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = 0$, $CIN = 0$ | | | 450 | μA |
| I_{qcc} | Quiescent current | $V_{CC} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; $\overline{LIN} = 5\text{ V}$; $HIN = 0$, $CIN = 0$ | | | 3.5 | mA |
| V_{ref} | Internal comparator (CIN) reference voltage | | 0.5 | 0.54 | 0.58 | V |

Table 9. Bootstrapped voltage

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|---|--|------|------|------|---------------|
| V_{BS_hys} | V_{BS} UV hysteresis | | 1.2 | 1.5 | 1.8 | V |
| V_{BS_thON} | V_{BS} UV turn ON threshold | | 10.6 | 11.5 | 12.4 | V |
| V_{BS_thOFF} | V_{BS} UV turn OFF threshold | | 9.1 | 10 | 10.9 | V |
| I_{QBSU} | Undervoltage V_{BS} quiescent current | $V_{BS} = 10\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $CIN = 0$ | | 70 | 110 | μA |
| I_{QBS} | V_{BS} quiescent current | $V_{BS} = 15\text{ V}$ $\overline{SD}/OD = 5\text{ V}$; \overline{LIN} and $HIN = 5\text{ V}$; $CIN = 0$ | | 150 | 210 | μA |
| $R_{DS(on)}$ | Bootstrap driver on resistance | LVG ON | | 120 | | Ω |

Table 10. Logic inputs

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|---|--------------------------------|------|------|------|---------------|
| V_{il} | Low logic level voltage | | | | 0.8 | V |
| V_{ih} | High logic level voltage | | 2.25 | | | V |
| I_{HINh} | HIN logic "1" input bias current | $HIN = 15\text{ V}$ | 110 | 175 | 260 | μA |
| I_{HINI} | HIN logic "0" input bias current | $HIN = 0\text{ V}$ | | | 1 | μA |
| I_{LINI} | \overline{LIN} logic "0" input bias current | $\overline{LIN} = 0\text{ V}$ | 3 | 6 | 20 | μA |
| I_{LINh} | \overline{LIN} logic "1" input bias current | $\overline{LIN} = 15\text{ V}$ | | | 1 | μA |
| I_{SDh} | \overline{SD} logic "1" input bias current | $\overline{SD} = 15\text{ V}$ | 30 | 120 | 300 | μA |

Table 10. Logic inputs (continued)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|--|------------------------------|------|------|------|---------------|
| I_{SDI} | \overline{SD} logic "0" input bias current | $\overline{SD} = 0\text{ V}$ | | | 3 | μA |
| Dt | Dead time | see Figure 7 | | 600 | | ns |

Table 11. Sense comparator characteristics ($V_{CC} = 15\text{ V}$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------------|--|------|------|------|--------------------|
| I_{ib} | Input bias current | $V_{CP+} = 1\text{ V}$ | - | | 3 | μA |
| V_{ol} | Open-drain low-level output voltage | $I_{od} = -3\text{ mA}$ | - | | 0.5 | V |
| t_{d_comp} | Comparator delay | \overline{SD}/OD pulled to 5 V through 100 k Ω resistor | - | 90 | 130 | ns |
| SR | Slew rate | $C_L = 180\text{ pF}$; $R_{pu} = 5\text{ k}\Omega$ | - | 60 | | V/ μsec |

Table 12. Truth table

| Condition | Logic input (V_I) | | | Output | |
|---|-----------------------|------------------|-------|--------|-----|
| | \overline{SD}/OD | \overline{LIN} | HIN | LVG | HVG |
| Shutdown enable half-bridge tri-state | L | X | X | L | L |
| Interlocking half-bridge tri-state | H | L | H | L | L |
| 0 "logic state" half-bridge tri-state | H | H | L | L | L |
| 1 "logic state" low side direct driving | H | L | L | H | L |
| 1 "logic state" high side direct driving | H | H | H | L | H |

Note: X: don't care

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching frequency (1)

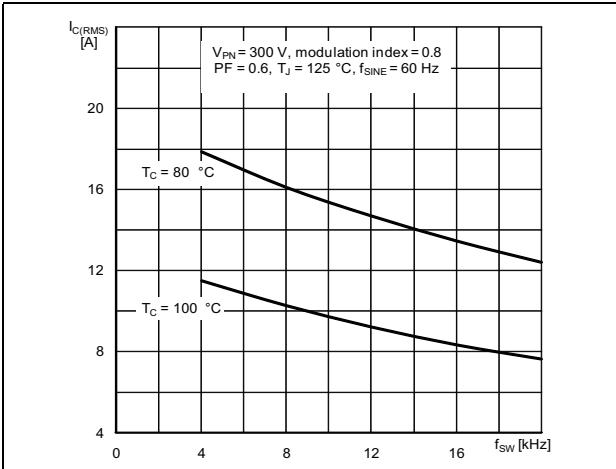
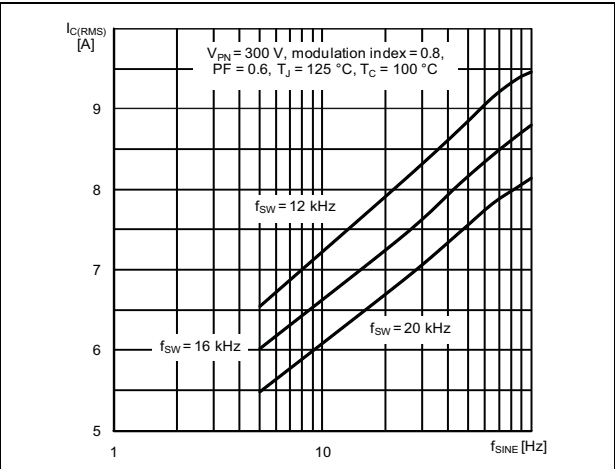


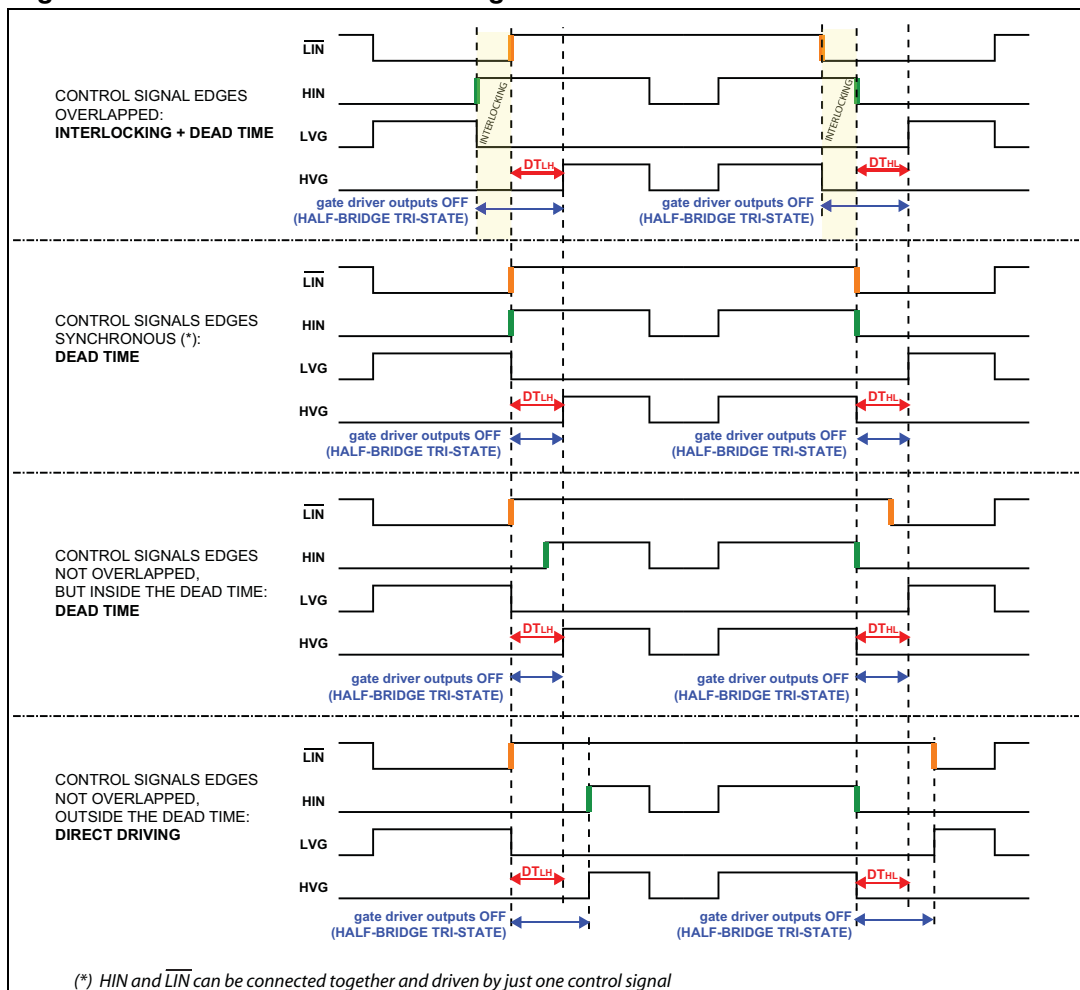
Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{SINE} (1)



1. Simulated curves refer to typical IGBT parameters and maximum R_{thj-c} .

3.2 Waveforms definitions

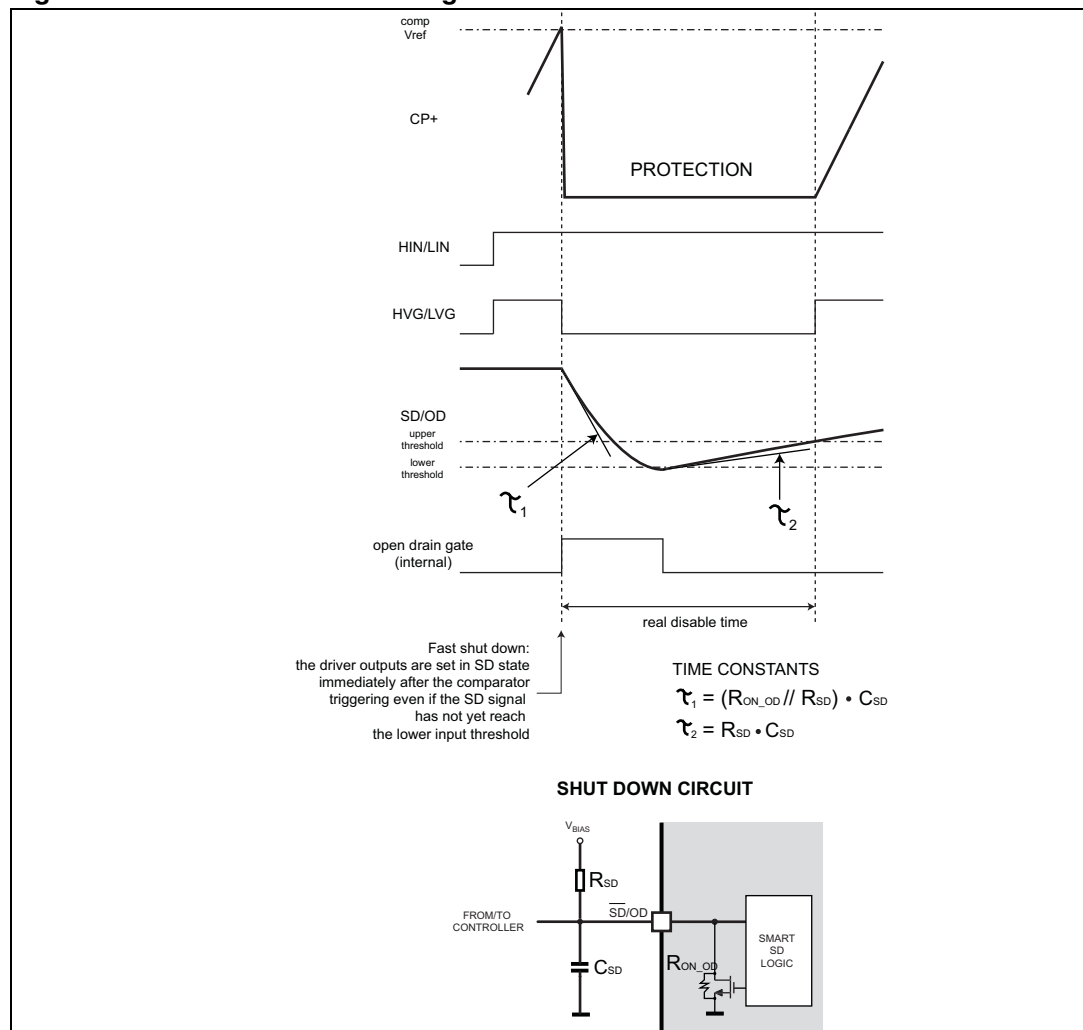
Figure 7. Dead time and interlocking waveforms definitions



4 Smart shutdown function

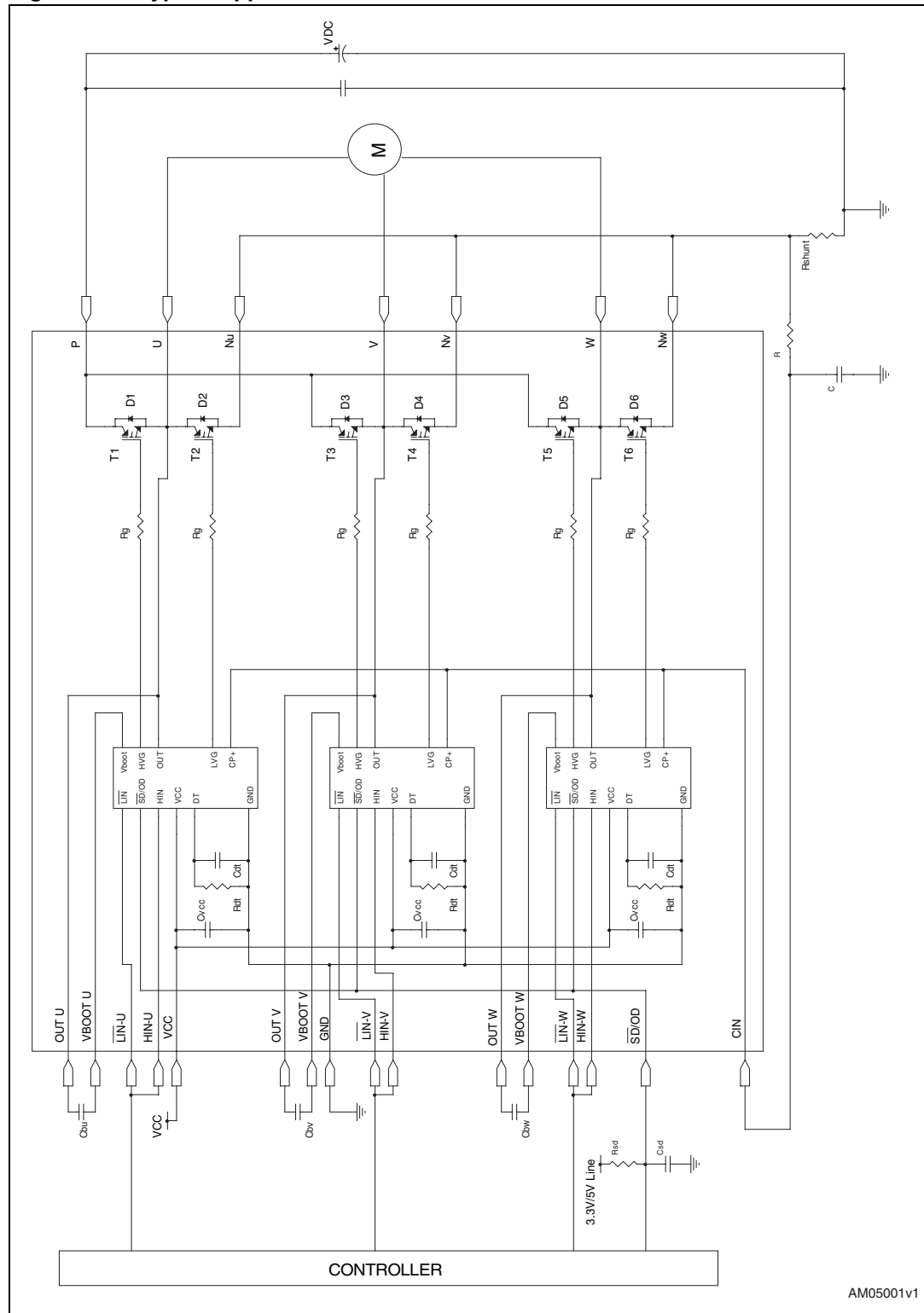
The STGIPS20K60 integrates a comparator for fault sensing purposes. The comparator non-inverting input (CIN) can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half-bridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 8. Smart shutdown timing waveforms



5 Applications information

Figure 9. Typical application circuit



5.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The $\overline{\text{SD}}/\text{OD}$ signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 4: Smart shutdown function](#) for detailed info).

Table 13. Recommended operating conditions

| Symbol | Parameter | Conditions | Value | | | Unit |
|-------------------|------------------------------------|--|-------|------|------|---------------|
| | | | Min. | Typ. | Max. | |
| V_{PN} | Supply Voltage | Applied between P-Nu,Nv,Nw | | 300 | 400 | V |
| V_{CC} | Control supply voltage | Applied between V_{CC} -GND | 13.5 | 15 | 18 | V |
| V_{BS} | High side bias voltage | Applied between V_{BOOTi} - OUT_i for $i=\text{U,V,W}$ | | | 18 | V |
| t_{dead} | Blanking time to prevent Arm-short | For each input signal | 1 | | | μs |
| f_{PWM} | PWM input signal | $-40^\circ\text{C} < T_c < 100^\circ\text{C}$ $-40^\circ\text{C} < T_j < 125^\circ\text{C}$ | | | 20 | kHz |

6 Package mechanical data

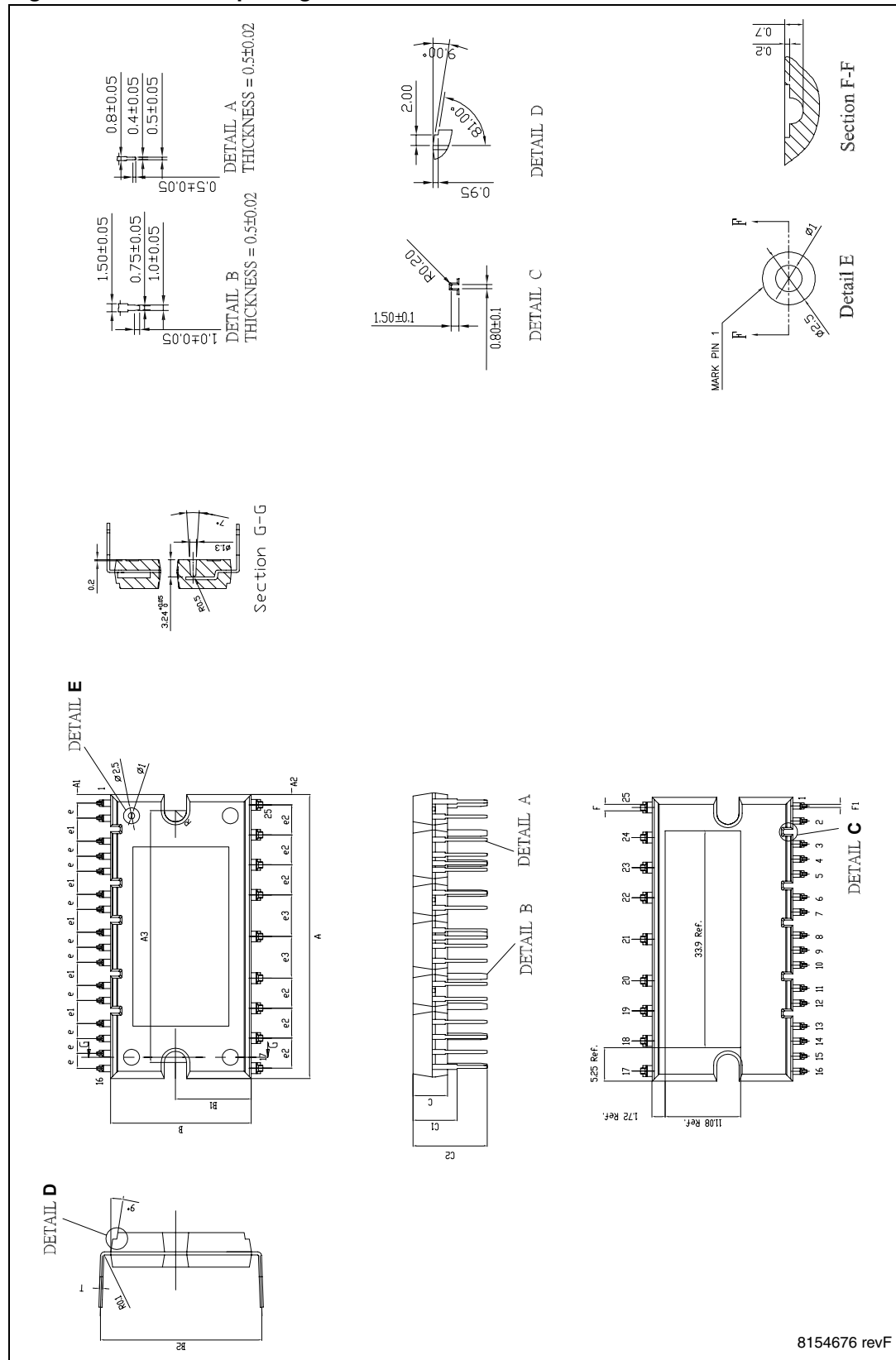
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.

Table 14. SDIP-25L package mechanical data

| Dim. | (mm.) | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 44 | | 44.8 |
| A1 | 0.95 | | 1.75 |
| A2 | 1.2 | | 2 |
| A3 | 39 | | 39.8 |
| B | 21.6 | | 22.4 |
| B1 | 11.45 | | 12.25 |
| B2 | 24.83 | 25.22 | 25.63 |
| C | 5 | | 5.8 |
| C1 | 6.4 | | 7.4 |
| C2 | 11.1 | | 12.1 |
| e | 1.95 | 2.35 | 2.75 |
| e1 | 3.2 | 3.6 | 4 |
| e2 | 4.3 | 4.7 | 5.1 |
| e3 | 6.1 | 6.5 | 6.9 |
| F | 0.8 | 1.0 | 1.2 |
| F1 | 0.3 | 0.5 | 0.7 |
| R | 1.35 | | 2.15 |
| T | 0.4 | 0.55 | 0.7 |

Figure 10. SDIP-25L package mechanical data



7 Revision history

Table 15. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 10-Aug-2009 | 1 | Initial release |
| 01-Jul-2010 | 2 | Document status promoted from preliminary to datasheet. Updated package mechanical data (Section 6: Package mechanical data). Minor text changes to improve readability. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com