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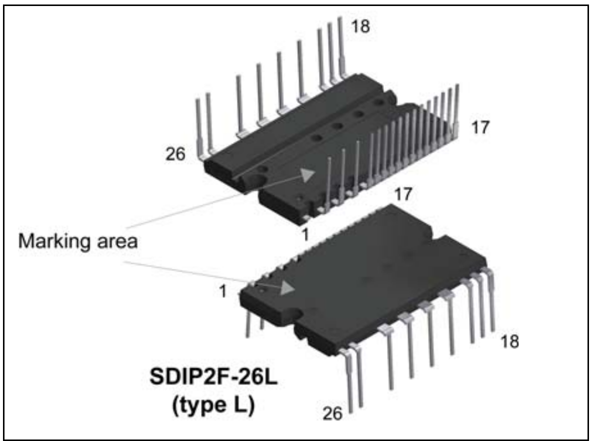
STGIF10CH60TS-L

SLLIMM™ - 2nd series

IPM, 3-phase inverter, 15 A, 600 V short-circuit rugged IGBT

Datasheet - production data



Features

- IPM 15 A, 600 V 3-phase IGBT inverter bridge including 2 control ICs for gate driving and freewheeling diodes
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Internal bootstrap diode
- Under-voltage lockout of gate drivers
- Smart shutdown function
- Short-circuit protection
- Shutdown input/fault output
- Separate open emitter outputs
- Built-in temperature sensor
- Comparator for fault protection
- Short-circuit rugged TFS IGBTs
- Very fast, soft recovery diodes
- 85 kΩ NTC UL 1434 CA 4 recognized
- Fully isolated package
- Isolation rating of 1500 Vrms/min

Applications

- 3-phase inverters for motor drives
- Home appliances such as washing machines, refrigerators, air conditioners and sewing machine

Description

This second series of SLLIMM (small low-loss intelligent molded module) provides a compact, high performance AC motor drive in a simple, rugged design. It combines new ST proprietary control ICs (one LS and one HS driver) with the improved short-circuit rugged trench gate field-stop (TFS) IGBT, making it ideal for 3-phase inverter systems such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Table 1. Device summary

Order code	Marking	Package	Packaging
STGIF10CH60TS-L	GIF10CH60TS-L	SDIP2F-26L	Tube

Contents

1 Internal schematic and pin description

Figure 1. Internal schematic diagram and pin configuration

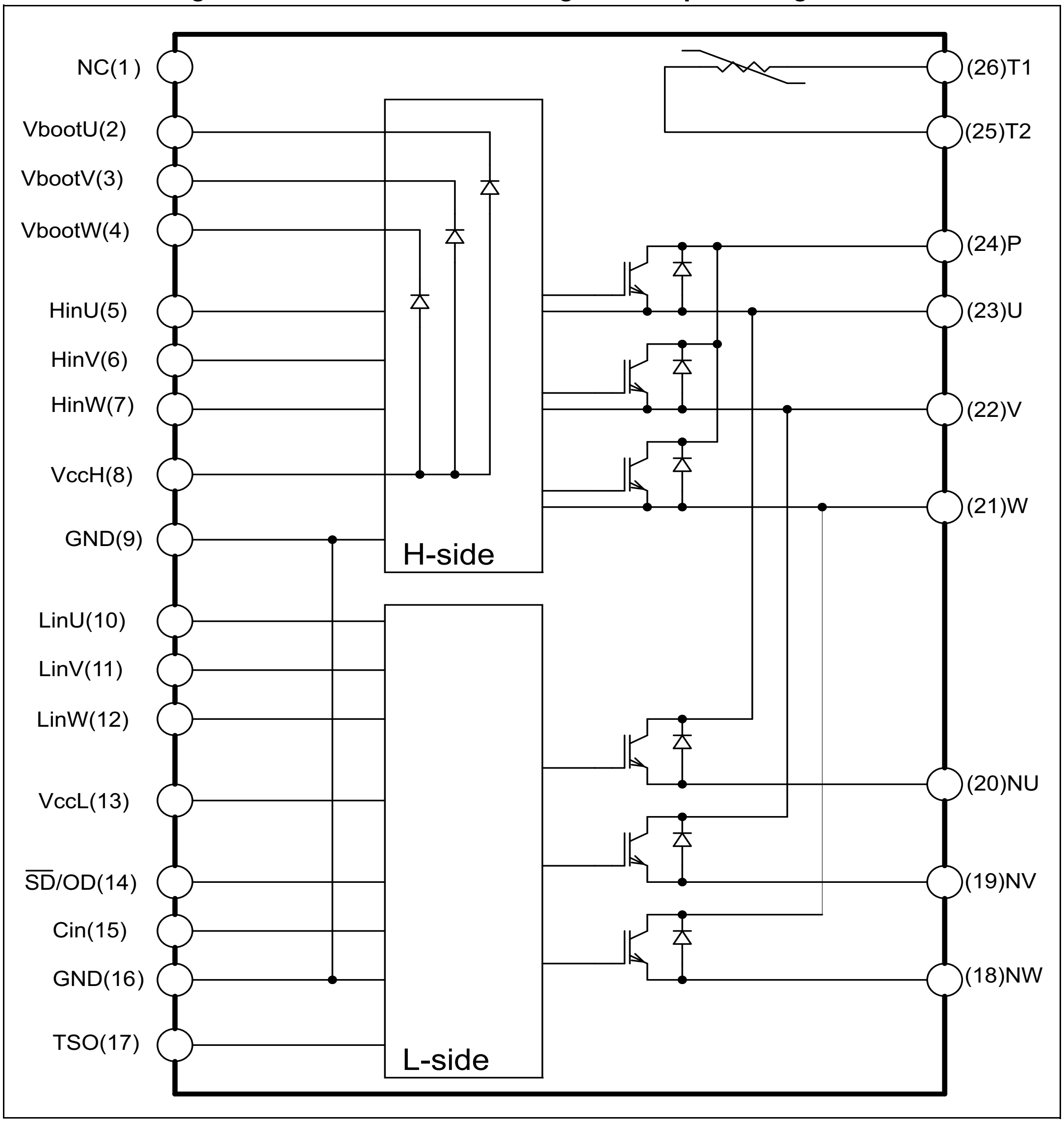


Table 2. Pin description

Pin	Symbol	Description
1	NC	-
2	VBOOTu	Bootstrap voltage for U phase
3	VBOOTv	Bootstrap voltage for V phase
4	VBOOTw	Bootstrap voltage for W phase
5	HINu	High-side logic input for U phase
6	HINv	High-side logic input for V phase
7	HINw	High-side logic input for W phase
8	VCCH	High-side low voltage power supply
9	GND	Ground
10	LINu	Low-side logic input for U phase
11	LINv	Low-side logic input for V phase
12	LINw	Low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	$\overline{SD}$/OD	Shutdown logic input (active low) / open-drain (comparator output)
15	CIN	Comparator input
16	GND	Ground
17	TSO	Temperature sensor output
18	NW	Negative DC input for W phase
19	NV	Negative DC input for V phase
20	NU	Negative DC input for U phase
21	W	W phase output
22	V	V phase output
23	U	U phase output
24	P	Positive DC input
25	T2	NTC thermistor terminal 2
26	T1	NTC thermistor terminal 1

2 Absolute maximum ratings

(T_j= 25°C unless otherwise noted).

Table 3. Inverter parts

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage between P -N_U, -N_V, -N_W	450	V
$V_{PN(surge)}$	Supply voltage surge between P -N_U, -N_V, -N_W	500	V
V_{CES}	Collector-emitter voltage each IGBT	600	V
$\pm I_C$	Continuous collector current each IGBT (T_C = 25 °C)	15	A
	Continuous collector current each IGBT (T_C = 80 °C)	10	
$\pm I_{CP}$	Peak collector current each IGBT (less than 1ms)	30	A
P_{TOT}	Total dissipation at T_C=25°C each IGBT	33	W
t_{scw}	Short circuit withstand time, V_{CE} = 300V, T_J = 125 °C, V_{CC} = V_{boot} = 15 V, V_{IN} = 0 to 5 V	5	µs

Table 4. Control parts

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply voltage between V_{CCH}-GND, V_{CCL}-GND	-0.3	20	V
V_{BOOT}	Bootstrap voltage	-0.3	619	V
V_{OUT}	Output voltage between U, V, W and GND	V_{BOOT} - 21	V_{BOOT} + 0.3	V
V_{CIN}	Comparator input voltage	-0.3	20	V
V_{IN}	Logic input voltage applied between HINx, LINx and GND	-0.3	15	V
$V_{\overline{SD}}$/OD	Open drain voltage	-0.3	7	V
$I_{\overline{SD}}$/OD	Open drain sink current	-	10	mA
V_{TSO}	Temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	Temperature sensor output current		7	V

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60sec.)	1500	Vrms
T_J	Power chips operating junction temperature	-40 to 175	°C
T_C	Module case operation temperature	-40 to 125	°C

Table 6. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Thermal resistance junction-case single IGBT	4.6	°C/W
	Thermal resistance junction-case single diode	5.5	

3 Electrical characteristics

(T_j= 25°C unless otherwise noted).

Table 7. Inverter parts

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{CES}	Collector-cut off current	V_{CE} = 600 V, V_{CC} = V_{boot} = 15 V	-		100	µA
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{CC} = V_{Boot} = 15 V, V_{IN}(1)= 0 to 5 V, I_C = 10 A,	-	1.5	1.95	V
		V_{CC} = V_{Boot} = 15 V, V_{IN}(1)= 0 to 5 V, I_C = 15 A,	-	1.65		
V_F	Diode forward voltage	V_{IN}(1) = 0, I_C = 10 A	-	1.6	2.25	V
		V_{IN}(1) = 0, I_C = 15 A	-	1.7		V
Inductive load switching time and energy (2)						
t_{on}	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 10 A	-	287		ns
$t_{c(on)}$	Cross-over time on		-	146		
t_{off}	Turn-off time		-	370		
$t_{c(off)}$	Cross-over time off		-	105		
t_{rr}	Reverse recovery time		-	270		
E_{on}	Turn-on switching loss		-	281		µJ
E_{off}	Turn-off switching loss		-	121		
E_{rr}	Reverse recovery energy loss			23		
t_{on}	Turn-on time	V_{DD} = 300 V, V_{CC} = V_{boot} = 15 V, V_{IN}(1) = 0 to 5 V, I_C = 15 A	-	315		ns
$t_{c(on)}$	Cross-over time on		-	175		
t_{off}	Turn-off time		-	346		
$t_{c(off)}$	Cross-over time off		-	89		
t_{rr}	Reverse recovery time		-	280		
E_{on}	Turn-on switching loss		-	459		µJ
E_{off}	Turn-off switching loss		-	175		
E_{rr}	Reverse recovery energy loss			34		

1. Applied between HINx, LINx and GND for x = U, V, W
2. t_{on} and t_{off} include the propagation delay time of the internal drive. $t_{C(on)}$ and $t_{C(off)}$ are the switching time of IGBT itself under the internally given gate driving condition.

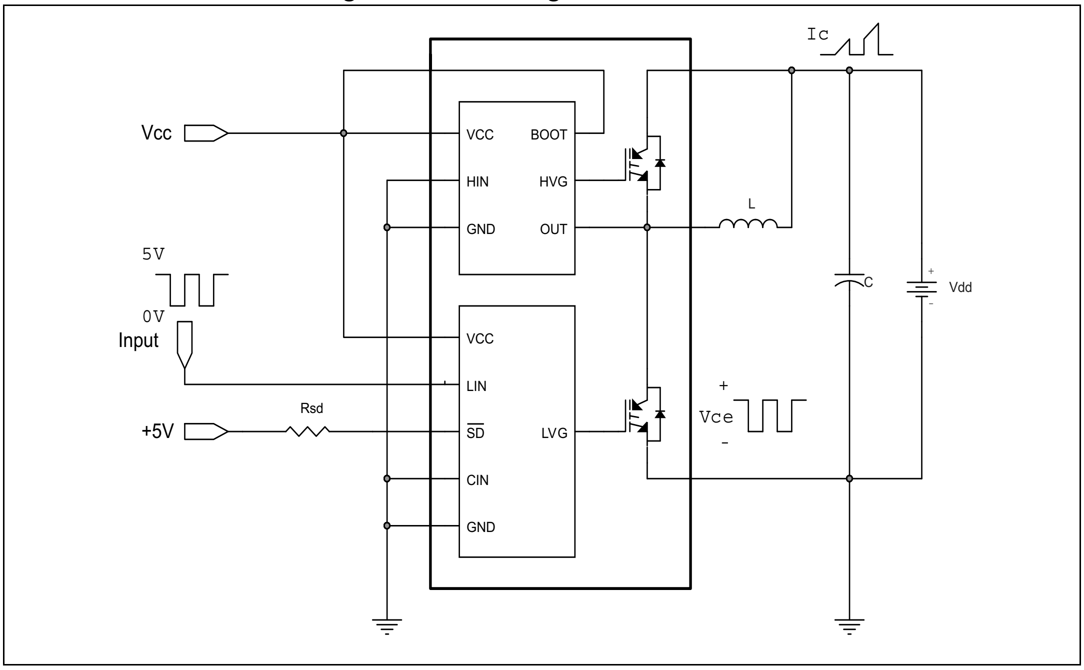


Figure 2. Switching time test circuit

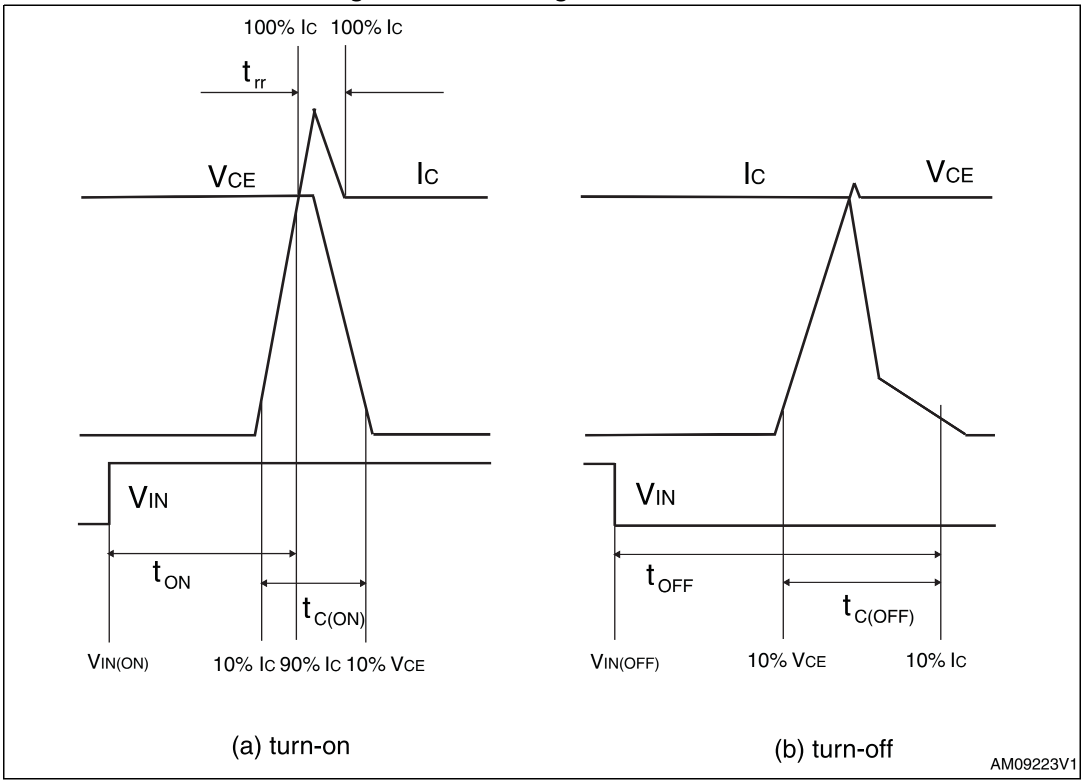


Figure 3. Switching time definition

Table 8. Control / protection parts

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2			V
I_{INh}	IN logic “1” input bias current	IN_x=15V	80	150	200	µA
I_{INl}	IN logic “0” input bias current	IN_x=0V			1	µA
High side						
V_{CC_hys}	V_{CC} UV hysteresis		1.2	1.4	1.7	V
$V_{CCH\_th(on)}$	V_{CCH} UV turn-on threshold		11	11.5	12	V
$V_{CCH\_th(off)}$	V_{CCH} UV turn-off threshold		9.6	10.1	10.6	V
V_{BS_hys}	V_{BS} UV hysteresis		0.5	1	1.6	V
$V_{BS\_th(on)}$	V_{BS} UV turn-on threshold		10.1	11	11.9	V
$V_{BS\_th(off)}$	V_{BS} UV turn-off threshold		9.1	10	10.9	V
I_{QBSU}	Under voltage V_{BS} quiescent current	V_{BS} = 9 V, HINx(1) = 5V;		55	75	µA
I_{QBS}	V_{BS} quiescent current	V_{CC} = 15 V, HINx (1) = 5V		125	170	µA
I_{qccu}	Under voltage quiescent supply current	V_{CC} = 9 V, HINx (1) = 0		190	250	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V, HINx (1) = 0		560	730	µA
$R_{DS(on)}$	BS driver ON resistance			150		Ω
Low side						
V_{CC_hys}	V_{CC} UV hysteresis		1.1	1.4	1.6	V
$V_{CCL\_th(on)}$	V_{CCL} UV turn-on threshold		10.4	11.6	12.4	V
$V_{CCL\_th(off)}$	V_{CCL} UV turn-off threshold		9.0	10.3	11	V
I_{qccu}	Under voltage quiescent supply current	V_{CC} = 10 V, $\overline{SD}$ pulled to 5V through R_{SD} = 10kΩ, CIN = LINx 1) = 0;		600	800	µA
I_{qcc}	Quiescent current	V_{CC} = 15 V, $\overline{SD}$ = 5V, CIN = LINx 1) = 0;		700	900	µA
V_{SSD}	Smart $\overline{SD}$ unlatch threshold		0.5	0.6	0.75	V
I_{SDh}	$\overline{SD}$ logic “1” input bias current	$\overline{SD}$ = 5V	25	50	70	µA
I_{SDl}	$\overline{SD}$ logic “0” input bias current	$\overline{SD}$ =0V			1	µA

Table 8. Control / protection parts (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Temperature sensor output						
V_{TSO}	Temperature sensor output voltage	T_j = 25 °C		1.4		V
I_{TSO_SNK}	Temperature sensor sink current capability			0.1		mA
I_{TSO_SRC}	Temperature sensor source current capability		4			mA

1. Applied between HINx, LINx and GND for x = U, V, W

Table 9. Sense comparator (V_{CC} = 15 V, unless otherwise is specified)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{CIN}	CIN input bias current	V_{CIN} =1V	-0.2		0.2	µA
V_{ref}	Internal reference voltage		460	510	560	mV
V_{OD}	Open drain low level output voltage	I_{od} = 5mA			500	mV
t_{CIN_SD}	C_{IN} comparator delay to SD	$\overline{SD}$ pulled to 5V through R_{SD}=10kΩ; measured applying a voltage step 0-1V to Pin CIN 50% CIN to 90% $\overline{SD}$	150	230	320	ns
SR_{SD}	$\overline{SD}$ fall slew rate	$\overline{SD}$ pulled to 5V through R_{SD}=10kΩ; C_L=1nF through $\overline{SD}$ and ground; 90% $\overline{SD}$ to 10% $\overline{SD}$		25		V/µs

Note: Comparator stay enabled even if V_{CC} is in UVLO condition but higher than 4 V.

4 Fault management

The device integrates an open-drain output connected to $\overline{SD}$ Pin. As soon as a fault occurs the open-drain is activated and LVGx outputs are forced low. Two types of fault can be pointed out:

- Overcurrent (OC) sensed by the internal comparator (see more detail in *Section 4.2: Smart shutdown function*);
- Undervoltage on supply voltage (V_{CC});

Each fault enables the SD open drain for a different time; refer to the following *Table 10: Fault timing*.

Table 10. Fault timing

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Over-current event	≤ 20 µs	20 µs
		≥ 20µs	OC time
UVLO	Under-voltage lock out event	≤ 50 µs	50µs
		≥ 50µs until the VCC_LS exceed the VCC_LS UV turn ON threshold	UVLO time

Actually the device remains in a fault condition ($\overline{SD}$ at low logic level and LVGx outputs disabled) for a time also depending on RC network connected to $\overline{SD}$ pin. The network generate a time contribute that add up to the internal value.

Figure 4. Overcurrent timing (without contribution of RC network on $\overline{SD}$)

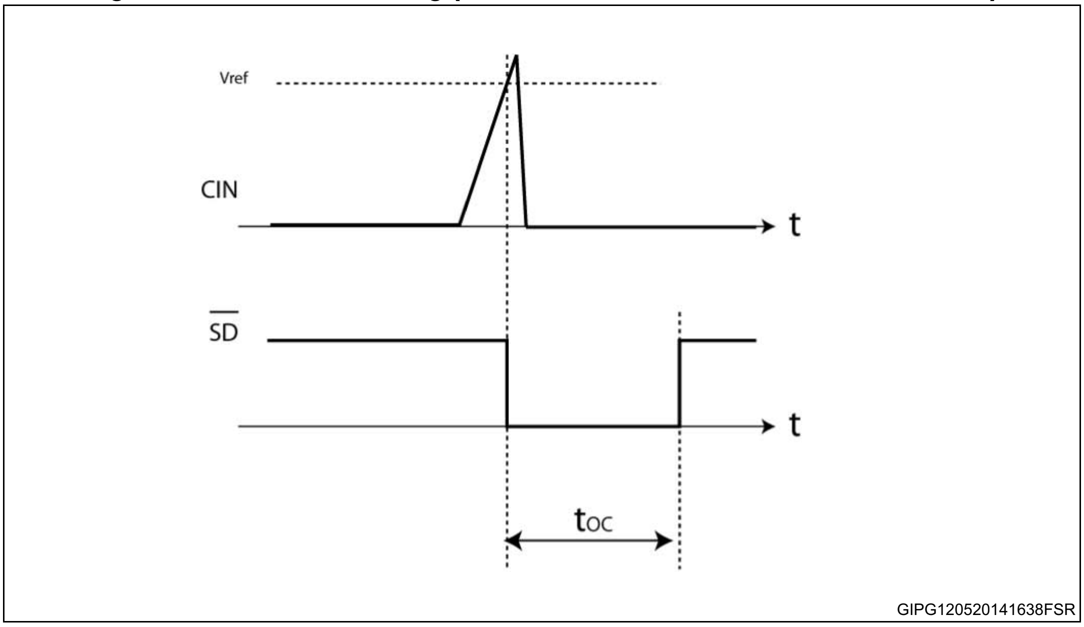
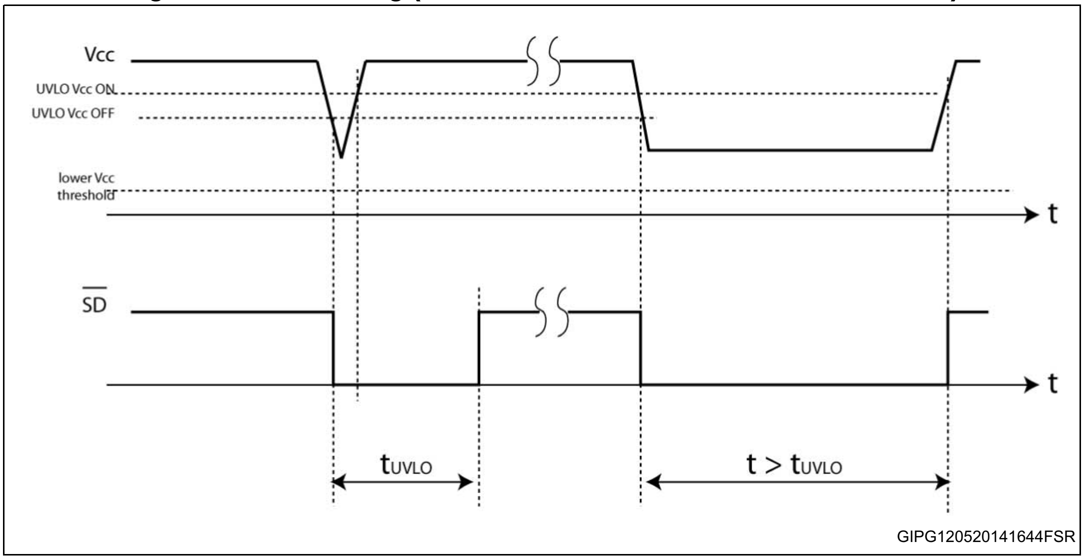


Figure 5. UVLO timing (without contribution of RC network on $\overline{SD}$)



4.1 TSO output

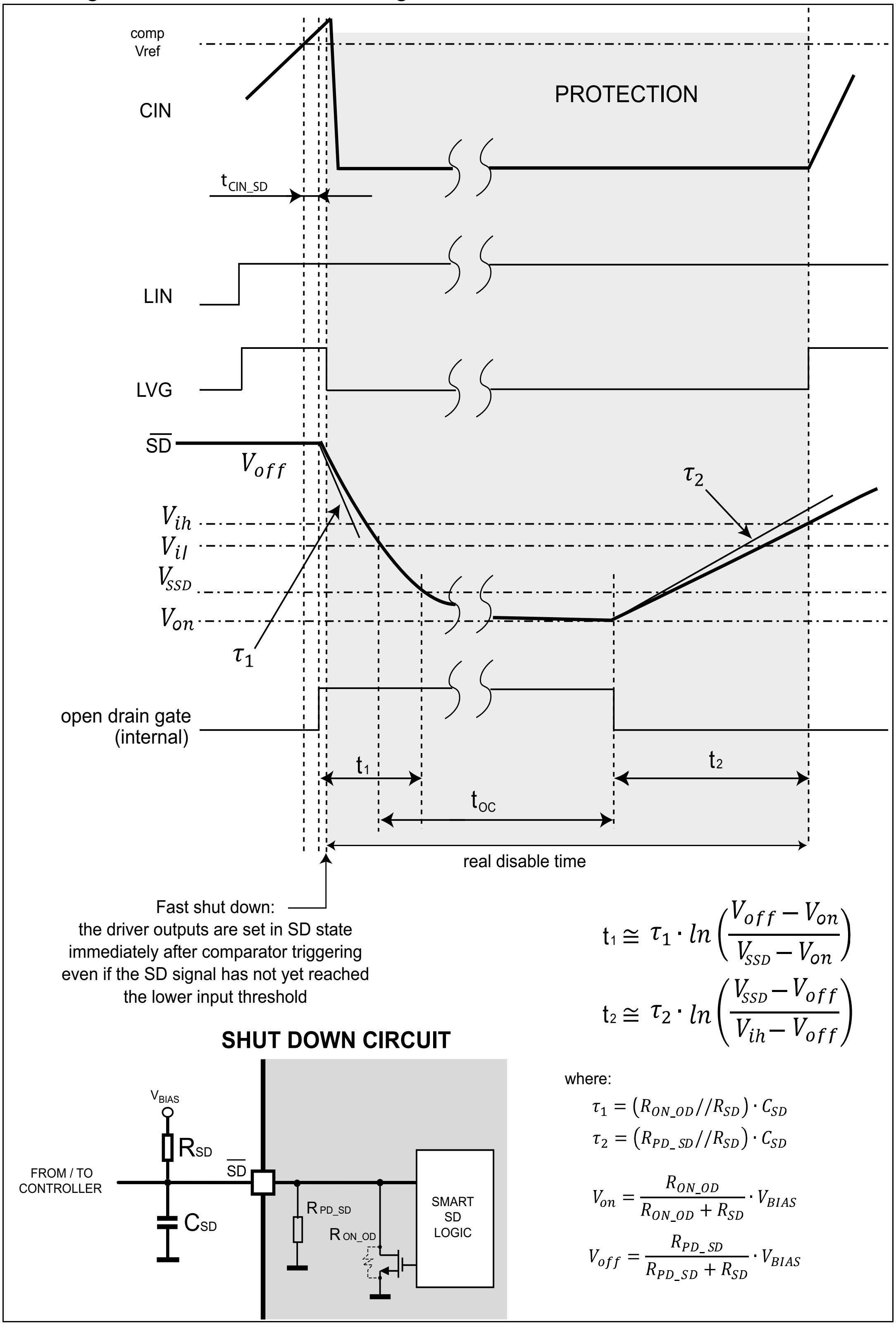
The device integrates temperature sensor. A voltage proportional to die temperature is available on TSO pin. When this function is not used the Pin can be left floating.

4.2 Smart shutdown function

The device integrates a comparator committed to the fault sensing function. The comparator input can be connected to an external shunt resistor in order to implement a simple overcurrent detection function.

The output signal of the comparator is fed to an integrated MOSFET with the open drain output available on $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and its outputs are all set to low level.

Figure 6. Smart shutdown timing waveforms in case of overcurrent event



Note: $R_{ON\_OD}=V_{OD}/5$ *mA see Table 9;* R_{PD_SD} *(typ) =5 V/*I_{SDh}

In common over-current protection architectures the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$ line in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition.

Differently from the common fault detection systems, the device Smart shutdown architecture allows to immediately turn-off the outputs gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual outputs switch-off. In fact the time delay between the fault and the outputs turn off is no more dependent on the RC value of the external network connected to the pin.

In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering.

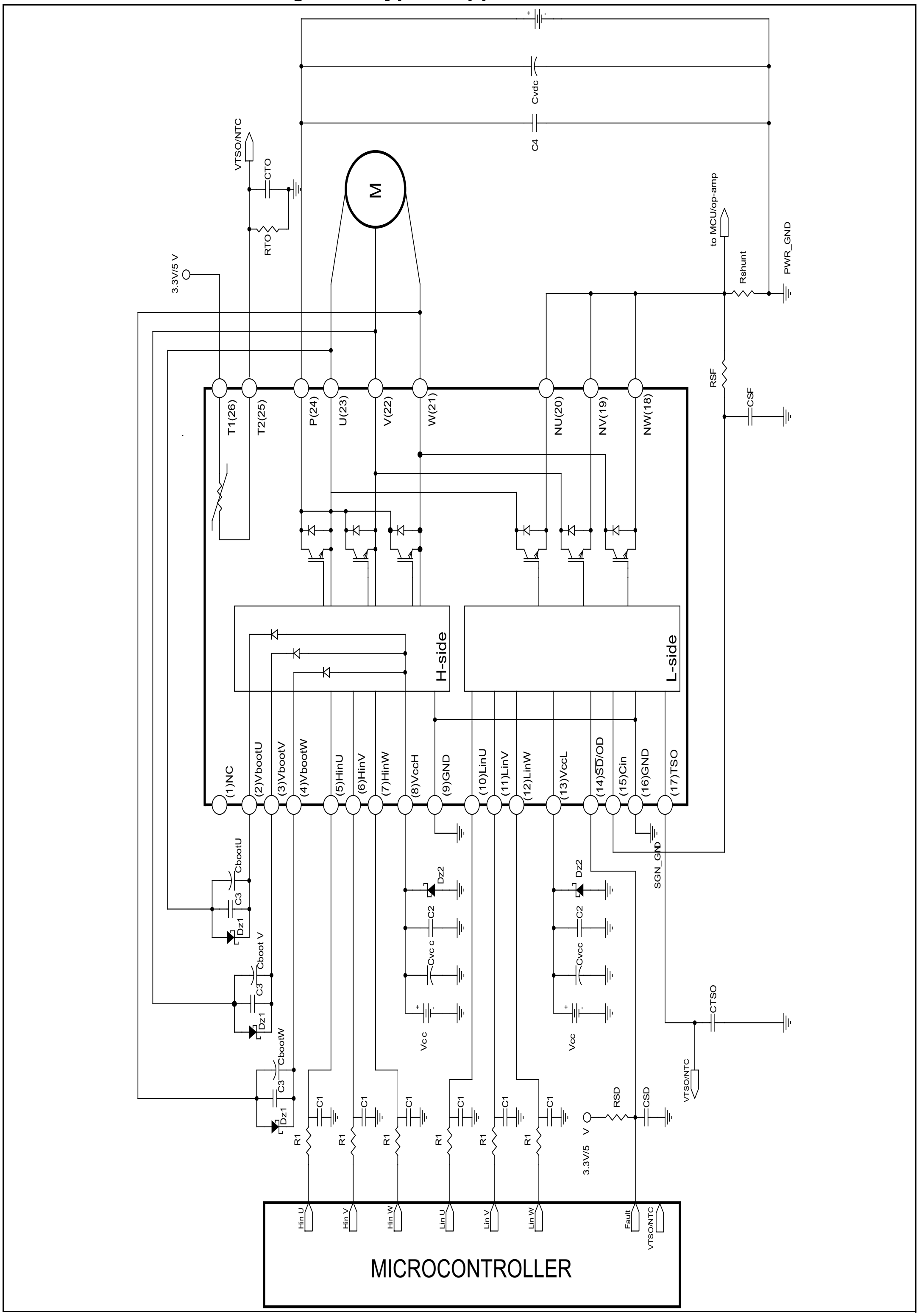
At the same time the internal logic turns on the open drain output and holds it on until the $\overline{SD}$ voltage goes below the V_{SSD} threshold and t_{oc} time is elapsed.

The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$ pin reaches the higher threshold of the $\overline{SD}$ logic input.

The Smart shutdown system provides the possibility to increase the time constant of the external RC network (that is the disable time after the fault event) up to very large values without increasing the delay time of the protection.

5 Typical application circuit

Figure 7. Typical application circuit



6 Recommendations

1. Input signals HIN, LIN are active-high logic. A 500 kΩ (typ.) pull-down resistor is built-in for each high side input. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R1, C1) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and must be placed as close as possible to the IPM input pins.
2. The bypass capacitor Cvcc (aluminum or tantalum) is recommended to reduce the transient circuit demand on the power supply. In addition, a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) is suggested, to reduce high frequency switching noise distributed on the power supply lines. It must be placed as close as possible to each Vcc pin and in parallel to the bypass capacitor.
3. The use of RC filter (RSF, CSF) for preventing protection circuit malfunction is recommended. The time constant (RSF x CSF) should be set to 1us and the filter must be placed as close as possible to the CIN pin.
4. The $\overline{SD}$ is an input/output pin (open drain type if used as output). It should be pulled up to MCU power supply (3.3/5 V) by a resistor higher than 1.0 kΩ in order to keep I_{od} lower than 5 mA. The filter on $\overline{SD}$ has to be sized to get a desired re-starting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.
5. To increase the noise immunity of the TSO thermal sensor, it is recommended to parallel a decoupling capacitor C_{TSO} between 1 nF and 10 nF. Similarly, if the NTC thermistor is available and used, it is recommended to parallel a decoupling capacitor C_{OT} between 10 nF and 100 nF. In both cases, the capacitors must be placed close to the MCU.
6. The decoupling capacitor C_3 (100 to·220 nF, with low ESR and low ESL) in parallel with each C_{boot} is recommended to filter high frequency disturbances. Both C_{boot} and C_3 must be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to U,V,W terminals directly and separated from the main output wires.
7. A Zener diode (Dz1) between each V_{cc} pin and GND, and in parallel (Dz2) with each Cboot is suggested in order to prevent overvoltage.
8. The decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor Cvdc is recommended, in order to prevent surge destruction. Both capacitors C_4 and Cvdc should be placed as close as possible to the IPM (C_4 has priority over Cvdc).
9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
10. Low inductance shunt resistors should be used for phase leg current sensing
11. In order to avoid malfunctions, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
12. It is recommended to connect SGN_GND to PWR_GND at only one point (near the terminal of shunt resistor), in order to avoid any malfunction due to power ground fluctuation.

Table 11. Recommended operating conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{PN}	Supply voltage	Applied between P-Nu, N_V, N_W		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1.0			µs
f_{PWM}	PWM input signal	-40 °C < T_C < 100 °C -40 °C < T_j < 125 °C			20	kHz
T_C	Case operation temperature				100	°C

7 NTC thermistor

Table 12. NTC thermistor

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_{25}	Resistance	T = 25°C		85	-	kΩ
R_{125}	Resistance	T = 125°C		2.6	-	kΩ
B	B-constant	T = 25°C to 100°C		4092	-	K
T	Operating temperature range		-40		125	°C

Figure 8. NTC resistance vs. temperature

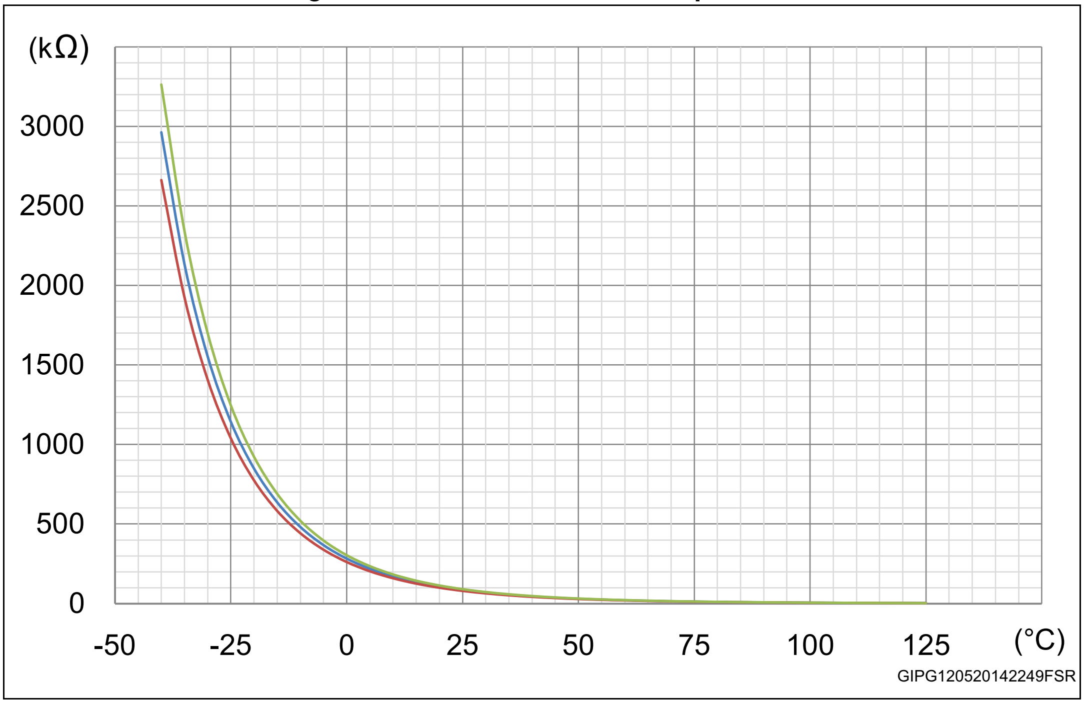
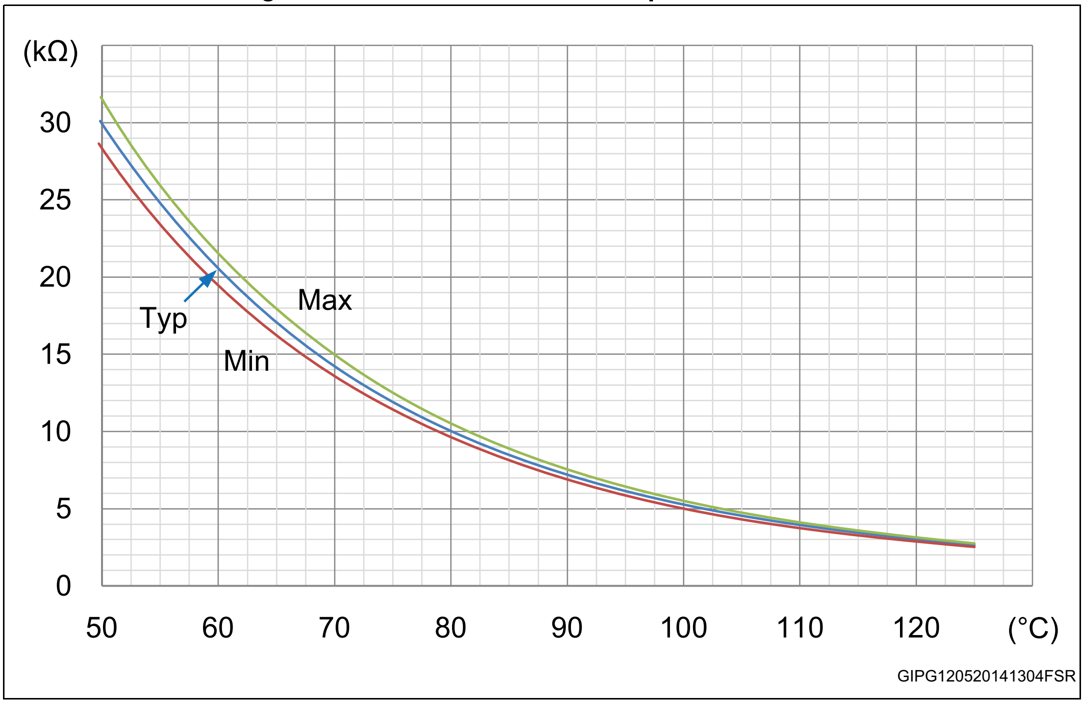


Figure 9. NTC resistance vs. temperature - zoom



8 Electrical characteristics (curves)

Figure 10. Output characteristics

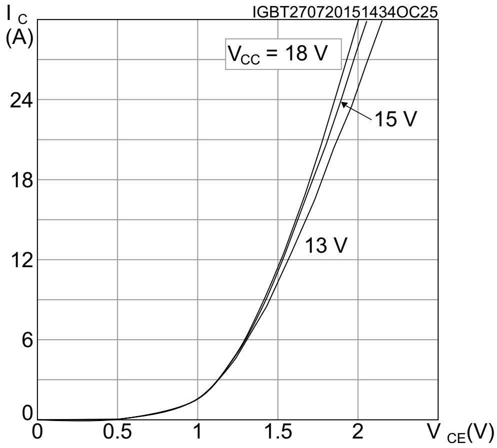


Figure 11. $V_{ce(sat)}$ vs collector current

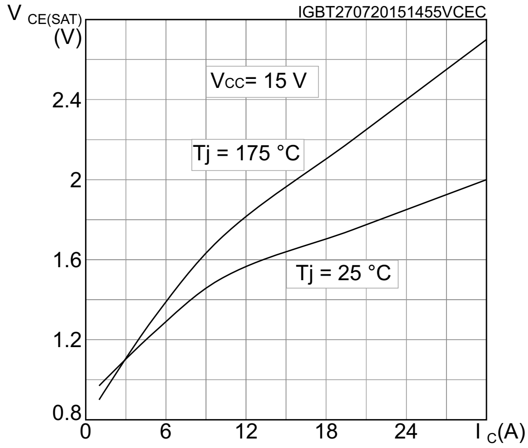


Figure 12. Diode VF vs forward current

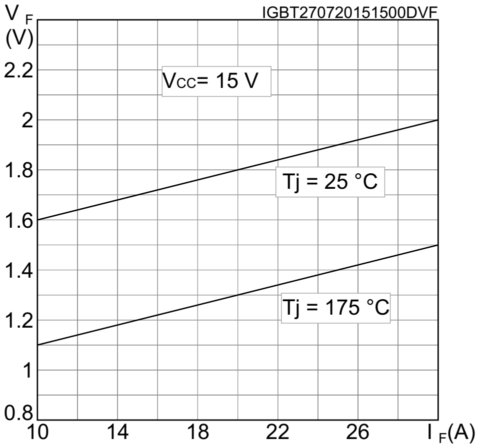


Figure 13. E_{on} switching loss vs collector current

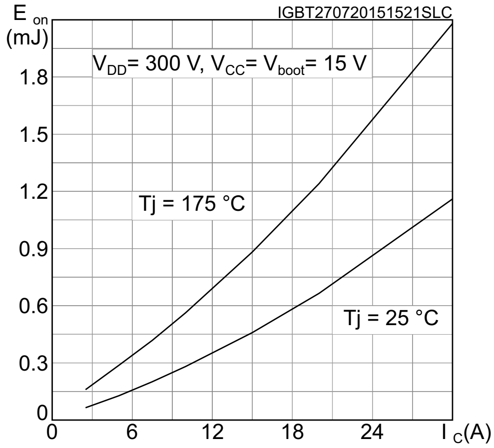


Figure 14. E_{off} switching loss vs collector current

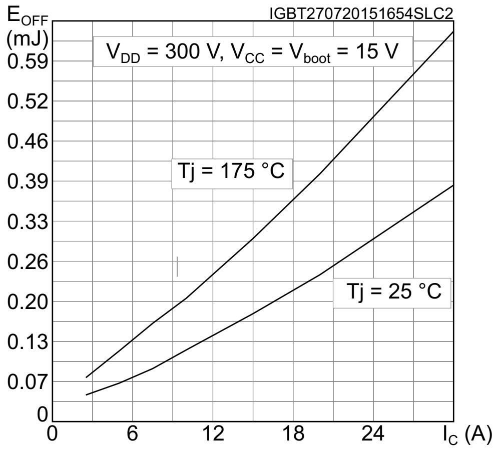


Figure 15. VTSO output characteristics vs LVIC temperature

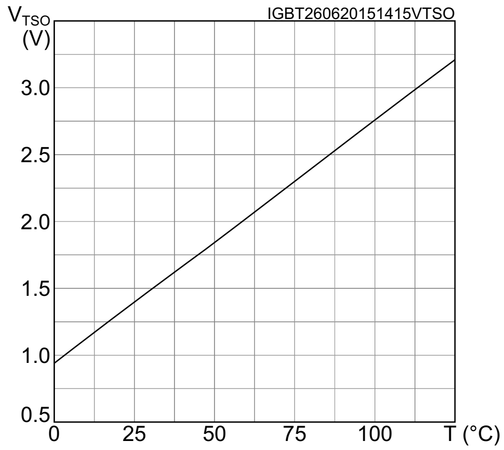
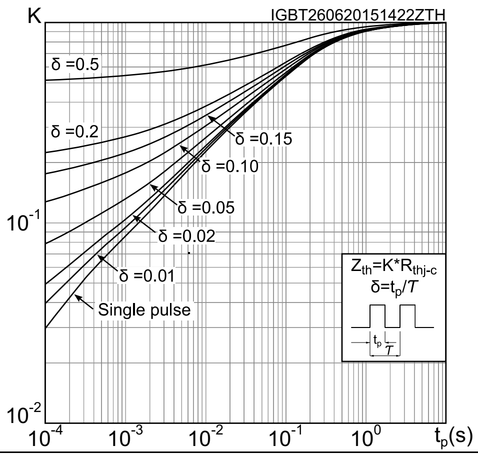


Figure 16. Thermal impedance for SDIP2F-26L IGBT



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 17. SDIP2F-26L type L mechanical drawing

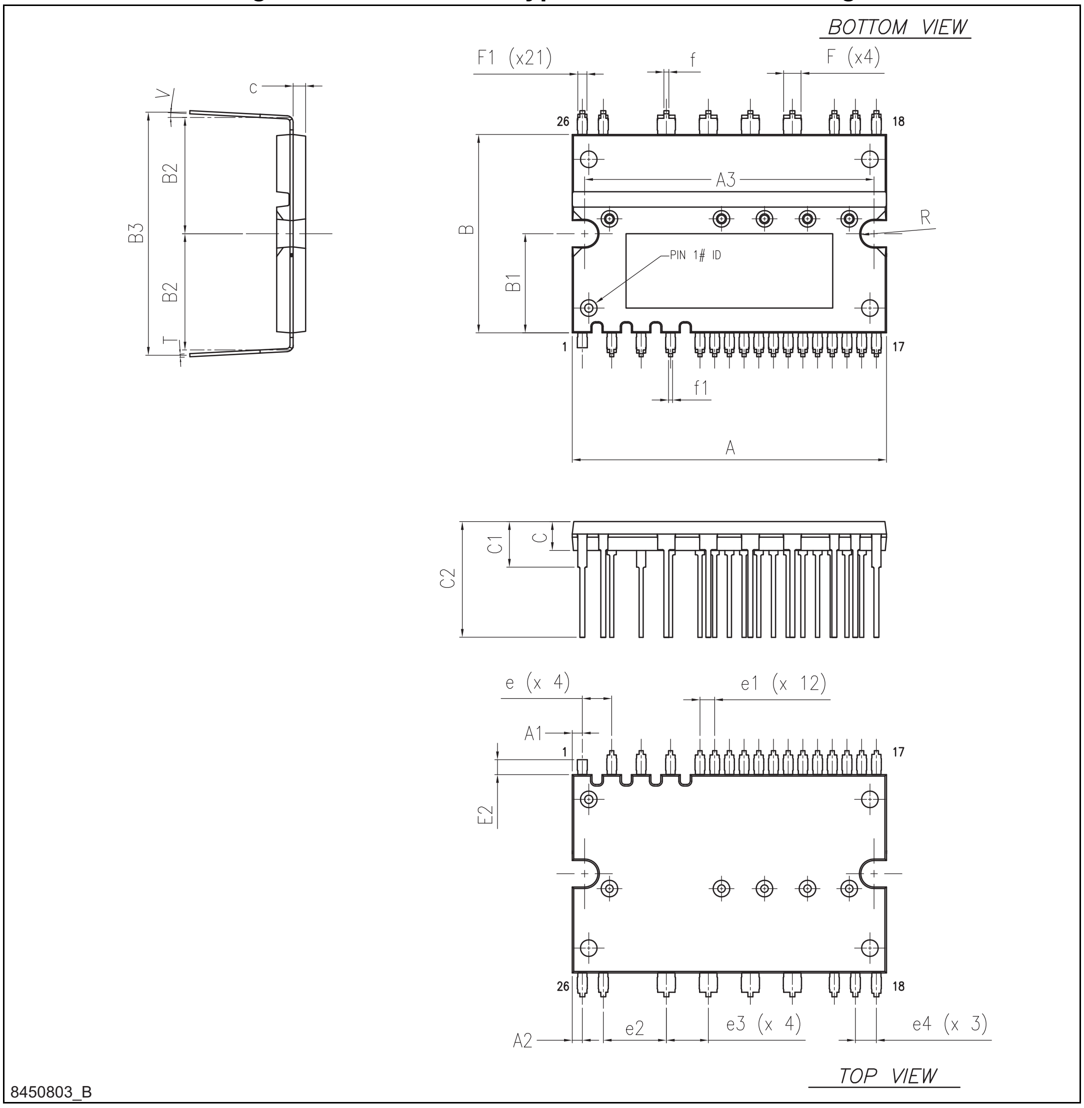


Table 13. SDIP2F-26L type L mechanical dimensions(1)

Ref.	Dimensions	Ref.	Dimensions	Ref.	Dimensions
A	38.00 ± 0.50	B3	29.40 ± 0.50	e4	2.54 ± 0.20
A1	1.22 ± 0.25	C	3.50 ± 0.20	f	0.60 ± 0.15
A2	1.22 ± 0.25	C1	5.50 ± 0.50	f1	0.50 ± 0.15
A3	35.00 ± 0.30	C2	14.00 ± 0.50	F	2.10 ± 0.15
c	1.50 ± 0.05	e	3.556 ± 0.200	F1	1.10 ± 0.15
B	24.00 ± 0.50	e1	1.778 ± 0.200	R	1.60 ± 0.20
B1	12.00	e2	7.62 ± 0.20	T	0.400 ± 0.025
B2	14.40 ± 0.50	e3	5.08 ± 0.20	V	0° / 5°

1. All dimensions are expressed in millimeters.

10 Revision history

Table 14. Document revision history

Date	Revision	Changes
15-May-2014	1	Initial release.
27-Aug-2014	2	Updated Table 1: Device summary.
27-Jul-2015	3	Updated Section 2: Absolute maximum ratings, Section 3: Electrical characteristics. Added Section 8: Electrical characteristics (curves).
03-Sep-2015	4	Modified: Features Modified: Figure 1, 6 and 7 Minor text changes
01-Oct-2015	5	Document status promoted from preliminary to production data.