

## N-channel 800 V, 0.37 $\Omega$ typ., 12 A MDmesh™ K5 Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data

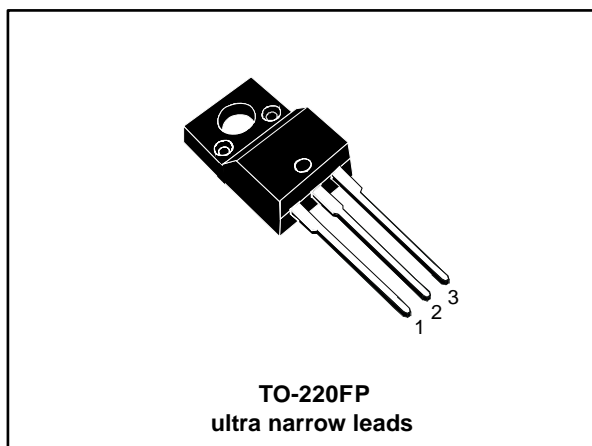
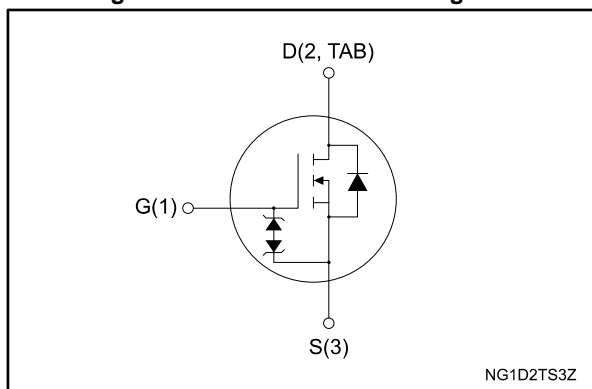


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>	P <sub>TOT</sub>
STFU13N80K5	800 V	0.45 $\Omega$	12 A	35 W

- Industry's lowest R<sub>DS(on)</sub> x area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STFU13N80K5	13N80K5	TO-220FP ultra narrow leads	Tube

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	12 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	7.6 <sup>(1)</sup>	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	48 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	35	W
$I_{AR}$	Max current during repetitive or single pulse avalanche (pulse width limited by $T_{Jmax}$ )	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	148	mJ
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^{\circ}\text{C}$ )	2500	V
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt$ <sup>(4)</sup>	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^{\circ}\text{C}$
$T_j$	Operating junction temperature		

**Notes:**<sup>(1)</sup>Limited by package.<sup>(2)</sup>Pulse width limited by safe operating area.<sup>(3)</sup> $I_{SD} \leq 12\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{Peak} \leq V_{(BR)DSS}$ .<sup>(4)</sup> $V_{SD} \leq 640\text{ V}$ .

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.57	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	

## 2 Electrical characteristics

( $T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4: On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	800			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 800\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}$			50	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 6\text{ A}$		0.37	0.45	$\Omega$

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	870	-	pF
$C_{oss}$	Output capacitance		-	50	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2	-	pF
$C_{o(tr)}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }640\text{ V}$	-	110	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			43		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 640\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 10\text{ V}$	-	29	-	nC
$Q_{gs}$	Gate-source charge		-	7	-	nC
$Q_{gd}$	Gate-drain charge		-	18	-	nC

**Notes:**

<sup>(1)</sup>Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

<sup>(2)</sup>Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$ , $I_D = 6\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	16	-	ns
$t_r$	Rise time		-	16	-	ns
$t_{d(off)}$	Turn-off delay time		-	42	-	ns
$t_f$	Fall time		-	16	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		14	A
$I_{SDM}$	Source-drain current (pulsed)		-		56	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 12\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	406		ns
$Q_{rr}$	Reverse recovery charge		-	5.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	28		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	600		ns
$Q_{rr}$	Reverse recovery charge		-	7.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	26		A

**Notes:**

<sup>(1)</sup>Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%.

Table 8: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ V}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

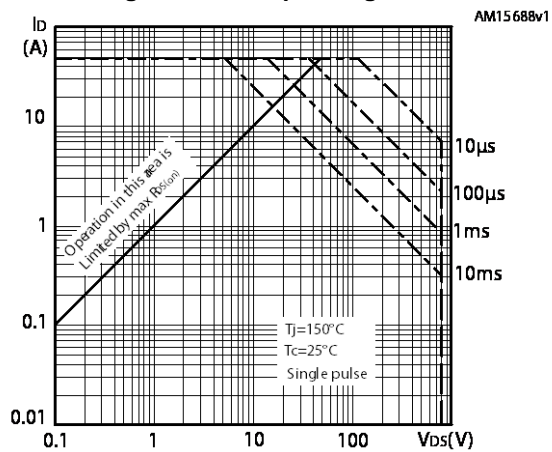


Figure 3: Thermal impedance

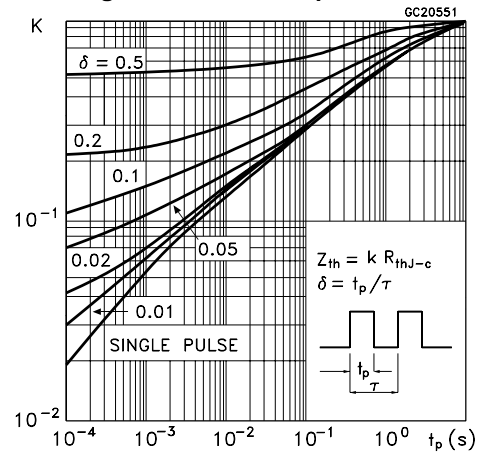


Figure 4: Output characteristics

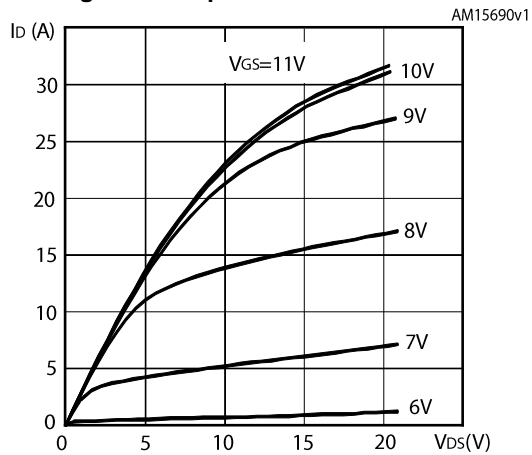


Figure 5: Transfer characteristics

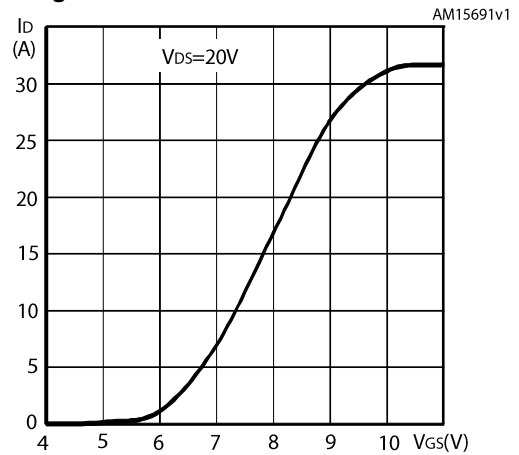


Figure 6: Gate charge vs gate-source voltage

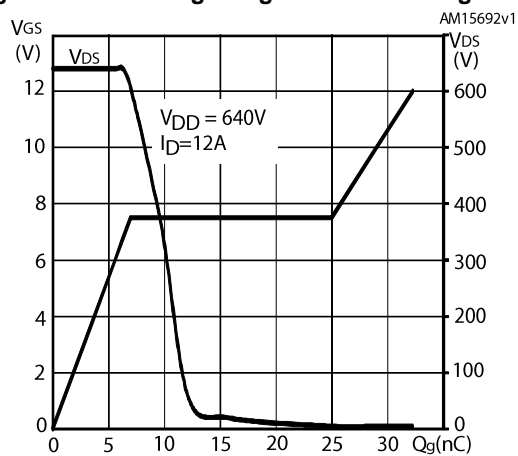


Figure 7: Static drain-source on-resistance

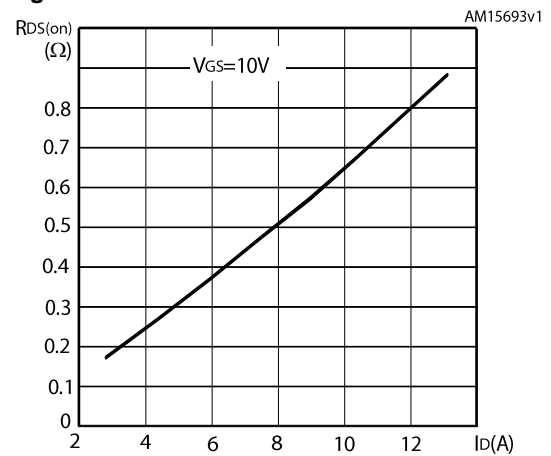


Figure 8: Capacitance variations

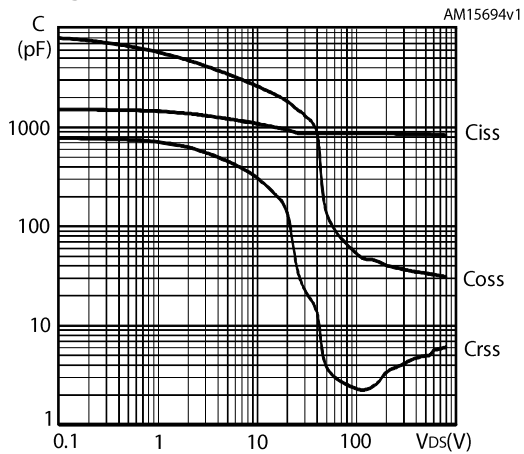


Figure 9: Source-drain diode forward characteristics

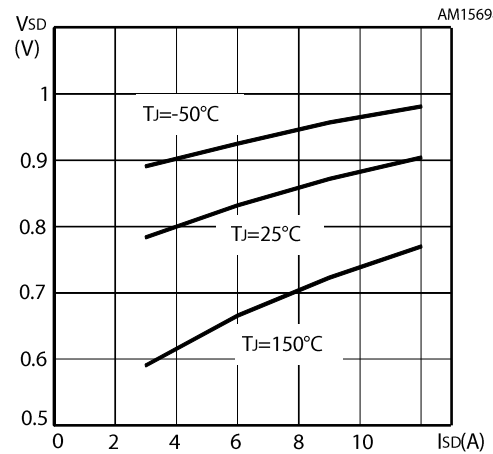


Figure 10: Normalized gate threshold voltage vs temperature

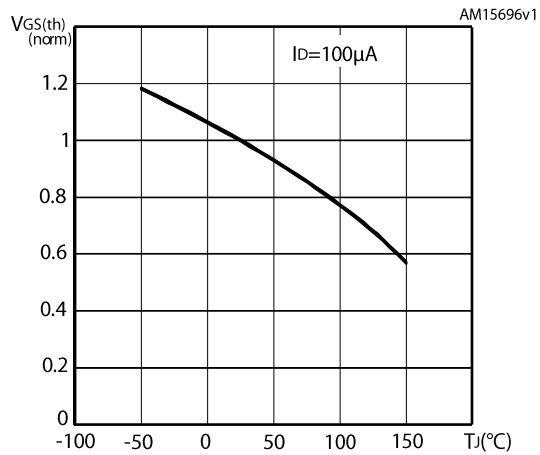


Figure 11: Normalized on-resistance vs temperature

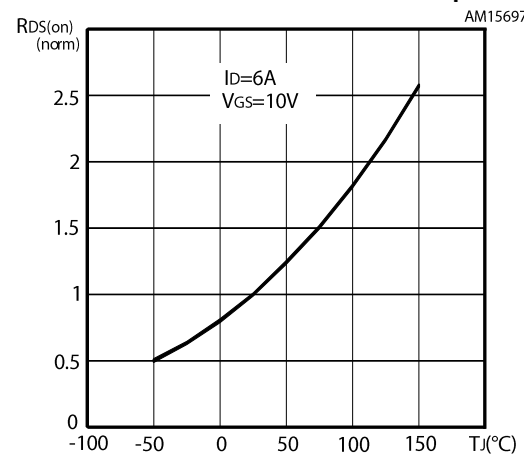


Figure 12: Output capacitance stored energy

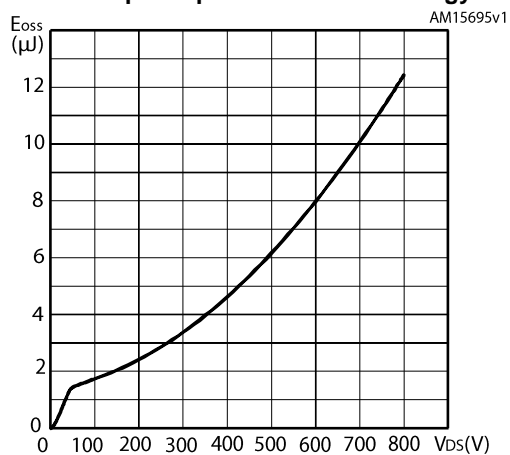


Figure 13: Normalized VDS vs temperature

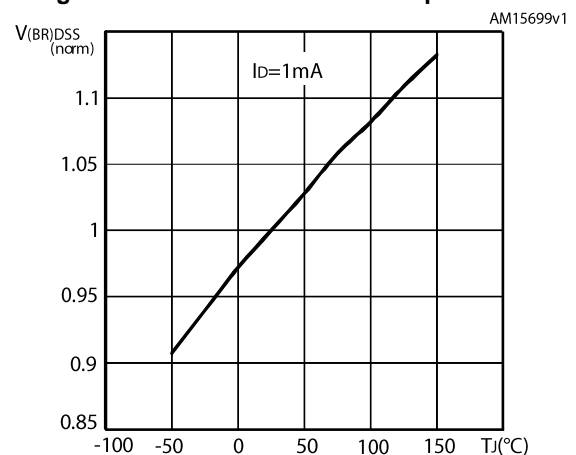
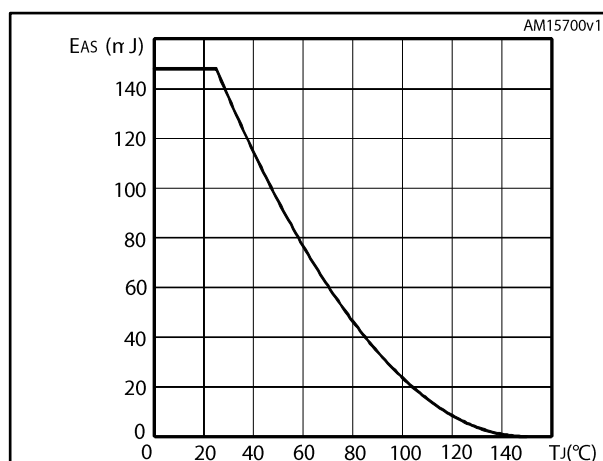
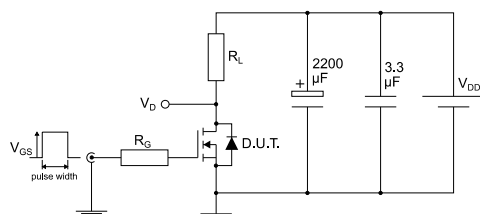


Figure 14: Maximum avalanche energy vs temperature





**Figure 15: Test circuit for resistive load switching times**



AM01468v1

AM01469v1

AM01470x1

AM01471v1

AM01472v1

AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 TO-220FP ultra narrow leads package information

Figure 21: TO-220FP ultra narrow leads package outline

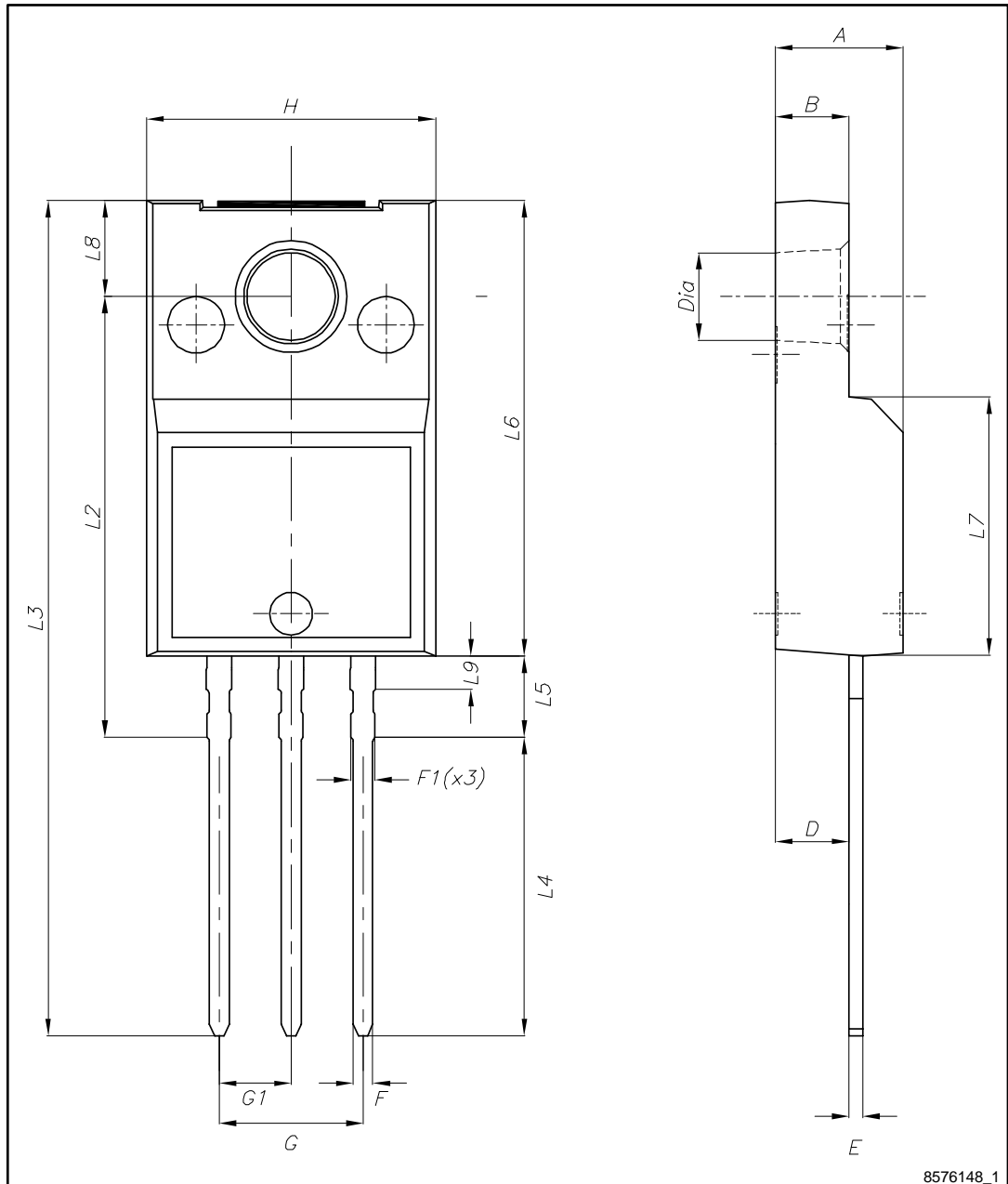


Table 9: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
08-Oct-2015	1	Initial release

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