# STF15NM65N,STFI15NM65N

## N-channel 650 V, 0.35 Ω typ., 12 A MDmesh™ II Power MOSFETs in TO-220FP and I²PAKFP packages

**Datasheet - production data**

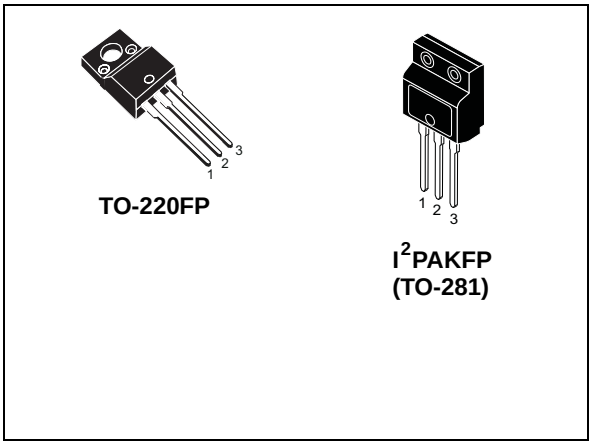
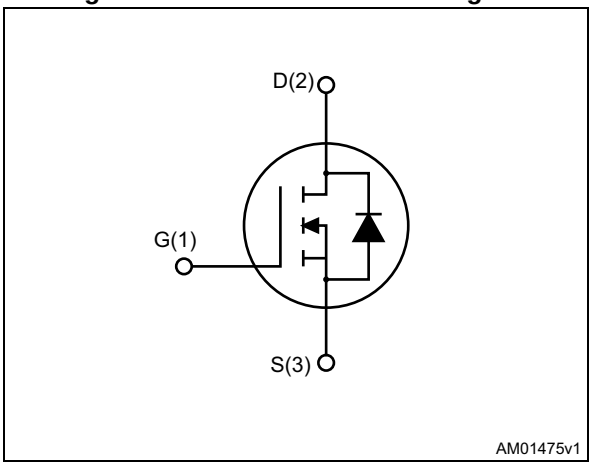



**Figure 1. Internal schematic diagram**




## Features

| Order code | $V_{DSS}$ @$T_{jmax}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STF15NM65N | 710 V | 0.38 Ω | 12 A |
| STFI15NM65N | | | |

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFETs associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

| Order code | Marking | Packages | Packing |
|---|---|---|---|
| STF15NM65N | 15NM65N | TO-220FP | Tube |
| STFI15NM65N | | I²PAKFP (TO-281) | |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | TO-220FP | $I^2$PAKFP | |
| $V_{DS}$ | Drain source voltage | 650 | | V |
| $V_{GS}$ | Gate source voltage | ± 25 | | V |
| $I_D$ | Drain current continuous Tc = 25 °C | 12(1) | | A |
| $I_D$ | Drain current continuous Tc = 100 °C | 7.56 | | A |
| $I_{DM}$(2) | Drain current pulsed | 48 | | A |
| $P_{TOT}$ | Total dissipation at Tc = 25 °C | 30 | | W |
| dv/dt(3) | Peak diode recovery voltage slope | 15 | | V/ns |
| $V_{ISO}$ | Insulation withstand voltage (RMS from all three leads to external heatsink (t = 1 s; $T_C$ = 25 °C) | 2500 | | V |
| $T_J$ | Operating junction temperature range | -55 to 150 | | °C |
| $T_{stg}$ | Storage temperature range | | | |

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD}$ ≤12 A, di/dt ≤ 400 A/µs, $V_{DSpeak}$ ≤ $V_{(BR)DSS}$, VDD = 80 % $V_{(BR)DSS}$

**Table 3. Thermal data**

| Symbol | Parameters | Value | | Unit |
|---|---|---|---|---|
| | | TO-220FP | $I^2$PAKFP | |
| $R_{thjc}$ | Thermal resistance junction-case | 4.17 | | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient | 62.5 | | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameters | Value | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{jmax}$) | 3 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 187 | mJ |

# 2 Electrical characteristics

($T_{CASE}$ = 25 °C unless otherwise specified).

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0, $I_D$ = 1 mA | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DD}$ = 650 V, $V_{GS}$=0 | | | 1 | µA |
| | | $V_{DD}$ = 650 V, $V_{GS}$ = 0 $T_C$ = 125 °C(1) | | | 100 | µA |
| $I_{GSS}$ | Gate body leakage | $V_{GS}$= ±25 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $I_D$= 250 µA, $V_{GS}$ =$V_{DS}$ | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $I_D$= 6 A, $V_{GS}$= 10V | | 0.35 | 0.38 | Ω |

1. Defined by design, not subject to production test

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Ma. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$= 50 V, f = 1MHz, $V_{GS}$= 0 V | - | 983 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 57 | - | pF |
| $C_{rss}$ | Reverse capacitance | | - | 4.5 | - | pF |
| $C_{osseq}$ (1) | Equivalent output. capacitance | $V_{DS}$ = 0 V to 520 V, $V_{GS}$ = 0 V | - | 146 | - | pF |
| $R_g$ | Intrinsic gate resistance | f = 1MHz $I_D$ = 0 A | - | 4.6 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$= 520 V, $I_D$=12 A, $V_{GS}$= 10 V (see *Figure 13: Gate charge test circuit*) | - | 33.3 | - | nC |
| $Q_{gs}$ | Gate source charge | | - | 5.7 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 17 | - | nC |

1. Cross eq: defined as a constant equivalent capacitance giving the same charging time as $C_{OSS}$ when $V_{DS}$ increases from 0 to 80 % $V_{DSS}$.

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$= 325 V, $I_D$ = 6 A $R_g$= 4.7 Ω, $V_{GS}$ = 10 V(see *Figure 12: Switching times test circuit for resistive load* and *Figure 17: Switching time waveform*) | - | 55.5 | - | ns |
| $t_r$ | Rise time | | - | 8.5 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 14 | - | ns |
| $t_f$ | Fall time | | - | 11.4 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source drain current | | - | | 12 | A |
| $I_{SDM}$(1) | Source drain current (pulsed) | | - | | 48 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 12 A, $V_{GS}$ = 0 V | - | | 1.6 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 12 A, di/dt = 100 A/µs $V_{DD}$ = 60 V(see *Figure 14: Test circuit for inductive load switching and diode recovery times*) | - | 428 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 4.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 21.5 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$= 12 A, di/dt = 100 A/µs $V_{DD}$ = 60 V, $T_j$ = 150 °C (see *Figure 14: Test circuit for inductive load switching and diode recovery times*) | - | 570 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 6.2 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 22 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

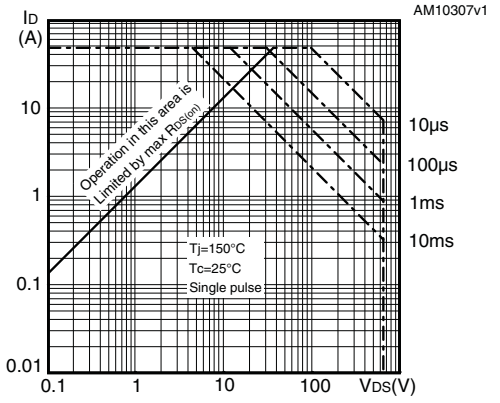



**Figure 3. Thermal impedance**

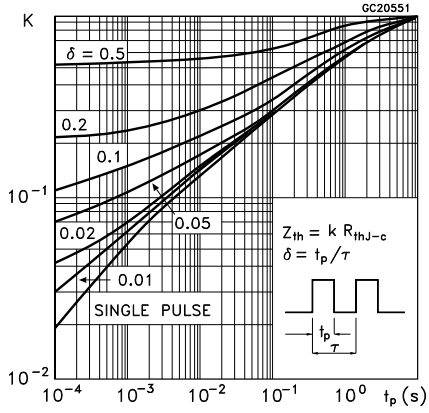



**Figure 4. Output characteristics**

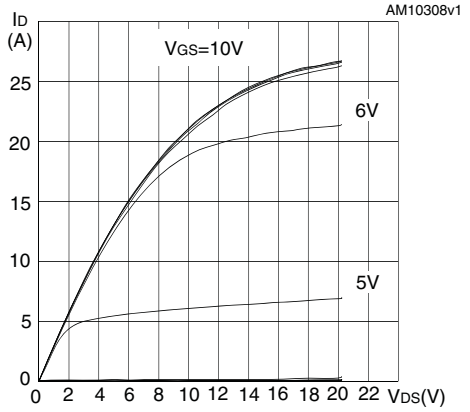



**Figure 5. Transfer characteristics**

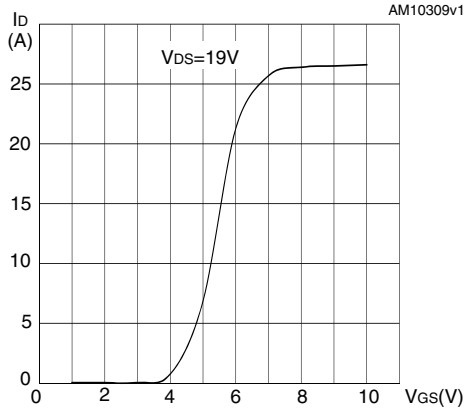



**Figure 6. Static drain-source on-resistance**

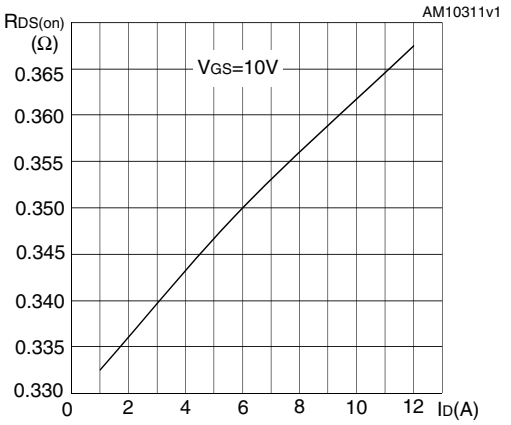



**Figure 7. Gate charge vs gate-source voltage**

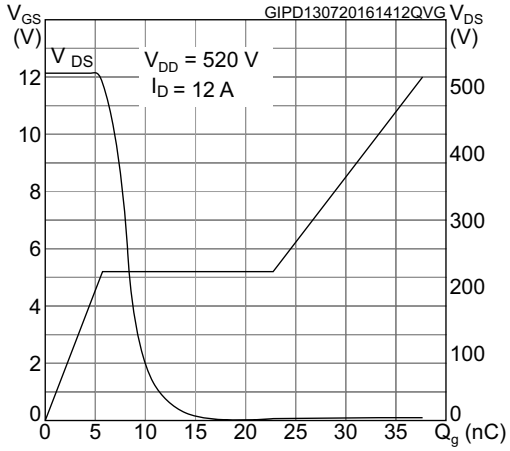


**Figure 8. Capacitance variations**

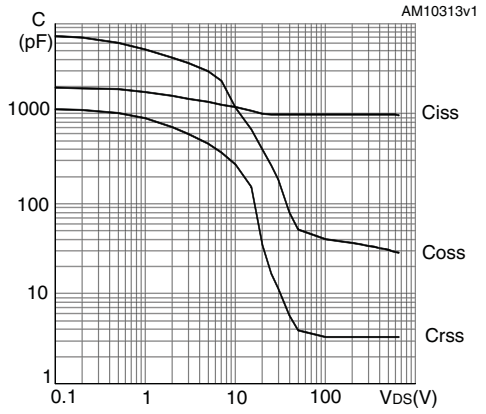



**Figure 9. Normalized gate threshold voltage vs temperature**

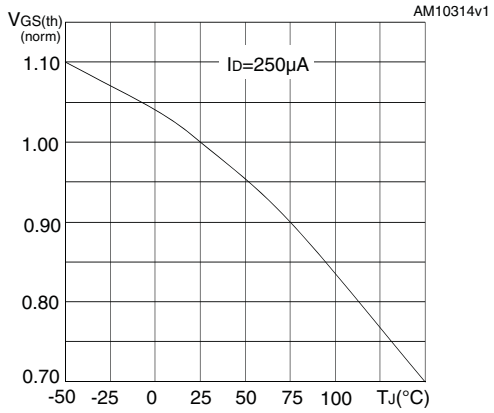
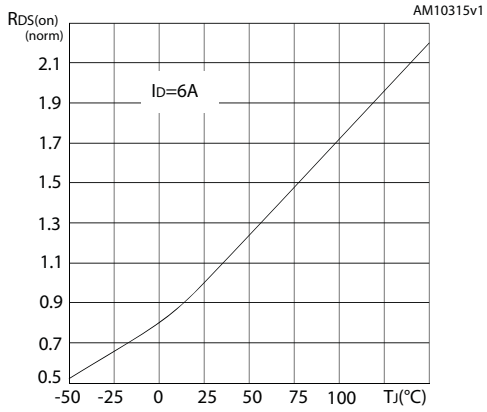



**Figure 10. Normalized on-resistance vs temp.**




**Source-drain diode forward characteristics**

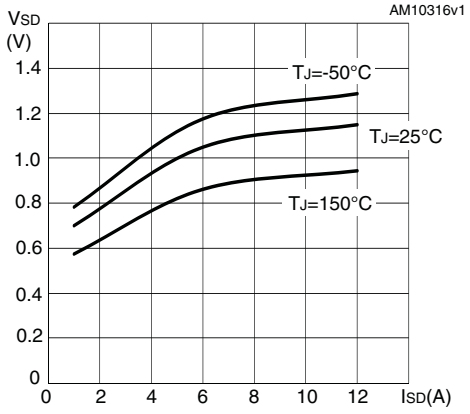
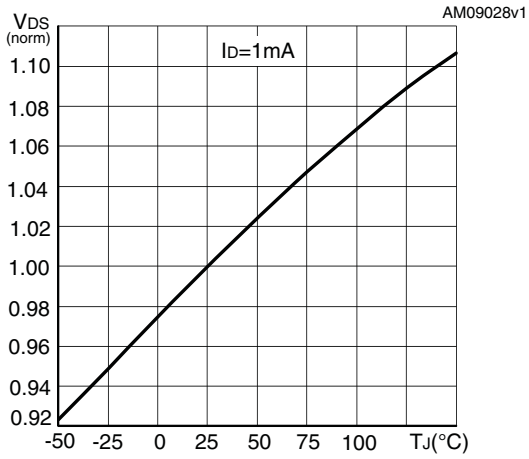



**Figure 11. Normalized $V_{DS}$ vs temperature**



# 3 Test circuits

**Figure 12. Switching times test circuit for resistive load**

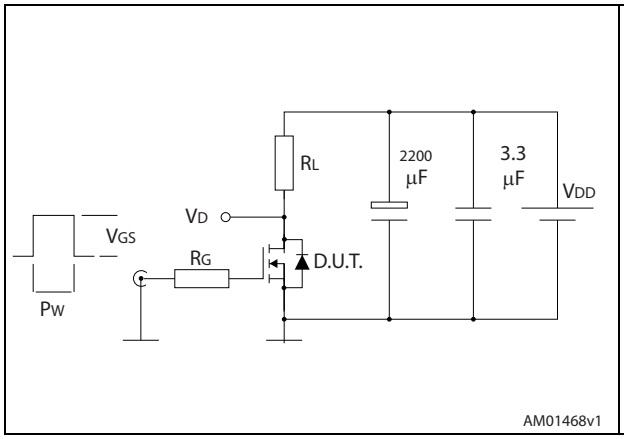



**Figure 13. Gate charge test circuit**

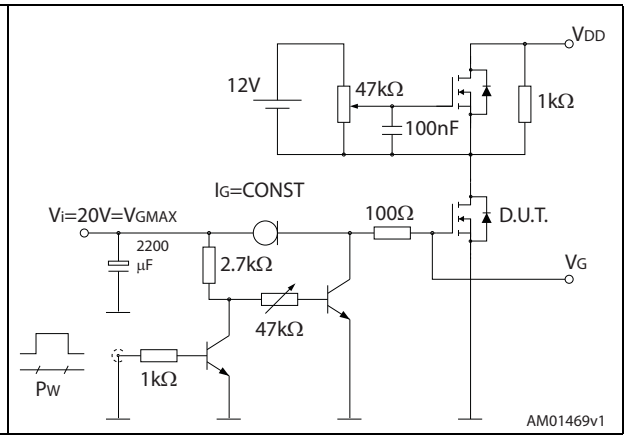



**Figure 14. Test circuit for inductive load switching and diode recovery times**

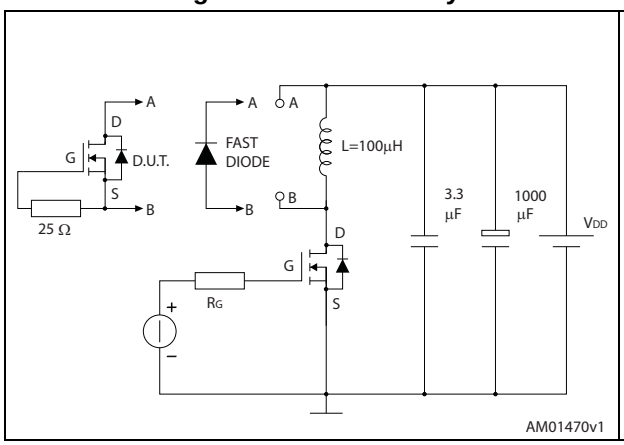



**Figure 15. Unclamped inductive load test circuit**

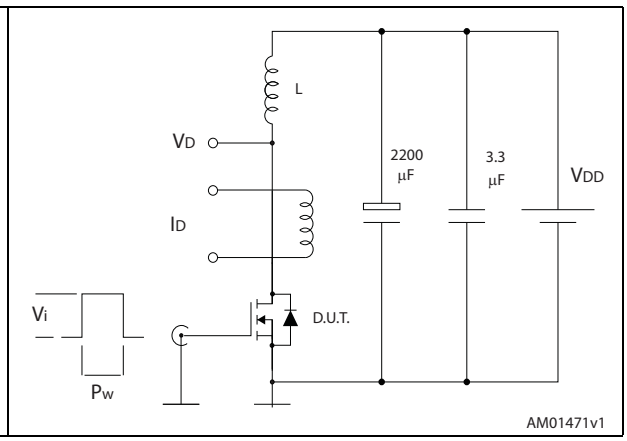



**Figure 16. Unclamped inductive waveform**

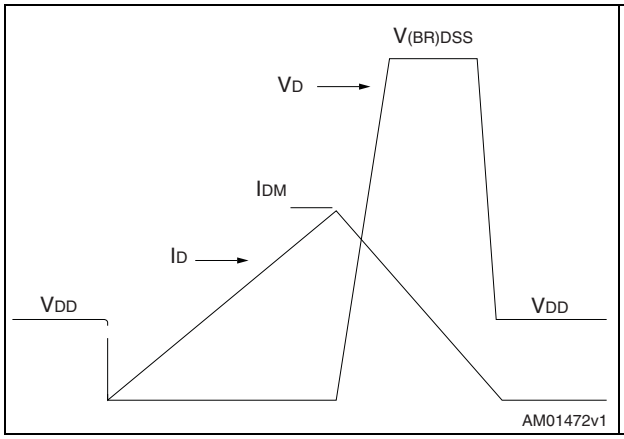
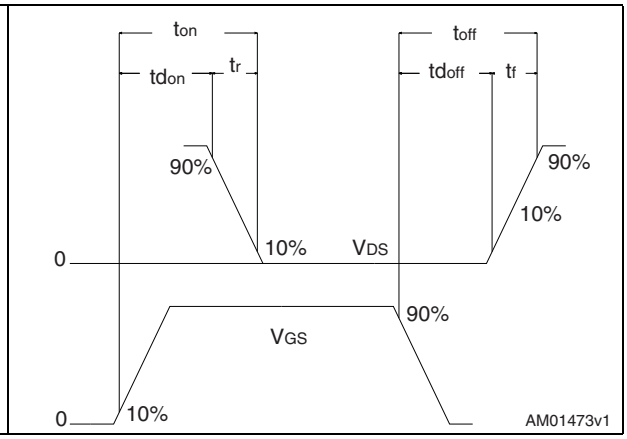



**Figure 17. Switching time waveform**



# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 4.1 TO-220FP package information

Figure 18. TO-220FP package outline

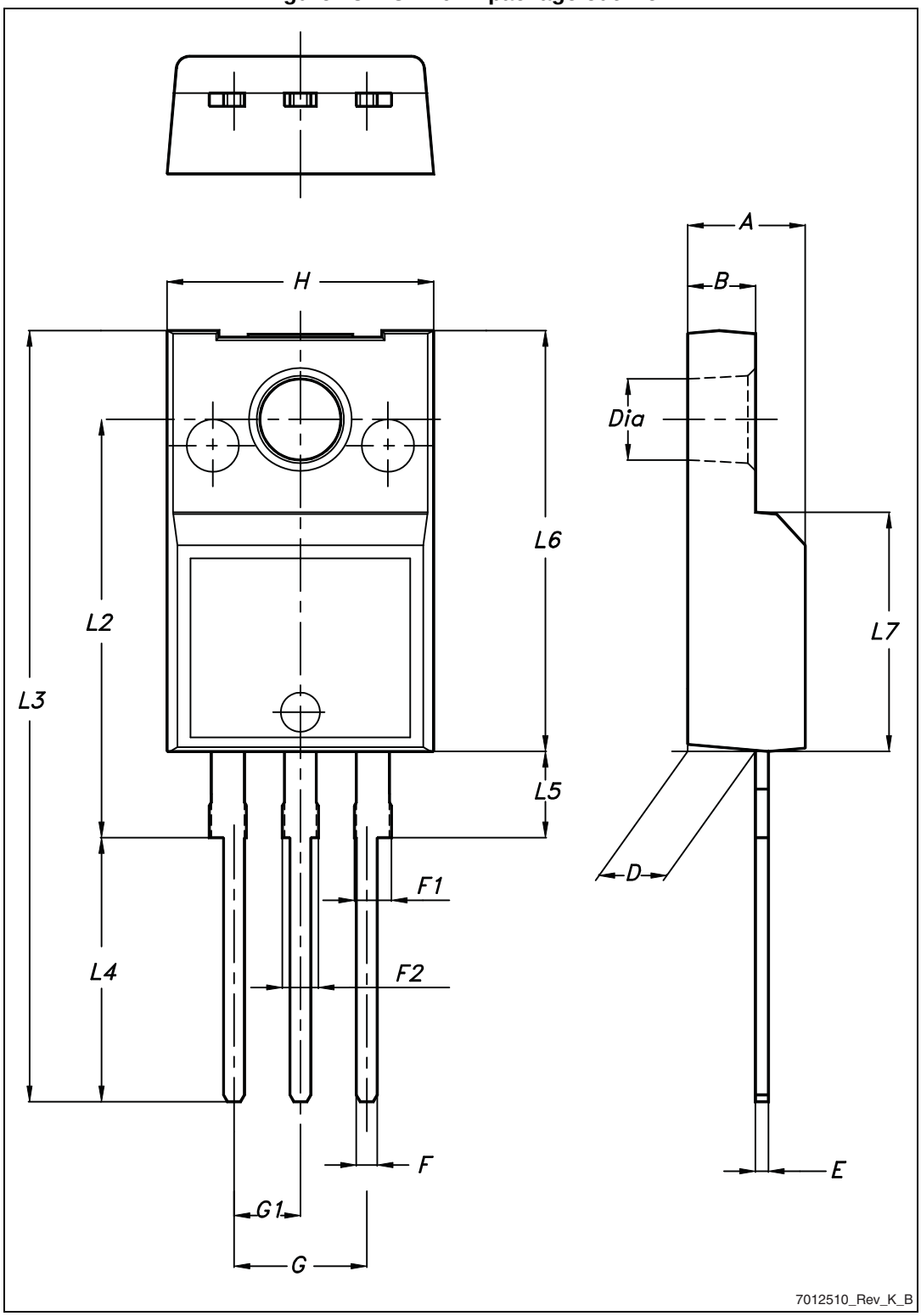


Table 9. TO-220FP package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

## 4.2 I²PAKFP (TO-281) package information

Figure 19. I²PAKFP (TO-281) package outline

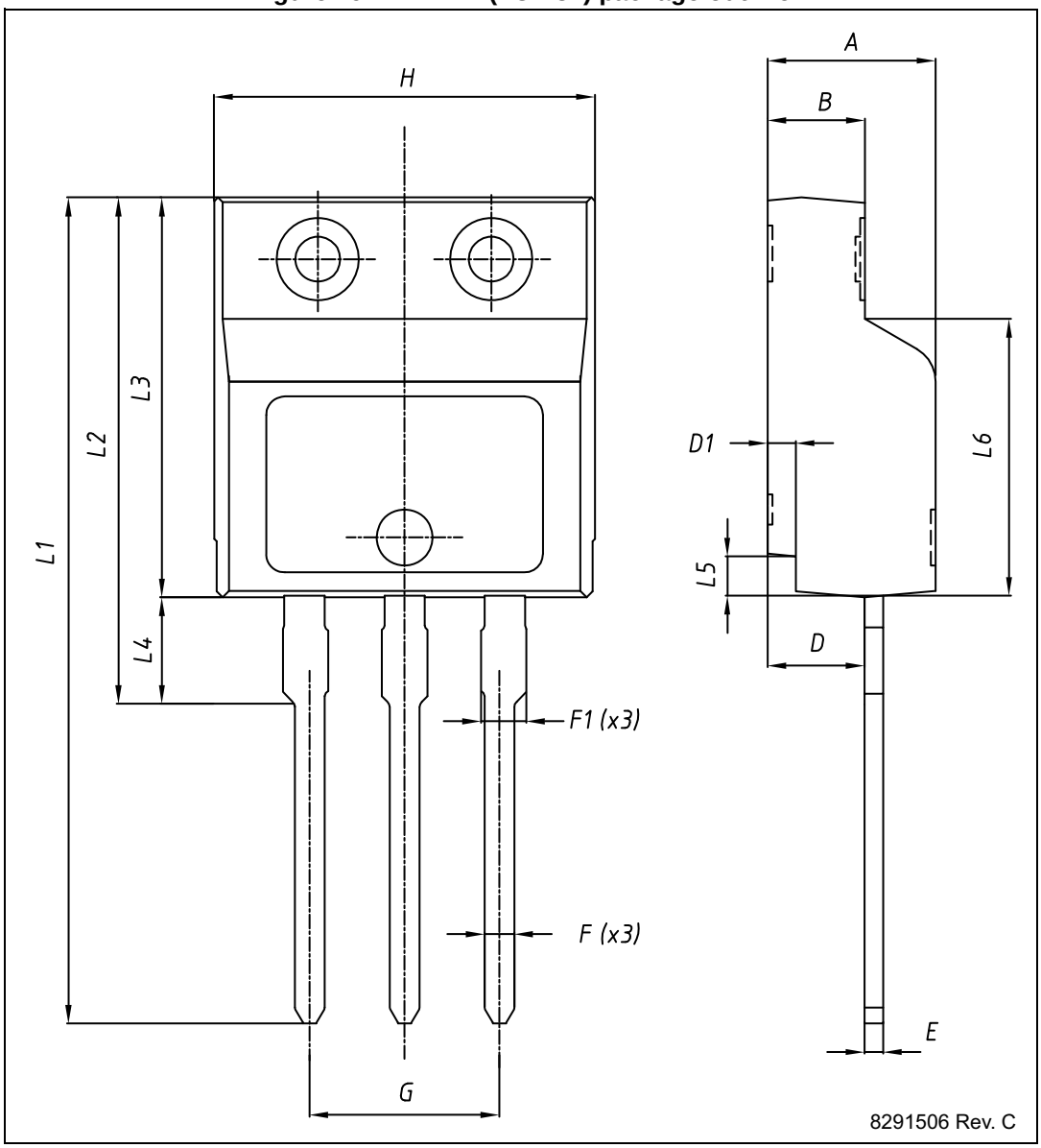


Table 10. $I^2PAKFP$ (TO-281) package mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| B | 2.50 | | 2.70 |
| D | 2.50 | | 2.75 |
| D1 | 0.65 | | 0.85 |
| E | 0.45 | | 0.70 |
| F | 0.75 | | 1.00 |
| F1 | | | 1.20 |
| G | 4.95 | | 5.20 |
| H | 10.00 | | 10.40 |
| L1 | 21.00 | | 23.00 |
| L2 | 13.20 | | 14.10 |
| L3 | 10.55 | | 10.85 |
| L4 | 2.70 | | 3.20 |
| L5 | 0.85 | | 1.25 |
| L6 | 7.50 | 7.60 | 7.70 |

# 5 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 11-May-2011 | 1 | Initial release. |
| 21-Jun-2011 | 2 | Document status promoted form preliminary data to datasheet, added Section 2.1: Electrical characteristics (curves). |
| 17-Jul-2013 | 3 | – Added: $I^2$PAKFP package<br>– Added: *Table 10* and *Figure 22*<br>– Updated: *Section 4: Package information*<br>– Minor text changes. |
| 25-Jul-2016 | 4 | The part number STP15NM65N has been moved to a separate datasheet.<br>Minor text changes. |