

N-channel 650 V, 0.6 Ω typ., 7 A MDmesh™ M2 Power MOSFETs in TO-220FP and I²PAKFP packages

Datasheet - production data

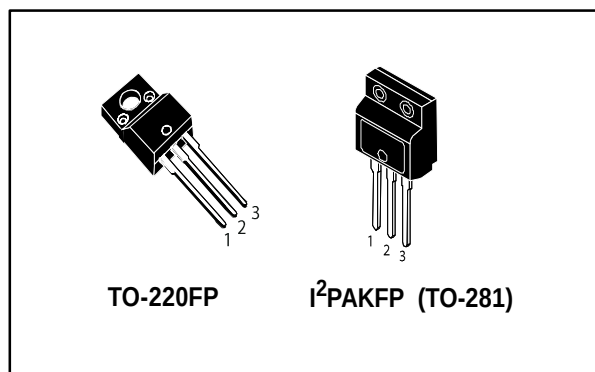
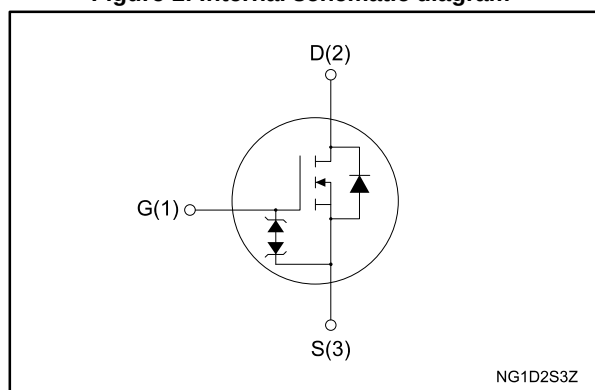


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STF11N65M2	650 V	0.68 Ω	7 A	25 W
STFI11N65M2				

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, these devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STF11N65M2	11N65M2	TO-220FP	Tube
STFI11N65M2		I ² PAKFP	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	7	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	4.4	
$I_{DM}^{(2)}$	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	25	W
$dv/dt^{(3)(4)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(5)}$	MOSFET dv/dt ruggedness	50	
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_c = 25\text{ }^{\circ}\text{C}$)	2500	V
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature		

Notes:

- (1) The value is rated according to $R_{thj-case}$ and limited by package.
 (2) Pulse width limited by T_{jmax} .
 (3) starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$.
 (4) $I_{SD} \leq 7\text{ A}$, $di/dt = 400\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.
 (5) $V_{DS} \leq 520\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	1.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	110	mJ

Notes:

- (1) Pulse width limited by T_{jmax} .
 (2) starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	650			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 650 V			1	μA
		V _{GS} = 0 V, V _{DS} = 650 V, T _{case} = 125 °C			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.5 A		0.6	0.68	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	410	-	pF
C _{oss}	Output capacitance		-	20	-	
C _{rss}	Reverse transfer capacitance		-	0.95	-	
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	83	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	6.4	-	Ω
Q _g	Total gate charge	V _{DD} = 520 V, I _D = 7 A, V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	12.5	-	nC
Q _{gs}	Gate-source charge		-	3.2	-	
Q _{gd}	Gate-drain charge		-	5.8	-	

Notes:

⁽¹⁾ C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 3.5 A R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	9.5	-	ns
t _r	Rise time		-	7.5	-	
t _{d(off)}	Turn-off delay time		-	26	-	
t _f	Fall time		-	15	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 7\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	318		ns
Q_{rr}	Reverse recovery charge		-	2.5		μC
I_{RRM}	Reverse recovery current		-	15.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16 : "Test circuit for inductive load switching and diode recovery times")	-	437		ns
Q_{rr}	Reverse recovery charge		-	3.2		μC
I_{RRM}	Reverse recovery current		-	15		A

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

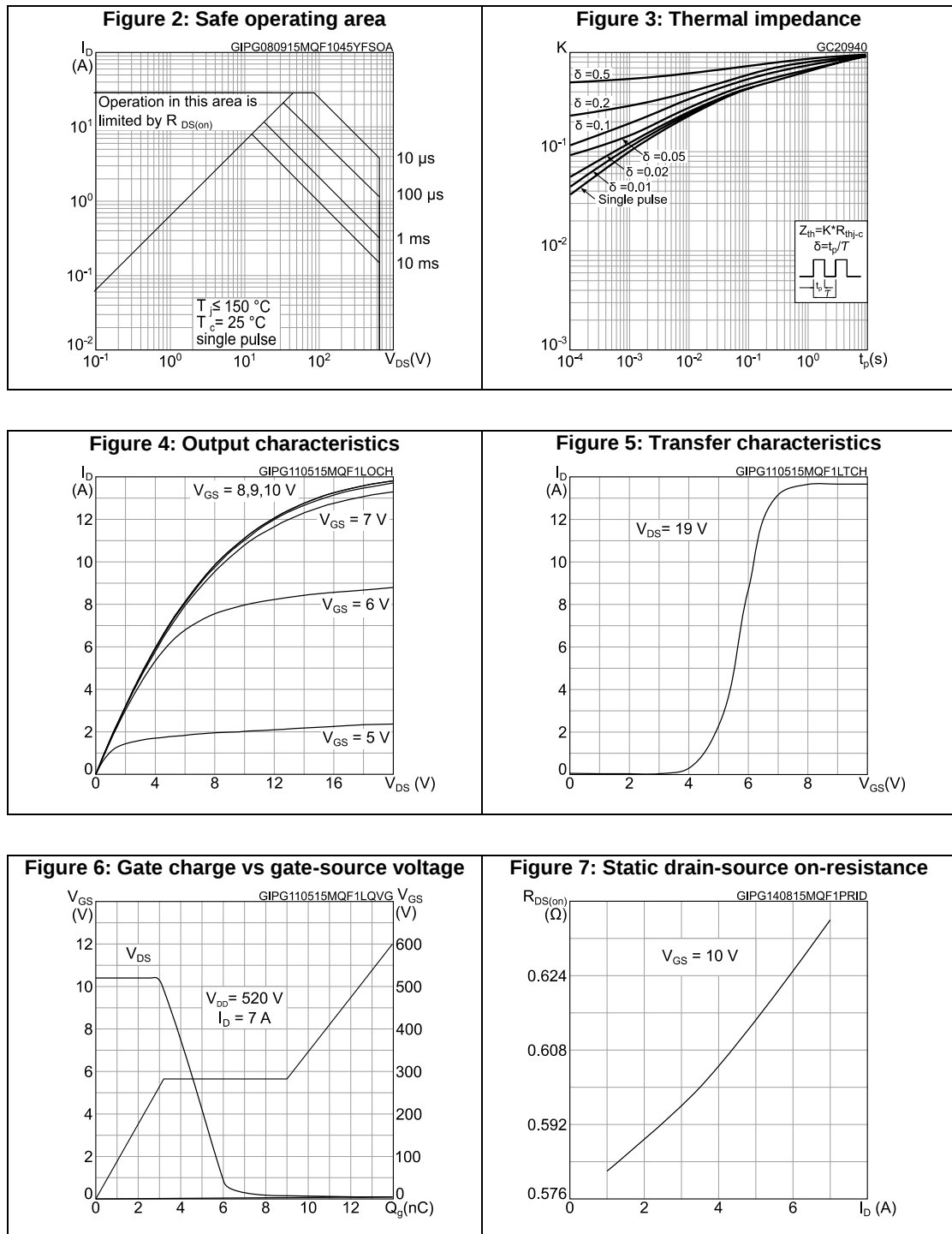


Figure 8: Capacitance variations

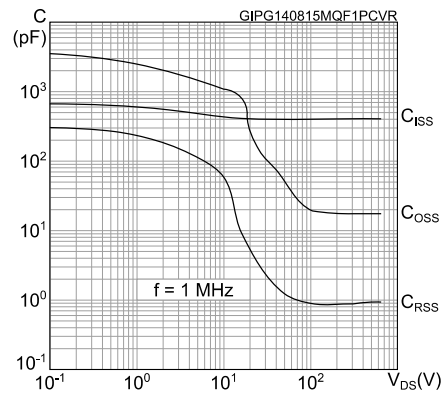


Figure 9: Normalized gate threshold voltage vs temperature

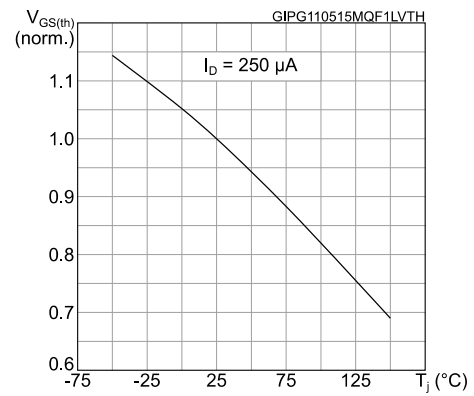


Figure 10: Normalized on-resistance vs temperature

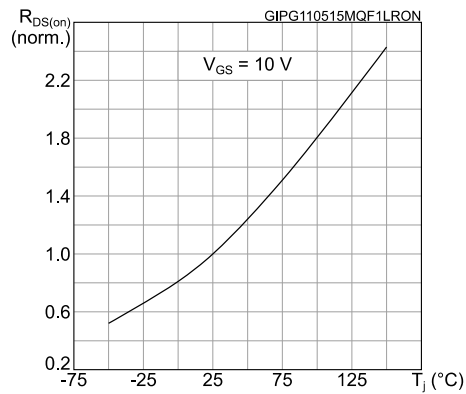


Figure 11: Normalized V(BR)DSS vs temperature

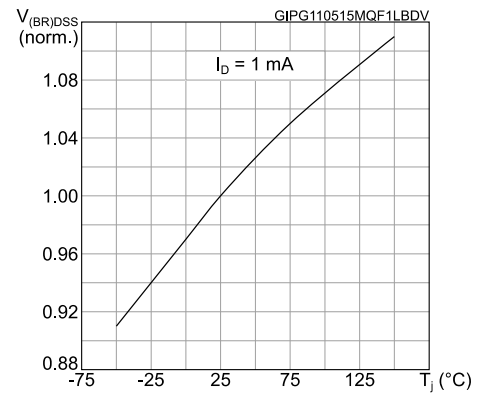


Figure 12: Output capacitance stored energy

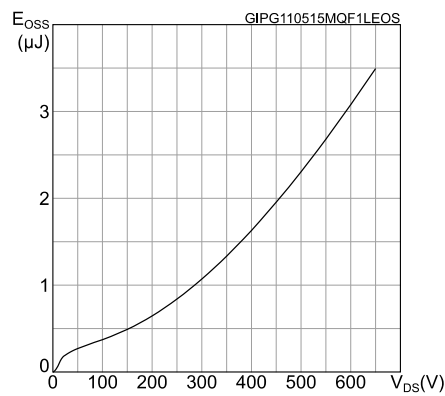
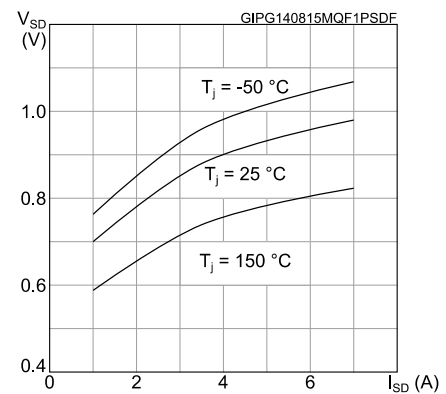
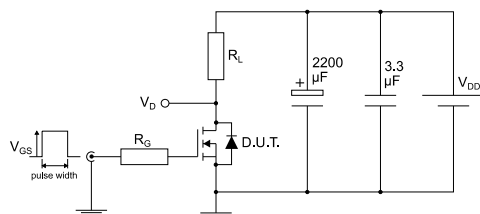


Figure 13: Source- drain diode forward characteristics



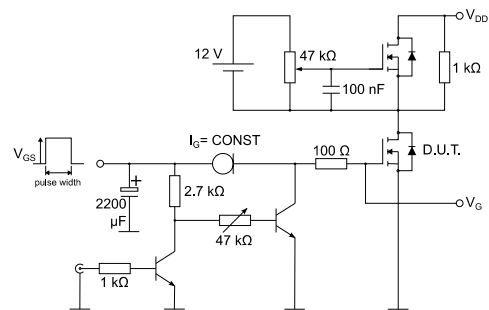
3 Test circuits

Figure 14: Test circuit for resistive load switching times



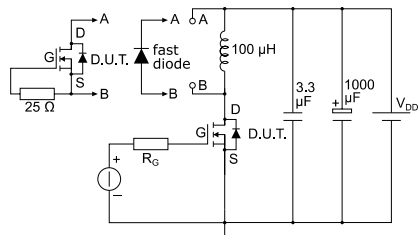
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Figure 15: Test circuit for gate charge behavior



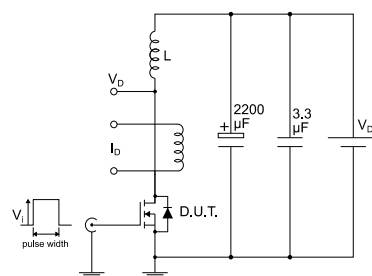
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Figure 16: Test circuit for inductive load switching and diode recovery times



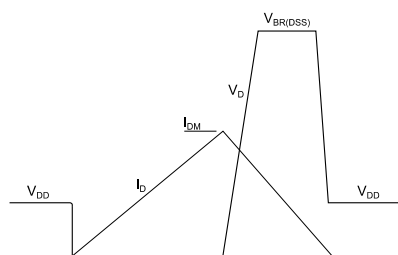
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Figure 17: Unclamped inductive load test circuit



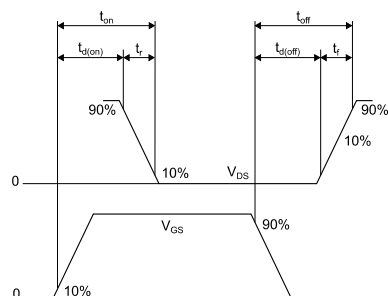
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20: TO-220FP package outline

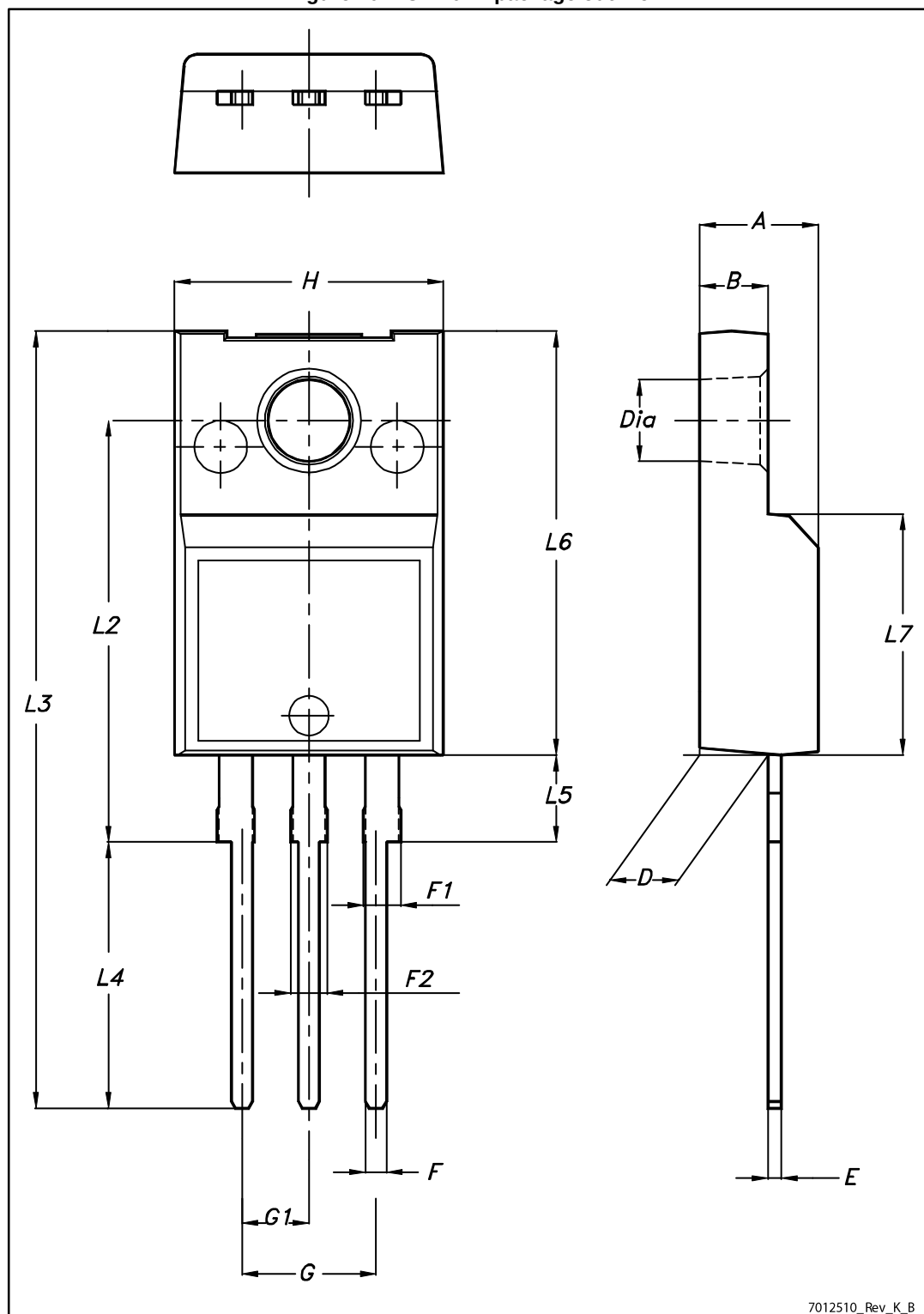


Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

4.2 I²PAKFP (TO-281) package information

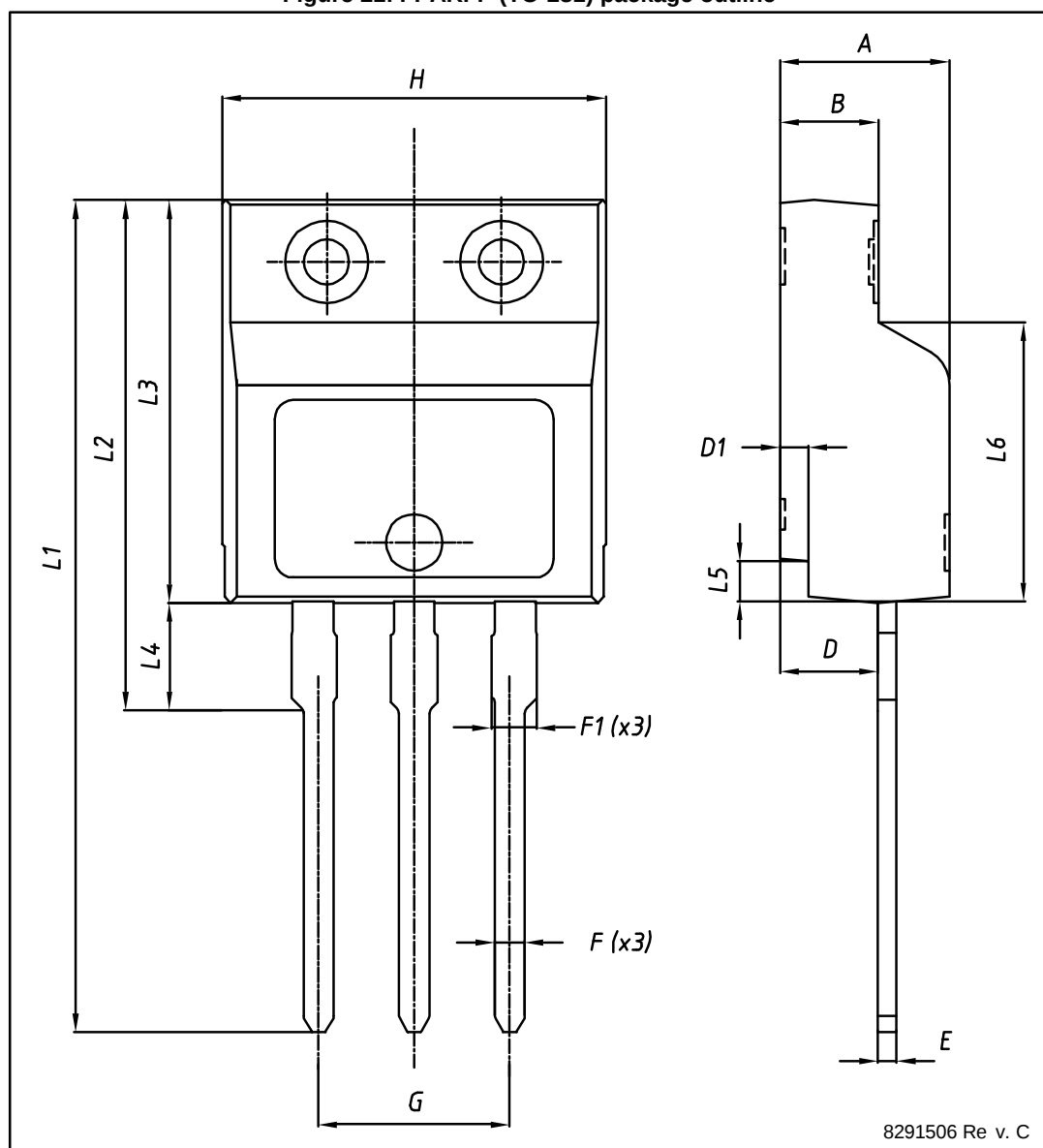
Figure 21: I²PAKFP (TO-281) package outline

Table 10: I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
09-May-2014	1	First release.
08-Sep-2015	2	Text and formatting changes throughout document. On cover page: - updated <i>Title</i> and <i>Features</i> In section <i>Electrical characteristics</i> : - updated and renamed table <i>Static</i> (was On /off states) Updated section <i>Electrical characteristics (curves)</i> Updated and renamed section <i>Package information</i> (was Package mechanical data)

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