



# STDP9310, STDP9320, STDP9210, STDP7320, STDP7310

Athena — Premium high resolution multimedia monitor controller  
with 3D video

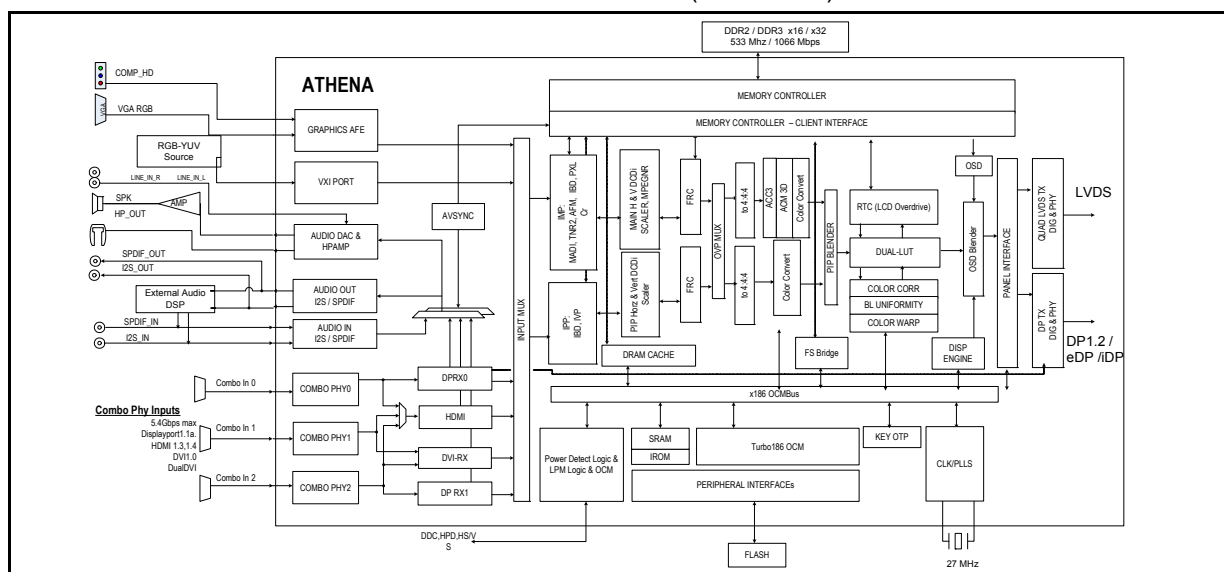
Data brief

## Features

- Single-chip WQXGA (2560 x 1600) monitor scaler (STDP93x0)
- Single-chip 3D FHD (1920 x 1080 120 Hz) monitor scaler (STDP9210)
- Single-chip WUXGA (1920 x 1200) monitor scaler (STDP73x0)
- Integrated DisplayPort® (DP) 1.2 compliant Rx and Tx with support for eDP, multistream, and 3D video formats
- Supports VESA Mobility DisplayPort (MyDP) standard
- Video processing supports full or partial capture of 4096 x 2160 format scaled to 2560 x 2160 output format
- Integrated HDMI 1.4 and dual-DVI receiver to support 3D video
- 10-bit triple ADCs (sampling rate up to 205 MHz)
  - Integrated 2:1 MUX to receive VGA and component input
- High-speed dual LVDS Tx (STDP73x0) or quad LVDS Tx (STDP93x0/STDP9210)
- DDR2/DDR3 memory interface 32 bits wide (STDP93x0/STDP9210) or 16 bits wide (STDP73x0)
- Supports daisy chaining of monitors of up to four streams (STDP9320/STDP7320)
- Video window detection for multimedia content display
- Panel backlight RGB uniformity compensation
- Advanced Faroudja® video processing: MADi and DCDi
- 6-axis color control independent of ACC
- Advanced bit-mapped OSD controller
- 3D Frame Rate Conversion (FRC) and advanced overdrive to support 3D video
- 4K x 2K screen resolution support
- Advanced PIP for all input sources

## Applications

- Multifunctional monitors including 3D monitor, max input and output resolution up to WQXGA (STDP93x0), FHD (STDP9210), and WUXGA (STDP73x0)



# 1 Description

The STDP93x0, STDP9210, and STDP73x0 (i.e. Athena) ICs are a series of innovative System-on-Chip (SoC) controllers designed for multifunctional monitors with a maximum resolution of up to 2560 x 1600 (STDP93x0), 1920 x 1200 (STDP73x0), and 120 Hz FHD (STDP9210).

The Athena chips are the first ICs to combine a DP 1.2 receiver/transmitter, HDMI 1.4 receiver, and dual DVI receiver to support 3D video source from graphics cards and Blu-rays for full HD 120 Hz display. The Athena ICs can capture a maximum of 4096 pixels by 2160 lines. This can be either bypassed unchanged or scaled down to a maximum of 2560 x 1600 or 2048 x 2160 (STDP93x0) or 1920 x 1200 (STDP73x0) or 120 Hz FHD (STDP92x0). Two types of output ports (i.e. LVDS and DP) deliver unparalleled image quality and supports display resolutions of up to WQXGA, WUXGA, and FHD as well. Both outputs simultaneously output the scaled video, or the bypassed captured input video. Alternately, the DisplayPort transmitters may be programmed to drive a multi-stream display.

The Athena SoCs allow for a flexible LCD/notebook panel interface by providing high-speed dual (STDP73x0) and quad (STDP93x0/STDP9210) LVDS transmitters as well as iDP/eDP1.2 transmitters. DP 1.2 enables multi-monitor displays (i.e. daisy chain support) in STDP9320 and STDP7320 by providing multiple streams through a signal cable connection. The DisplayPort receiver in the Athena chips is in compliance with the VESA Mobility DisplayPort (MyDP) standard. As a MyDP sink, the Athena SoCs can receive 1080P 60 Hz video and audio from a MyDP enabled smartphone and tablet to mirror the mobile video on a large screen display.

## 2 Introduction

The Athena SoCs greatly simplify the design for WQXGA monitors, 120 Hz FHD monitors, and WUXGA multifunctional monitors with their unique integration of video inputs/outputs, video processors, advanced video quality enhancement engines, DDR2 and DDR3 controllers, usability features such as PIP video window detection, and cost-effective firmware update technology. In addition, the Athena ICs allow design of 4K x 2K monitors using multiple devices.

Their rich feature sets, high level of integration, improved scaling and video processing, and color management technologies (e.g. 6-axis color control and RGB uniformity compensation) make STDP93x0, STDP9210, and STDP73x0 the ideal answers for high-quality, integrated multimedia monitor solutions.

A new feature—Video Window Detection—automatically detects video content on selected PC DVI, HDMI, or DP input and frames the content in a window to enable selective video processing such as Adaptive Contrast Control 3 (ACC3) and Active Color Management-3D (ACM-3D), enhancer, and sharpness. This enables viewers to enjoy watching Web-based multimedia content with image enhancement applied inside the detected active video window.

The new technology, EZ-Display UP, provides the ability to upgrade to the latest firmware through the existing DisplayPort or HDMI interfaces on the monitor scaler. This new feature enables faster and easier firmware upgrades than the traditional method—without the need to open the monitor cabinet.

The Athena SoCs offer DisplayPort (DP) 1.2 interface for receiver and transmitter applications. The integrated receiver and transmitter support an open industry “DisplayPort Standard” AV interface introduced by VESA. This new interface standard offers high bandwidth AV signal transmission over fewer lines for interconnects within multimedia monitor applications. The DisplayPort standard includes an optional HDCP 1.3 content protection scheme for secured audio-visual data transmission between sources and sink devices.

**Table 1. Athena selection table**

Part number	Application	DDR I/F	TTL Input	Output	Package
STDP9320-BB	WQXGA with daisy chain	32-bit	Yes	Quad LVDS and DP 1.2	521-ball HSBGA
STDP9310-BB	WQXGA	32-bit	Yes	Quad LVDS or DP 1.2	521-ball LFBGA
STDP9210-BB	3D FHD 120 Hz	32-bit	Yes	Quad LVDS or DP 1.2	521-ball LFBGA
STDP7320-BB	WUXGA with daisy chain	16-bit	No	Dual LVDS and DP 1.2	361-ball LFBGA
STDP7310-BB	WUXGA	16-bit	No	Dual LVDS or DP 1.2	361-ball LFBGA

## 3 Main features

### 3.1 Resolutions

- WQXGA (2560 x 1600 / 1440) 60 Hz input and output
- 3D FHD (1920 x 1080) 120 Hz input and output
- 4K x 2K screen resolution support
- 4096 x 2160 input frame capture & bypass
- 2560 x 2160 video processing output

### 3.2 Dual integrated DisplayPort receivers

- Two 4-lane DisplayPort receivers, one DP1.2 & the other DP1.1a compliant
- Max DP link speed up to 5.4 GHz for DP1.2 and max 2.7 GHz speed on the DP1.1a receiver
- Support MyDP and eDP input
- Max video resolution 2560x1600
- Support 3D stereo video format
- Max video stream pixel clock: 300 MHz
- Support GTC AV Sync and HBR audio format
- Support repeater for multi-stream daisy-chain monitor
- HDCP 1.3 content protection with integrated key storage

### 3.3 Integrated HDMI 1.4 receiver

- Max HDMI speed up to 3 GHz
- Deep color and wide gamut support
- Max video resolution 2560x1600
- Support 3D stereo video format
- Max video stream pixel clock out: 300 MHz
- Support HBR audio format
- HDCP 1.4 content protection with integrated key storage

### 3.4 Dual integrated DVI receiver

- Support Dual DVI input for 3D Video up to 300 MHz
- Max DVI speed up to 165 MHz in single DVI Mode
- Max video resolution 2560x1600
- HDCP 1.2 content protection with integrated key storage

### 3.5 Analog video input port

- Integrated 10-bit triple ADCs
- 1x VGA(RGB) and 1x component input
- Max ADC sampling rate: 205 MHz
- Low power mode support and sync detection

### 3.6 TTL video input port

- 24-bit multi-format video input port

### 3.7 Dual input video capture ports

- Flexible PIP (PAP, PBP, POP) support capability (video, graphics) between any 2 input ports
- Input Format Detection & video processing

### 3.8 Audio input and output system

- 8-CH HBR audio source from DP or HDMI receivers
- SPDIF & I2S Rx ports: max input sampling rate 192 KHz
- Analog audio line In for HP, line-out bypass
- 24 b audio DAC with mute ramp @ 44.1 KHz, 48 KHz, stereo line out/headphone out
- SPDIF Tx port: output sampling rate 192 KHz, HD audio
- Quad stereo I2S Tx port: output sampling rate 192 KHz

### 3.9 3D monitor support

- Comprehensive 3D input format decode from HDMI1.4, DP1.2 or dual DVI sources up to 120 Hz inputs
- Enhanced overdrive with temperature compensation
- 3D Frame Rate Conversion and formatting for 120 Hz frame
- Sequential or line interleaved panels
- Shutter glass on-off timing control signal
- Scanning backlight PWM control to reduce crosstalk

### 3.10 Active video window detection and enhancement

- Robust detection works with complex background condition
- Applies enhancer, sharpness, ACC3, ACM3D inside detected window

### 3.11 Video image processing

- Dual path input video processing
- Dual path vertical and horizontal downscale or upscale
- High quality linear sharpness control via peaking filter
- Support non-linear scaling for aspect ratio conversion
- Support spatial de-interlacing through vertical filter
- Maximum input resolution: 4096 x 2160
- Maximum scaled output resolution: 2560 x 2160
- Maximum bypass resolution: 4096 x 2160

### 3.12 Faroudja technology for image quality

- DCDi
- Frame/field-based motion detection and pixel-based Motion Detection for Adaptive De-Interlacing (MADI)
- Film mode detection
- Non-linear video enhancer

### 3.13 Output video processing

- Main, PIP & OSD blender with multi-PIP support
- Independent 6-Axis color control engine
- Quick-Match2 enhanced dual gamma Look Up Table
- RGB uniformity compensation
- LCD overdrive with temperature compensation and 3D display enhancement
- Left-Right dual-drive panel format support
- Enhanced line interleaved and frame sequential 3D panel interface support

### 3.14 DDR memory controller

- Support DDR2 and DDR3 memory interface
- Supports 16/32-bit memory I/F 1x16, 2x16, 1x32
- DDR max frequency 533 MHz for DDR data speed 1066 bps compatible devices

### 3.15 Output ports

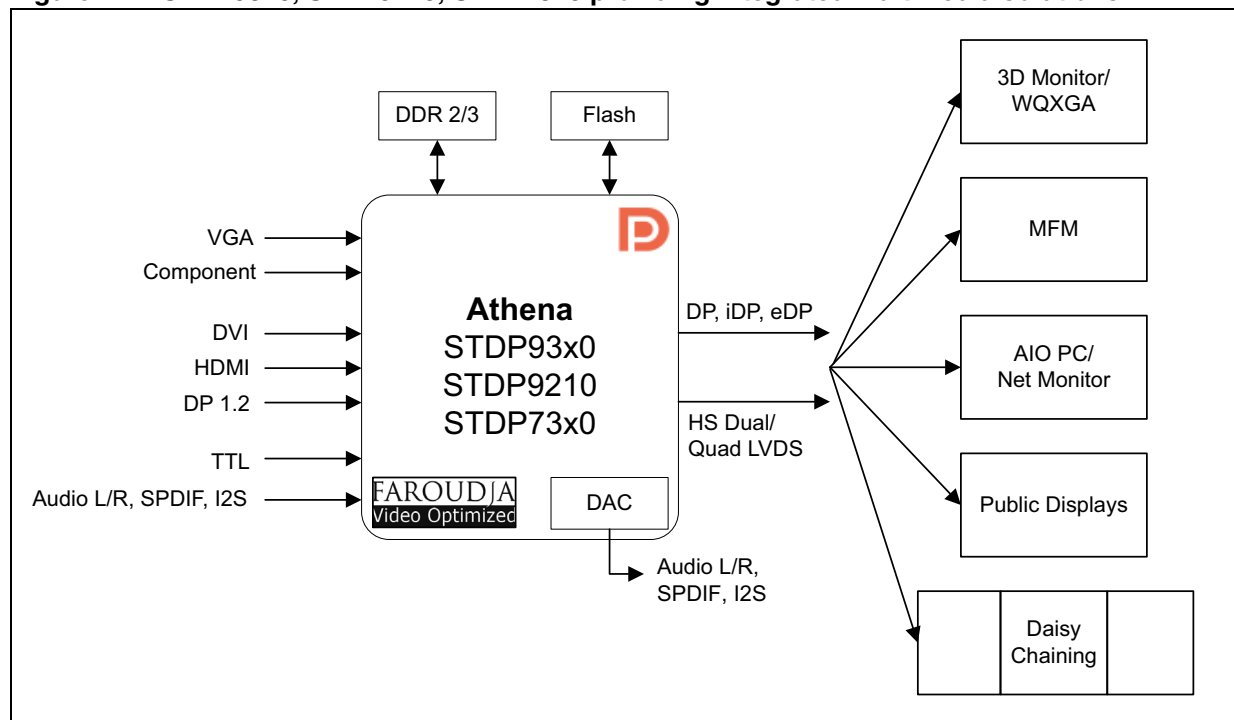
- Quad/dual channel LVDS transmitter
- DisplayPort 1.2, 5.4 GHz transmitter with multi-stream capability for daisy-chaining monitors
- Support eDP1.2 for notebook monitor
- Simultaneous output on LVDS & DPTx
- Bypass mode to bypass video from capture source to output port

### 3.16 On-chip microprocessor and OSD controller

- Integrated 150 MHz x186-turbo microprocessor with rich function library
- Advanced bit-mapped OSD controller with 3D support
- Integrated UART, DDC2BI
- General Purpose Inputs/Outputs (GPIOs)

## 4 Application overview

Figure 1. STDP93x0, STDP9210, STDP73x0 providing integrated multimedia solutions



## 5 Ordering information

**Table 2. Order codes**

Part number	Description
STDP9320-BB	521-ball HSBGA
STDP9310-BB	521-ball LFBGA
STDP9210-BB	521-ball LFBGA
STDP7320-BB	361-ball LFBGA
STDP7310-BB	361-ball LFBGA

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## 6 Revision history

**Table 3. Document revision history**

Date	Revision	Changes
10-Mar-2011	1	Initial release.
10-Nov-2011	2	Updated Features, Descriptions, and Main features sections. Removed Benefits section (content was already covered in Features section). Updated Table 2, Athena selection table.
17-Sep-2012	3	Updated for silicon rev. BB: Athena Block diagram MyDP content added in Section 1, Description and Section 2, Main features Table 1 and Table 2, Athena part numbers updated Section 3.14, DDR memory controller Section 3.16, On-chip microprocessor and OSD controller

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