

**N-CHANNEL 200V - 0.10Ω - 18A TO-220/TO-220FP/DPAK  
LOW GATE CHARGE STripFET™ II MOSFET**
**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>d</sub>	P <sub>TOT</sub>
STD20N20	200 V	< 0.125 Ω	18 A	90 W
STF20N20	200 V	< 0.125 Ω	18 A	25 W
STP20N20	200 V	< 0.125 Ω	18 A	90 W

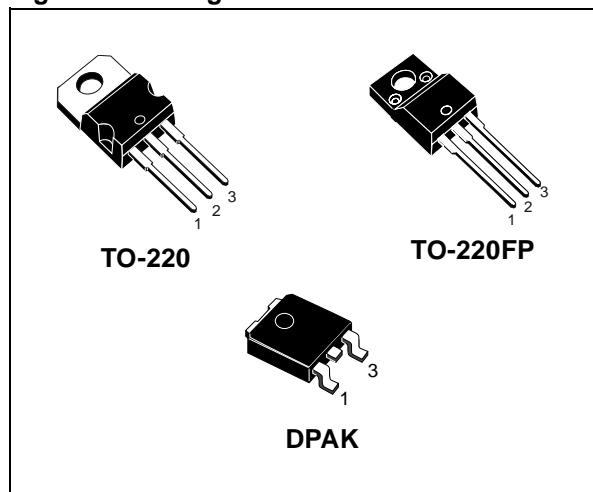
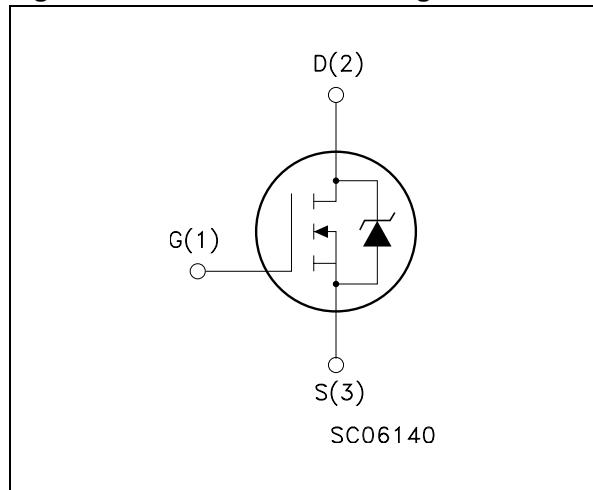
- TYPICAL R<sub>DS(on)</sub> = 0.10 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- LOW GATE CHARGE
- 100% AVALANCHE TESTED

**DESCRIPTION**

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

**APPLICATIONS**

- HIGH CURRENT SWITCHING APPLICATIONS
- HIGH EFFICIENCY DC-DC CONVERTERS
- PRIMARY SIDE SWITCH

**Figure 1: Package**

**Figure 2: Internal Schematic Diagram**

**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD20N20T4	D20N20	DPAK	TAPE & REEL
STF20N20	F20N20	TO-220FP	TUBE
STP20N20	P20N20	TO-220	TUBE

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220/DPAK	TO-220FP	
V <sub>DS</sub>	Drain-source Voltage ( $V_{GS} = 0$ )	200		V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	200		V
V <sub>GS</sub>	Gate- source Voltage	$\pm 20$		V
I <sub>D</sub>	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	18		A
I <sub>D</sub>	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	11		A
I <sub>DM</sub> (•)	Drain Current (pulsed)	72		A
P <sub>TOT</sub>	Total Dissipation at $T_C = 25^\circ\text{C}$	90	25	W
	Derating Factor	0.72	0.2	W/ $^\circ\text{C}$
dv/dt(1)	Peak Diode Recovery voltage slope	15		V/ns
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-50 to 150		$^\circ\text{C}$

(•) Pulse width limited by safe operating area

(1)  $I_{SD} \leq 18\text{A}$ ,  $dI/dt \leq 400\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(\text{BR})\text{DSS}}$ 
**Table 4: Thermal Data**

		TO-220	DPAK	TO-220FP	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	1.38	1.38	5	$^\circ\text{C/W}$
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5	50(#)	62.5	$^\circ\text{C/W}$
T <sub>I</sub>	Maximum Lead Temperature For Soldering Purpose	300			$^\circ\text{C}$

(#) When mounted on 1inch<sup>2</sup> FR-4, 2 Oz copper board.
**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	18	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	110	mJ

## ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> =25°C UNLESS OTHERWISE SPECIFIED)

**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	200			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
I <sub>GSS</sub>	Gate-body Leakage Current ( $V_{DS} = 0$ )	V <sub>GS</sub> = $\pm 20\text{V}$			$\pm 100$	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 $\mu\text{A}$	2	3	4	V
R <sub>DSS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 10 A		0.10	0.125	$\Omega$

**ELECTRICAL CHARACTERISTICS (CONTINUED)****Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ (1)	Forward Transconductance	$V_{DS} = 25 \text{ V}$ , $I_D = 10 \text{ A}$		13		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$		940 197 30		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 100 \text{ V}$ , $I_D = 10 \text{ A}$ , $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$ (see Figure 17)		15 30 40 10		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 160 \text{ V}$ , $I_D = 20 \text{ A}$ , $V_{GS} = 10 \text{ V}$ (see Figure 20)		28 5.6 14.5	39	nC nC nC

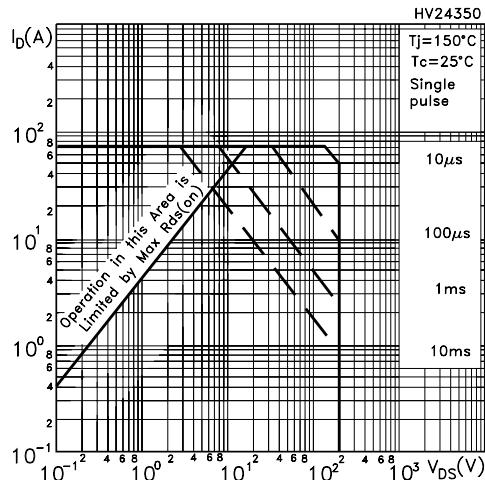
**Table 8: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (2)	Source-drain Current Source-drain Current (pulsed)				18 72	A A
$V_{SD}$ (1)	Forward On Voltage	$I_{SD} = 20 \text{ A}$ , $V_{GS} = 0$			1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 50 \text{ V}$ , $T_j = 25^\circ\text{C}$ (see Figure 18)		155 775 10		ns nC A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 50 \text{ V}$ , $T_j = 150^\circ\text{C}$ (see Figure 18)		183 1061 11.6		ns nC A

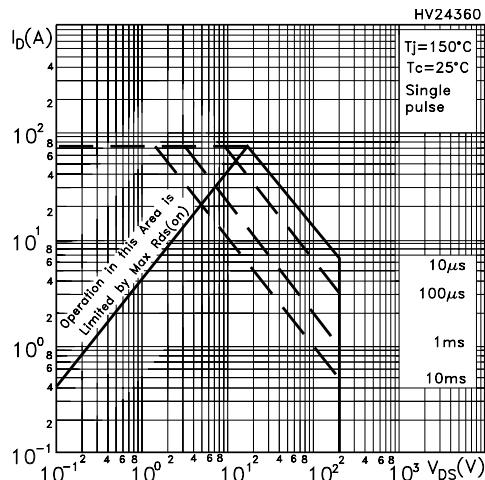
(1) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

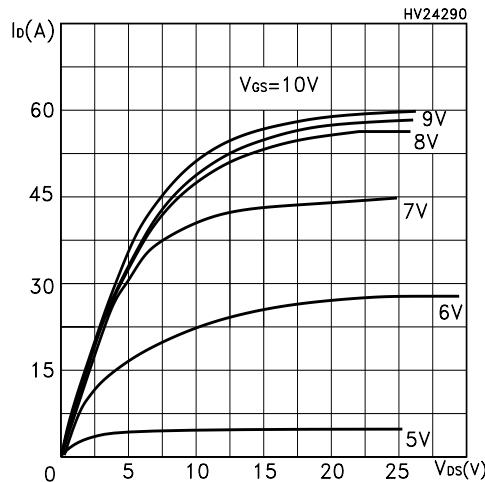
**Figure 3: Safe Operating Area For TO-220/DPAK**



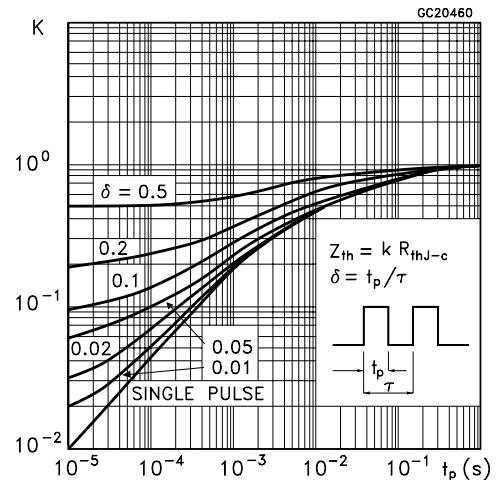
**Figure 4: Safe Operating Area For TO-220FP**



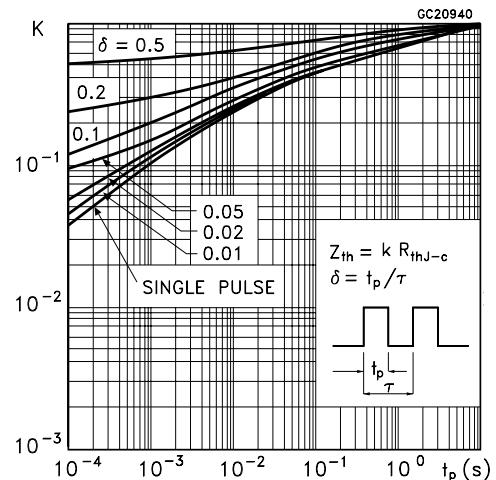
**Figure 5: Output Characteristics**



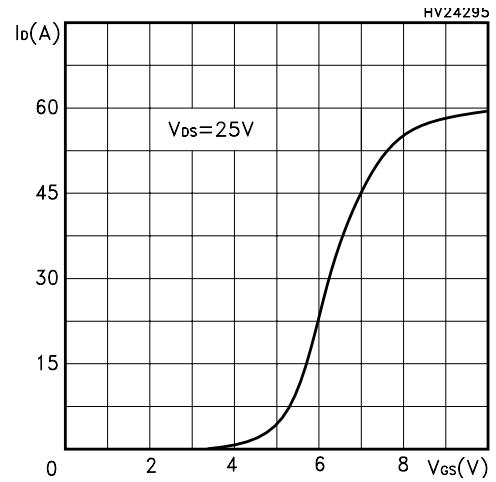
**Figure 6: Thermal Impedance For TO-220/DPAK**

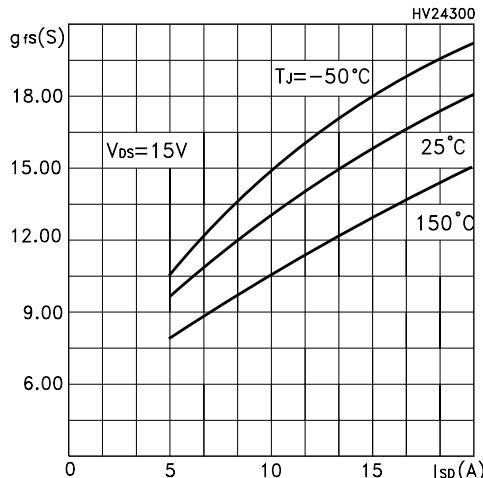
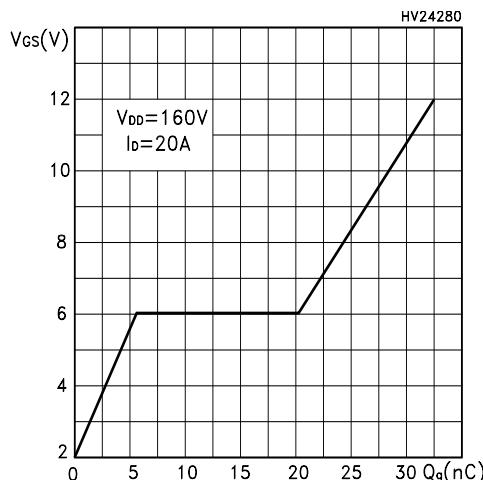
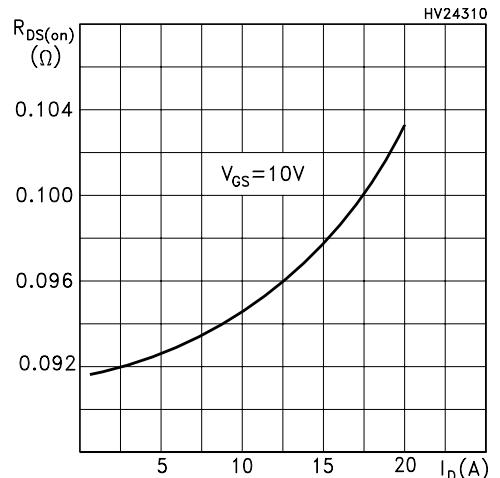
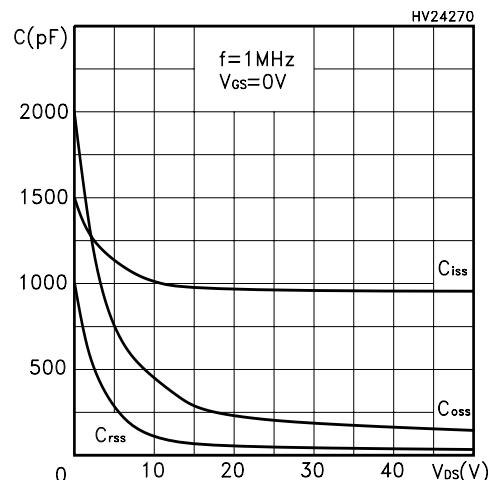
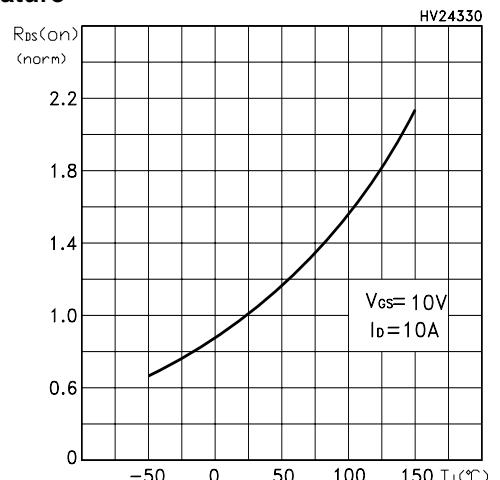
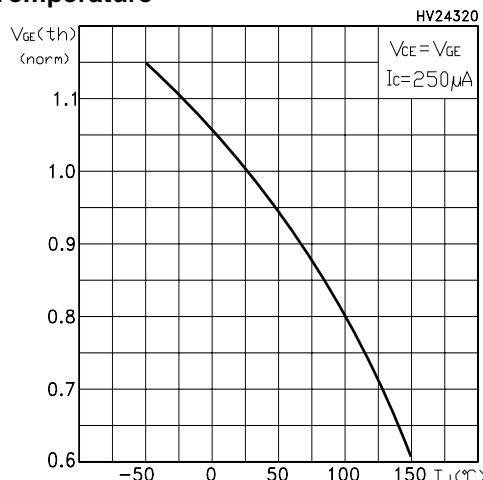


**Figure 7: Thermal Impedance For TO-220FP**

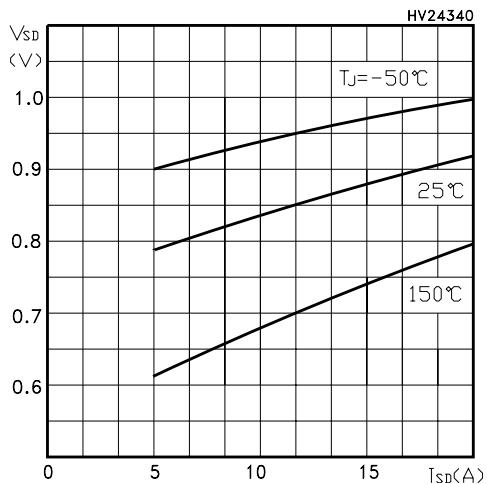


**Figure 8: Transfer Characteristics**

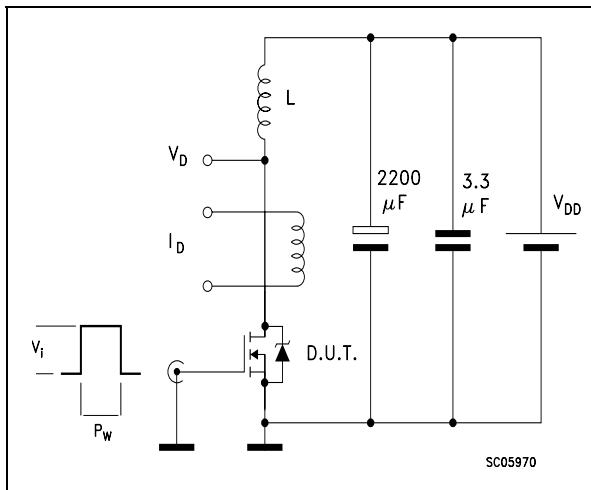


**Figure 9: Transconductance****Figure 10: Gate Charge vs Gate-source Voltage****Figure 11: Normalized Gate Threshold Voltage vs Temperature****Figure 12: Static Drain-source On Resistance****Figure 13: Capacitance Variations****Figure 14: Normalized On Resistance vs Temperature**

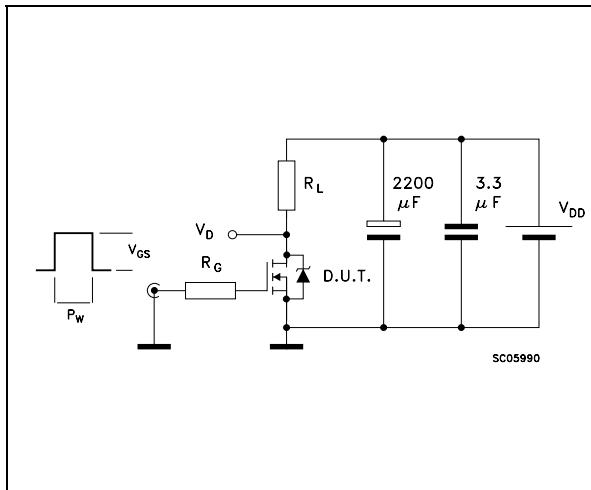
**Figure 15: Source-Drain Forward Characteristics**



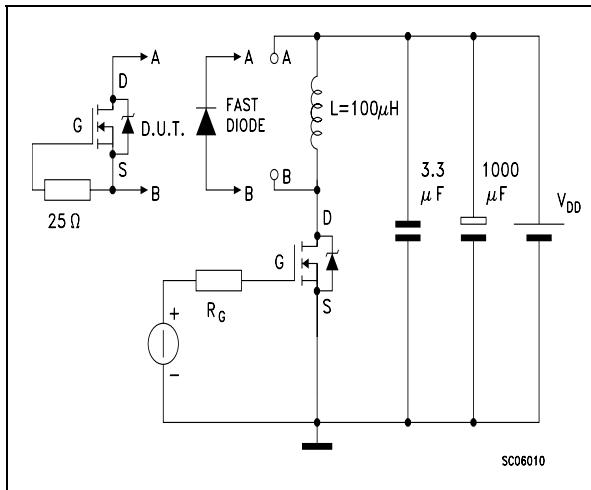
**Figure 16: Unclamped Inductive Load Test Circuit**



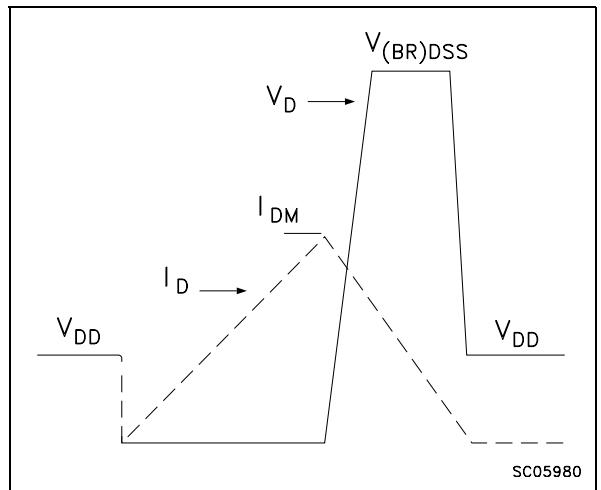
**Figure 17: Switching Times Test Circuit For Resistive Load**



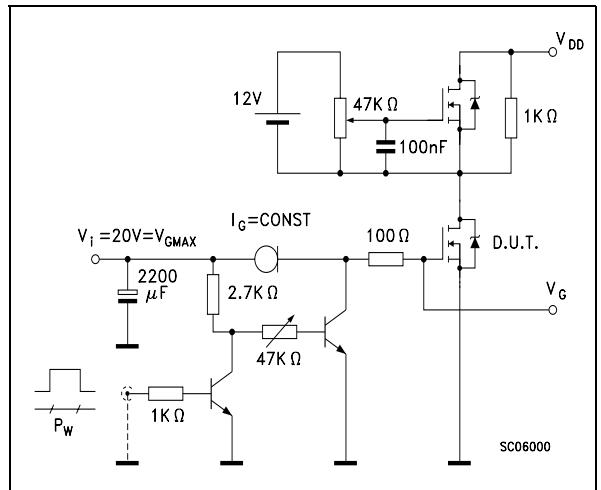
**Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times**



**Figure 19: Unclamped Inductive Wafeform**

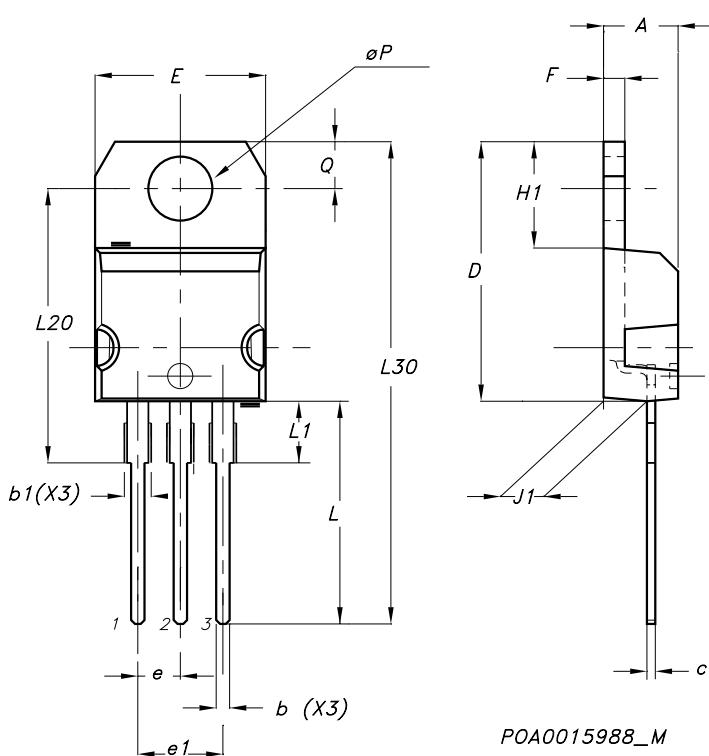


**Figure 20: Gate Charge Test Circuit**



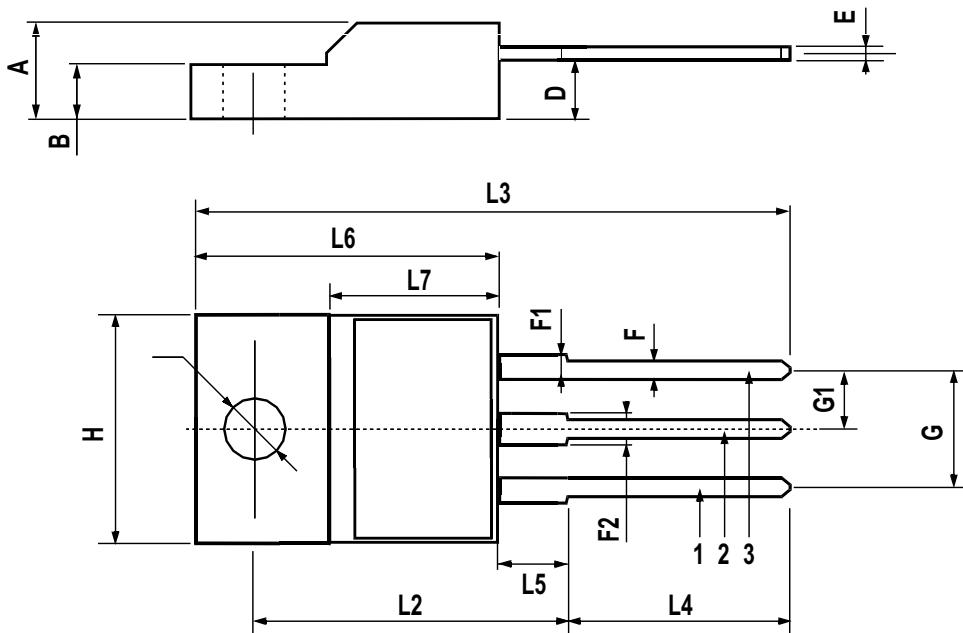
## TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
$\phi P$	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



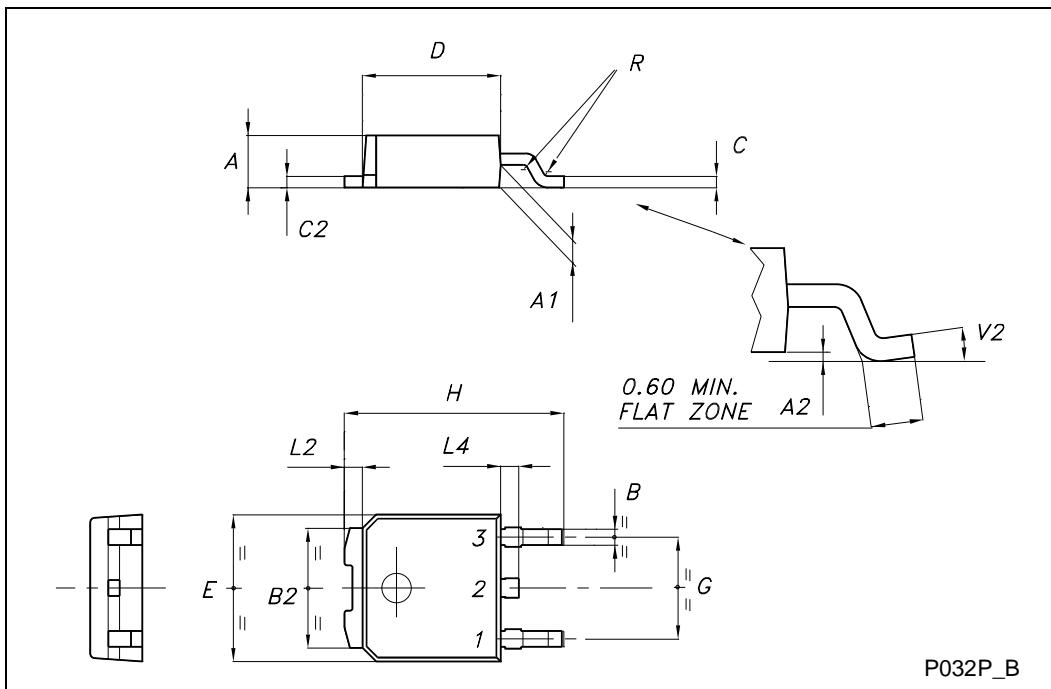
## TO-220FP MECHANICAL DATA

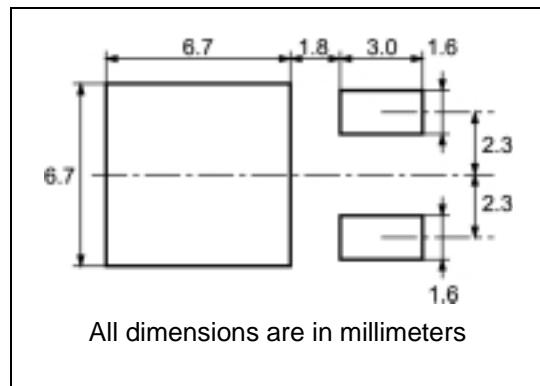
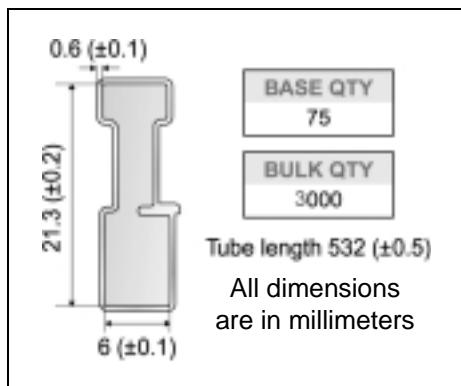
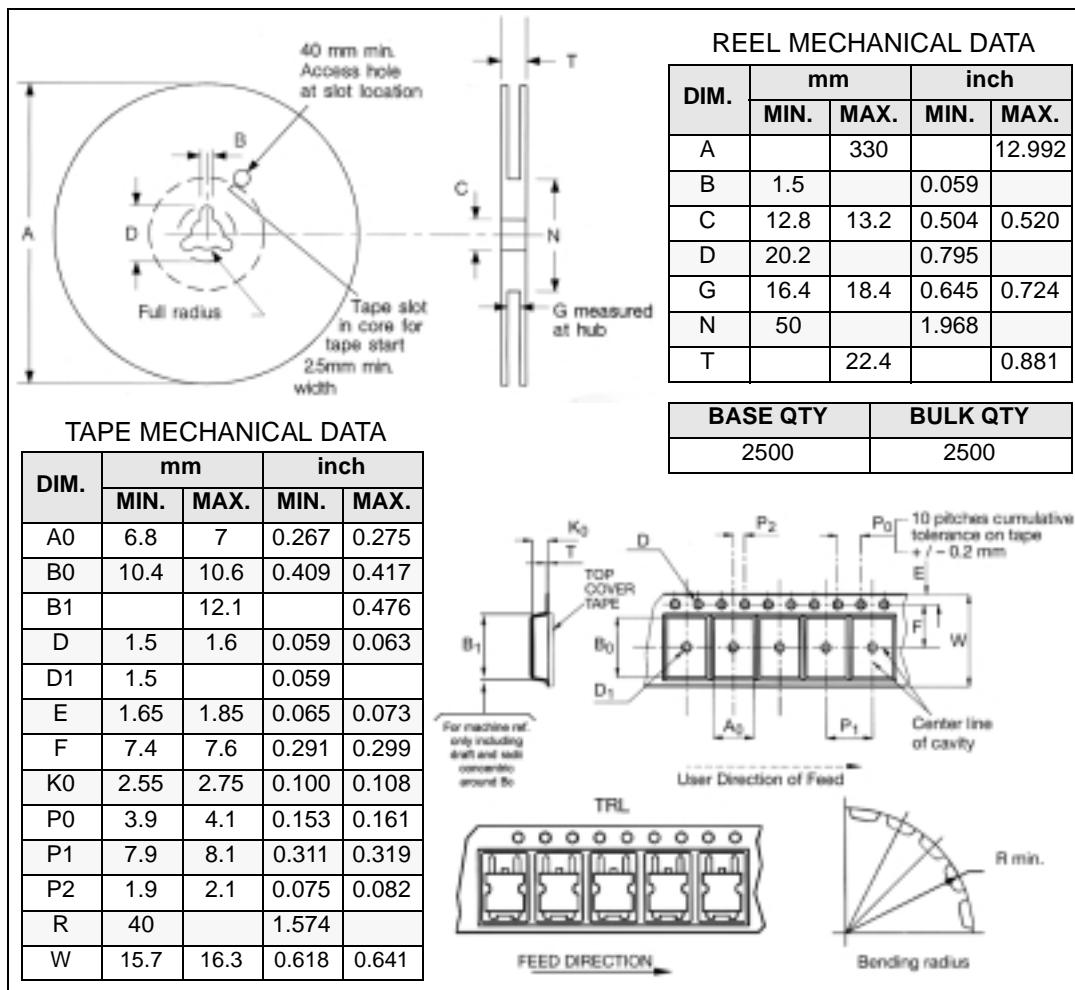
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



## TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



**DPAK FOOTPRINT****TUBE SHIPMENT (no suffix)\*****TAPE AND REEL SHIPMENT (suffix "T4")\***

\* on sales type

**Table 9: Revision History**

Date	Revision	Description of Changes
06-Dec-2004	1	Data Brief
07-Dec-2004	2	First Revision
12-Jan-2005	3	Final datasheet

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