

## Automotive-grade N-channel 500 V, 0.336 $\Omega$ typ., 10 A MDmesh™ M2 Power MOSFET in a DPAK package

Datasheet - production data

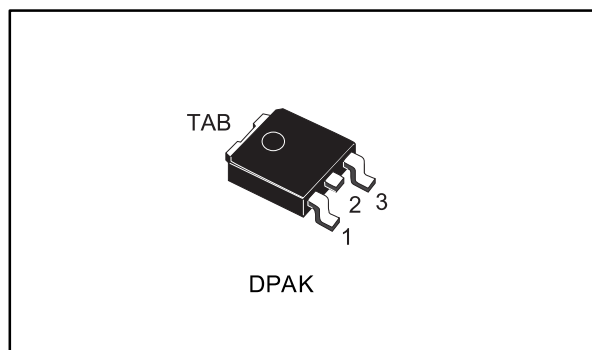
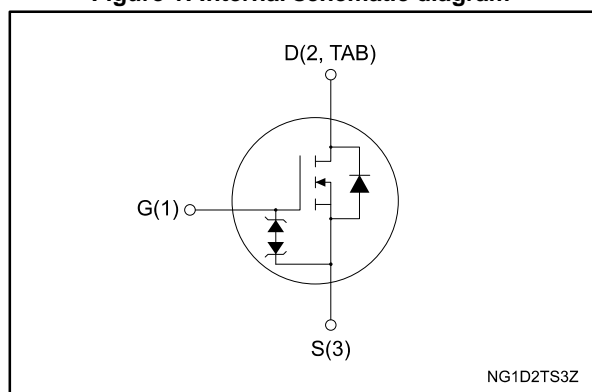


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD15N50M2AG	500 V	0.380 $\Omega$	10 A	85 W

- Designed for automotive applications and AEC-Q101 qualified
- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD15N50M2AG	15N50M2	DPAK	Tape and reel

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	10	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	7	
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	25	
$T_{stg}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

(1) Pulse width is limited by safe operating area.

(2)  $I_{SD} \leq 10\text{ A}$ ,  $di/dt = 800\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

(3)  $V_{DS} \leq 400\text{ V}$ .

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1.47	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	50	

**Notes:**

(1) When mounted on a 1 inch<sup>2</sup> FR-4, 2 Oz copper board

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	3.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	200	mJ

**Notes:**

(1) pulse width limited by  $T_{jmax}$

(2) starting  $T_j = 25\text{ }^{\circ}\text{C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	500			V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 500 V			1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 500 V, T <sub>case</sub> = 125 °C			100	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±5	μA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5 A		0.336	0.380	Ω

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	530	-	pF
C <sub>oss</sub>	Output capacitance		-	33	-	
C <sub>rss</sub>	Reverse transfer capacitance		-	0.8	-	
C <sub>oss eq. (1)</sub>	Equivalent output capacitance	V <sub>DS</sub> = 0 to 400 V, V <sub>GS</sub> = 0 V	-	125	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz, I <sub>D</sub> = 0 A	-	6.9	-	Ω
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 400 V, I <sub>D</sub> = 9 A, V <sub>GS</sub> = 10 V (see <a href="#">Figure 15: "Test circuit for gate charge behavior"</a> )	-	13	-	nC
Q <sub>gs</sub>	Gate-source charge		-	2.8	-	
Q <sub>gd</sub>	Gate-drain charge		-	5.1	-	

**Notes:**

(1) C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 4.5 A R <sub>G</sub> = 4.7 Ω, V <sub>GS</sub> = 10 V (see <a href="#">Figure 14: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	10	-	ns
t <sub>r</sub>	Rise time		-	3.2	-	
t <sub>d(off)</sub>	Turn-off delay time		-	84	-	
t <sub>f</sub>	Fall time		-	8.8	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 10\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	230		ns
$Q_{rr}$	Reverse recovery charge		-	2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17.4		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> : "Test circuit for inductive load switching and diode recovery times")	-	310		ns
$Q_{rr}$	Reverse recovery charge		-	2.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17.5		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250\text{ }\mu\text{A}$ , $I_D = 0\text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

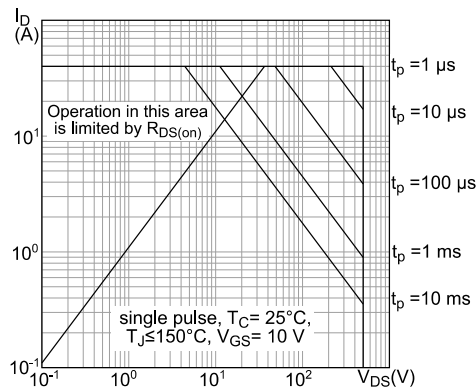


Figure 3: Thermal impedance

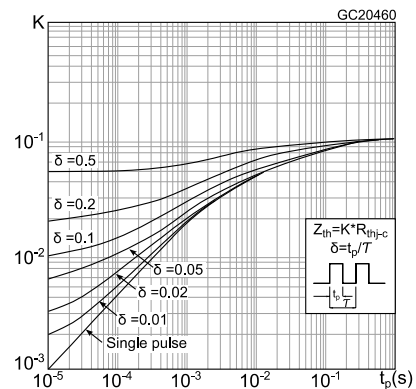


Figure 4: Output characteristics

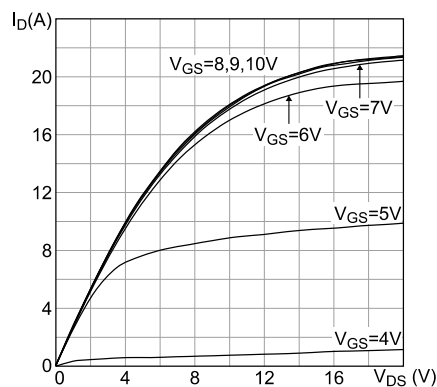


Figure 5: Transfer characteristics

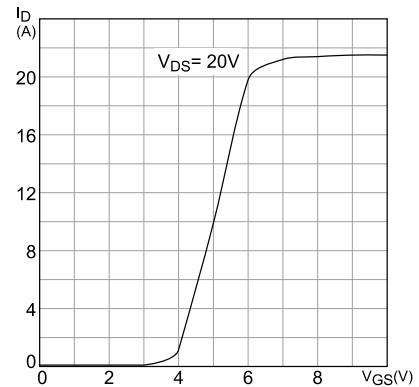


Figure 6: Gate charge vs gate-source voltage

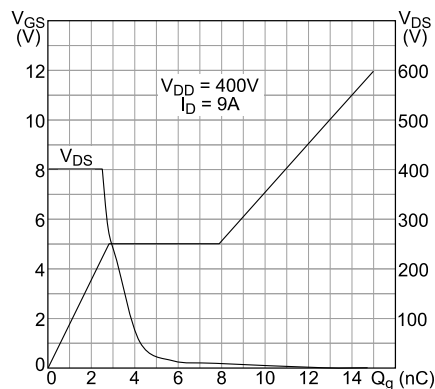


Figure 7: Static drain-source on-resistance

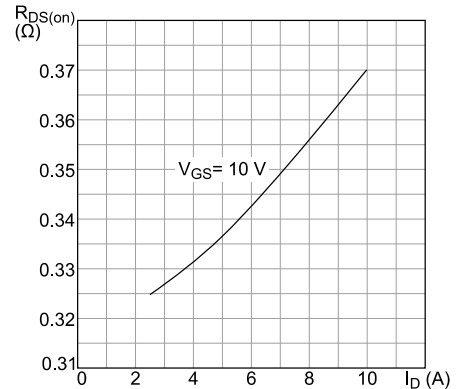


Figure 8: Capacitance variations

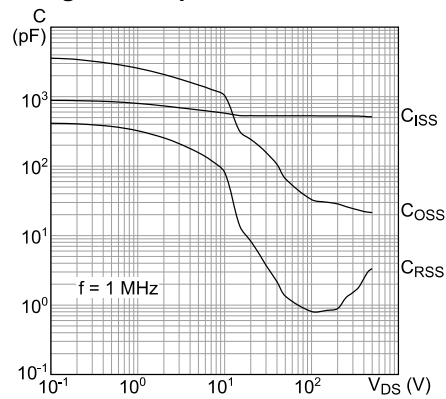


Figure 9: Normalized gate threshold voltage vs temperature

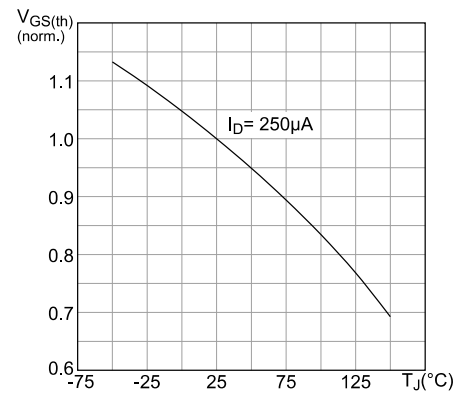


Figure 10: Normalized on-resistance vs temperature

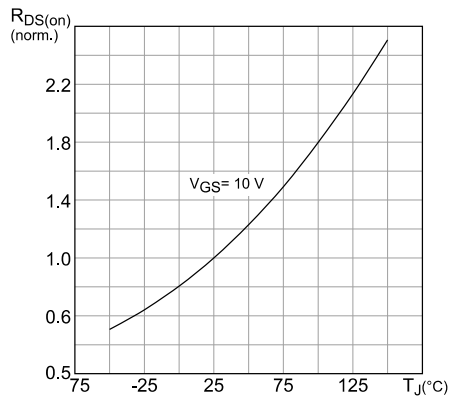


Figure 11: Normalized V(BR)DSS vs temperature

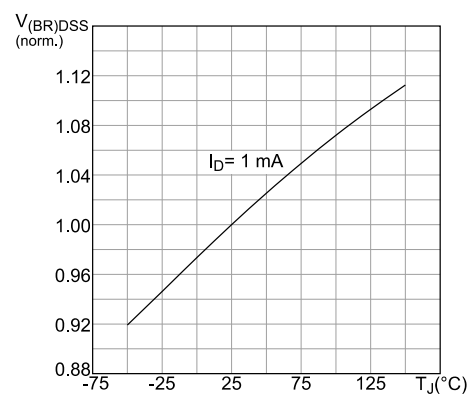


Figure 12: Output capacitance stored energy

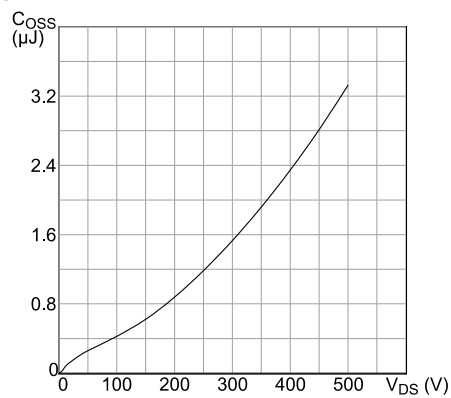
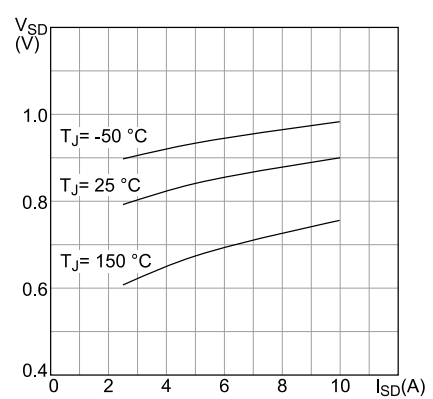
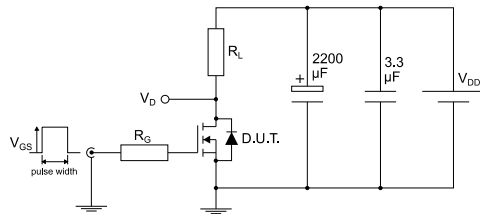


Figure 13: Source-drain diode forward characteristics



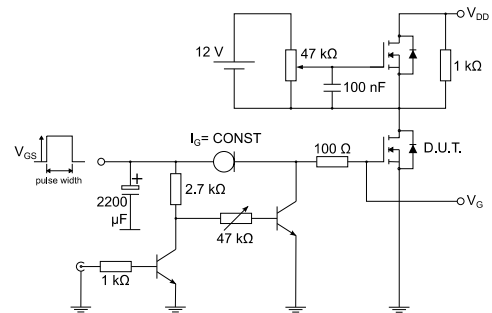
### 3 Test circuits

**Figure 14: Test circuit for resistive load switching times**



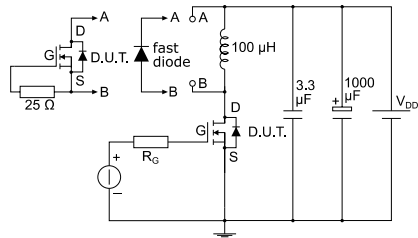
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**Figure 15: Test circuit for gate charge behavior**



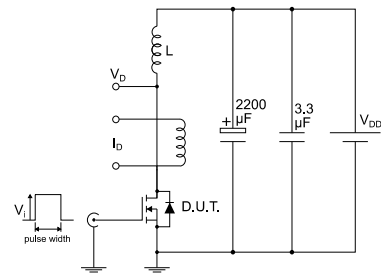
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**Figure 16: Test circuit for inductive load switching and diode recovery times**



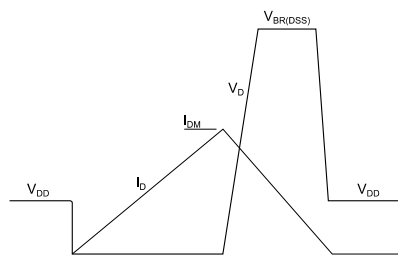
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**Figure 17: Unclamped inductive load test circuit**



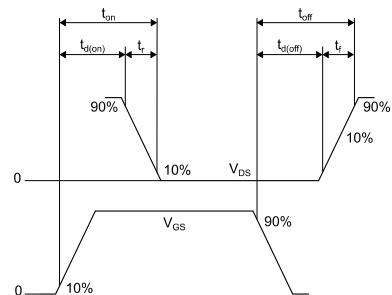
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**Figure 18: Unclamped inductive waveform**



AM01472v1

**Figure 19: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **[www.st.com](http://www.st.com)**.  
ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

Figure 20: DPAK (TO-252) type A2 package outline

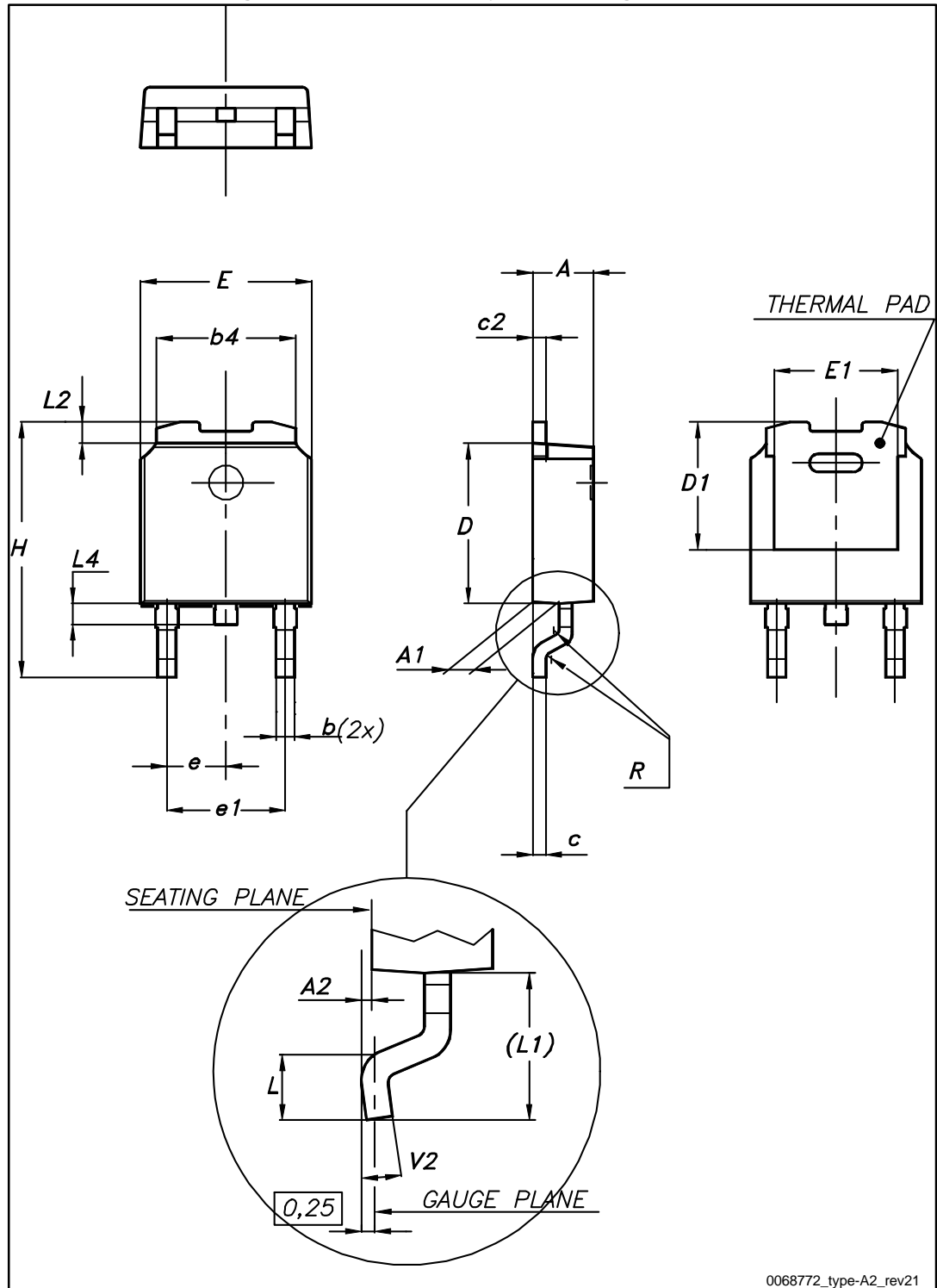
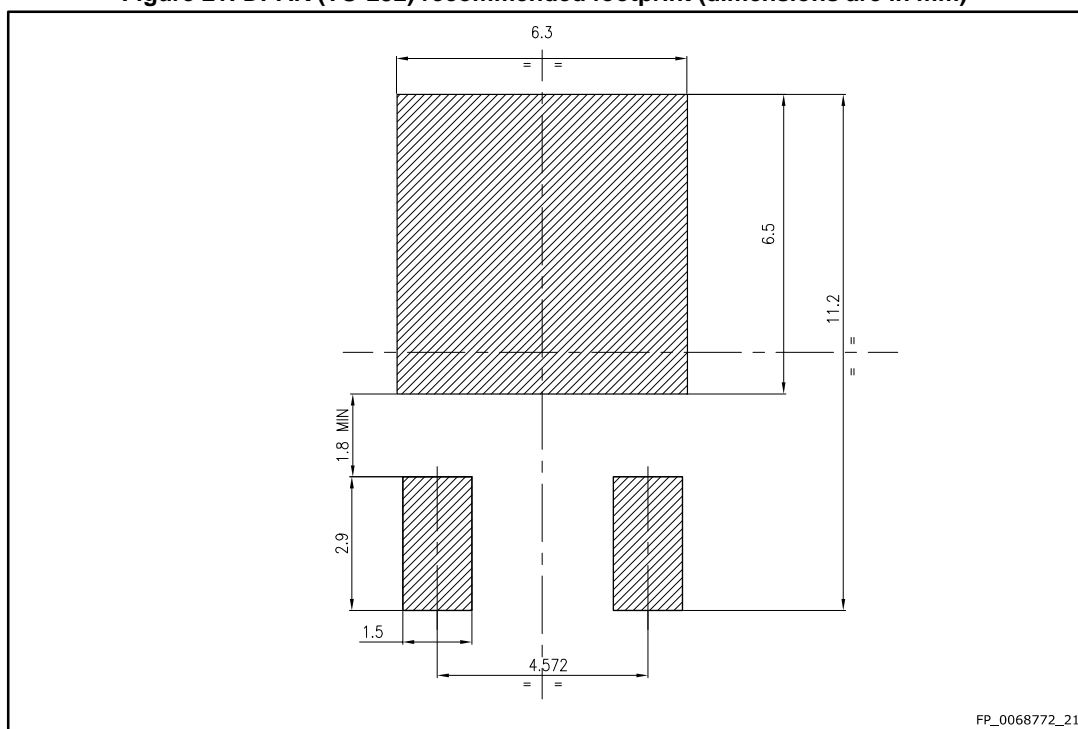


Table 10: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



## 4.2 DPAK (TO-252) packing information

Figure 22: DPAK (TO-252) tape outline

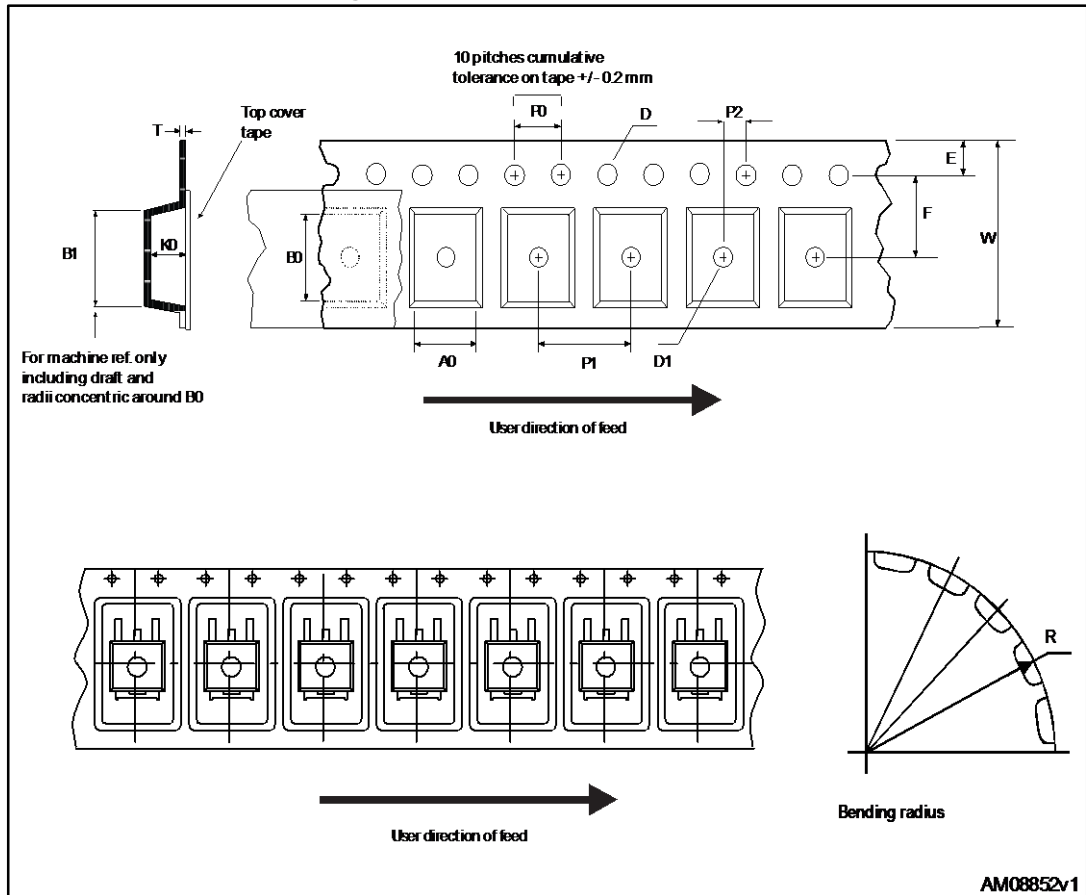


Figure 23: DPAK (TO-252) reel outline

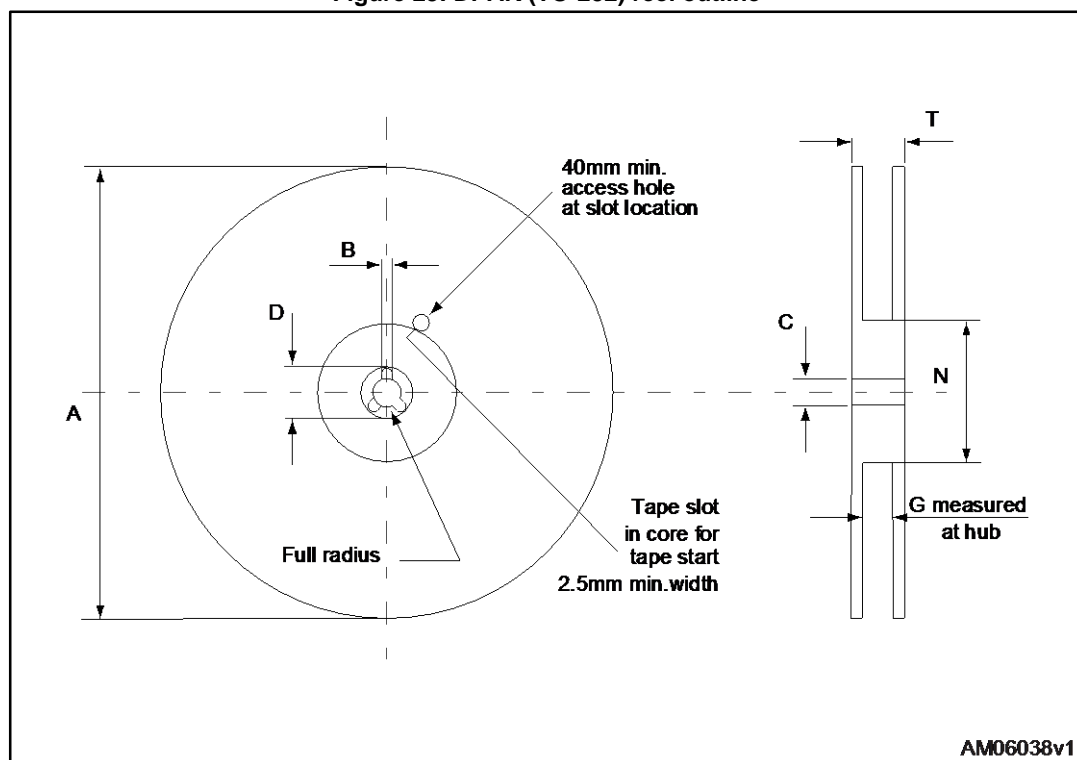


Table 11: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

Table 12: Document revision history

Date	Revision	Changes
13-Apr-2015	1	First release.
07-May-2016	2	Minor text edits Document status promoted to production data Updated <a href="#">Section 1: "Electrical ratings"</a> Updated <a href="#">Section 2: "Electrical characteristics"</a> Updated <a href="#">Section 2.1: "Electrical characteristics (curves)"</a> Updated <a href="#">Section 4.1: "DPAK (TO-252) type A2 package information"</a>

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