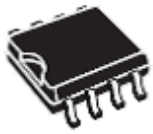
STCH02

Offline PWM controller for ultra-low standby adapters

Datasheet - preliminary data



SO-8

Features

- Advanced power management for ultra-low standby power consumptions (under 10 mW at 230 Vac)
- Fully integrated primary side constant current output regulation (CC)
- 650 V embedded HV start-up circuit with zero power consumption.
- Quasi resonant (QR) zero voltage switching (ZVS) operation
- Automatic self-supply
- Accurate and adjustable output OVP with autorestart after fault
- Input voltage feedforward compensation for mains-independent CC regulation
- Intelligent frequency jitter for EMI suppression
- SO-8 package

Applications

- AC-DC chargers for smartphones, tablets, camcorders and other handheld equipment
- AC/DC adapters for STB, notebooks and auxiliary power supplies

Description

The STCH02 is a PWM quasi resonant controller specifically designed for ultra-low standby power supplies.

The built-in HV startup cell with zero power consumption, the fully integrated blocks for primary side constant current output regulation and the advanced power management make this IC the best choice to build a high efficiency and ultra-low standby consumption power supply, with high overall and excellent dynamic performances.

Figure 1. Typical application

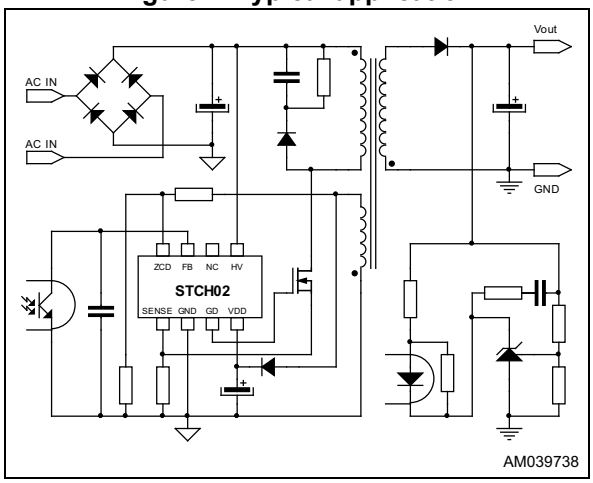


Table 1. Device summary

Order code	Package	Packing
STCH02	SO-8	Tube
STCH02TR		Tube and reel

Contents

1 Device description and block diagram

The STCH02 is a current mode controller designed for offline quasi resonant ZVS (zero voltage switching at switch turn-on) flyback converters.

It combines a high performance low voltage PWM controller chip and a 650 V HV start-up cell in the same package.

The device features a unique characteristic: it is capable to provide a constant output current (CC) regulation using primary-sensing feedback. This eliminates the need for a dedicated current reference IC, as well as the current sensor, still maintaining a quite accurate output current regulation.

The quasi resonant operation is achieved by means of a transformer demagnetization sensing input that triggers MOSFET's turn-on, connected on the ZCD pin. This input serves also to monitor the output voltage monitor and to achieve the mains independent CC regulation (line voltage feedforward).

The maximum switching frequency is top-limited below 260 kHz, so that at the medium-light-load a special function automatically lowers the operating frequency still maintaining the operation as close to ZVS as possible. At the very light-load, the device enters a controlled burst mode operation that, along with the zero power high voltage start-up circuit, the extremely low quiescent current of the device, helps minimize the residual input consumption, thus meeting the requirements of the most stringent standards.

During the CC regulation, where the flyback voltage generated by the auxiliary winding drops and may be not enough to supply the internal circuits, the chip is able to power itself directly from the rectified mains through the high voltage start-up circuit.

During the burst mode operation the self-supply feature is disabled (due to very stringent no load consumption requirement), and the V_{DD} supply voltage has to be guaranteed by proper application design.

In any case, an innovative adaptive UVLO helps minimize the issues related to the fluctuations of the self-supply voltage with the output load, due to transformer's parasitic and further reducing the IC's bias consumption.

In addition to the said functions that optimize power handling under different operating conditions, the device offers also a protection against the transformer saturation and secondary diode short-circuit and an adjustable output overvoltage protection. All of them are in the autorestart mode.

An embedded leading edge blanking on the current sense input for greater noise immunity completes the equipment of this device.

Figure 2. Block diagram

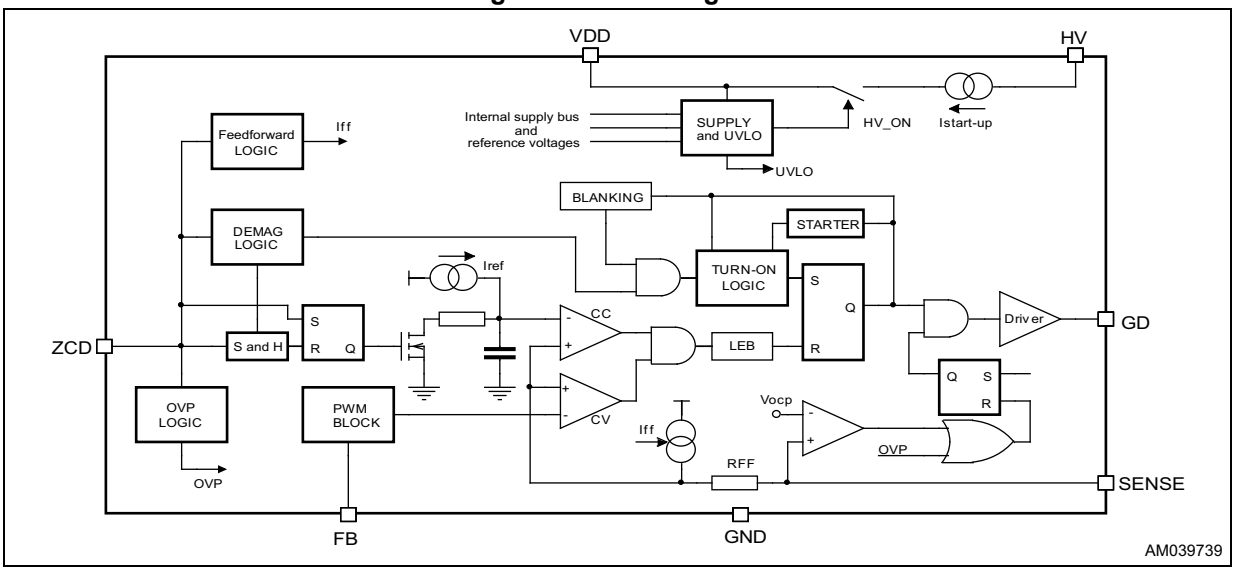


Table 2. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient	150	°C

Table 3. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HV}	1	Voltage range (referred to GND)	-0.3 to 650	V
I_{HV}	1	Output current	Self limited	mA
	3 to 6	Analog inputs and outputs	-0.3 to 3.6	V
I_{ZCD}	4	Zero current detector current	± 3	mA
I_{GD}	7	Output totem pole peak current	Self limited	
V_{DD}	8	Supply voltage (I_{CC} < 25 mA)	Self limited	V
I_{DD}	8	Device supply current + internal Zener capability	25	mA
T_J		Junction temperature range	-40 to 150	°C
T_{STG}		Storage temperature	-55 to 150	°C

Figure 3. Pin connection (top view)

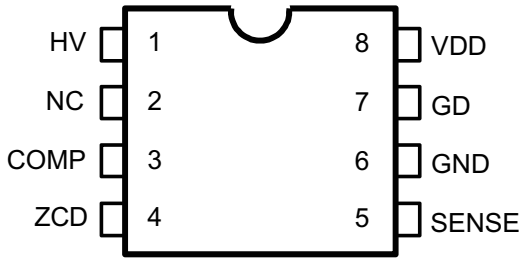


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Table 4. Pin functions

No.	Name	Function
1	HV	High voltage start-up. The pin, able to withstand 650 V, is to be tied directly to the rectified mains voltage. When the voltage on the pin reaches the HV_{START} voltage (50 V typ.) a 7 mA internal current source charges the capacitor connected between V_{DD} and GND to start-up the IC. When the voltage on the V_{DD} pin reaches the turn-on threshold (13 V typ.) the generator is shut down and re-enabled as the V_{DD} voltage falls below the turn-off threshold (10 V typ.). In this way, if the auxiliary winding is not delivering sufficient voltage or it is not used at all, the IC keeps on running. This feature is disabled in case a protection is tripped, and the generator is restarted after V_{DD} has dropped below V_{DDR} (4.5 V typ.)
2	NC	Not internally connected. A provision for clearance on the PCB to meet safety requirements.

Table 4. Pin functions (continued)

No.	Name	Function
3	FB	Control input for duty cycle control. A voltage set 65 mV below the threshold V_{FBB} activates the burst mode operation. A level close to the threshold V_{FBL} means that we are approaching the cycle-by-cycle overcurrent setpoint.
4	ZCD	Transformer's demagnetization sensing for the quasi resonant operation and input/output voltage monitor. A negative-going edge triggers the MOSFET's turn-on. The current sourced by the pin during MOSFET's ON-time is monitored to get an image of the input voltage to the converter, in order to compensate the internal delay of the current sensing circuit and achieve a CC regulation independent of the mains voltage. Still, the pin voltage is sampled-and-held right at the end of transformer's demagnetization to get an accurate image of the output voltage to be used for overvoltage protection (OVP). Please note that the maximum IZCD sunk/sourced current has to not exceed ± 3 mA (AMR) in the entire input voltage range. No capacitor is allowed between the pin and the auxiliary winding of the transformer.
5	SENSE	Input to the PWM comparators. The current flowing in the MOSFET is sensed through a resistor connected between the pin and GND. The resulting voltage is compared with an internal reference (0.75 V max.) to determine the MOSFET's turn-off. The pin is equipped with 380 ns blanking time after the gate drive output goes high for improved noise immunity. If a second comparison level located at 1 V is exceeded the IC is stopped and restarted after V_{DD} has dropped below V_{DDR} (4.5 V typ.).
6	GND	Circuit ground reference and current return for both - the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to the trace going to this pin and kept separate from any pulsed current return.
7	GD	A gate driver with a totem pole output stage for the external power MOSFET.
8	VDD	Supply voltage of the device. An electrolytic capacitor, connected between this pin and ground, is initially charged by the internal high voltage start-up generator. When the device is running the same generator will keep it charged in case the voltage supplied by the auxiliary winding is not sufficient. This feature is disabled in case a protection is tripped. Sometimes a small bypass capacitor (0.1 µF typ.) connected between the pin and GND might be useful to get a clean bias voltage for the signal part of the IC.

Table 5. Electrical characteristics
(Tj = - 25° to 125 °C, V_{DD} = 14 V, unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
High voltage start-up generator						
V_{HV}	HV voltage	I_{HV} < 2 µA, Tj = 25 °C			650	V
$I_{LEAKAGE}$	HV leakage current	V_{HV} = 400 V, Tj = 25 °C			1	µA
H_{VSTART}	HV start voltage		40	50	60	V
I_{CHARGE}	V_{DD} start-up charge current	V_{HV} > HV_{START}; V_{DD} ≤ 0.6 V or after protection tripping	0.3	0.6	0.9	mA
		V_{HV} > HV_{START}; 2 < V_{DD} < V_{DDOn}	4.5	7	10.3	
$V_{DD-FOLD}$	V_{DD} foldback threshold	V_{HV} > HV_{START}	1		2	V
Supply voltage						
V_{DD}	Operating range	After turn-on	11.5		23	V
V_{DD-ON}	Turn-on threshold		12	13	14	V
V_{DD-OFF}	Restart threshold	V_{FB} > V_{FBF}	9	10	11	V
$V_{DD-UVLO}$	UVLO threshold	V_{FB} > V_{FBF}	8.55	9.5	10.45	V
		V_{FB} < (0.6 - 65 mV)	6.75	7.5	8.25	V
V_{DDR}	V_{DD} restart voltage (falling)	After protection tripping		4.5		V
		In burst mode		3.2		
V_Z	V_Z clamping voltage	I_{DD} = 20 mA	23		26.5	V
Supply current						
I_Q	Quiescent current	Burst operation		190	230	µA
I_{DD}	Operating supply current	C_{out} = 1 nF, f_{sw} = 100 KHz		2.3	2.7	mA
$I_{DD-FAULT}$	Fault quiescent current	During hiccup		330	420	µA
Start-up timer and frequency limit						
T_{START}	Start timer period			220		µs
F_{LIM}	Internal frequency limit			260		kHz
Zero current detector						
I_{ZCDb}	Input bias current	V_{ZCD} = 0.1 to 2.7 V			1	µA
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 1 mA		3		V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 1 mA		-60		mV
V_{ZCDA}	Arming voltage	Positive-going edge	80	110	140	mV
V_{ZCDT}	Triggering voltage	Negative-going edge	40	60	80	mV
T_{BLANK}	Trigger blanking time after MOSFET's turn-on	V_{FB} ≥ 1.65 V		3.8		µs
		V_{FB} = 0.6 V		24		

Table 5. Electrical characteristics
(Tj = - 25° to 125 °C, V_{DD} = 14 V, unless otherwise specified) (continued)

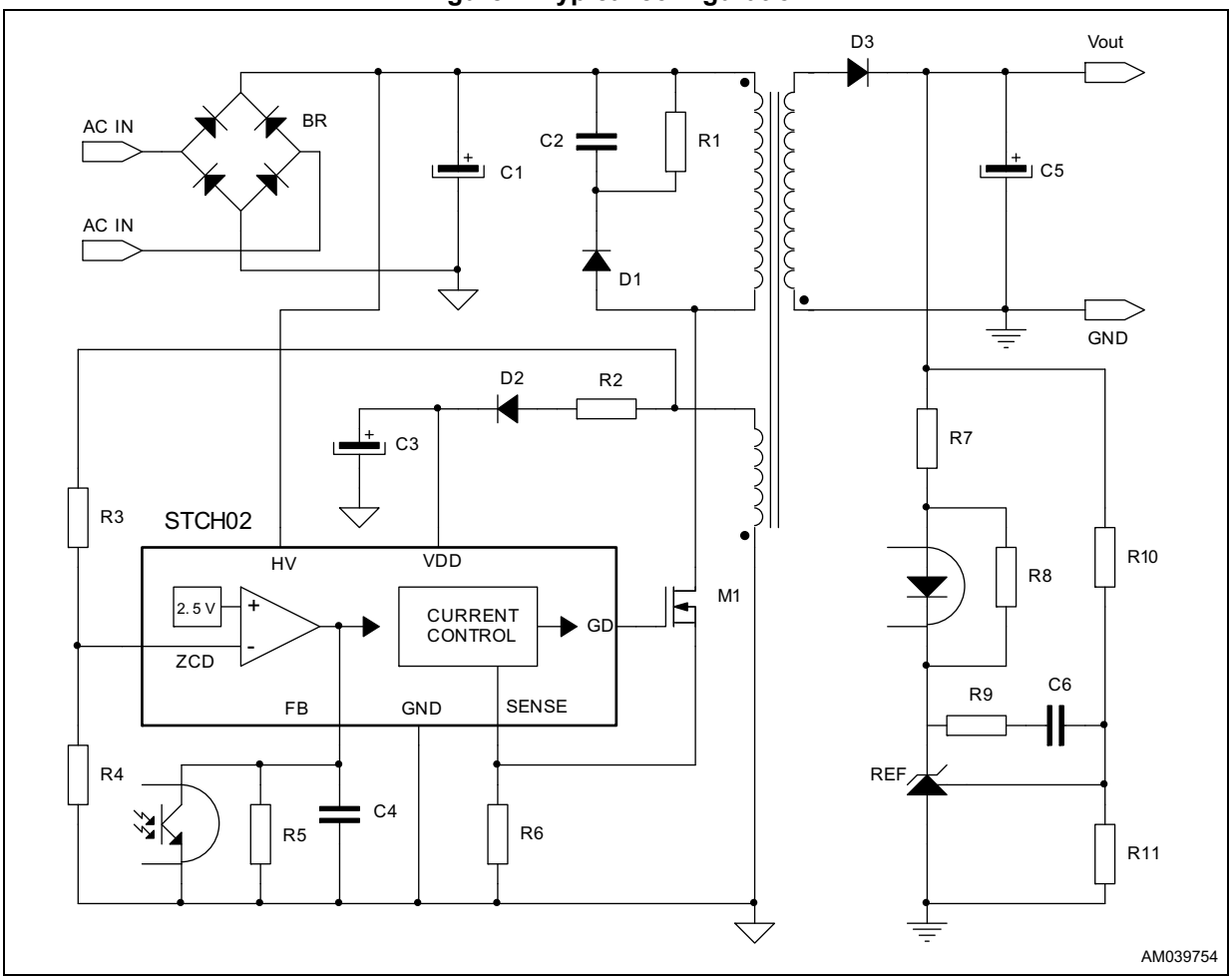
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
T_{D-ON}	Turn-on delay time after triggering	V_{GATE} = 6 V, C_{GATE} = 1 nF		270		ns
T_{FORCE}	Force turn-on time after blanking			10	14	µs
Gate driver						
V_{GDL}	Output high voltage	V_{DD} = 8.5 V; I_{GATE} = 5 mA	7			V
		I_{GATE} = 5 mA	10.5	13		
T_{RISE}	Rising time	C_{GATE} = 1 nF	70	110	150	ns
T_{FALL}	Falling time	C_{GATE} = 1 nF	20	40	60	ns
V_{GDL}	Output low voltage	$I_{GD-SINK}$ = 50 mA			1	V
Line feedforward						
R_{FF}	Equivalent feedforward resistor	I_{ZCD} = 1 mA	63	70	77	Ω
Feedback input						
V_{FBH}	Upper saturation			3.45		V
H_{FB}	Current sense gain		3.22	3.29	3.36	
I_{FB}	Feedback source current		70	100	130	µA
V_{FBB}	Burst mode threshold	Voltage falling	0.54	0.6	0.66	V
V_{FBF}	Exit burst mode threshold		0.64	0.72	0.8	V
V_{HYST}	Burst mode hysteresis		50	65	75	mV
Current reference						
V_{REFx}	Maximum value	Internal, not measured		0.8		V
K_I	Current loop gain		0.19	0.2	0.21	V
Overvoltage protection						
V_{OVP}	OVP threshold		2.375	2.5	2.625	V
N_{OVP}	Consecutive cycles for OVP triggering	V_{OVP} = 2.5 V		4		
Current sense						
T_{LEB}	Leading edge blanking	V_{GATE} = 6 V, C_{OUT} = 1 nF	270	380	490	ns
T_D	Gate delay to output	V_{GATE} = 6 V, C_{OUT} = 1 nF			150	ns
V_{CSx}	Max. clamp value	dV_{CS}/dt = 200 mV/µs	0.7	0.75	0.8	V
V_{OCP}	Hiccup mode OCP level		0.95	1	1.05	V
V_{SENSE_BM}	Minimum burst mode sense voltage			72		mV

Table 5. Electrical characteristics
(Tj = - 25° to 125 °C, V_{DD} = 14 V, unless otherwise specified) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Frequency jittering						
F_D	Modulation frequency			9		kHz
V_{ZCDH}	Modulation duty cycle			50		%
ΔIpk	Peak current change			5		%

2 Typical circuit

Figure 4. Typical configuration



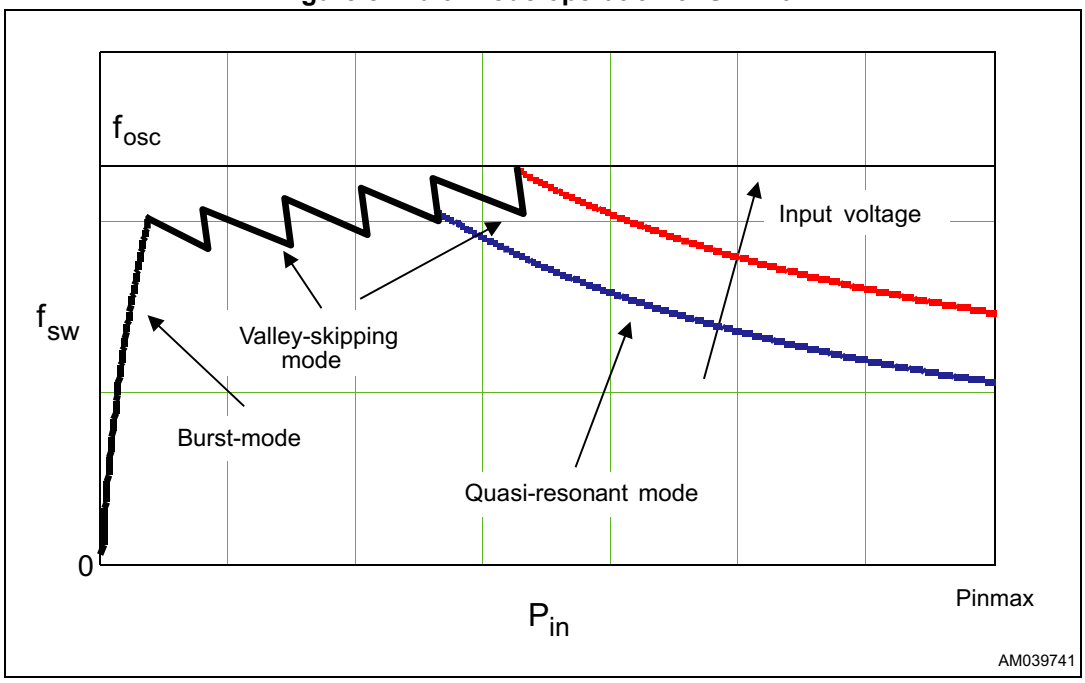
3 Application information

The STCH02 is an offline CC mode primary sensing switching controller, specific for offline quasi resonant ZVS (zero voltage switching at switch turn-on) flyback converters.

Depending on converter's load condition, the device is able to work in different modes (see *Figure 5*):

1. QR mode at the heavy load. Quasi resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency will be different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 5*). Minimum turn-on losses, low EMI emission and safe behavior in the short-circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at the medium/light-load. Depending on voltage on the FB pin, the device defines the maximum operating frequency of the converter. As the load is reduced MOSFET's turn-on will not any more occur on the first valley but on the second one, the third one and so on. In this way the switching frequency will no longer increase.
3. Burst mode with no or a very light-load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with the constant peak current. Decreasing the load will then result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 5. Multi-mode operation of STCH02



3.1 Gate driver

The gate driver of the power MOSFET is designed to supply a controlled gate current during both turn-on and turn-off in order to minimize the common mode EMI. Under UVLO conditions an internal pull-down circuit holds the gate low in order to ensure that the power MOSFET cannot be turned on accidentally.

3.2 Frequency jittering for EMI reduction

Although the STCH02 device works in the QR mode and the switching frequency is already modulated at twice of the mains frequency, dedicated frequency jittering circuitry is embedded inside the IC to further reduce the EMI filtering. A proprietary frequency jitter technique is implemented in the controller, based on the injection of a modulating signal at 9 kHz (above the feedback loop bandwidth) with 50% duty cycle on the current sense signal: this signal is a square waveform that modulates the amplitude of the peak primary current. The percentage of this amplitude is set as a default at 5%. As the peak current reduces with decreasing load levels, the effect of this modulation automatically attenuates at lower loads, where the energy of EMI noise is highly reduced.

3.3 High voltage start-up generator

Based on a 650 V rated depletion MOSFET embedded into the startup cell, the HV current generator is supplied through the DRAIN pin and is enabled only if the voltage on the HV pin is higher than the HVSTART threshold (50 V typical value).

With reference to the timing diagram in *Figure 6*, when the power is applied to the circuit and the voltage on the input bulk capacitor is high enough, the HV generator is sufficiently biased to start operating, thus it will draw the current I_{CHARGE} (7 mA typ. value) through the HV pin and will charge the capacitor connected between the V_{DD} pin and ground. This charging current will be reduced at 0.6 mA in case the voltage on the V_{DD} is lower than $V_{DD-FOLD}$, in order to prevent exceeding IC dissipation when the pin is accidentally shorted to ground or during a restart after protection triggering.

As the V_{DD} voltage reaches the start-up threshold (13 V typ.) the chip starts operating and the control logic disables the HV generator.

While the generator is off, there are virtually no losses across the HV startup cell, except a few hundreds nA of the leakage current through the depletion MOSFET.

The IC is powered by the energy stored in the V_{DD} capacitor until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation.

The chip is able to power itself directly from the rectified mains: when the voltage on the V_{DD} pin falls below V_{DD-OFF} (10 V typ.), the HV current generator is turned on and charges the supply capacitor until it reaches the V_{DD-ON} threshold.

In this way, the self-supply circuit develops a voltage high enough to sustain the operation of the device. This feature is useful especially during the CC regulation, when the flyback voltage generated by the auxiliary winding alone may not be able to keep V_{DD} within the operative range.

At converter power-down the system will the lose the regulation as soon as the input voltage falls below HV_{START}. This prevents converter's restart attempts and ensures monotonic output voltage decay at system power-down.

Figure 6. Timing diagram: normal power-up and power-down sequences

3.4 Zero current detection and triggering block

The zero current detection (ZCD) and triggering blocks switch on the power MOSFET if a negative-going edge falling below 50 mV is applied to the ZCD pin. To do so, the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is used to detect transformer demagnetization for the QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the IC.

The triggering block is blanked after the MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

This blanking time is dependent on the voltage on the FB pin: it is T_{BLANK} = 24 µs for V_{FB} = 0.6 V, and decreases linearly down to T_{BLANK} = 3.8 µs for $V_{FB} \geq$ 1.65 V.

The voltage on the pin is both top and bottom limited by a double clamp. The upper clamp is typically located at 3 V, while the lower clamp is located at -60 mV. The interface between the pin and the auxiliary winding will be a resistor divider. Its resistance ratio as well as the individual resistance values will be properly chosen (see *Section 3.10: Overvoltage protection on page 18* and *Section 3.7: Voltage feedforward block on page 16*.

Please note that the maximum IZCD sunk/sourced current has to not exceed ± 3 mA (AMR) in all the Vin range conditions (88 - 265 Vac). No capacitor is allowed between the ZCD pin and the auxiliary winding of the transformer.

The switching frequency is top-limited below 260 kHz, as the converter's operating frequency tends to increase excessively at the light-load and high input voltage.

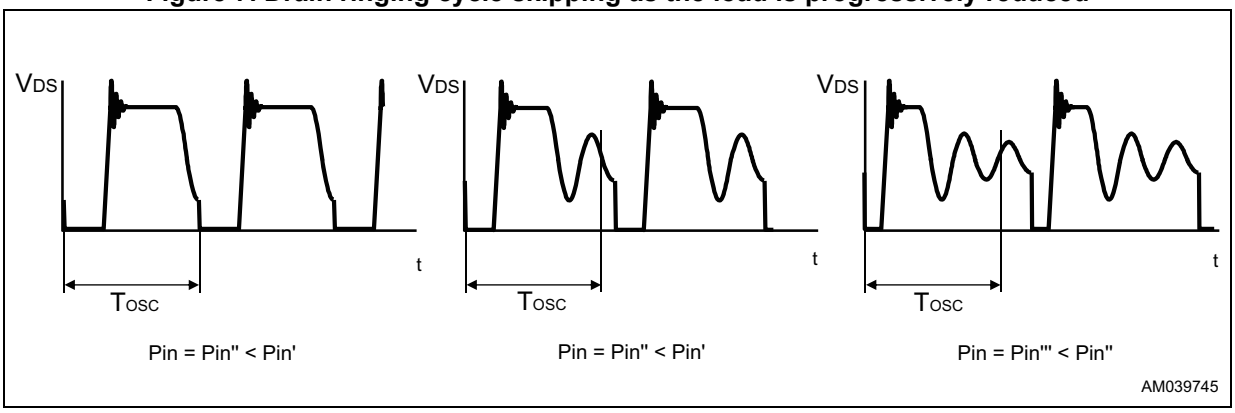
A starter block is also used to start-up the system when the signal on the ZCD pin is not high enough to trigger the MOSFET

After the first few cycles initiated by the starter, as the voltage developed across the auxiliary winding becomes large enough to arm the ZCD circuit, MOSFET's turn-on will start to be locked to transformer demagnetization, hence setting up the QR operation.

The starter is activated also when the IC is in the CC regulation and the output voltage is not high enough to allow the ZCD triggering.

If the demagnetization completes - hence a negative-going edge appears on the ZCD pin - after a time exceeding time T_{BLANK} from the previous turn-on, the MOSFET will be turned on again, with some delay to ensure minimum voltage at turn-on. If, instead, the negative-going edge appears before T_{BLANK} has elapsed, it will be ignored and only the first negative-going edge after T_{BLANK} will turn-on the MOSFET. In this way one or more drain ringing cycles will be skipped ("valley-skipping mode", *Figure 7*) and the switching frequency will be prevented from exceeding $1/T_{BLANK}$.

Figure 7. Drain ringing cycle skipping as the load is progressively reduced



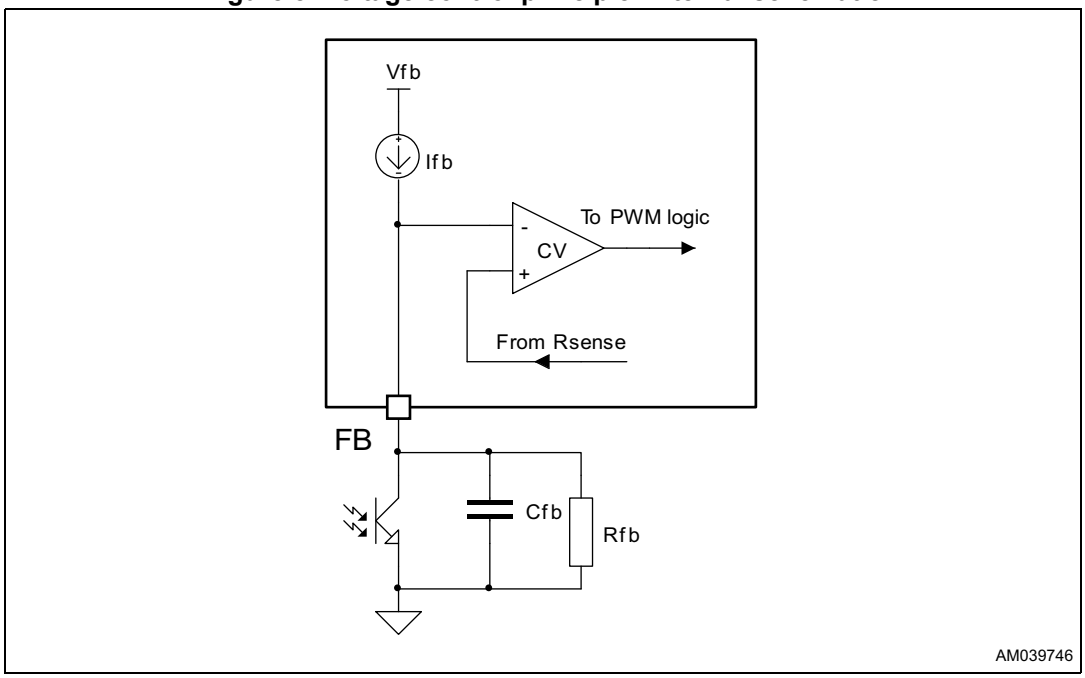
When the system operates in the valley-skipping mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

3.5 Constant voltage operation

The device is specific for secondary feedback. The FB pin is connected to an optocoupler which transmits the error signal from the regulation loop located on the secondary side of the converter. Typically, a TS431 is used as a voltage reference.

The FB pin is driven directly by the phototransistor's collector to modulate the duty cycle. The voltage coming from the FB pin is compared with the voltage across the sense resistor, controlling the peak drain current cycle-by-cycle.

Figure 8. Voltage control principle: internal schematic



3.6 Constant current operation

The voltage of the auxiliary winding is fed into the internal CC block trough the ZCD pin to achieve an output constant current regulation.

Equation 1 can be used to define to output current in CC mode.

Equation 1

$$I_{OUT} = \frac{N_{PRI}}{N_{SEC}} \cdot \frac{K_I}{2 \cdot R_{SENSE}}$$

This formula shows that the average output current does not depend anymore on the input or the output voltage, neither on transformer inductance values. The external parameters defining the output current are the transformer ratio and the sense resistor R_{SENSE}. The current loop gain K_I is internally defined (see *Table 5 on page 7*).

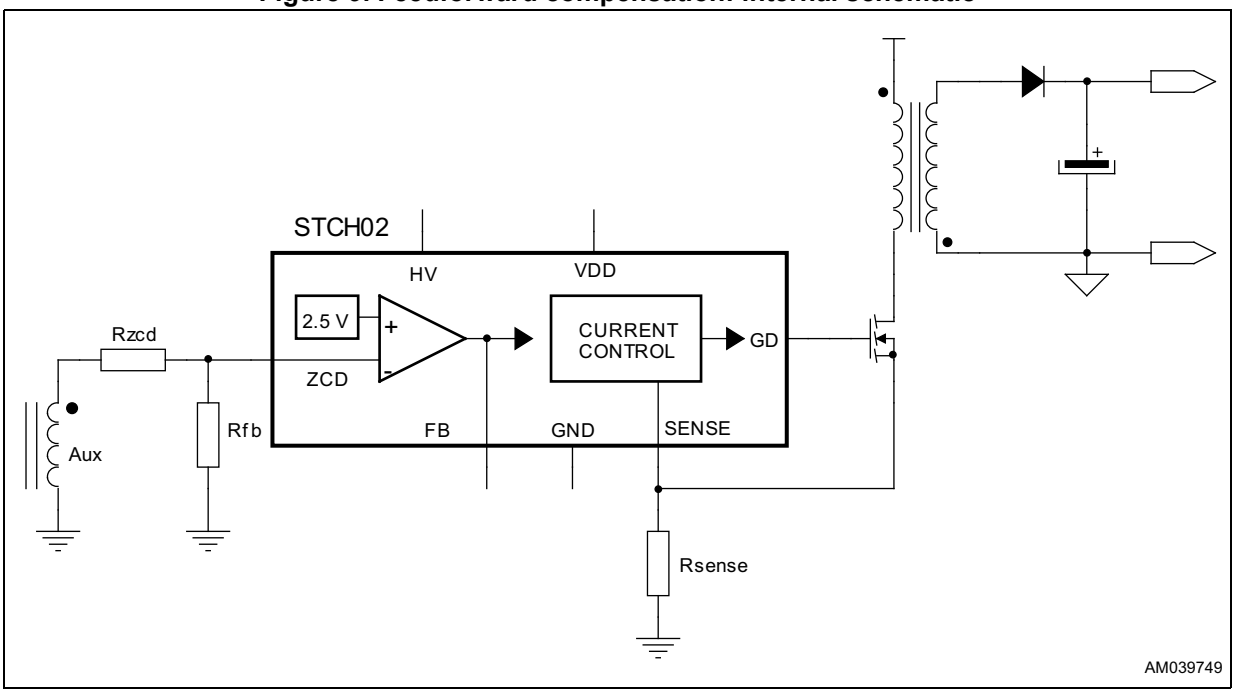
3.7 Voltage feedforward block

The current control structure uses the voltage V_C to define the output current, according to *Equation 1*. Actually, the CC comparator will be affected by an internal propagation delay Td, which will switch off the MOSFET with a peak current than higher the foreseen value.

The STCH02 device implements a line feedforward function, which solves the issue by introducing an input voltage dependent offset on the current sense signal, in order to adjust the cycle-by-cycle current limitation.

The external schematic configuration is shown in *Figure 9*.

Figure 9. Feedforward compensation: internal schematic



The R_{ZCD} resistor can be calculated as follows:

Equation 2

$$R_{ZCD} = \frac{N_{AUX}}{N_{PRI}} \cdot \frac{L_{PR} \cdot R_{FF}}{T_D \cdot R_{SENSE}}$$

where R_{FF} is an internal parameter, defined in *Table 5 on page 7*.

In this case the peak drain current does not depend on input voltage anymore.

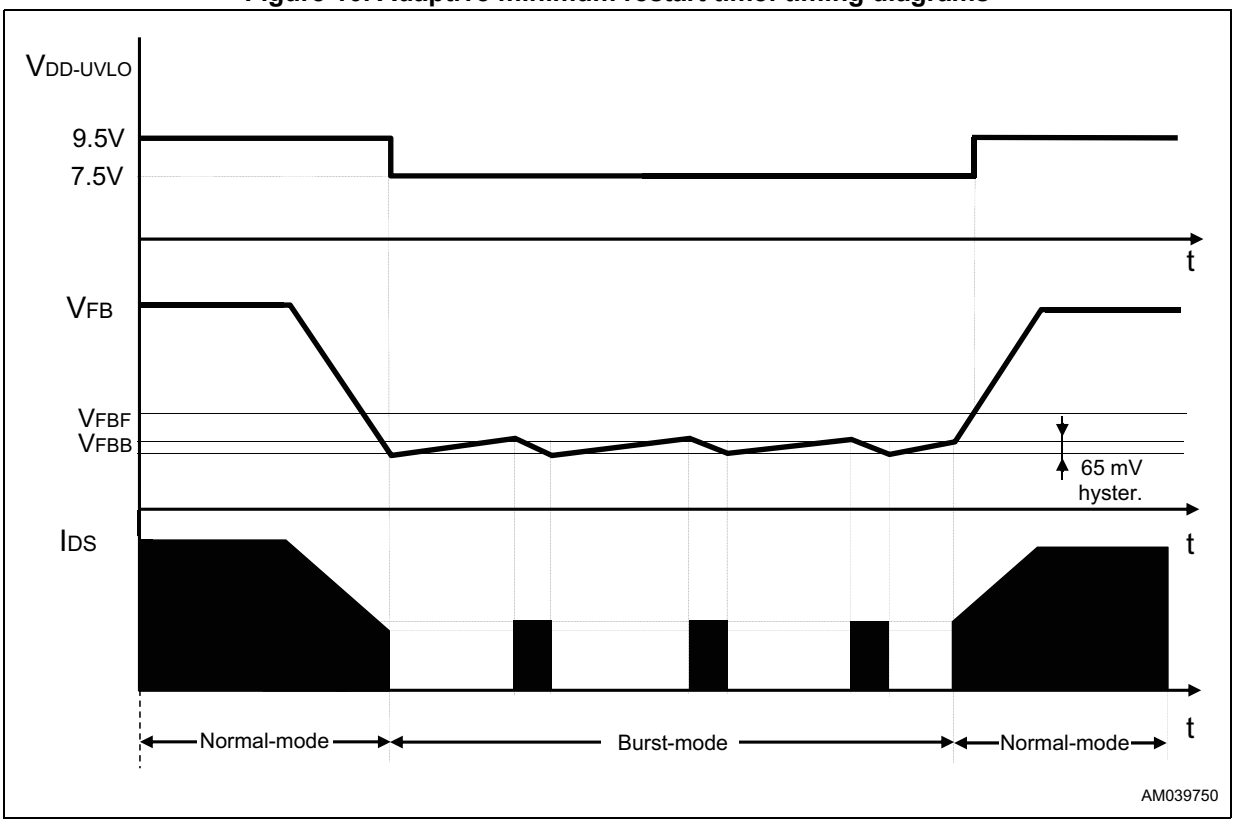
3.8 Burst mode operation

When the voltage at the FB pin falls down 65 mV below than V_{FBB}, the burst mode operation starts: the MOSFET is turned OFF in order to reduce the consumption. After the MOSFET turn OFF, the FB pin voltage, as result of the feedback reaction to the energy delivery stop, increases up to the V_{FBB} and the device restarts the switch again.

During these switching cycles the max. peak current is fixed (about V_{SENSE_BM}/R_{SENSE}) by an internal clamp inside the current limit circuit. The effect of the burst mode operation is to reduce the equivalent switching frequency, which can go down even to few hundred hertz, minimizing all frequency related losses and making it easier to comply with energy saving regulations.

This kind of operation, shown in the timing diagrams of *Figure 10* along with the other ones, is audible noise free since the peak current is low.

Figure 10. Adaptive minimum restart time: timing diagrams



3.9 Adaptive UVLO

A major problem when optimizing a converter for minimum no load consumption is that the voltage generated by the auxiliary winding under these conditions falls considerably as compared even to a few mA load. This very often causes the supply voltage VDD of the control IC to drop and, as the self-supply is disabled during the burst mode, it can go below the UVLO threshold so that the operation becomes intermittent, which is undesired.

Furthermore, this must be traded off against the need of generating a voltage not exceeding the maximum allowed by the control IC at the full load but low enough to reduce the bias losses as much as possible.

To help the designer to overcome this problem, the device besides reducing its own consumption during the burst mode operation, also features a proprietary adaptive UVLO function.

It consists of shifting the $V_{DD\text{-}UVLO}$ threshold downwards at the light-load, namely when the voltage at the FB pin falls 65 mV below the burst mode threshold V_{FBB} (0.6 V typ.), to have more headroom.

To prevent any malfunction the normal threshold (9.5 V typ.) is re-established when the voltage at the FB pin exceeds the exit burst mode threshold V_{FBF}.

The normal UVLO threshold ensures that at full medium-heavy loads the MOSFET will be driven with a proper gate to source voltage.

The mode of operation is reported in *Figure 10*.

3.10 Overvoltage protection

The overvoltage function of the STCH02 device monitors the voltage on the ZCD pin during MOSFET's OFF-time, where the voltage generated by the auxiliary winding tracks converter's output voltage. If the voltage applied to the pin exceeds an internal 2.5 V reference, a comparator is triggered, an overvoltage condition is assumed and the device is shut down.

Once R_{ZCD} is fixed by feedforward considerations (see *Section 3.7: Voltage feedforward block*) it is possible to calculate the value of the R_{OVP} resistor to activate the OVP protection for a certain output voltage level, $V_{OUT\text{-}OVP}$:

Equation 3

$$R_{OVP} = \frac{V_{OVP}}{\frac{N_{AUX}}{N_{SEC}} V_{OUT\text{-}OVP} - V_{OVP}} R_{ZCD}$$

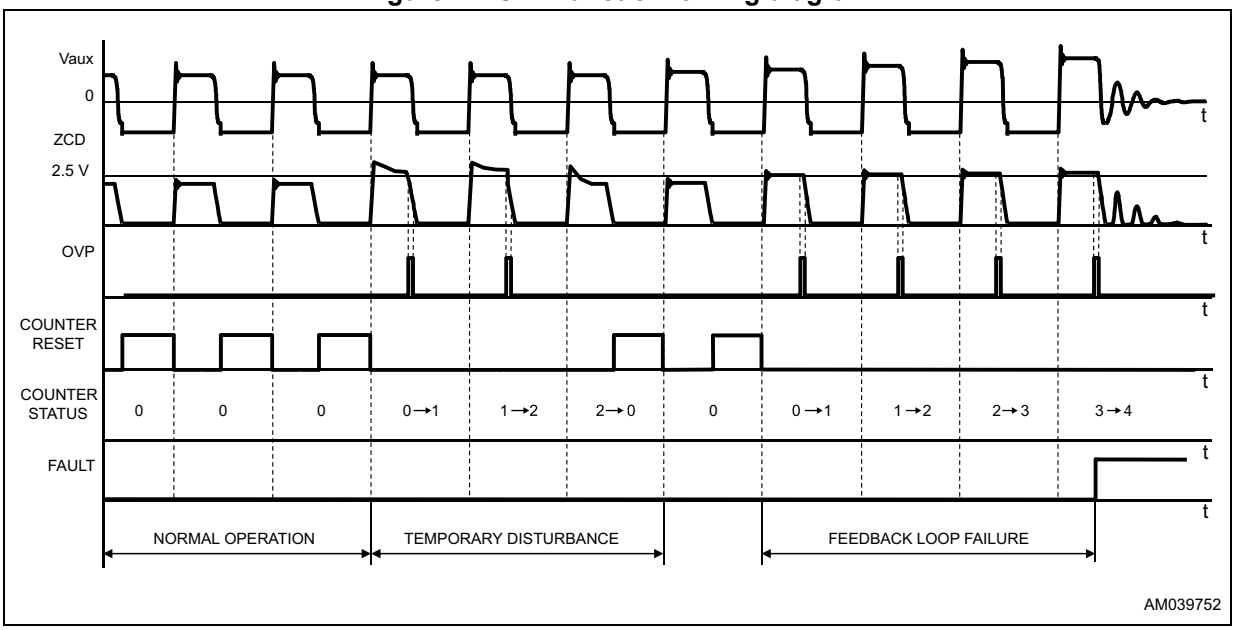
Where V_{OVP} is the internal OVP threshold, N_{SEC} and N_{AUX} are the secondary and auxiliary turn's number respectively.

To reduce sensitivity to noise and prevent the latch from being erroneously activated, the OVP comparator must be triggered for four consecutive oscillator cycles before the STCH02 device is stopped. A counter, which is reset every time the OVP comparator is not triggered in one oscillator cycle, is provided to this purpose.

Figure 11 illustrates the timing of the function.

Once the protection is tripped, the condition is maintained until V_{DD} goes below V_{DDR} restart voltage. While it is disabled, however, no energy is coming from the self-supply circuit; and the voltage on the V_{DD} capacitor will drop down to V_{DDR} restart voltage, before the V_{DD} capacitor is charged again and the device restarted (V_{DD-ON}). Ultimately, this will result into a low frequency intermittent operation (hiccup mode operation).

Figure 11. OVP function: timing diagram



3.11 Soft-start and starter block

The soft start feature is automatically implemented by the constant current block, as the primary peak current will be limited from the voltage on the internal CC block capacitor.

During the start-up, as the output voltage is zero, the IC will start in the CC mode with no high peak current operations. In this way the voltage on the output capacitor will increase slowly and the soft-start feature will be ensured.

3.12 Hiccup mode OCP

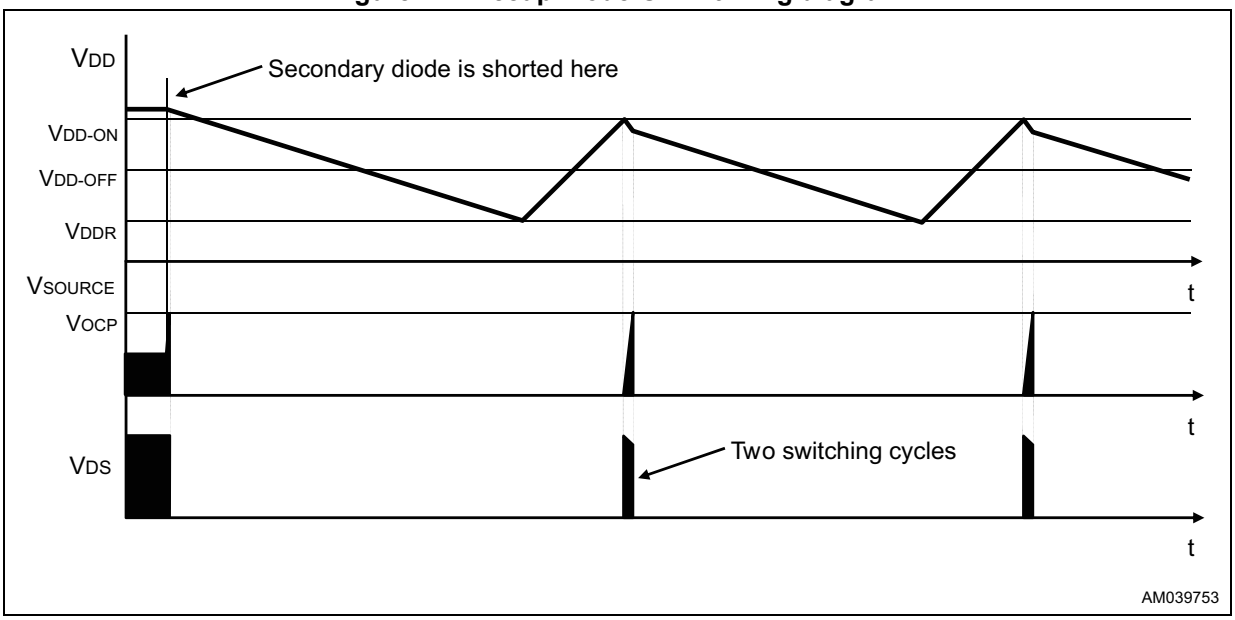
The device is also protected against the short-circuit of the secondary rectifier, short-circuit on the secondary winding or a hard-saturated flyback transformer. A comparator monitors continuously the voltage on the R_{SENSE} and activates protection circuitry if this voltage exceeds the V_{OCP} value (1 V typ. value).

To distinguish an actual malfunction from a disturbance (e.g.: induced during ESD tests), the first time the comparator is tripped the protection circuit enters a “warning state”. If in the subsequent switching cycle the comparator is not tripped, a temporary disturbance is assumed and the protection logic will be reset in its idle state; if the comparator will be tripped again a real malfunction is assumed and the device will be stopped.

Once the protection is tripped, the condition is maintained until V_{DD} goes below V_{DDR} restart voltage. While it is disabled, however, no energy is coming from the self-supply circuit; hence the voltage on the V_{DD} capacitor will decay and cross the UVLO threshold after some

time, which clears the latch. The internal start-up generator is still off, then the V_{DD} voltage still needs to go below its restart voltage before the V_{DD} capacitor is charged again and the device restarted. Ultimately, this will result in a low frequency intermittent operation (hiccup mode operation), with very low stress on the power circuit. This special condition is illustrated in the timing diagram of *Figure 12*.

Figure 12. Hiccup mode OCP: timing diagram



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

4.1 SO-8 package information

Figure 13. SO-8 package outline

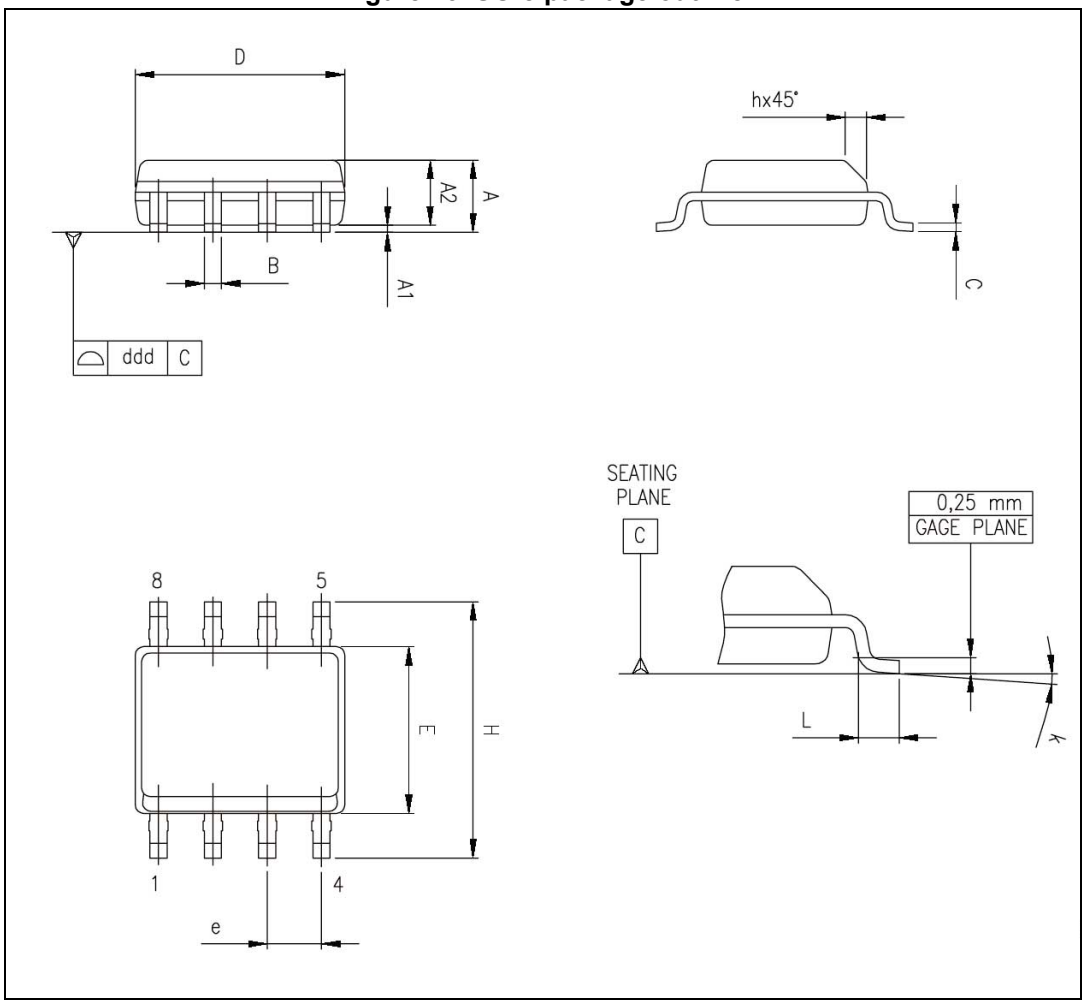


Table 6. SO-8 package mechanical data

Symbol	Dimensions					
	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D(1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 inch) in total (both sides).

5 Revision history

Table 7. Document revision history

Date	Revision	Changes
15-Dec-2015	1	Initial release.