STB30NF20L

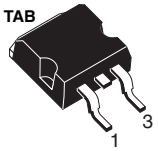
N-channel 200 V, 0.065 Ω, 30 A STripFET™ Power MOSFET in D²PAK package

Datasheet — production data

Features

Order code	V_{DSS}	$R_{DS(on)}$	I_D	P_{TOT}
STB30NF20L	200 V	0.075 Ω	30 A	150 W

- Gate charge minimized
- 100% avalanche tested
- Excellent figure of merit (R_{DS}* Q_g)
- Very good manufacturing repeatability
- Very low intrinsic capacitance



D²PAK

Applications

- Automotive

Description

This N-channel enhancement mode Power MOSFET benefits from the latest refinement of STMicroelectronics' unique "single feature size" strip-based process, which decreases the critical alignment steps to offer exceptional manufacturing reproducibility. The result is a transistor with extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Figure 1. Internal schematic diagram

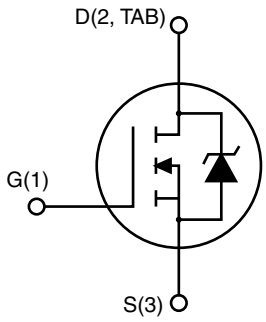


Table 1. Device summary

Order code	Marking	Package	Packaging
STB30NF20L	30NF20L	D²PAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	200	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	30	A
I_D	Drain current (continuous) at T_C=100 °C	19	A
I_{DM}(1)	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
	Derating factor	1	W/°C
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C
T_l	Maximum lead temperature for soldering purpose	300	°C

1. Pulse width limited by safe operating area.
2. I_{SD} ≤30A, di/dt ≤200A/µs, V_{DD} = 80%$V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case max.	1	°C/W
R_{thJA}	Thermal resistance junction-ambient max.	62.5	°C/W

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by Tjmax)	30	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, I_D=I_{AR}, V_{DD}=50 V)	140	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified).

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 200 V, V_{DS} = 200 V, Tc=125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	2	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 5 V, I_D= 15 A		0.065	0.075	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	1990 297 42	-	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=160 V, I_D = 30 A V_{GS} =10 V (see Figure 14)	-	65 7 21	-	nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=100 V, I_D=15 A, R_G=4.7 Ω, V_{GS}=10 V (see Figure 13)	-	14 12	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=100 V, I_D=15 A, R_G=4.7 Ω, V_{GS}=10 V (see Figure 13)	-	68 14	-	ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain current Source-drain current (pulsed)	V_{SD}=1.5 V	-		30 120	A A
V_{SD}(2)	Forward on voltage	I_{SD}=30 A, V_{GS}=0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=30 A, di/dt = 100 A/µs, V_{DD}=100 V	-	140 750 13		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=30 A, di/dt = 100 A/µs, V_{DD}=100 V, Tj=150 °C	-	170 1.1 14		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

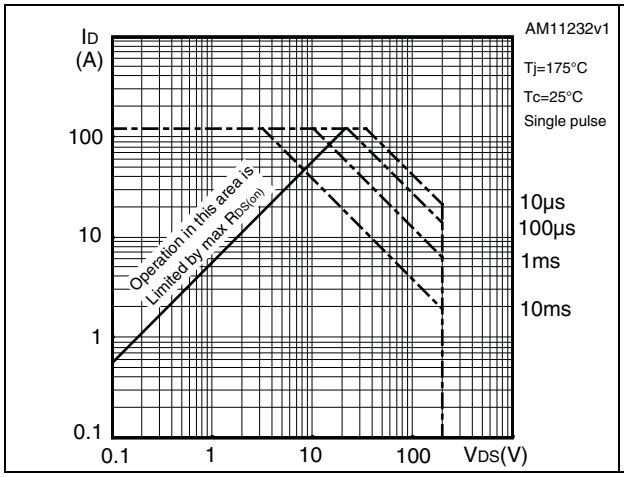


Figure 3. Thermal impedance

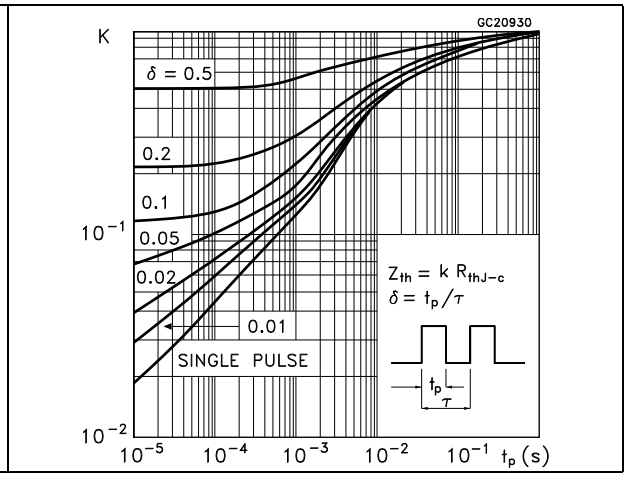


Figure 4. Output characteristics

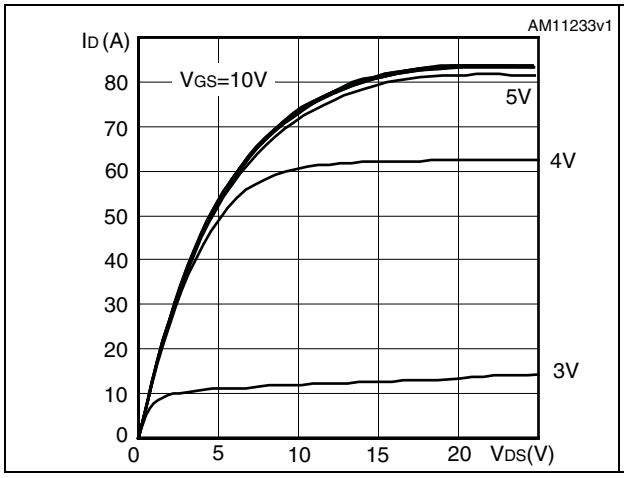


Figure 5. Transfer characteristics

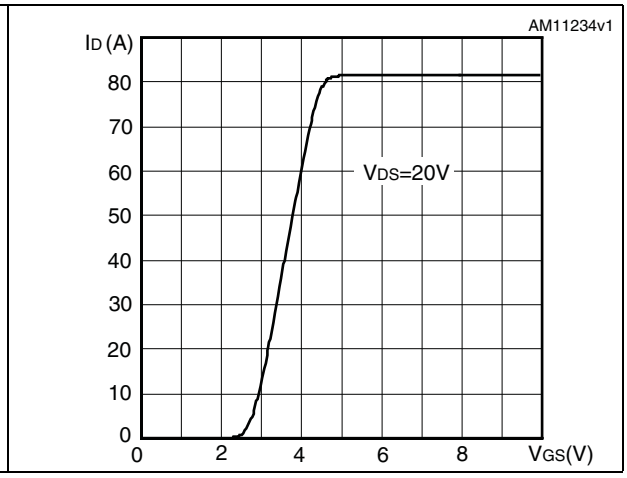


Figure 6. Normalized B_{VDSS} vs temperature

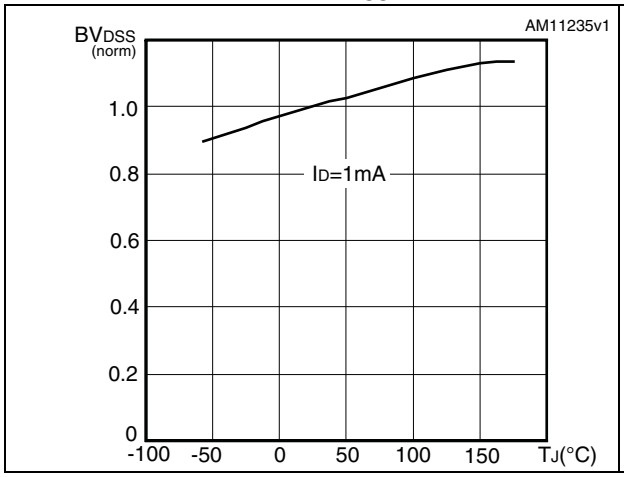


Figure 7. Static drain-source on-resistance

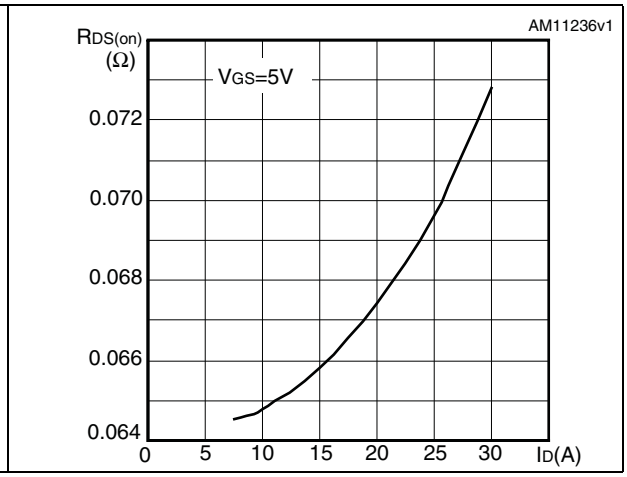


Figure 8. Gate charge vs gate-source voltage

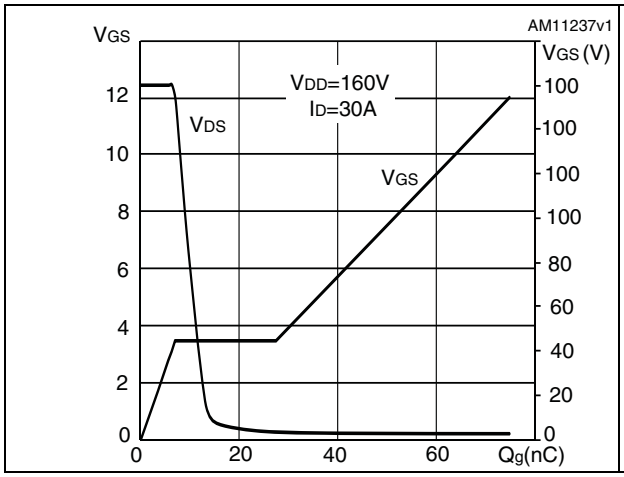


Figure 9. Capacitance variations

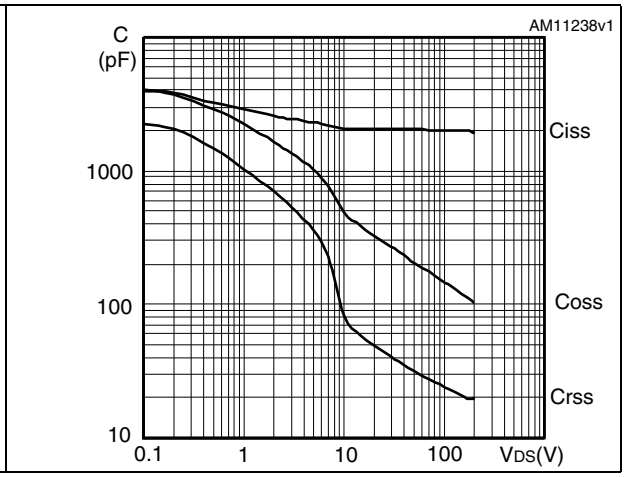


Figure 10. Normalized gate threshold voltage vs temperature

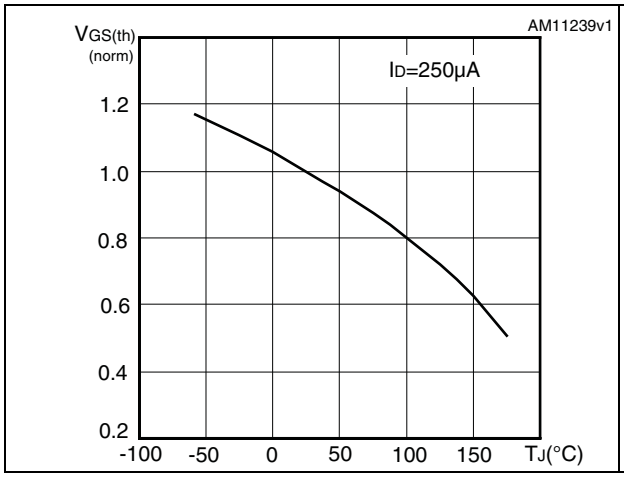


Figure 11. Normalized on-resistance vs temperature

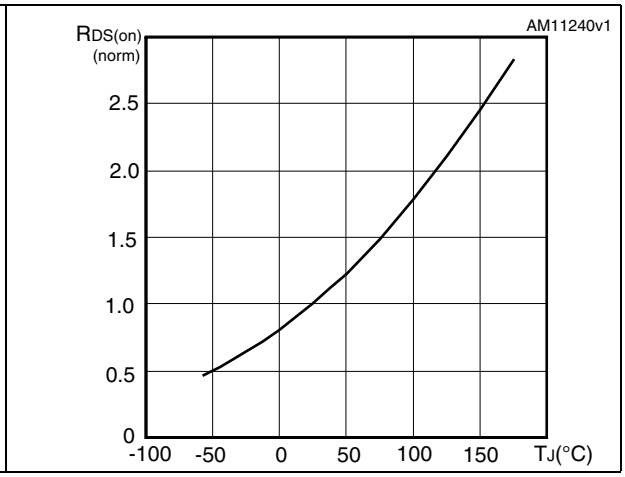
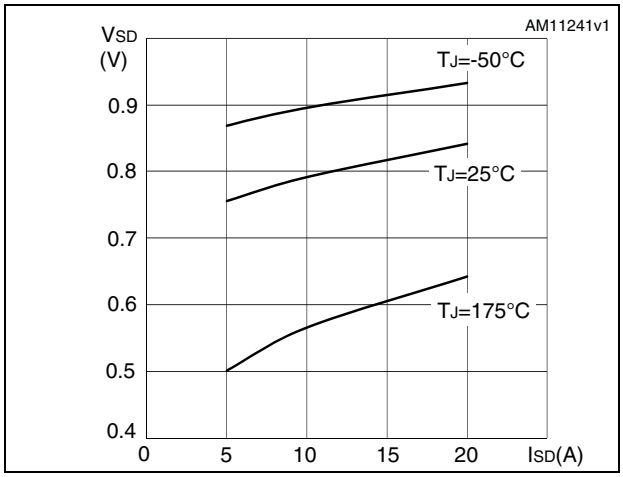


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

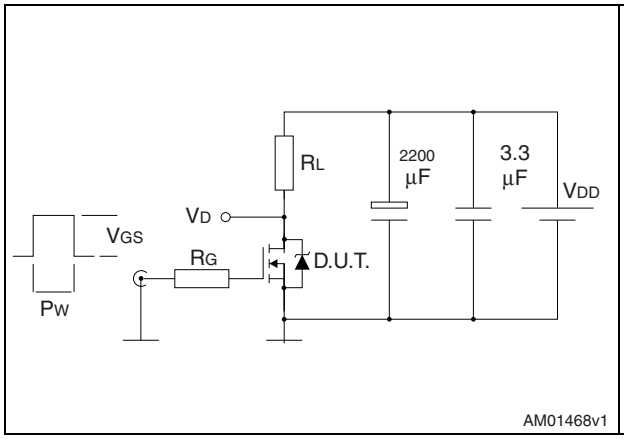


Figure 14. Gate charge test circuit

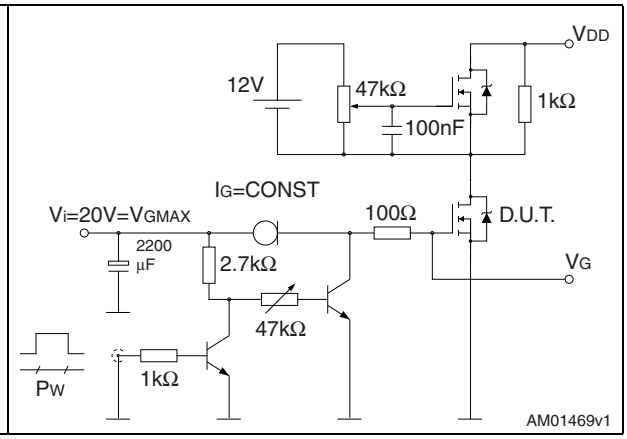


Figure 15. Test circuit for inductive load switching and diode recovery times

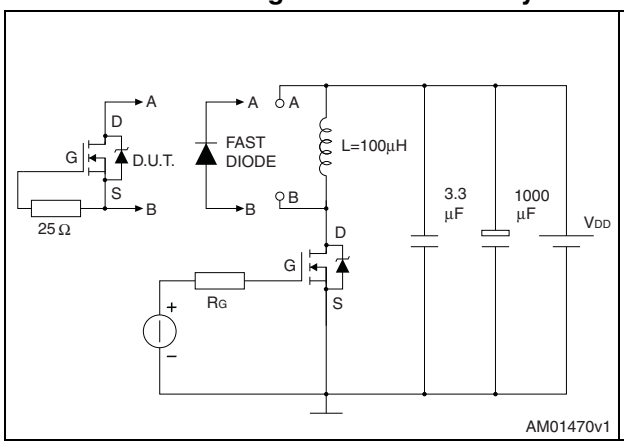


Figure 16. Unclamped inductive load test circuit

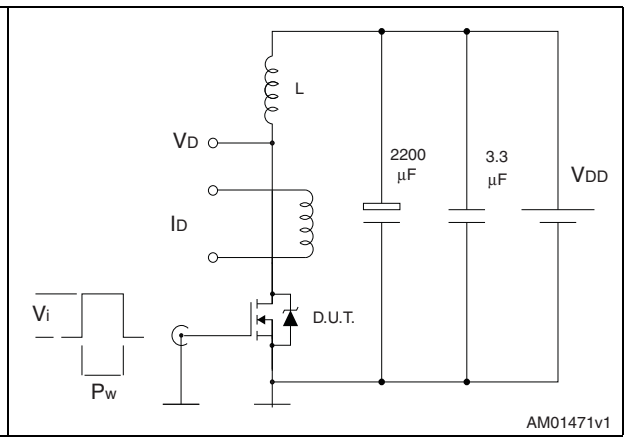


Figure 17. Unclamped inductive waveform

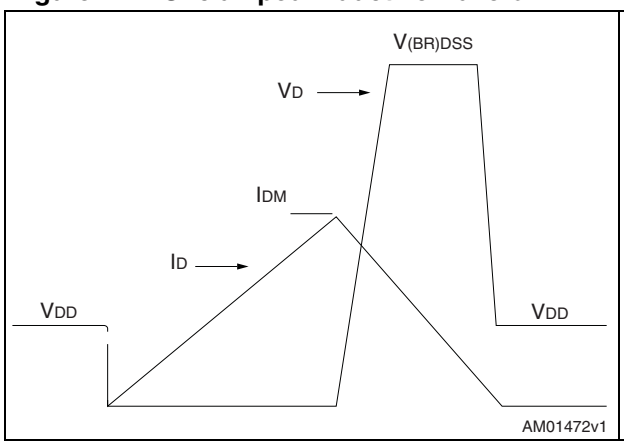
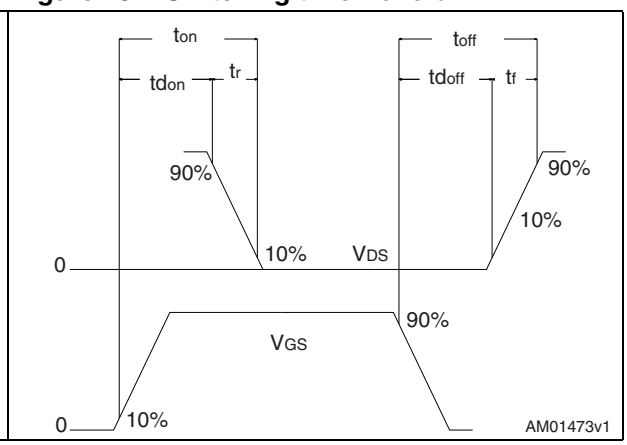


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 19. D²PAK (TO-263) drawing

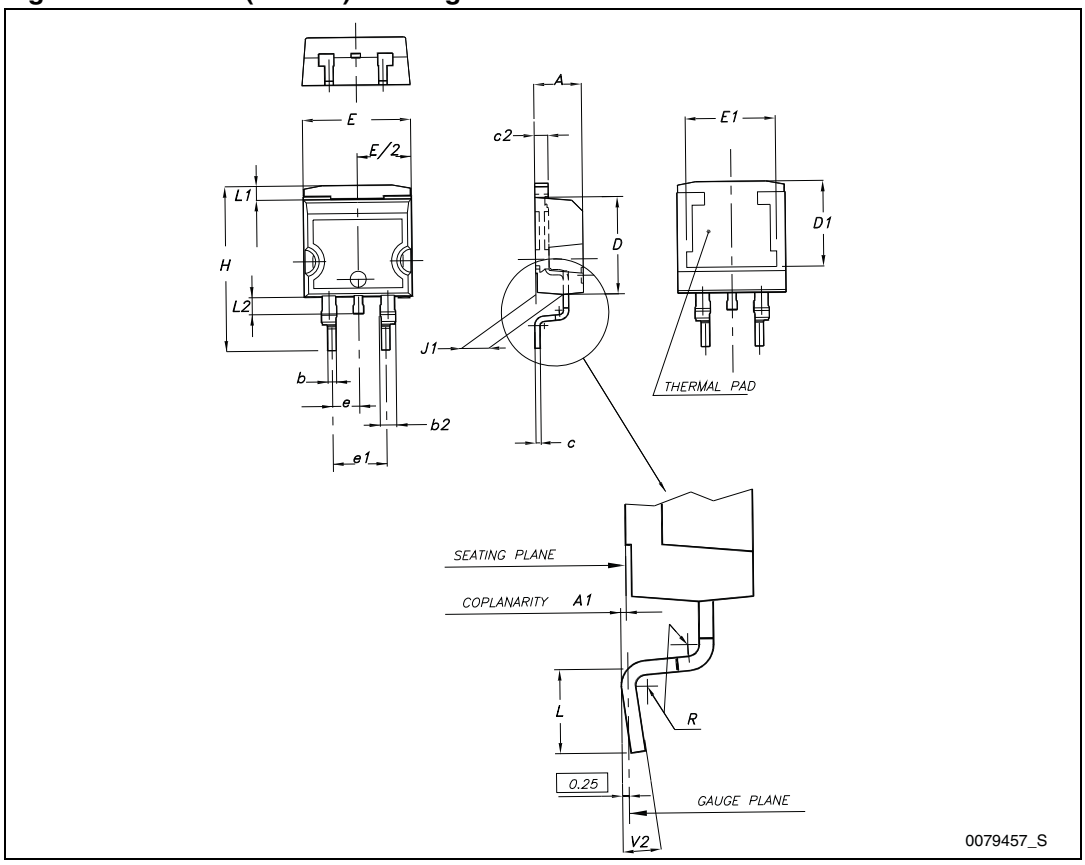
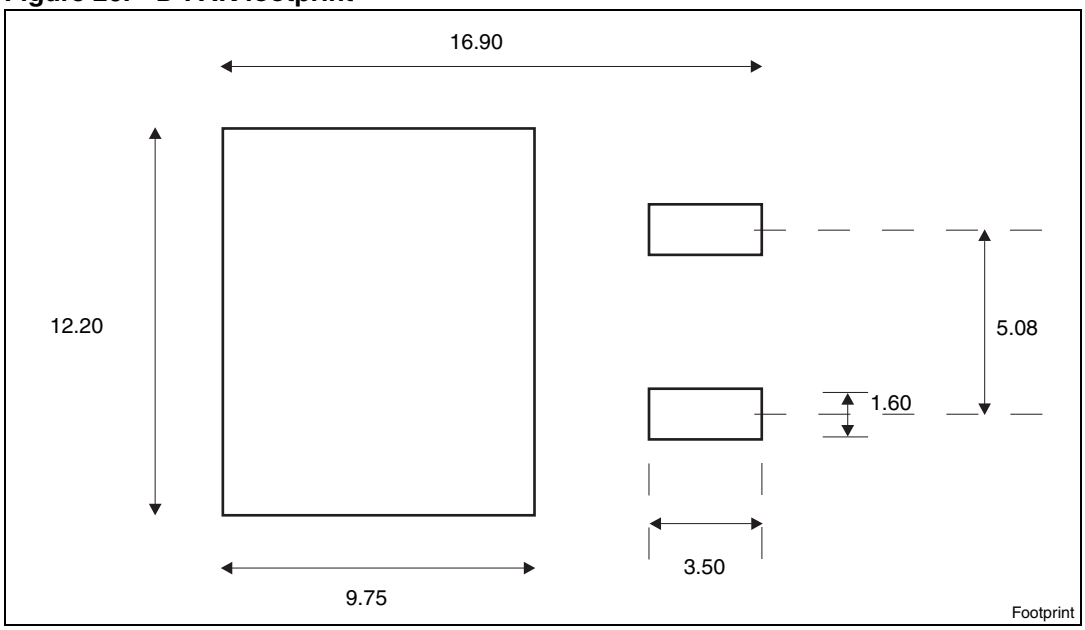


Figure 20. D²PAK footprint[a]



a. All dimensions are in millimeters.

5 Packaging mechanical data

Table 10. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 21. Tape

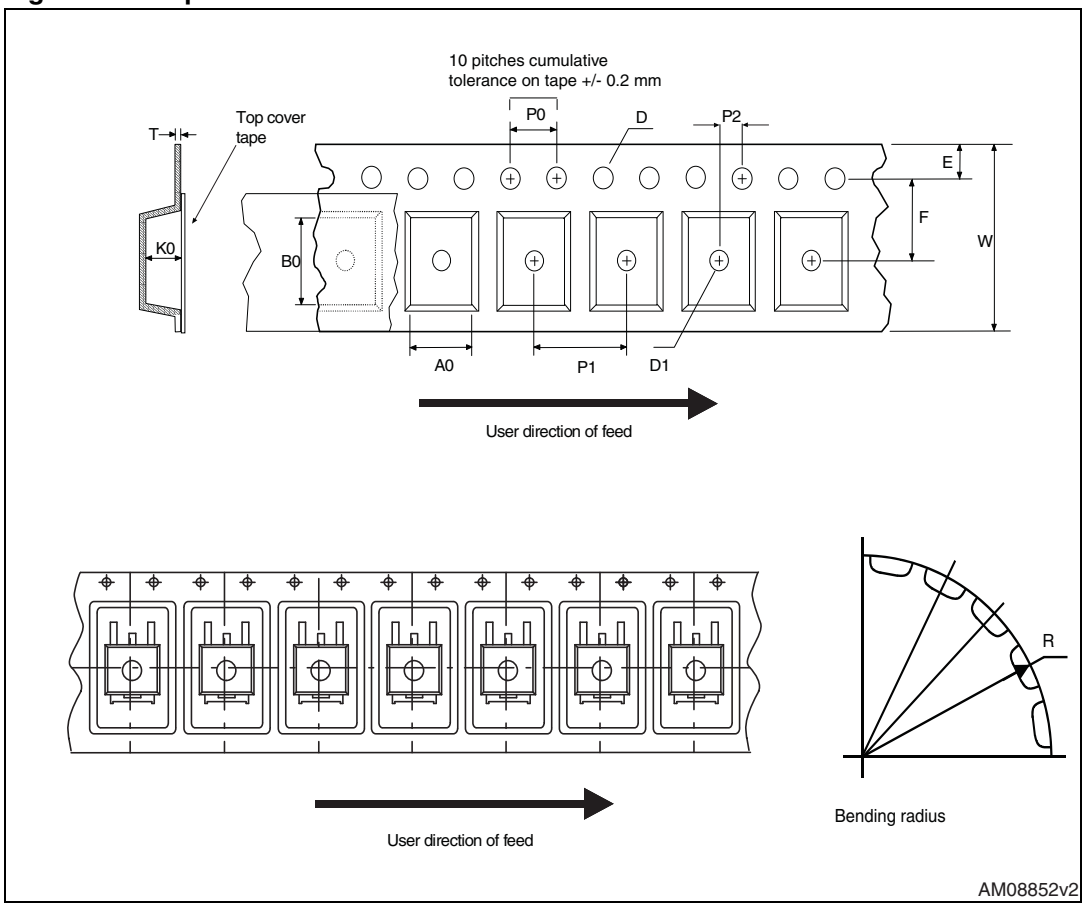
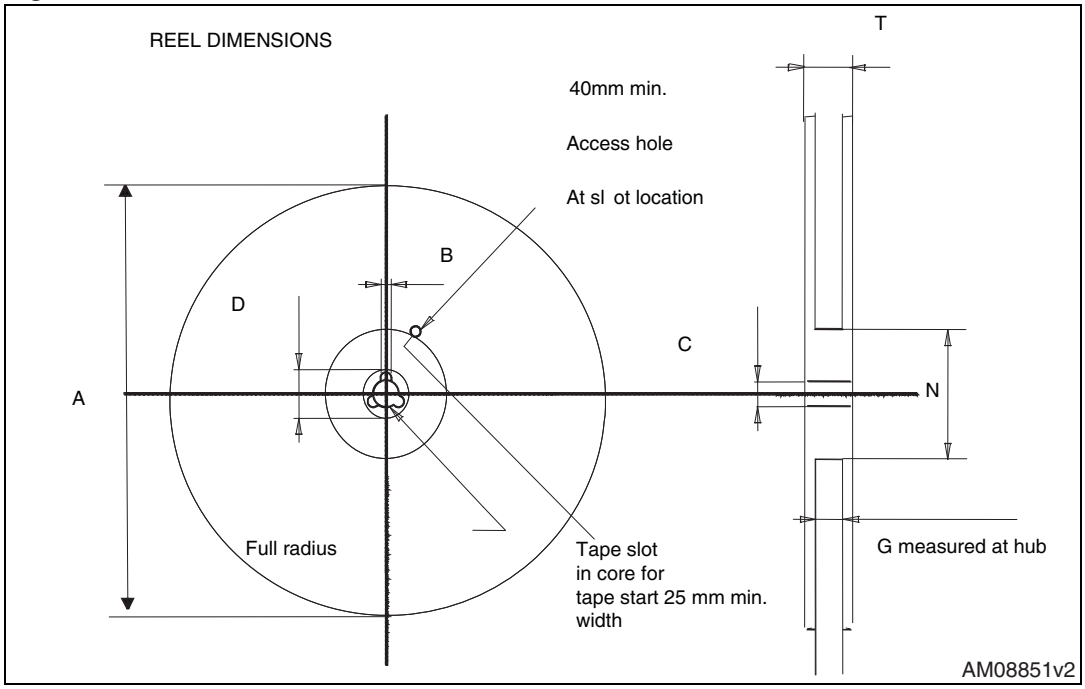


Figure 22. Reel



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
01-Feb-2012	1	First release.
07-Mar-2012	2	P_{TOT} in cover page and in *Table 2* has been updated. *Figure 2*, *Figure 6*, *Figure 10* and *Figure 11* have been updated.