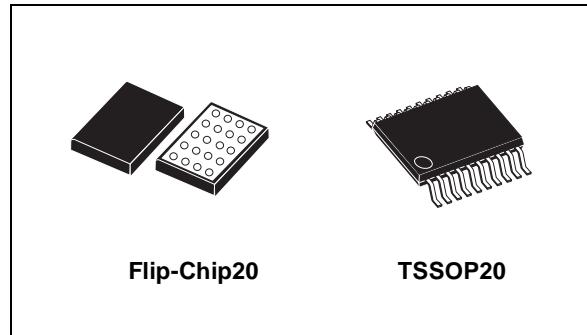


## 8-bit dual supply 1.71V to 5.5V level translator with I/O $V_{CC} \pm 15\text{KV}$ ESD protection

### General features

- High speed:
  - $t_{PD} = 15\text{ns}$  (Max.) at  $T_A = 85^\circ\text{C}$
  - $V_L = 1.8\text{V}$
  - $V_{CC} = 5.5\text{V}$
- Guaranteed data rate:
  - 13Mbps ( $1.8\text{V} \leq V_L \leq V_{CC} \leq 5.5\text{V}$ )
- Low power dissipation:
  - $I_{TS-VL} = I_{TS-VCC} = 1\mu\text{A}$  (Max.) at  $T_A = 85^\circ\text{C}$
  - $I_{QVL} = 100\mu\text{A}$  (Max.) at  $T_A = 85^\circ\text{C}$
  - $I_{QCC} = 10\mu\text{A}$  (Max.) at  $T_A = 85^\circ\text{C}$
- Output impedance:
  - $|I_{OHA}| = 20\mu\text{A}$ (Min.) at  $V_L=1.8\text{V}; V_{CC} = 5.5\text{V}$
  - $I_{OLA} = 1.0\mu\text{A}$ (Min.) at  $V_L=1.8\text{V} V_{CC} = 5.5\text{V}$
- Bi-directional level translation
- Totem pole and open drain driving for I<sup>2</sup>C communications
- 5V tolerant on enable pin
- Wide operating voltage range:
  - $V_L(\text{Opr}) = 1.71\text{V}$  to  $V_{CC}$
  - $V_{CC}(\text{Opr}) = 1.71\text{V}$  to  $5.5\text{V}$
- ESD performance
- HBM > 15KV ESD protection on I/O  $V_{CC}$  lines
- Leadfree Flip-Chip and TSSOP packages



### Description

The ST2378E is an 8-bit, dual supply, bi-directional level translator with  $\pm 15\text{kV}$  ESD-protection on I/Os at  $V_{CC}$  side. It is designed to interface data transfer between low-voltage ASICs/PLDs and higher voltage systems. Externally applied voltage,  $V_{CC}$  and  $V_L$ , set logic levels at both sides with range specified as  $1.71\text{V} \leq V_L \leq 5.5\text{V}$  and  $V_L \leq V_{CC} \leq 5.5\text{V}$ . For proper operation,  $V_{CC}$  should be set higher than  $V_L$ .

Utilizing a transmission-gate-based design, this device allows bi-directional asynchronous data transfer, which means each channel is allowed to have either  $V_{CC}$  to  $V_L$  or  $V_L$  to  $V_{CC}$  data transfer direction independently and no direction pin is required. ST2378E operates at guaranteed data rate of 13Mbps over the entire specified operating voltage range.

Among the other features is included the OE pin which allows disable-mode operation whereby current consumption is reduced to less than  $1\mu\text{A}$ .

### Order codes

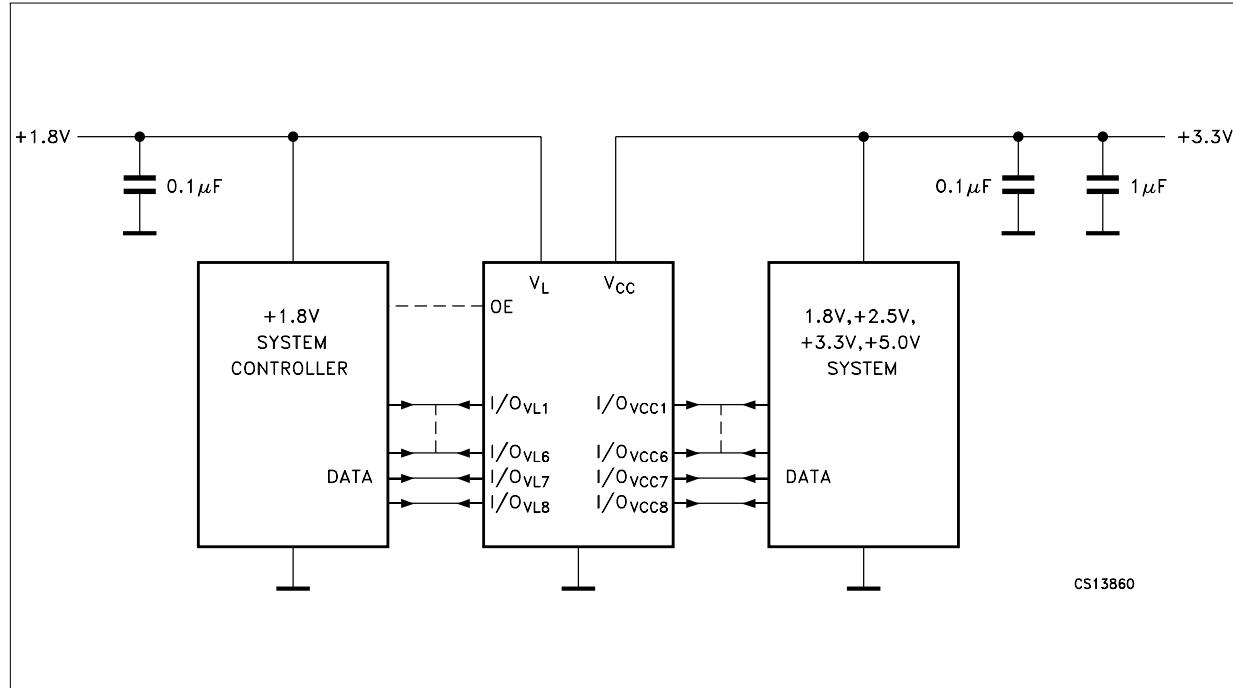
Part number	Temperature range	Package	Comments
ST2378EBJR	-40 to 85 °C	Flip-Chip20 (Tape and Reel)	3000 parts per reel
ST2378ETTR	-40 to 85 °C	TSSOP20 (Tape and Reel)	2500 parts per reel

## Contents

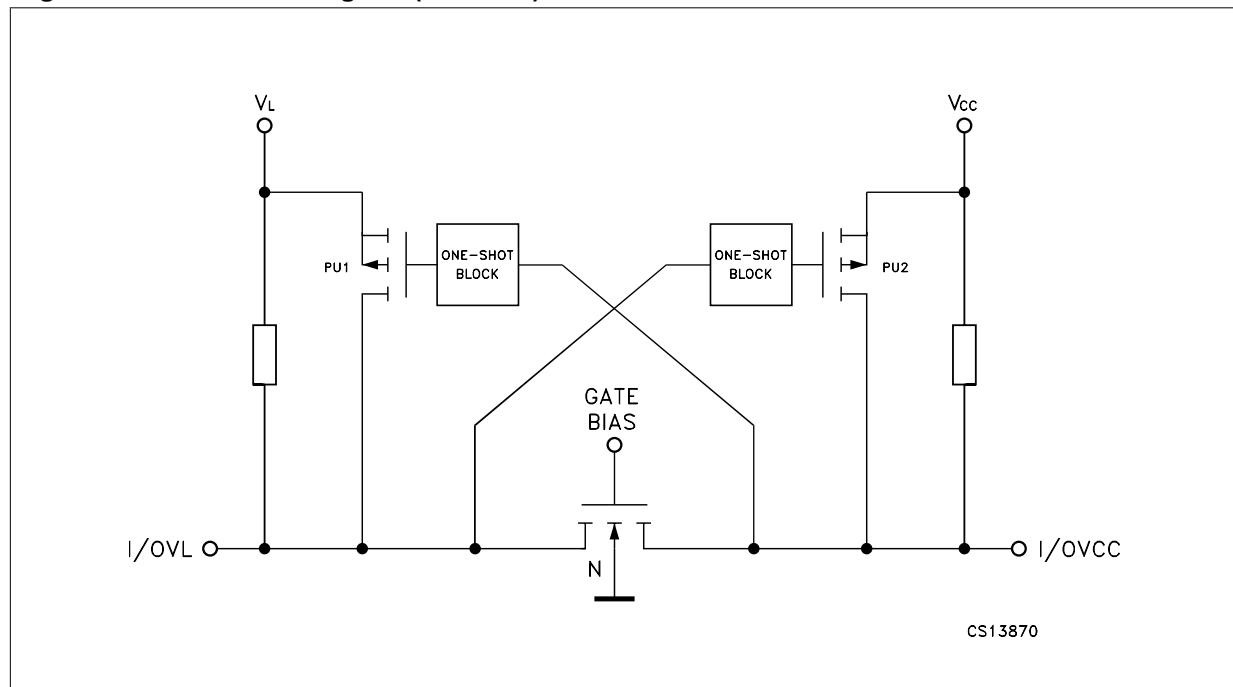
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# 1 Block diagram

**Figure 1. Block diagram**



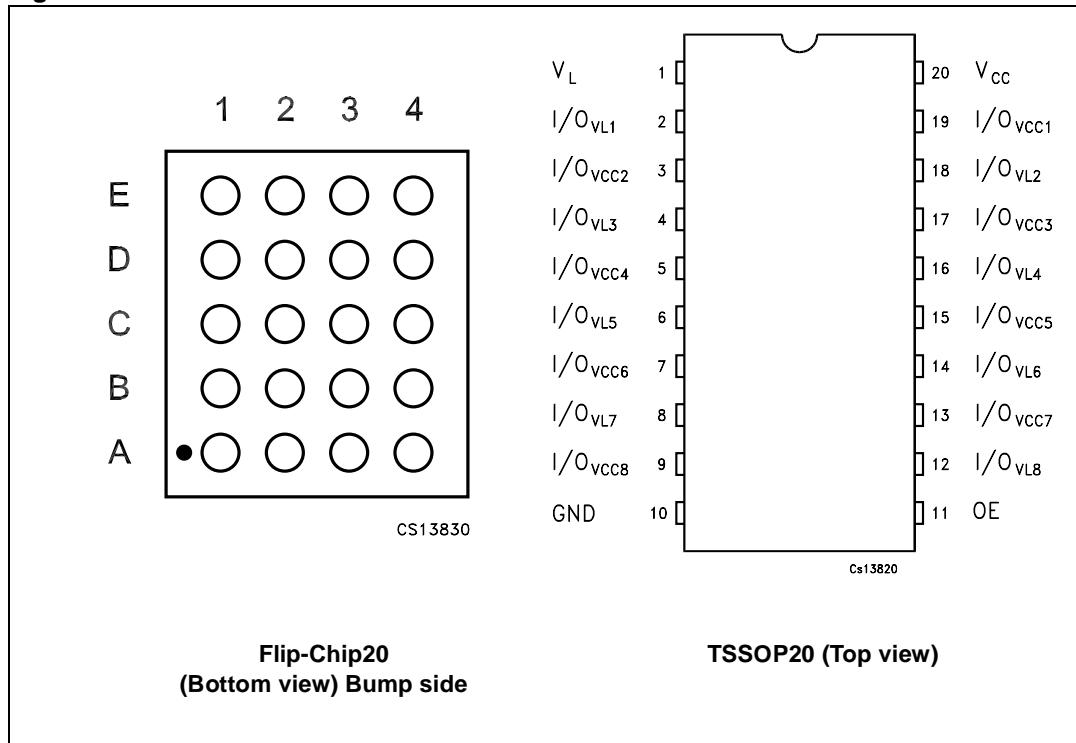
**Figure 2. Functional diagram (1 I/O line)**



## 2 Pin settings

### 2.1 Pin connection

**Figure 3.** Pin connection



### 2.2 Pin description

**Table 1.** Pin description

Flip-Chip20 Pin N°	TSSOP20 Pin N°	Symbol	Name and function
E2, D1, D2, C1, C2, B1, B2, A1	2, 18, 4, 16, 6, 14, 8, 12	I/O <sub>VL1</sub> to I/O <sub>VL8</sub>	Data Inputs/Outputs
E3, D4, D3, C4, C3, B4, B3, A4	19, 3, 17, 5, 15, 7, 13, 9	I/O <sub>VCC1</sub> to I/O <sub>VCC8</sub>	Data Inputs/Outputs
A2	11	OE	Output Enable Inputs
A3	10	GND	Ground (0V)
E1	1	V <sub>L</sub>	Positive Supply Voltage
E4	20	V <sub>CC</sub>	Positive Supply Voltage

## 3 Electrical data

### 3.1 Maximum ratings

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_L$	Supply Voltage	-0.3 to $V_{CC}$	V
$V_{CC}$	Supply Voltage	-0.3 to +7.0	V
$V_{OE}$	DC Control Input Voltage	-0.3 to +7.0	V
$V_{I/OVL}$	DC I/O <sub>VL</sub> Input Voltage (OE = Gnd or $V_L$ )	-0.3 to $V_L + 0.3$	V
$V_{I/OVCC}$	DC I/O <sub>VCC</sub> Input Voltage (OE = Gnd or $V_L$ )	-0.3 to $V_{CC} + 0.3$	V
$I_{IK}$	DC Input Diode Current (OE Control Pin)	-20	mA
$I_{IOVL}$	DC Output Current	$\pm 25$	mA
$I_{IOVCC}$	DC Output Current	$\pm 25$	mA
$I_{SCTOUT}$	Short Circuit Duration I/O <sub>VL</sub> , I/O <sub>VCC</sub> Driven from 40mA Source	Continuous	mA
$I_{CCB}$	DC $V_{CC}$ or Ground Current	$\pm 100$	mA
$P_d$	Power Dissipation <sup>(1)</sup>	500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature (10 sec)	300	°C

1. 500mW:  $\equiv 65^{\circ}\text{C}$  derated to 300mW by 10mW/°C:  $65^{\circ}\text{C}$  to  $85^{\circ}\text{C}$

## 3.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

Symbol	Parameter	Value	Unit
$V_L$	Supply Voltage	1.71 to $V_{CC}$	V
$V_{CC}$	Supply Voltage	1.71 to 5.5	V
$V_I$	Input Voltage (OE Output Enable Pin, $V_L$ Power Supply referred)	0 to 5.5	V
$V_{I/OVL}$	I/O <sub>VL</sub> Voltage	0 to $V_L$	V
$V_{I/OVCC}$	I/O <sub>VCC</sub> Voltage	0 to $V_{CC}$	V
$T_{op}$	Operating Temperature	-40 to 85	°C
$dt/dv$	Input Rise and Fall Time (OE Control Pin) <sup>(1)</sup>	0 to 10	ns/V
$dt/dv$	Input Rise and Fall Time <sup>(2)</sup>	1.71 < $V_L$ < $V_{CC}$ < 5V	0 to 10
		$V_{CC} = V_L = 5V$	0 to 3
			ns/V

1.  $V_{OE}$  from 10%  $V_L$  to 90%  $V_L$

2.  $V_{I/OVL}$  from 10%  $V_L$  to 90%  $V_L$ ;  $V_{I/OVCC}$  from 10%  $V_{CC}$  to 90%  $V_{CC}$

## 4 Electrical characteristics

Table 4. DC Specification

Symbol	Parameter	Test Condition			Value					Unit	
		$V_L^{(*)}$ (V)	$V_{CC}^{(*)}$ (V)		$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$			
					Min.	Typ	Max.	Min.	Max.		
$V_{IHL}$	High Level Input Voltage ( $I/O_{VL}$ )	1.8	$V_L$ to 5.5		$V_L - 0.2$			$V_L - 0.2$		V	
		2.5	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
		3.3	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
		5.0	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
$V_{ILL}$	Low Level Input Voltage ( $I/O_{VL}$ )	1.8	$V_L$ to 5.5				0.15		0.15	V	
		2.5	$V_L$ to 5.5				0.30		0.30		
		3.3	$V_L$ to 5.5				0.30		0.30		
		5.0	$V_L$ to 5.5				0.30		0.30		
$V_{IHC}$	High Level Input Voltage ( $I/O_{VCC}$ )	1.8	$V_L$ to 5.5		$V_L - 0.2$			$V_L - 0.2$		V	
		2.5	$V_L$ to 5.5		0.75 $V_{CC}$			0.75 $V_{CC}$			
		3.3	$V_L$ to 5.5		0.75 $V_{CC}$			0.75 $V_{CC}$			
		5.0	$V_L$ to 5.5		0.75 $V_{CC}$			0.75 $V_{CC}$			
$V_{ILC}$	Low Level Input Voltage ( $I/O_{VCC}$ )	1.8	$V_L$ to 5.5				0.15		0.15	V	
		2.5	$V_L$ to 5.5				0.30		0.30		
		3.3	$V_L$ to 5.5				0.30		0.30		
		5.0	$V_L$ to 5.5				0.30		0.30		

Table 4. DC Specification

Symbol	Parameter	Test Condition			Value					Unit	
		$V_L^{(*)}$ (V)	$V_{CC}^{(*)}$ (V)		$T_A = 25^\circ C$			$-40 \text{ to } 85^\circ C$			
					Min.	Typ	Max.	Min.	Max.		
$V_{IH-TS}$	High Level Input Voltage (OE)	1.8	$V_L$ to 5.5		$V_L - 0.2$			$V_L - 0.2$		V	
		2.5	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
		3.3	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
		5.0	$V_L$ to 5.5		0.75 $V_L$			0.75 $V_L$			
$V_{IL-TS}$	Low Level Input Voltage (OE)	1.8	$V_L$ to 5.5				0.15		0.15	V	
		2.5	$V_L$ to 5.5				0.25 $V_L$		0.25 $V_L$		
		3.3	$V_L$ to 5.5				0.25 $V_L$		0.25 $V_L$		
		5.0	$V_L$ to 5.5				0.25 $V_L$		0.25 $V_L$		
$V_{OHL}$	High Level Output Voltage I/O $V_L$	1.8 to 5.5	$V_L$ to 5.5	$I_O = -20 \mu A$ $I/O_{VCC} \geq V_{CC} - 0.2$	0.67 $V_L$			0.67 $V_L$		V	
$V_{OLL}$	Low Level Output Voltage I/O $V_L$			$I_O = 1.0 \text{ mA}$ $I/O_{VCC} \leq 0.15V$			0.40		0.40		
$V_{OHC}$	High Level Output Voltage I/O $V_{CC}$	1.8 to 5.5	$V_L$ to 5.5	$I_O = -20 \mu A$ $I/O_{VL} \geq V_L - 0.2$	0.67 $V_{CC}$			0.67 $V_{CC}$		V	
$V_{OLC}$	Low Level Output Voltage I/O $V_{CC}$			$I_O = 1.0 \text{ mA}$ $I/O_{VL} \leq 0.15V$			0.40		0.40		
$I_{TSL}$	Control Input Leakage Current (OE)	1.8 to 5.5	$V_L$ to 5.5	$V_I = GND$ or 5.5			1		1	$\mu A$	
$I_{TS-LKG}$	High Impedance Input Leakage Current ( $I_{O_{VL}}$ , $I/O_{VCC}$ )	1.8 to 5.5	$V_L$ to 5.5	OE = GND			1		1	$\mu A$	
$I_{QVCC}$	Quiescent Supply Current $V_{CC}$	1.8 to 5.5	$V_L$ to 5.5	$I/O_{VL}$ , $I/O_{VCC}$ unconnected		0.1	1		10	$\mu A$	

**Table 4. DC Specification**

Symbol	Parameter	Test Condition			Value				Unit	
		$V_L^{(*)}$ (V)	$V_{CC}^{(*)}$ (V)		$T_A = 25^\circ C$		$-40 \text{ to } 85^\circ C$			
					Min.	Typ	Max.	Min.		
$I_{QVL}$	Quiescent Supply Current $V_L$	1.8 to 5.5	$V_L$ to 5.5	$I/O_{VL}$ , $I/O_{VCC}$ unconnected		13	20		100 $\mu A$	
$I_{TS-VCC}$	High Impedance Mode Quiescent Supply Current $V_{CC}$	1.8 to 5.5	$V_L$ to 5.5	$OE = GND$			1		1 $\mu A$	
$I_{TS-VL}$	High Impedance Mode Quiescent Supply Current $V_L$	1.8 to 5.5	$V_L$ to 5.5	$OE = GND$ $I/O_{VL} = GND$ to $V_L$ $I/O_{VCC} = GND$ to $V_{CC}$			1		1 $\mu A$	

Note: 1 Typical values are referred to  $T_A = 25^\circ C$

2 Power Supply Range:  $V_L$ ,  $V_{CC}$   $1.8V \pm 5\%$ ,  $2.5 \pm 0.2V$ ,  $3.3 \pm 0.3V$ ,  $5.0 \pm 0.5V$

3 For normal operation, ensure  $V_L < (V_{CC} + 0.3V)$ . During power-up,  $V_L > (V_{CC} + 0.3V)$  will not damage the device

**Table 5. AC Electrical characteristics (totem pole driving)**

Symbol	Parameter	Test Condition <sup>(1)</sup>		Value		Unit	
		$C_L=15\text{pF}$ $t_r=t_f \leq 6\text{ns}$ Driver output $R_T \leq 50\Omega$ <sup>(2)</sup>		-40 to +85 °C			
		$V_L$ (V) <sup>(3)</sup>	$V_{CC}$ (V) <sup>(3)</sup>	Min.	Typ. <sup>(4)</sup>	Max.	
t <sub>RVCC</sub>	Rise Time I/O <sub>VCC</sub> <sup>(3)(8)</sup>	1.8	1.8		11	15	ns
		1.8	2.5		11	15	
		1.8	3.3		10	15	
		1.8	5.0		9	15	
		2.5	3.3		8	15	
t <sub>FCC</sub>	Fall Time I/O <sub>VCC</sub> <sup>(3)(8)</sup>	1.8	1.8		6	15	ns
		1.8	2.5		7	15	
		1.8	3.3		8	15	
		1.8	5.0		10	15	
		2.5	3.3		6	15	
t <sub>RVL</sub>	Rise Time I/O <sub>VL</sub> <sup>(3)(8)</sup>	1.8	1.8		12	15	ns
		1.8	2.5		10	15	
		1.8	3.3		9	15	
		1.8	5.0		10	15	
		2.5	3.3		7	15	
t <sub>FVL</sub>	Fall Time I/O <sub>VL</sub> <sup>(3)(8)</sup>	1.8	1.8		7	15	ns
		1.8	2.5		6	15	
		1.8	3.3		6	15	
		1.8	5.0		7	15	
		2.5	3.3		4	15	
t <sub>I<sub>OVL-VCC</sub></sub>	Propagation Delay Time <sup>(4)</sup> I/O <sub>VL-LH</sub> to I/O <sub>VCC-LH</sub> I/O <sub>VL-HL</sub> to I/O <sub>VCC-HL</sub>	t <sub>PLH</sub>	1.8	1.8	6	15	ns
			1.8	2.5	7	15	
			1.8	3.3	7	15	
			1.8	5.0	7	15	
			2.5	3.3	4	15	
		t <sub>PHL</sub>	1.8	1.8	5	15	
			1.8	2.5	5	15	
			1.8	3.3	6	15	
			1.8	5.0	8	15	
			2.5	3.3	4	15	

**Table 5. AC Electrical characteristics (totem pole driving)**

Symbol	Parameter	Test Condition		Value			Unit	
		$C_L = 15\text{pF}$ $t_r = t_f \leq 6\text{ns}$ Driver output $R_T \leq 50\Omega$			-40 to +85 °C			
		$V_L$ (V)	$V_{cc}$ (V)	Min.	Typ.	Max.		
$t_{iovcc-vl}$	Propagation Delay Time(4) I/OVCC-LH to I/OVL-LH I/OVCC-HL to I/OVL-HL	$t_{PLH}$	1.8	1.8		2	15	ns
			1.8	2.5		2	15	
			1.8	3.3		2	15	
			1.8	5.0		2	15	
			2.5	3.3		2	15	
		$t_{PHL}$	1.8	1.8		5	15	
			1.8	2.5		5	15	
			1.8	3.3		5	15	
			1.8	5.0		6	15	
			2.5	3.3		4	15	
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PZL}$	Output Enable and Disable Time	1.8	1.8		60	80	ns	
		1.8	5.0		150	200		
$t_{OSLH}$ $t_{OSHl}$	Channel to channel Skew Time (6)(7)	1.8	1.8		0.1	1	ns	
		1.8	5.0		0.5	1		
DR	Maximum Data Rate	1.8 to 5.0	$V_L$ to 5.0	13			Mbps	

1. For normal operation, ensure  $V_L < (V_{CC} + 0.3V)$ . During power-up,  $V_L > (V_{CC} + 0.3V)$  will not damage the device
2. For  $V_{CC} = V_L = 1.8V$ ,  $t_r = t_f \leq 4\text{ns}$
3. Power Supply Range:  $V_L, V_{CC} 1.8V \pm 5\%$ ,  $2.5 \pm 0.2V$ ,  $3.3 \pm 0.3V$ ,  $5.0 \pm 0.5V$ .
4. Typical values are referred to  $T_A=25^\circ\text{C}$  Typical values are referred to  $T_A=25^\circ\text{C}$
5. Rise Time: 10% to 90%, Fall Time 90% to 10%
6. tpd: 50% to 50%
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHl} = |t_{PHLm} - t_{PHLn}|$ )
8. Each translator equally loaded; parameter guaranteed by design

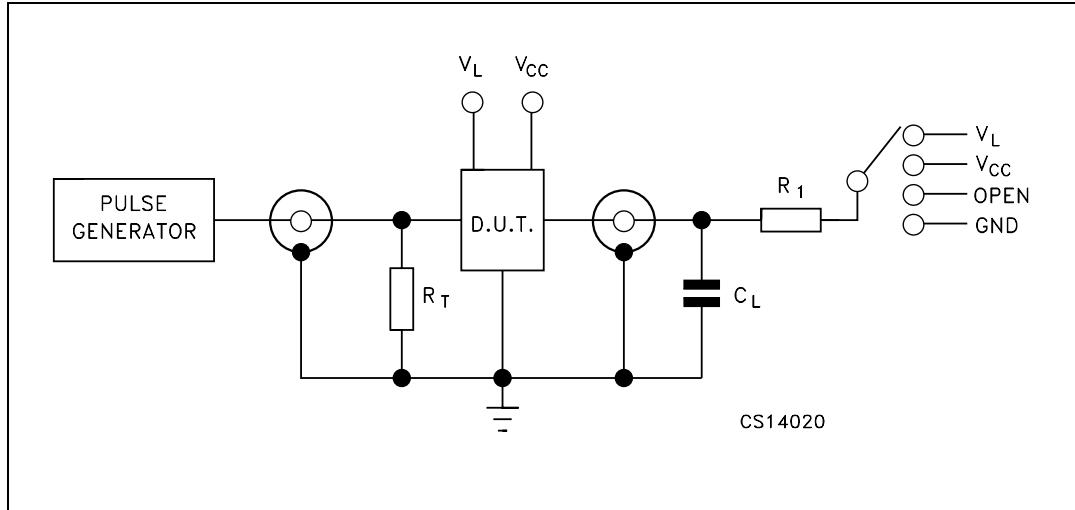
**Table 6. AC characteristic (open drain driving)**

Symbol	Parameter	Test Condition <sup>(1)</sup>		Value			Unit	
		$C_L = 15\text{pF}$ $t_r = t_f \leq 6\text{ns}$ Driver output $R_T \leq 50\Omega$ <sup>(2)</sup>		-40 to +85 °C				
		$V_L$ (V) <sup>(3)</sup>	$V_{CC}$ (V) <sup>(3)</sup>	Min.	Typ. <sup>(4)</sup>	Max.		
$t_{RVCC}$	Rise Time I/O <sub>VCC</sub> <sup>(3)(8)</sup>	1.8	1.8		210	300	ns	
		1.8	5.0		59	150		
$t_{FCC}$	Fall Time I/O <sub>VCC</sub> <sup>(3)(8)</sup>	1.8	1.8		12	30	ns	
		1.8	5.0		20	30		
$t_{RVL}$	Rise Time I/O <sub>VL</sub> <sup>(3)(8)</sup>	1.8	1.8		210	300	ns	
		1.8	5.0		96	150		
$t_{FVL}$	Fall Time I/O <sub>VL</sub> <sup>(3)(8)</sup>	1.8	1.8		11	30	ns	
		1.8	5.0		11	30		
$t_{IOVL-VCC}$	Propagation Delay Time(4) I/O <sub>VL-LH</sub> to I/O <sub>VCC-LH</sub> I/O <sub>VL-HL</sub> to I/O <sub>VCC-HL</sub>	$t_{PLH}$	1.8	1.8		210	300	ns
			1.8	5.0		100	150	
		$t_{PHL}$	1.8	1.8		7	20	
			1.8	5.0		14	20	
$t_{IOVCC-VL}$	Propagation Delay Time(4) I/O <sub>VCC-LH</sub> to I/O <sub>VL-LH</sub> I/O <sub>VCC-HL</sub> to I/O <sub>VL-HL</sub>	$t_{PLH}$	1.8	1.8		210	300	ns
			1.8	5.0		57	150	
		$t_{PHL}$	1.8	1.8		7	20	
			1.8	5.0		8	20	
$t_{PZL} t_{PZH}$ $t_{PLZ} t_{PZL}$	Output Enable and Disable Time	1.8	1.8		60	80	ns	
		1.8	5.0		150	200		
$t_{OSLH}$ $t_{OSHl}$	Channel to channel Skew Time <sup>(6)(7)</sup>	1.8	1.8		10	20	ns	
		1.8	5.0		2	10		
DR	Maximum Data Rate	1.8 to 5.0	$V_L$ to 5.0	800			kbps	

1. For normal operation, ensure  $V_L < (V_{CC} + 0.3\text{V})$ . During power-up,  $V_L > (V_{CC} + 0.3\text{V})$  will not damage the device
2. For  $V_{CC} = V_L = 1.8\text{V}$ ,  $t_r = t_f \leq 4\text{ns}$
3. Power Supply Range:  $V_L, V_{CC} 1.8\text{V} \pm 5\%, 2.5 \pm 0.2\text{V}, 3.3 \pm 0.3\text{V}, 5.0 \pm 0.5\text{V}$ .
4. Typical values are referred to  $T_A=25^\circ\text{C}$
5. Rise Time:10% to 90%, Fall Time 90% to 10%
6. tpd: 50% to 50%
7. Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ( $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHl} = |t_{PHLm} - t_{PHLn}|$ )
8. Each translator equally loaded; parameter guaranteed by desig

## 5 Test circuit

**Figure 4. Test circuit**



**Table 7. Test circuit switches**

Test	Switch		
	Driving I/O $V_L$	Driving I/O $V_{CC}$	Open Drain Driving
$t_{PLH}, t_{PHL}$	Open	Open	Open
$t_{PZL}, t_{PLZ}$	$V_{CC}$	$V_L$	-
$t_{PZH}, t_{PHZ}$	Gnd	Gnd	-

Note:  $C_L = 15/50\text{pF}$  or equivalent (includes jig and probe capacitance)

$R_1 = 1\text{K}\Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Table 8. Truth table**

Control Pin	Bidirectional Input/Outputs	
	I/O $V_L$	I/O $V_{CC}$
H <sup>(1)</sup>	H <sup>(1)</sup>	H <sup>(2)</sup>
H <sup>(1)</sup>	L	L
L	Z	Z

1. High Level  $V_L$  Power Supply referred

2. High Level  $V_{CC}$  Power Supply referred

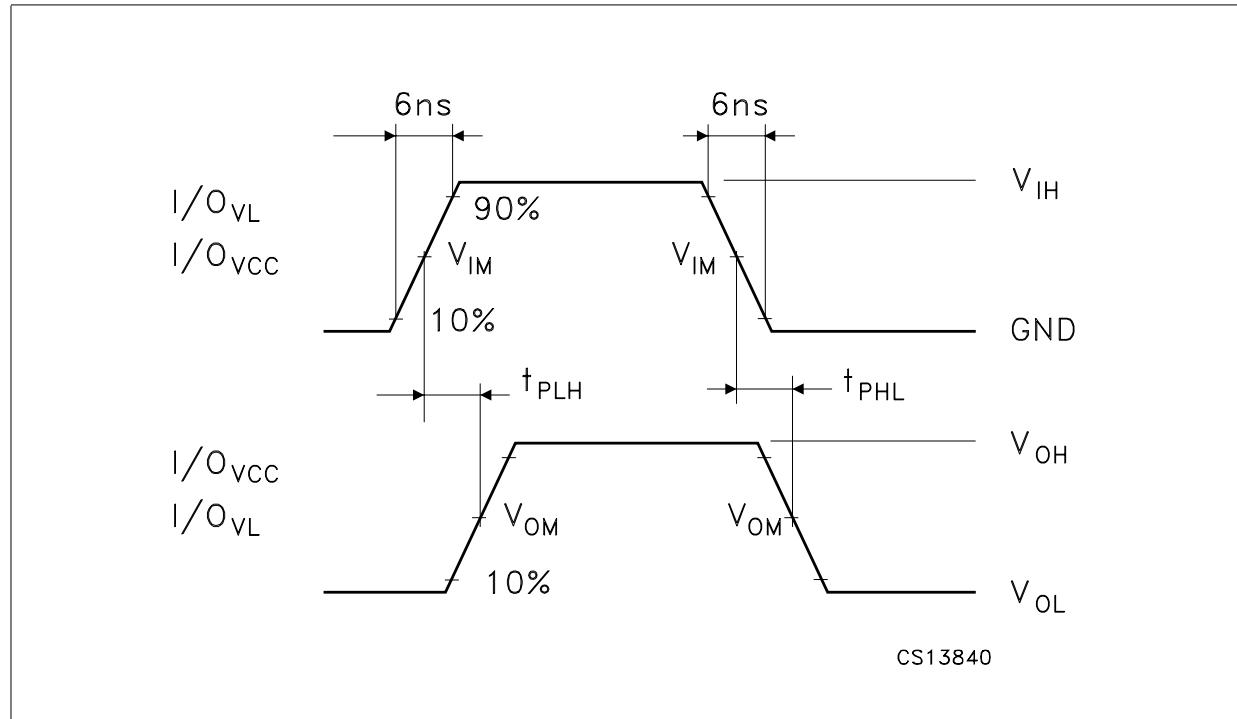
Note: X= Do not care; Z = High Impedance;

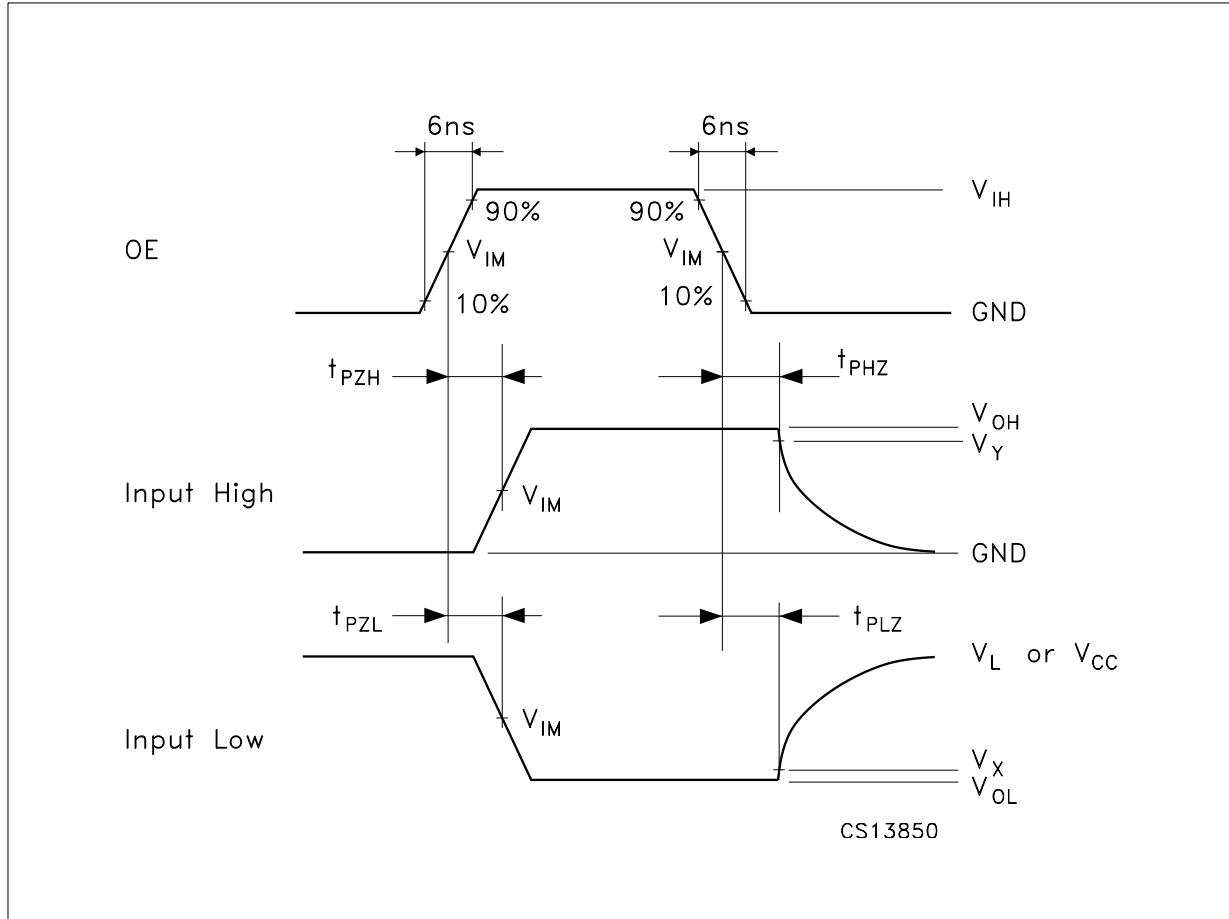
## 6 Waveforms

**Table 9. Waveform symbol value**

Symbol	Driving I/O <sub>VL</sub>		Driving I/O <sub>VCC</sub>	
	$1.8V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.0V$	$1.8V \leq V_L \leq V_{CC} \leq 2.5V$	$3.3V \leq V_L \leq V_{CC} \leq 5.0V$
$V_{IH}$	$V_L$	$V_L$	$V_{CC}$	$V_{CC}$
$V_{IM}$	$50\% V_L$	$50\% V_L$	$50\% V_{CC}$	$50\% V_{CC}$
$V_{OM}$	$50\% V_{CC}$	$50\% V_{CC}$	$50\% V_{CC}$	$50\% V_{CC}$
$V_X$	$V_{OL} + 0.15V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$	$V_{OL} + 0.3V$
$V_Y$	$V_{OH} - 0.15V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$	$V_{OH} - 0.3V$

**Figure 5. Waveform - propagation delay ( $f = 1MHz$ ; 50% duty cycle)**



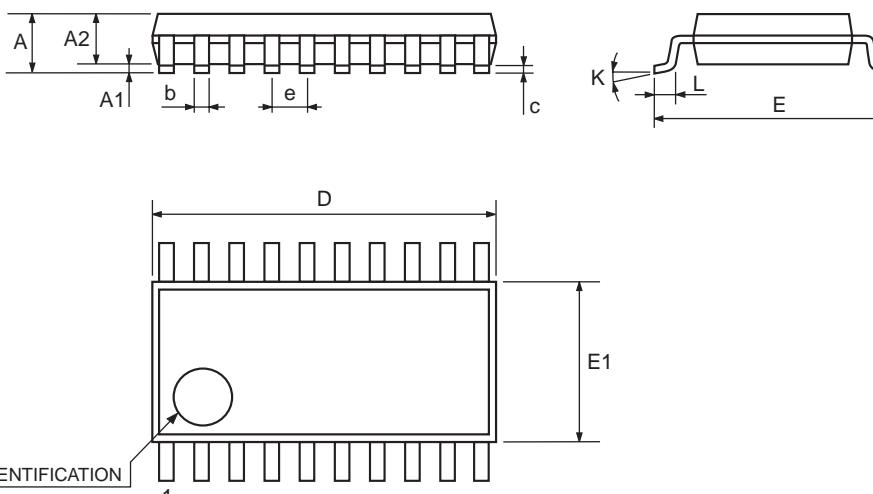
**Figure 6. Waveform - output enable and disable time ( $f = 1\text{MHz}$ ; 50% duty cycle)**

## 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Figure 7. TSSOP20 Mechanical data

TSSOP20 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

The diagram illustrates the physical dimensions of the TSSOP20 package. The top view shows the footprint with pins, and the side cross-sections show the lead profile. Key dimensions are labeled: A (total height), A1 (lead thickness), A2 (lead spacing), b (lead width), c (lead pitch), D (total width), E (total length), E1 (body length), K (lead angle), L (lead pitch), and the location of PIN 1 IDENTIFICATION.

0087225C

Figure 8. Flip-Chip20 Mechanical data

Flip-Chip20 MECHANICAL DATA						
DIM.	mm.			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.81	0.89	1.00	31.9	35.0	39.4
A1	0.15	0.24	0.35	5.9	9.4	13.8
A2		0.65			25.6	
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.41	2.46	2.51	94.9	96.9	98.8
D1		2.00			78.7	
E	1.93	1.98	2.03	76.0	78.0	79.9
E1		1.5			59.1	
e		0.50			19.7	
SE		0.25			9.8	

The drawing illustrates the physical dimensions of the package. Top view dimensions include A (width), D (length), E (height), and various internal features like A1, A2, b, and SE. Bottom view shows the seating plane with coplanarity requirements (0.08 mm) and distinguish features. A note specifies a pitch of 0.20 mm for the pins.

7487339-D

Figure 9. TSSOP20 Tape and reel

Tape & Reel TSSOP20 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Note: Drawing not in scale

Figure 10. Flip-Chip20 Tape and reel

Tape & Reel Flip-Chip20 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	2.13	2.23	2.33	0.084	0.088	0.092
Bo	2.62	2.72	2.82	0.103	0.107	0.111
Ko	1.05	1.15	1.25	0.041	0.045	0.049
Po	3.9		4.1	0.153		0.161
P	3.9		4.1	0.153		0.161

The drawing illustrates the physical dimensions of the tape and reel. The top view shows a circular reel with a central hole of diameter D and a total width A. The side view shows the height of the reel body as C, the thickness of the tape as T, and the overall height as N. The bottom view shows the tape wound onto the reel, with labels for Bo (width of the tape), Ko (width of the tape at the edge), Po (pitch of the tape), and P (width of the tape). A note at the bottom right states "Note: Drawing not in scale".

Note: Drawing not in scale

## 8 Revision history

**Table 10. Revision history**

Date	Revision	Changes
10-Apr-2006	1	Initial release.

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