ST2189

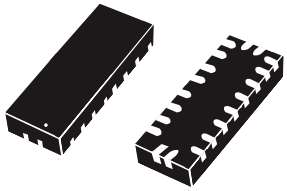
8-bit dual supply level translator without direction control pin

Features

- 46 MHz: 92 Mbps data transfer when V_{CCA} = 3.6 V
- Bidirectional level translation without direction control pin
- Wide voltage range of 1.65 V to 3.6 V for both V_{CCA} and V_{CCB}
- Configurable voltage translation:
  - V_{CCA} can be ≥ V_{CCB} or V_{CCA} can be ≤V_{CCB}
- Partial power down support - when V_{CCB} is grounded, all the outputs will automatically go to high impedance.
- Low quiescent current (5 µA)
- ESD performance:
  - ±4 kV HBM (human body model)

Applications

- Low voltage system level translation
- Mobile phones
- Other mobile devices



QFN20
(1.8 x 3.2 mm)

Description

The ST2189 is an 8-bit dual supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CCB} and V_{CCA}, set the logic levels on either side of the device. Its architecture allows bidirectional level translation without a control pin.

The ST2189 accepts V_{CCA} from 1.65 V to 3.6 V and V_{CCB} from 1.65 V to 3.6 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all I/Os.

In power down mode feature - when V_{CCB} supply is grounded, all I/Os go to high impedance automatically, with very low quiescent current on V_{CCA} supply.

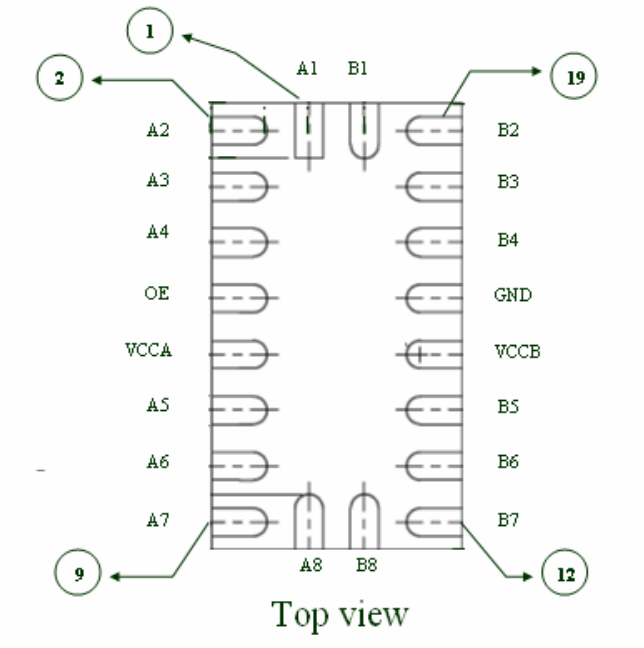
Table 1. Device summary

Order code	Package	Packing
ST2189QTR	QFN20 (3.2 x 1.8 mm)	Tape and reel

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection (top through view)



1.2 Pin description

Table 2. Pin description

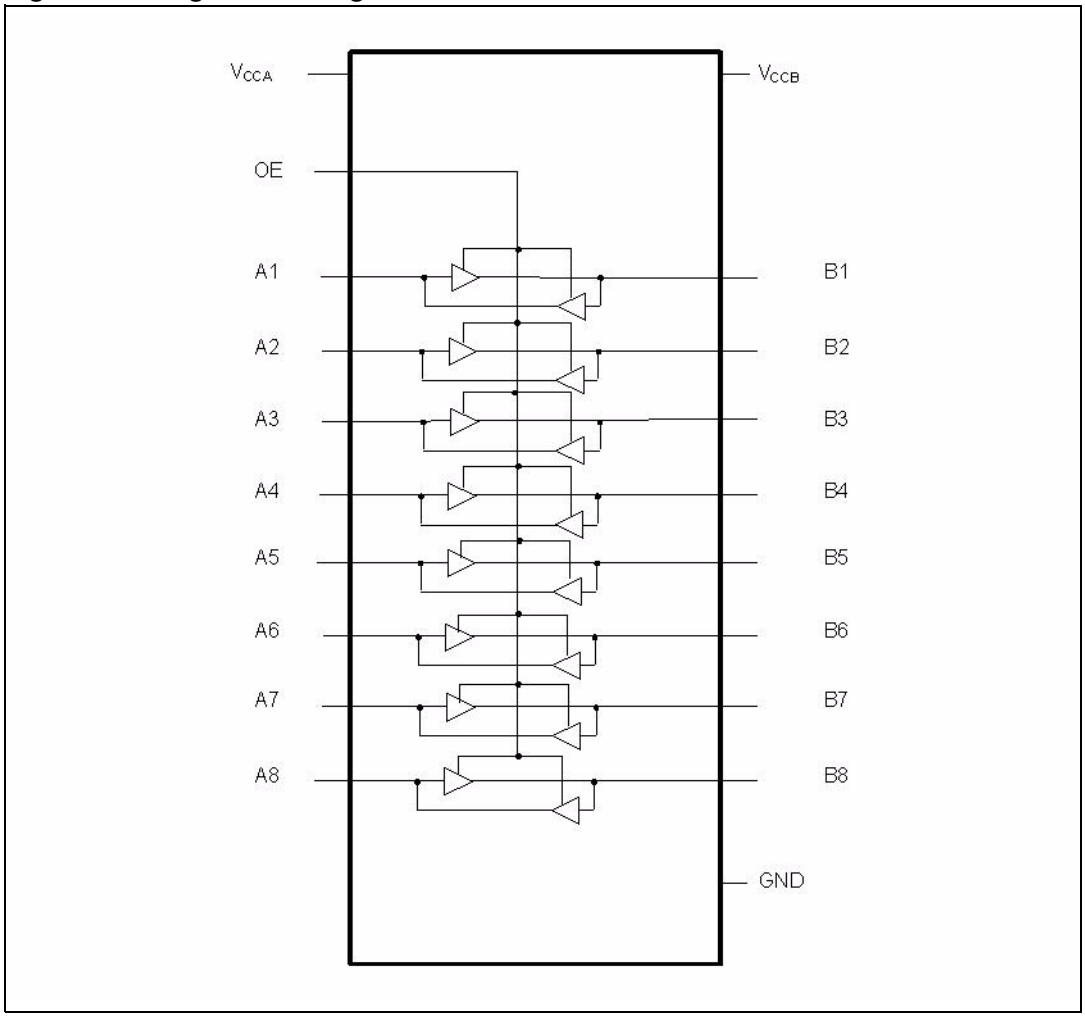
Pin number	Type	Side	Symbol	Name and function
1	I/O	V_{CCA}	A1	Input/output 1. Referenced to V_{CCA}
2	I/O	V_{CCA}	A2	Input/output 2. Referenced to V_{CCA}
3	I/O	V_{CCA}	A3	Input/output 3. Referenced to V_{CCA}
4	I/O	V_{CCA}	A4	Input/output 4. Referenced to V_{CCA}
5	-	V_{CCA}	OE	Output enabled. Pull OE low to put all output to tri-state mode. Referenced to V_{CCA}
6	-	V_{CCA}	V_{CCA}	A port supply voltage. $V_{CCA} \leq V_{CCB}$ or $V_{CCA} \geq V_{CCB}$
7	I/O	V_{CCA}	A5	Input/output 5. Referenced to V_{CCA}

Table 2. Pin description (continued)

Pin number	Type	Side	Symbol	Name and function
8	I/O	V_{CCA}	A6	Input/output 6. Referenced to V_{CCA}
9	I/O	V_{CCA}	A7	Input/output 7. Referenced to V_{CCA}
10	I/O	V_{CCA}	A8	Input/output 8. Referenced to V_{CCA}
11	I/O	V_{CCB}	B8	Input/output 8. Referenced to V_{CCB}
12	I/O	V_{CCB}	B7	Input/output 7. Referenced to V_{CCB}
13	I/O	V_{CCB}	B6	Input/output 6. Referenced to V_{CCB}
14	I/O	V_{CCB}	B5	Input/output 5. Referenced to V_{CCB}
15	-	V_{CCB}	V_{CCB}	B port supply voltage. $V_{CCB} \geq V_{CCA}$ or $V_{CCB} \leq V_{CCA}$
16	-	-	GND	Ground
17	I/O	V_{CCB}	B4	Input/output 4. Referenced to V_{CCB}
18	I/O	V_{CCB}	B3	Input/output 3. Referenced to V_{CCB}
19	I/O	V_{CCB}	B2	Input/output 2. Referenced to V_{CCB}
20	I/O	V_{CCB}	B1	Input/output 1. Referenced to V_{CCB}

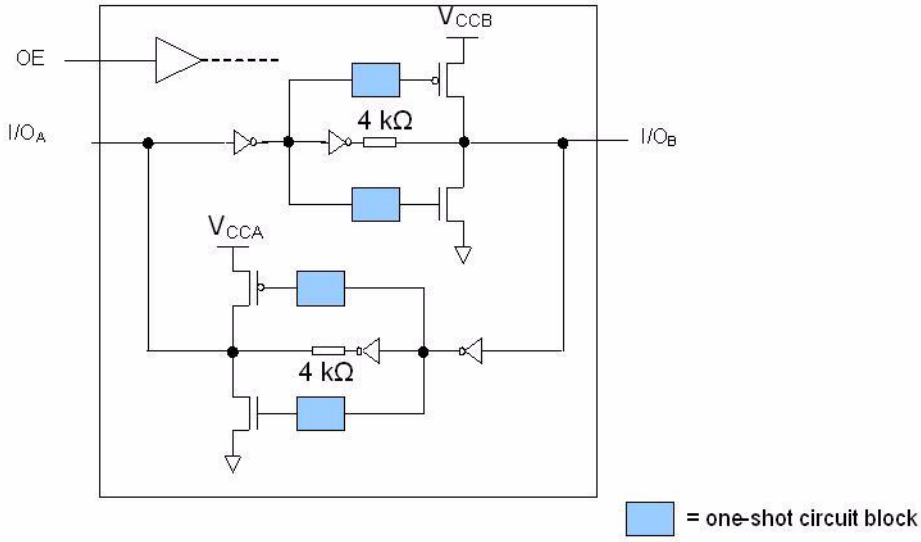
2 Logic diagram

Figure 2. Logic block diagram



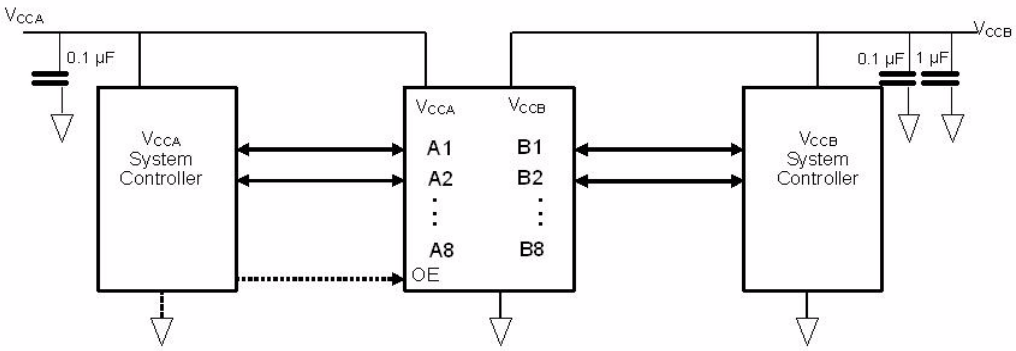
2.1 Device block diagram

Figure 3. ST2189 block diagram



* ST2189 has 8 channels. For simplicity, the above diagram shows only 1 channel.
* When OE is LOW, all I/Os are in high-impedance mode.

Figure 4. Application block diagram



3 Supplementary notes

3.1 Driver requirement

It must be ensured that the driver is able to source and sink a minimum of 1mA current on both sides of the device. The device requires the driver to source/sink a maximum current of (V_{CC}/4) mA to/from the weak 4 kΩ output buffer in order to change the state of the output.

3.2 Load driving capability

To support the level translation without direction pin architecture, the one-shot transistor at the output side is only turned ON during state transition. After the one-shot transistor is turned OFF, only the 4 kΩ pull-up/down resistor maintains the state of the output. As a result, resistive load or pull-up resistor less than 50 kΩ is not recommended.

3.3 Ensuring low current consumption during off state

The OE pin can be tied to the enable signal which is driving the enable pin of the slave device to ensure that the device will turn off and put all I/Os to tri-state mode whenever the slave device is not needed. On the event that the enable signal driving into the slave device is active low, the signal going into the OE pin for ST2189 (active high) needs to be inverted accordingly.

Alternatively, a pull-down resistor can be added to the V_{CCB} supply. This will ensure that the V_{CCB} supply does not float whenever the supply is turned off. All the I/Os go to high impedance automatically when this happens.

3.4 Truth table

Table 3. Truth table

Enable	Bidirectional Input/Output	
OE	I/O_{VCCB}	I/O_{VCCA}
H(1)	H(2)	H(1)
H(1)	L	L
L	High-Z(3)	High-Z(3)

1. High level V_{CCA} power supply referred.
2. High level V_{CCB} power supply referred.
3. Z = High impedance.

4 Maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CCA}	Supply voltage	-0.3 to 4.6	V
V_{CCB}	Supply voltage	-0.3 to 4.6	V
V_{OE}	DC control intput voltage	-0.3 to 4.6	V
$V_{I/OVCCA}$	DC I/O_{VCCA} input voltage (OE = GND or V_{CCA})	-0.3 to 4.6	V
$V_{I/OVCCB}$	DC I/O_{VCCB} input voltage (OE = GND or V_{CCA})	-0.3 to 4.6	V
I_{IK}	DC input diode current	-20	mA
$I_{I/OVCCA}$	DC output current	±25	mA
$I_{I/OVCCB}$	DC output current	±25	mA
T_{STG}	Storage temperature	-65 to 150	°C
T_L	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±4	kV

4.1 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Type	Max.	Unit
V_{CCA}	Supply voltage	1.65	-	3.6	V
V_{CCB}	Supply voltage	1.65	-	3.6	V
V_I	Input voltage (OE output enable pin,V_{CCA} power supply reference)	0	-	V_{CCA}	V
$V_{I/OVCCA}$	I/O_{VCCA} voltage	0	-	V_{CCA}	V
$V_{I/OVCCB}$	I/O_{VCCB} voltage	0	-	V_{CCB}	V
T_{OP}	Operating temperature	-40	-	85	°C
dt/dV	Input rise and fall time	-	-	1	ns/V

5 Electrical characteristics

Device electrical characteristics over recommended operating conditions (unless otherwise noted). All typical values are at T_A = 25 °C.

Table 6. DC characteristics

Symbol	Parameter	V_{CCA}	V_{CCB}	Test condition	Value				Unit
					T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V_{IHA}	High level input voltage (I/O_{VCCA})	1.65	1.65 to 3.6		1.2	-	1.2	-	V
		1.8			1.3	-	1.3	-	
		2.5			1.65	-	1.65	-	
		3.0			2.1	-	2.1	-	
		3.6			2.6	-	2.6	-	
V_{ILA}	Low level input voltage (I/O_{VCCA})	1.65	1.65 to 3.6		-	0.3	-	0.3	V
		1.8			-	0.4	-	0.4	
		2.5			-	0.55	-	0.55	
		3.0			-	0.85	-	0.85	
		3.6			-	0.95	-	0.95	
V_{IHB}	High level input voltage (I/O_{VCCB})	1.65 to 3.6	1.65		1.2	-	1.2	-	V
			1.8		1.3	-	1.3	-	
			2.5		1.65	-	1.65	-	
			3.0		2.1	-	2.1	-	
			3.6		2.6	-	2.6	-	
V_{ILB}	Low level input voltage (I/O_{VCCB})	1.65 to 3.6	1.65		-	0.3	-	0.3	V
			1.8		-	0.4	-	0.4	
			2.5		-	0.55	-	0.55	
			3.0		-	0.85	-	0.85	
			3.6		-	0.95	-	0.95	
V_{IH-OE}	High level input voltage (OE)	1.65	1.65 to 3.6		1.2	-	1.2	-	V
		1.8			1.3	-	1.3	-	
		2.5			1.4	-	1.4	-	
		3.0			1.65	-	1.65	-	
		3.6			2.1	-	2.1	-	

Table 6. DC characteristics (continued)

Symbol	Parameter	V_{CCA}	V_{CCB}	Test condition	Value				Unit
					T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
V_{IL-OE}	Low level input voltage (OE)	1.65	1.65 to 3.6		-	0.3	-	0.3	V
		1.8			-	0.4	-	0.4	
		2.5			-	0.55	-	0.55	
		3.0			-	0.85	-	0.85	
		3.6			-	0.95	-	0.95	
V_{OHA}	High level output voltage (I/O_{VCCA})	1.65 to 3.6	1.65 to 3.6	IO= -60 µA	0.7 V_{CCA}	-	0.7 V_{CCA}	-	V
V_{OLA}	Low level output voltage (I/O_{VCCA})			IO= +60 µA	-	0.4	-	0.4	V
V_{OHB}	High level output voltage (I/O_{VCCB})	1.65 to 3.6	1.65 to 3.6	IO= -60 µA	0.7 V_{CCB}	-	0.7 V_{CCB}	-	V
V_{OLB}	Low level output voltage (I/O_{VCCB})			IO= + 60 µA	-	0.4	-	0.4	V
I_{OE}	Control input leakage current (OE)	1.65 to 3.6	1.65 to 3.6	V_I = GND or V_{CCA}	-	0.2	-	2	µA
I_{IO_LKG}	High impedance I/O leakage current (I/O_{VCCA}, I/O_{VCCB})	1.65 to 3.6	1.65 to 3.6	OE = GND; I/O_{VCCA} = High I/O_{VCCB} = Low	-	0.2	-	2	µA
				OE = GND I/O_{VCCA} = Low, I/O_{VCCB} = High	-	0.2	-	2	µA
I_{QVCCB}	Quiescent supply current V_{CCB}	1.65 to 3.6	1.65 to 3.6	OE = V_{CCA} I/O = Hi-Z	-	0.5	-	5	µA
I_{QVCCA}	Quiescent supply current V_{CCA}	1.65 to 3.6	1.65 to 3.6	OE = V_{CCA} I/O = Hi-Z	-	5	-	7	µA
		1.65 to 3.6	0		-	0.3	-	3	
$I_{OE-VCCB}$	High impedance quiescent supply current V_{CCB}	1.65 to 3.6	1.65 to 3.6	OE = GND I/O = Hi-Z	-	0.5	-	5	µA

Table 6. DC characteristics (continued)

Symbol	Parameter	V_{CCA}	V_{CCB}	Test condition	Value				Unit
					T_A = 25 °C		-40 to 85 °C		
					Min	Max	Min	Max	
$I_{OE-VCCA}$	High impedance quiescent supply current V_{CCA}	1.65 to 3.6	1.65 to 3.6	OE = GND I/O = Hi-Z	-	0.5	-	5	µA
		1.65 to 3.6	0		-	0.3	-	3	

5.1 AC characteristics

Table 7. For test conditions: V_{CCA} = 1.65 V (load C_L= 15 pF; driver tr = $t_f \leq$ 2 ns) overtemperature range -40 °C to 85 °C

Symbol	Parameter		V_{CCB} = 1.65 V - 2.5 V		V_{CCB} = 2.7V - 3.6 V		Unit
			Min	Max	Min	Max	
t_{RVCCB}	Output rise time I/O_{VCCB}		-	2.7	-	1.6	ns
t_{FVCCB}	Output fall time I/O_{VCCB}		-	1.8	-	1.2	ns
t_{RVCCA}	Output rise time I/O_{VCCA}		-	3.0	-	3.0	ns
t_{FVCCA}	Output fall time I/O_{VCCA}		-	1.8	-	1.6	ns
$t_{I/OVCCA-VCCB}$	Propagation delay time $I/O_{VCCA-LH}$ to $I/O_{VCCB-LH}$	t_{PLH}	-	5.9	-	4.5	ns
	$I/O_{VCCA-HL}$ to $I/O_{VCCB-HL}$	t_{PHL}	-	4.0	-	4.0	ns
$t_{I/OVCCB-VCCA}$	Propagation delay time $I/O_{VCCB-LH}$ to $I/O_{VCCA-LH}$	t_{PLH}	-	6.2	-	5.8	ns
	$I/O_{VCCB-HL}$ to $I/O_{VCCA-HL}$	t_{PHL}	-	4.3	-	3.7	ns
t_{PZL} t_{PZH}	Output enable time		-	20	-	20	ns
t_{PLZ} t_{PHZ}	Output disable time		-	160	-	180	ns
D_R	Data rate(1)	Clock	28	-	32	-	MHz
		Data	56	-	64	-	Mbps

1. Data rates are measured at worst case condition when all 8 channels are switching at the same time. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than 50% ± 10%.

Table 8. For test conditions: V_{CCA} = 2.5 V (load C_L= 15 pF; driver $t_r = t_f \leq 2$ ns) overtemperature range -40 °C to 85 °C

Symbol	Parameter		V_{CCB} = 1.65V - 2.5 V		V_{CCB} = 2.7V - 3.6 V		Unit
			Min	Max	Min	Max	
t_{RVCCB}	Output rise time I/O_{VCCB}		-	2.5	-	1.4	ns
t_{FVCCB}	Output fall time I/O_{VCCB}		-	1.6	-	1.2	ns
t_{RVCCA}	Output rise time I/O_{VCCA}		-	2.1	-	2.0	ns
t_{FVCCA}	Output fall time I/O_{VCCA}		-	1.4	-	1.4	ns
$t_{I/OVCCA-VCCB}$	Propagation delay time $I/O_{VCCA-LH}$ to $I/O_{VCCB-LH}$ $I/O_{VCCA-HL}$ to $I/O_{VCCB-HL}$	t_{PLH}	-	4.7	-	3.3	ns
		t_{PHL}	-	2.9	-	2.6	ns
$t_{I/OVCCB-VCCA}$	Propagation delay time $I/O_{VCCB-LH}$ to $I/O_{VCCA-LH}$ $I/O_{VCCB-HL}$ to $I/O_{VCCA-HL}$	t_{PLH}	-	4.3	-	3.8	ns
		t_{PHL}	-	3.3	-	2.8	ns
t_{PZL} t_{PZH}	Output enable time		-	25	-	12	ns
t_{PLZ} t_{PHZ}	Output disable time		-	150	-	180	ns
D_R	Data rate(1)	Clock	40	-	42	-	MHz
		Data	80	-	84	-	Mbps

1. Data rates are measured at worst case condition when all 8 channels are switching at the same time. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than 50% ± 10%.

Table 9. For test conditions: V_{CCA} = 3.6 V (load C_L= 15 pF; driver $t_r = t_f \leq 2$ ns) overtemperature range -40 °C to 85 °C

Symbol	Parameter		V_{CCB} = 1.65 V - 2.5 V		V_{CCB} = 2.7 V - 3.6 V		Unit
			Min	Max	Min	Max	
t_{RVCCB}	Output rise time I/O_{VCCB}		-	2.5	-	1.4	ns
t_{FVCCB}	Output fall time I/O_{VCCB}		-	1.5	-	1.2	ns
t_{RVCCA}	Output rise time I/O_{VCCA}		-	1.7	-	1.7	ns
t_{FVCCA}	Output fall time I/O_{VCCA}		-	1.4	-	1.4	ns
$t_{I/OVCCA-VCCB}$	Propagation delay time $I/O_{VCCA-LH}$ to $I/O_{VCCB-LH}$ $I/O_{VCCA-HL}$ to $I/O_{VCCB-HL}$	t_{PLH}	-	4.4	-	3.0	ns
		t_{PHL}	-	2.6	-	2.2	ns
$t_{I/OVCCB-VCCA}$	Propagation delay time $I/O_{VCCB-LH}$ to $I/O_{VCCA-LH}$ $I/O_{VCCB-HL}$ to $I/O_{VCCA-HL}$	t_{PLH}	-	3.8	-	3.0	ns
		t_{PHL}	-	3.0	-	2.3	ns
t_{PZL} t_{PZH}	Output enable time		-	20	-	10	ns
t_{PLZ} t_{PHZ}	Output disable time		-	150	-	160	ns
D_R	Data rate(1)	Clock	43	-	46	-	MHz
		Data	86	-	92	-	Mbps

1. Data rates are measured at worst case condition when all 8 channels are switching at the same time. Data rate is guaranteed based on the condition that output I/O signal rise/fall time is less than 15% of period of input I/O signal; input I/O signal is at 50% duty-cycle and output I/O signal duty-cycle deviation is less than 50% ± 10%.

5.2 Capacitance characteristics

Table 10. Capacitance characteristics

Symbol	Parameter	Value							Unit
		V_{CCA}(V)	V_{CCB}(V)	T_A = 25 °C			-40 to 85 °C		
				Min	Typ	Max	Min	Max	
C_{INB}	Input capacitance	Open	Open	-	12	-	-	-	pF
$C_{I/O-VCCA}$	Input/output capacitance for V_{CCA}-side	1.65 - 3.6	1.65 - 3.6	-	12	-	-	-	pF
$C_{I/O-VCCB}$	Input/output capacitance for V_{CCB}-side	1.65 - 3.6	1.65 - 3.6	-	12	-	-	-	pF

6 Test circuit

Figure 5. Test circuit

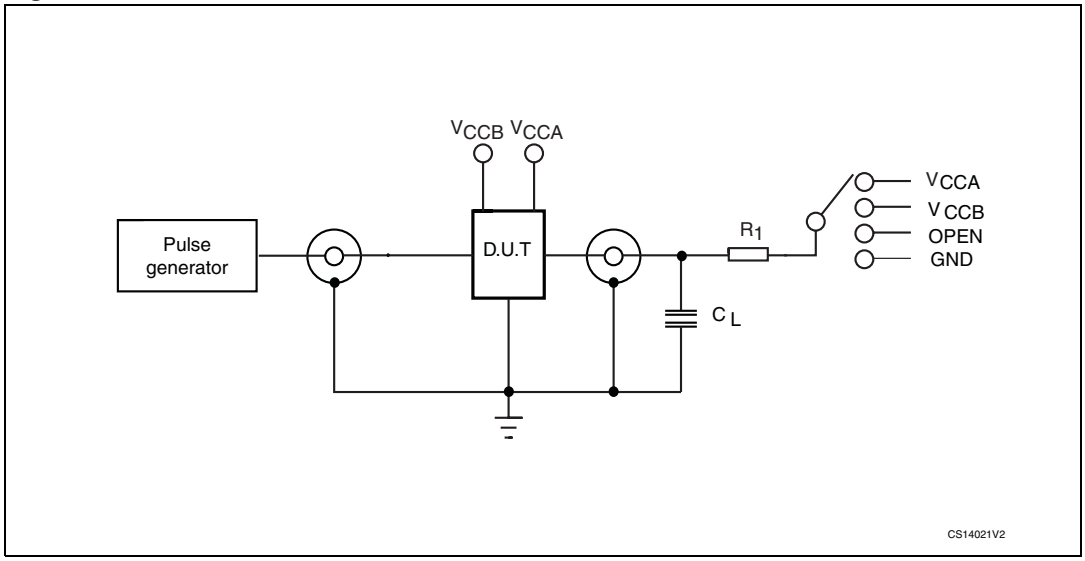


Table 11. Test circuit switches

Test	C_L	R_1	Switch
t_{PLH}, t_{PHL}	15 pF	20 kΩ	Open
t_r, t_f	15 pF	20 kΩ	Open
t_{PZL}, t_{PLZ}	15 pF	20 kΩ	V_{CCA} or V_{CCB}
t_{PZH}, t_{PHZ}	15 pF	20 kΩ	GND

7 Waveforms

Table 12. Waveform symbol value

Symbol	I/O_{VCCA} -> I/O_{VCCB}		I/O_{VCCB} -> I/O_{VCCA}	
	V_{CCB} 1.65 V - 2.5V	V_{CCB} 2.7 V - 3.6 V	V_{CCA} 1.65 V - 2.5 V	V_{CCA} 2.7 V - 3.6 V
V_{IH}	V_{CCA}	V_{CCA}	V_{CCB}	V_{CCB}
V_{IM}	50% V_{CCA}	50% V_{CCA}	50% V_{CCB}	50% V_{CCB}
V_{OM}	50% V_{CCB}	50% V_{CCB}	50% V_{CCA}	50% V_{CCA}
V_X	V_{OL} + 0.15V	V_{OL} + 0.3V	V_{OL} + 0.15V	V_{OL} + 0.3V
V_Y	V_{OH} - 0.15V	V_{OH} - 0.3V	V_{OH} - 0.15V	V_{OH} - 0.3V

Figure 6. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

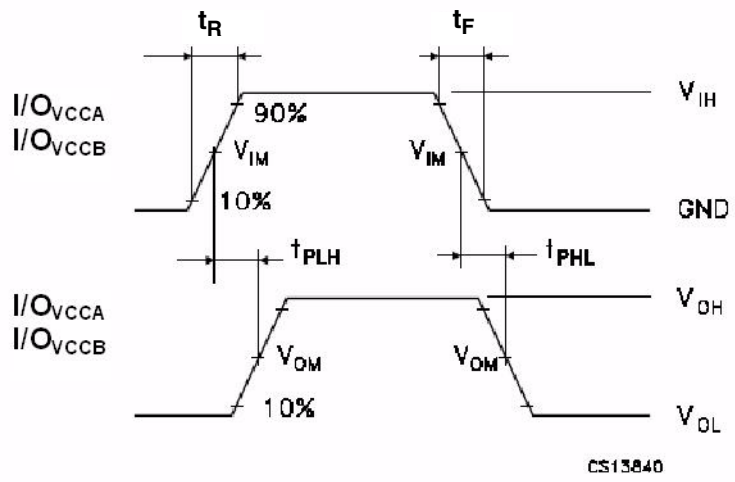
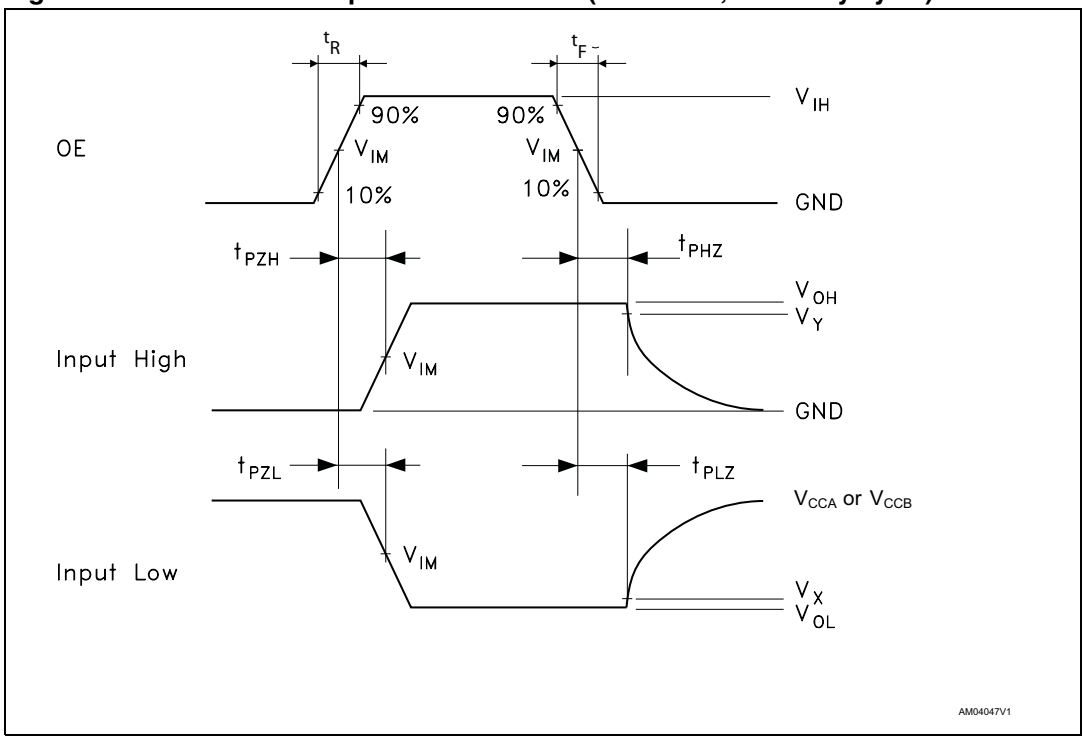


Figure 7. Waveform - output enable/disable (f = 50 kHz, 50% duty cycle)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 8. Package outline for QFN20 (1.8 x 3.2 x 0.5 mm) - pitch 0.4 mm

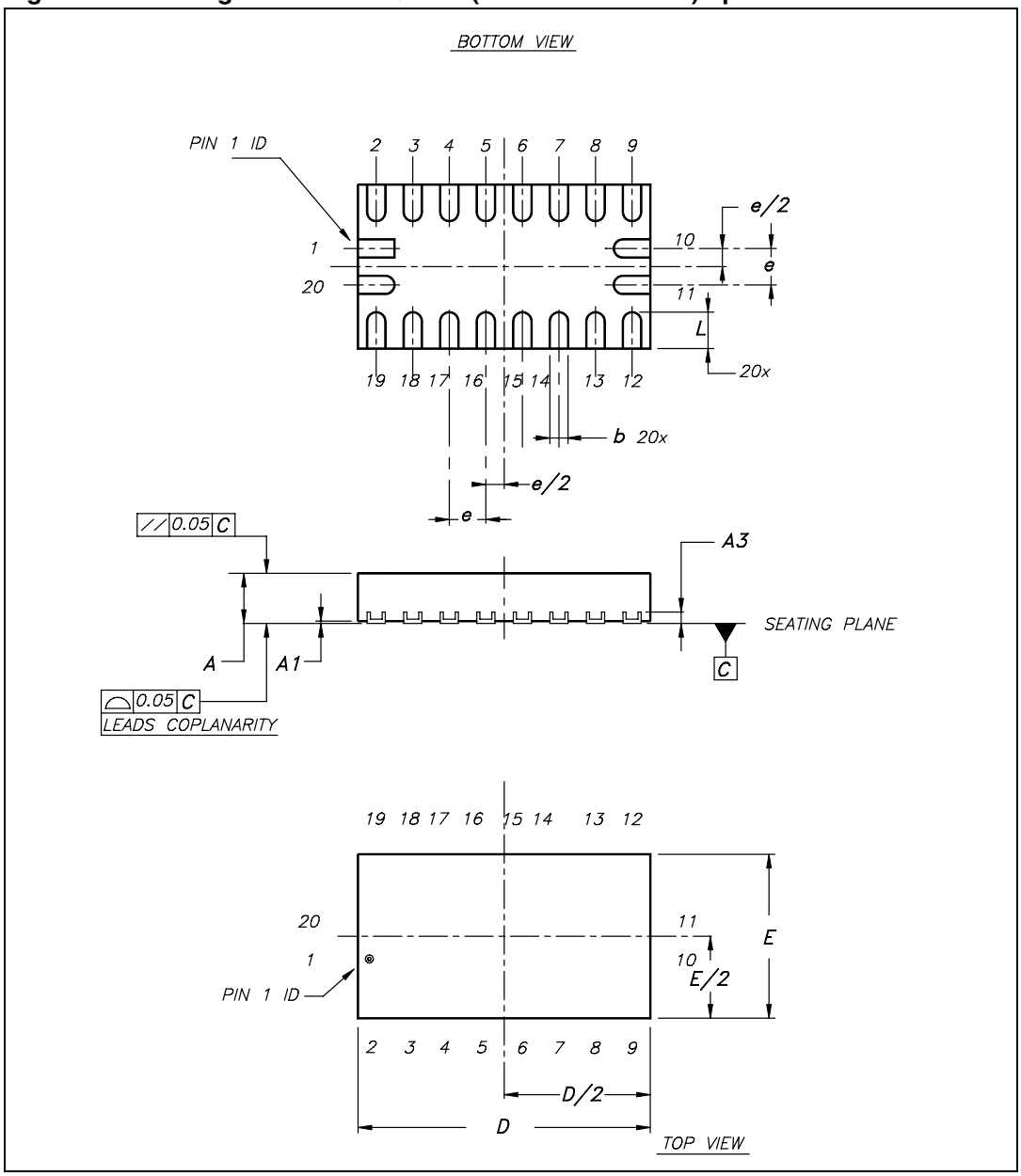


Table 13. Mechanical data for QFN20 (1.8 x 3.2 x 0.5 mm) - pitch 0.4 mm

Symbol	Milimeters		
	Nom	Min	Max
A	0.50	0.45	0.55
A1	0.02	0	0.05
A3	0.127	-	-
b	0.20	0.15	0.25
D	3.20	3.15	3.25
E	1.80	1.75	1.85
e	0.40	-	-
L	0.40	0.35	0.45

Figure 9. Footprint recommendation for QFN20 (1.8 x 3.2 x 0.5 mm) - pitch 0.4 mm

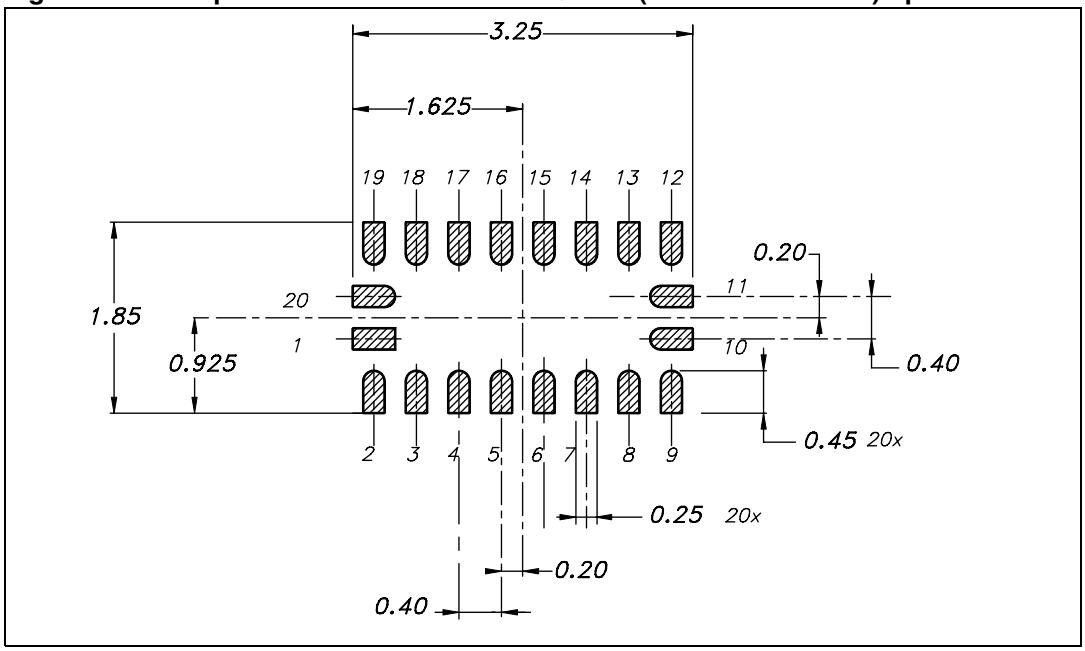
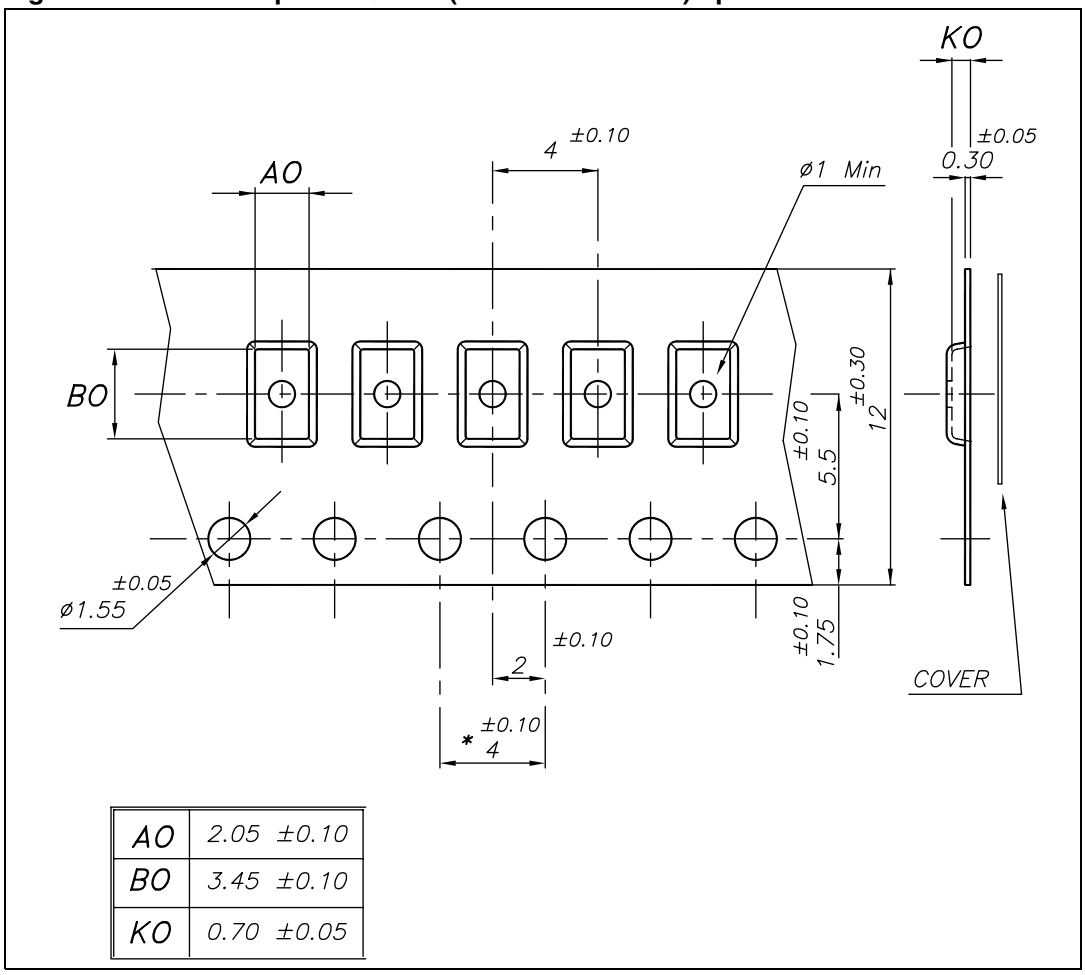
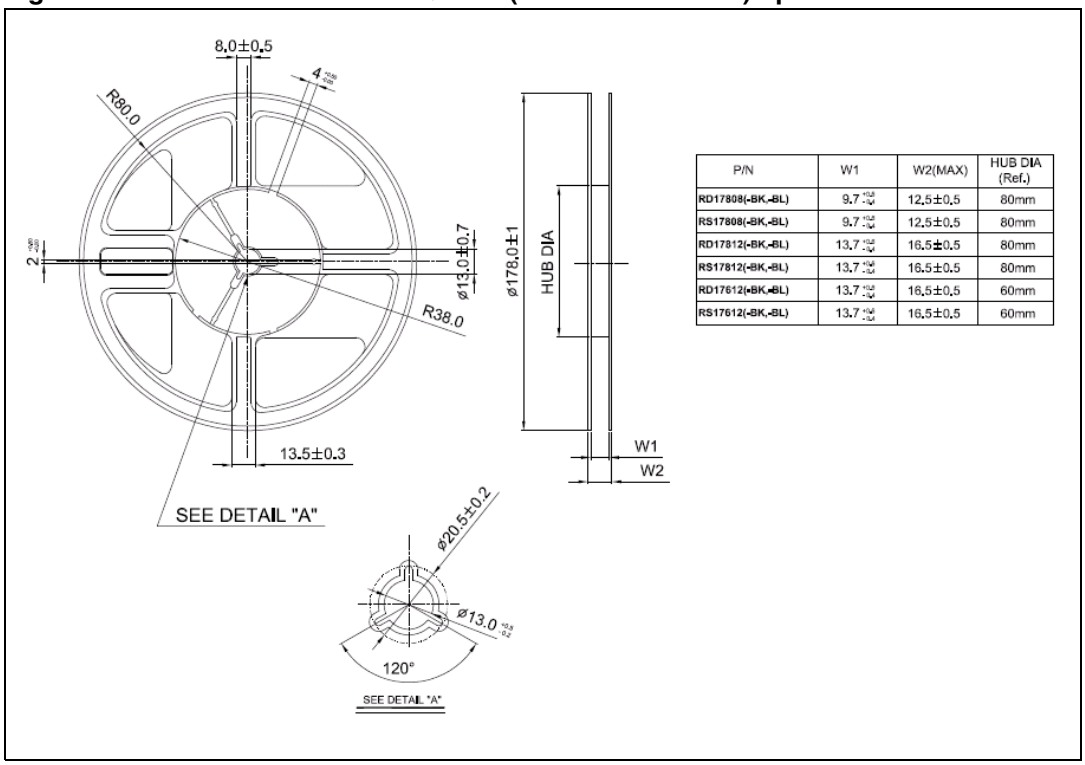


Figure 10. Carrier tape for QFN20 (1.8 x 3.2 x 0.5 mm) - pitch 0.4 mm



AO	2.05 ±0.10
BO	3.45 ±0.10
KO	0.70 ±0.05

Figure 11. Reel information for QFN20 (1.8 x 3.2 x 0.5 mm) - pitch 0.4 mm



P/N	W1	W2(MAX)	HUB DIA (Ref.)
RD17808(-BK,-BL)	9.7	12.5±0.5	80mm
RS17808(-BK,-BL)	9.7	12.5±0.5	80mm
RD17812(-BK,-BL)	13.7	16.5±0.5	80mm
RS17812(-BK,-BL)	13.7	16.5±0.5	80mm
RD17612(-BK,-BL)	13.7	16.5±0.5	60mm
RS17612(-BK,-BL)	13.7	16.5±0.5	60mm

9 Revision history

Table 14. Document revision history

Date	Rev	Changes
31-Jul-2009	1	Initial release.

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