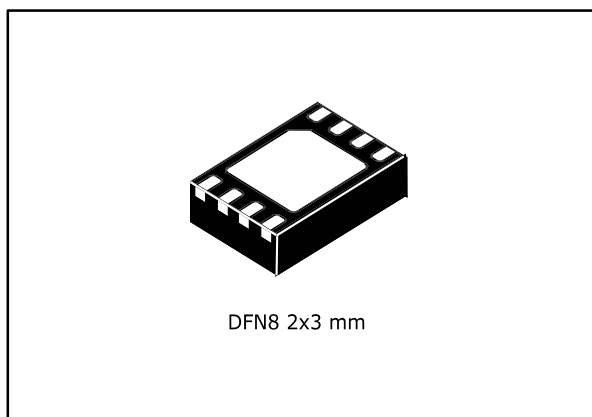


800 mA ultra low drop, high PSRR voltage regulator

Datasheet - production data



Applications

- Consumer
- Hard disk drives, SSD
- Computer
- Battery-powered systems
- Low voltage point of load

Description

The ST1L08 provides 0.8 A of maximum current from an input voltage in the range from 1 V to 5.5 V, with a typical dropout voltage as low as 70 mV.

It is stabilized with a ceramic capacitor on the output.

The very low drop voltage, low quiescent current and high PSRR features make it suitable for low power battery-powered applications.

Enable logic control function puts the ST1L08 in shutdown mode, reducing the total current consumption.

Power Good function and input voltage control feature the ST1L08Sxx version.

The device is equipped with current limit and thermal protection.

Features

- Input voltage from 1 to 5.5 V
- Ultra low-dropout voltage (90 mV max. @ 800 mA load)
- Low ground current (35 μ A typ. @ no load)
- Output voltage tolerance: $\pm 2.0\%$ @ 25 °C
- High PSRR: 80 dB @ 100 Hz, 50 dB @ 1 MHz
- 800 mA guaranteed output current
- Wide range of output voltages available on request: from 0.5 V to 4 V and adjustable
- Logic-controlled electronic shutdown
- Internal current and thermal limit
- Power Good function
- Available in DFN8 2x3 mm package
- Temperature range: -40 °C to 125 °C
- Input voltage control for the ST1L08Sxx

Table 1: Device summary

Order code	Power Good and VIN control	Package	Output voltages
ST1L08SPU12R	Yes	DFN8 (2x3 mm)	1.2 V
ST1L08SPU33R	Yes		3.3 V
ST1L08SPUR	Yes		Adjustable
ST1L08PUR	No		Adjustable

Contents

1	Diagram.....	3
2	Pin configuration.....	4
3	Typical application	5
4	Maximum ratings.....	6
5	Electrical characteristics	7
6	Application information	11
	6.1 Thermal and short-circuit protections	11
	6.2 Output voltage setting for ADJ version.....	11
	6.3 Bias pin voltage requirements.....	11
	6.4 External capacitors requirements.....	11
7	Typical characteristics.....	12
8	Package information	16
	8.1 DFN8 (2x3 mm) package information	16
	8.2 DFN8 (2x3 mm) packing information.....	18
9	Revision history	20

2 Pin configuration

Figure 2: Pin connection (top view)

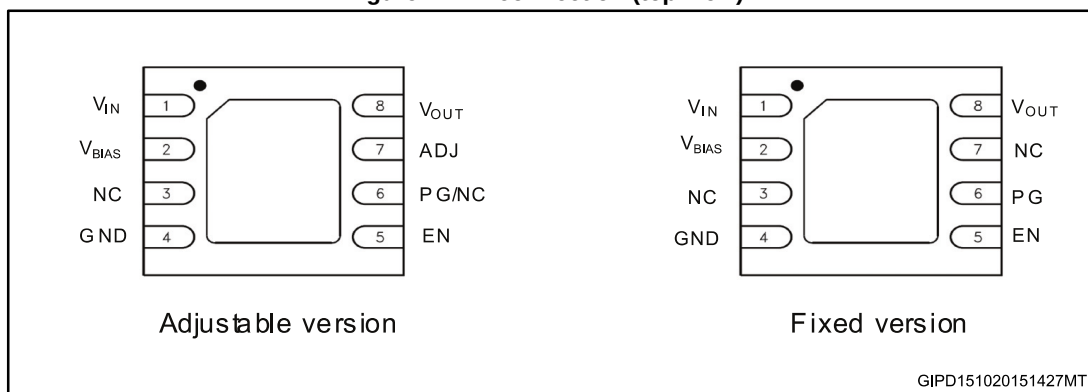
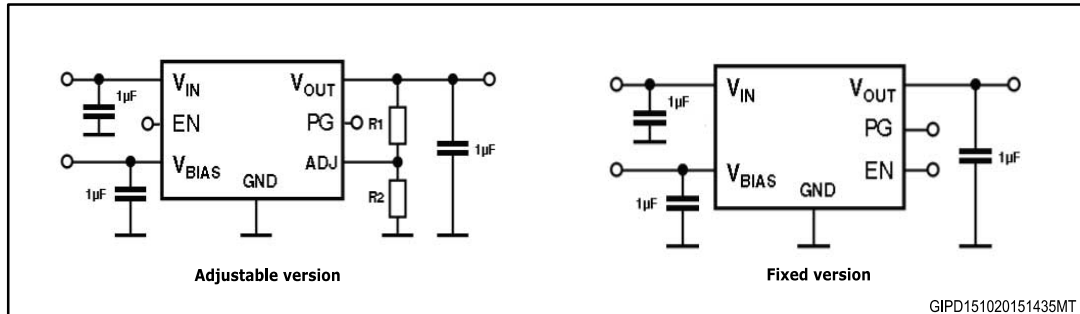


Table 2: Pin description

Symbol	Function
V_{IN}	Input voltage of the LDO (power element)
V_{BIAS}	Bias input of the LDO
GND	Common ground
EN	Enable pin logic input: low = shutdown, high = active
ADJ	Adjustable pin (on adjustable version)
V_{OUT}	Output voltage of the LDO
PG	Power Good pin (not connected on the ST1L08PUR)
NC	Not connected
EXP	Exposed pad (should be connected to GND)

3 Typical application

Figure 3: Typical application circuits



Power Good feature is not present on the ST1L08PUR.

4 Maximum ratings

Table 3: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	DC input voltage	- 0.3 to 7	V
V_{BIAS}	DC bias voltage	- 0.3 to 7	V
V_{OUT}	DC output voltage	- 0.3 to $V_I + 0.3$	V
V_{EN}	Enable input voltage	- 0.3 to $V_{BIAS} + 0.3$	V
V_{PG}	Power Good pin voltage	- 0.3 to $V_{BIAS} + 0.3$	V
V_{ADJ}	ADJ pin voltage	- 0.3 to $V_{BIAS} + 0.3$	V
I_{OUT}	Output current	Internally limited	mA
P_D	Power dissipation	Internally limited	mW
T_{STG}	Storage temperature range	- 65 to 150	°C
T_{OP}	Operating junction temperature range	- 40 to 125	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

Table 4: Thermal data

Symbol	Parameter	DFN8 (2x3 mm)	Unit
R_{thJA}	Thermal resistance junction-ambient	55	°C/W
R_{thJC}	Thermal resistance junction-case	12	°C/W

5 Electrical characteristics

$T_J = 25\text{ °C}$, $V_{IN} = 1.5\text{ V}$, $V_{BIAS} = 3.6\text{ V}$, $V_{OUT} = V_{ADJ}$, $C_{IN} = C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$,

$V_{EN} = V_{BIAS}$, unless otherwise specified.

Table 5: Electrical characteristics for the ST1L08 (adjustable)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1		5.5	V
V_{BIAS}	Operating bias voltage ⁽¹⁾		2.7		5.5	V
I_{IN}	V_{IN} operating current			0.2	10	μA
I_{BIAS}	V_{BIAS} operating current	$I_{OUT} = 10\text{ }\mu\text{A}$		40	150	μA
V_{ADJ}	V_{ADJ} accuracy	$I_{OUT} = 1\text{ mA to }800\text{ mA}$ $T_J = 25\text{ °C}$	0.490	0.500	0.510	V
		$-40\text{ °C} < T_J < 125\text{ °C}$ $V_{OUT} = 0.5\text{ V}$	0.487	0.500	0.512	
ΔV_{OUT}	V_{IN} static line regulation	$I_{OUT} = 1\text{ mA}$ $V_{OUT} = 0.5\text{ V}$ $V_{BIAS} = 3.6\text{ V}$ $1\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.002	0.01	%/V
	V_{BIAS} static line regulation	$I_{OUT} = 100\text{ mA}$ $V_{OUT} = 0.5\text{ V}$ $V_{IN} = 1.5\text{ V}$ $2.7\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$		0.04	0.2	%/V
ΔV_{OUT}	Static load regulation	$I_{OUT} = 1\text{ mA to }800\text{ mA}$		0.0002	0.001	%/mA
V_{DROP}	Dropout voltage	$I_{OUT} = 800\text{ mA}$ $V_{BIAS} = 3.6\text{ V}$		70	90	mV
		$40\text{ °C} < T_J < 125\text{ °C}$			120	
e_N	Output noise voltage	10 Hz to 100 kHz $I_{OUT} = 10\text{ mA}$		50		μV_{RMS}
SVR	Supply voltage rejection	$V_{IN} > V_{OUT} + 0.5\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.1\text{ V}$ $f = 100\text{ Hz}$		80		dB
		$f = 10\text{ kHz}$		60		
		$f = 1\text{ MHz}$		50		

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{GND}	Ground current	I _{OUT} = 0 mA T _J = 25 °C		35		
		I _{OUT} = 500 mA T _J = 25 °C		40		
		I _{OUT} = 800 mA 40 °C < T _J < 125 °C		40	150	μA
I _{SC}	Short-circuit current	R _L = 0		1.8		A
V _{EN}	Enable input logic low				0.8	
	Enable input logic high		1.3			V
I _{EN}	Enable pin input current	V _{EN} = 1.3 V			1	μA
PG ⁽²⁾	Power Good output threshold	Rising edge		0.92* V _{OUT}		V
		Falling edge		0.8* V _{OUT}		
	Power Good output voltage low	I _{sink} = 6 mA open drain output			0.4	V
T _{SHDN}	Thermal shutdown			165		
	Hysteresis			20		°C

Notes:

⁽¹⁾Important: in any case V_{BIAS} ≥ V_{OUT} + 1.5 V.

⁽²⁾Power Good feature is not available on the ST1L08PUR.

$T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = V_{OUT} + 0.5\text{ V}$, $V_{BIAS} = V_{OUT} + 1.5\text{ V}^a$, $C_{IN} = C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$,

$V_{EN} = V_{BIAS}$, unless otherwise specified.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage		1		5.5	V
V_{BIAS}	Operating bias voltage ⁽⁴⁾		2.7		5.5	V
V_{OUT}	Output voltage range		0.5		4	V
I_{IN}	V_{IN} operating current			4	10	μA
I_{BIAS}	V_{BIAS} operating current	$I_{OUT} = 10\text{ }\mu\text{A}$		45	150	μA
V_{OUT}	V_{OUT} accuracy	$I_{OUT} = 1\text{ mA to }800\text{ mA}$ $T_J = 25\text{ }^{\circ}\text{C}$	-2		2	
		$-40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$	-2.5		2.5	%
ΔV_{OUT}	V_{IN} static line regulation	$I_{OUT} = 1\text{ mA}$ $V_{BIAS} = V_{OUT} + 1.5\text{ V}$ $V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.003	0.015	%/V
	V_{BIAS} static line regulation	$I_{OUT} = 100\text{ mA}$ $V_{IN} = V_{OUT} + 0.5\text{ V}$ $V_{OUT} + 1.5\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$		0.04	0.2	%/V
ΔV_{OUT}	Static load regulation	$I_{OUT} = 1\text{ mA to }800\text{ mA}$		0.0005	0.0025	%/mA
V_{DROP}	Dropout voltage	$I_{OUT} = 800\text{ mA}$ $V_{BIAS} = 4.8\text{ V}$ $V_{OUT} = 3.3\text{ V}$		100		mV
		$40\text{ }^{\circ}\text{C} < T_J < 125\text{ }^{\circ}\text{C}$			150	
eN	Output noise voltage	10 Hz to 100 kHz $I_{OUT} = 10\text{ mA}$ $V_{OUT} = 3.3\text{ V}$		200		μV_{RMS}
SVR	Supply voltage rejection	$V_{IN} > V_{OUT} + 0.5\text{ V} \pm V_{RIPPLE}$ $V_{RIPPLE} = 0.1\text{ V}$ $f = 100\text{ Hz}$		70		dB
		$f = 10\text{ kHz}$		53		
		$f = 1\text{ MHz}$		30		
I_{GND}	Ground current	$I_{OUT} = 0\text{ mA}$ $T_J = 25\text{ }^{\circ}\text{C}$		40		μA
		$I_{OUT} = 500\text{ mA}$ $T_J = 25\text{ }^{\circ}\text{C}$		50		

^a Important: in any case $V_{BIAS} \geq V_{OUT} + 1.5\text{ V}$.

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		$I_{OUT} = 800 \text{ mA}$, $40 \text{ }^{\circ}\text{C} < T_J < 125 \text{ }^{\circ}\text{C}$		50	150	
I_{SC}	Short-circuit current	$R_L = 0$		1.8		A
V_{EN}	Enable input logic low				0.8	V
	Enable input logic high		1.3			
I_{EN}	Enable pin input current	$V_{EN} = 1.3 \text{ V}$			1	μA
PG	Power Good output threshold	Rising edge		0.92 * V_{OUT}		V
		Falling edge		0.8 * V_{OUT}		
	Power Good output voltage low	$I_{sink} = 6 \text{ mA}$ open drain output			0.4	V
T_{SHDN}	Thermal shutdown			165		$^{\circ}\text{C}$
	Hysteresis			20		

Notes:

⁽¹⁾Important: in any case $V_{BIAS} \geq V_{OUT} + 1.5 \text{ V}$.

6 Application information

6.1 Thermal and short-circuit protections

The ST1L08 is self-protected from short-circuit condition and overtemperature. When the output load is higher than the one supported by the device, the output current increases until the limit of typically 1.8 A is reached, at this point the current is kept constant even when the load impedance is zero.

Thermal protection acts when the junction temperature reaches 165 °C typical. At this point the output of the IC shuts down. As soon as the junction temperature falls below the thermal hysteresis value the device starts working again.

In order to calculate the maximum power that the device can dissipate, keeping the junction temperature below the TOP, the following formula is used:

Equation 1

$$P_{\text{DMAX}} = (125 - T_{\text{AMB}}) / R_{\text{THJA}}$$

6.2 Output voltage setting for ADJ version

In the adjustable version, the output voltage can be set from 0.5 V up to 4 V, by connecting a resistor divider between the ADJ pin and the output, thus allowing remote voltage sensing.

The resistor divider should be selected using the following equation:

Equation 2

$$V_{\text{OUT}} = V_{\text{ADJ}} (1 + R1 / R2), \text{ with } V_{\text{ADJ}} = 0.5 \text{ V (typ.)}$$

The resistors to be used, should have values in the range from 10 kΩ to 100 kΩ.

Lower values can also be suitable, but they increase current consumption.

6.3 Bias pin voltage requirements

The bias input is designed for low drop applications. The bias pin must be at least 2.7 V, and at least 1.5 V higher than the output, to ensure proper biasing to the N-channel power pass transistor.

If V_{IN} supply voltage meets these requirements, the bias pin can be tied to V_{IN} .

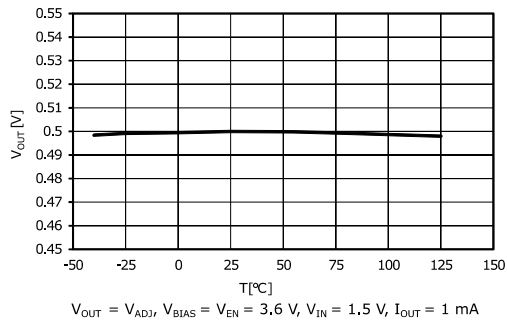
6.4 External capacitors requirements

The regulator is designed to be stable with ultra low ESR ceramic capacitors on the input and the output. The suggested minimum value of the input, bias and output capacitors is 1 μF. The input capacitor must be connected as closer as possible to the V_{IN} terminal. The output capacitor must also be connected as closer as possible to the output pin.

7 Typical characteristics

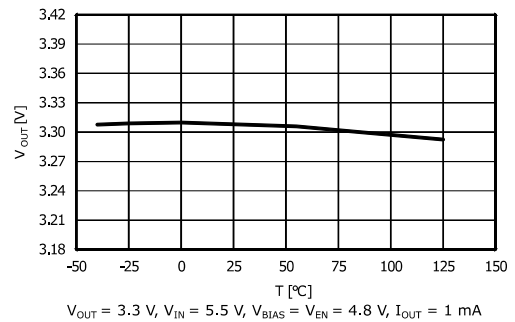
$T_J = 25\text{ }^{\circ}\text{C}$, $V_{IN} = 1.5\text{ V}$, $V_{BIAS} = 3.6\text{ V}$, $V_{OUT} = V_{ADJ}$, $C_{IN} = C_{BIAS} = 1\text{ }\mu\text{F}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $V_{EN} = V_{BIAS}$, unless otherwise specified.

Figure 4: Output voltage vs. temperature (adjustable, $I_{OUT} = 1\text{ mA}$)



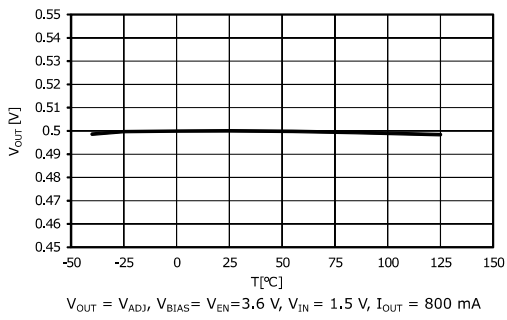
GIPG200620141502RV

Figure 5: Output voltage vs. temperature (fixed 3.3 V, $I_{OUT} = 1\text{ mA}$)



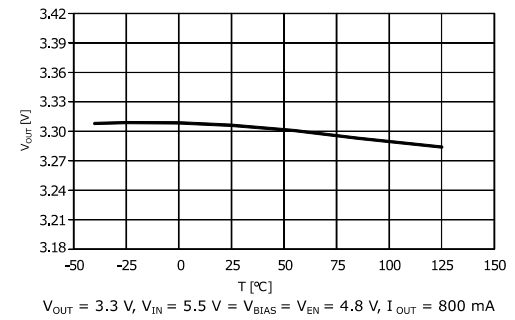
GIPG200620141539RV

Figure 6: Output voltage vs. temperature (adjustable, $I_{OUT} = 800\text{ mA}$)



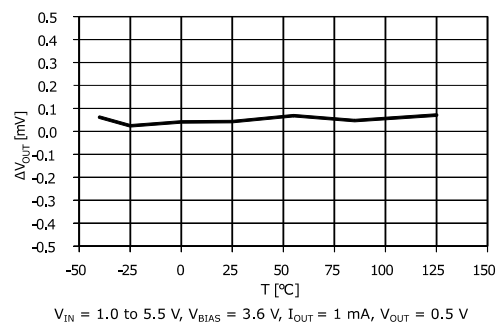
GIPG200620141526RV

Figure 7: Output voltage vs. temperature (fixed 3.3 V, $I_{OUT} = 800\text{ mA}$)



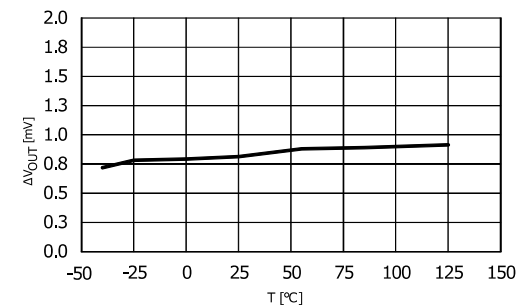
GIPG200620141548RV

Figure 8: V_{IN} line regulation vs. temperature (adjustable)

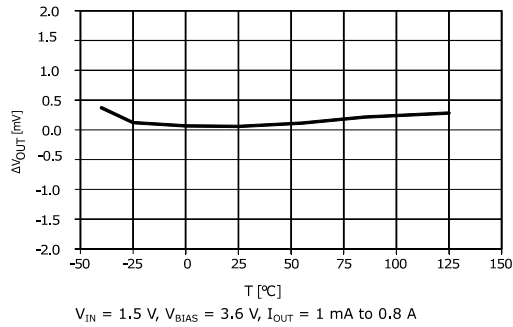


GIPG200620141601RV

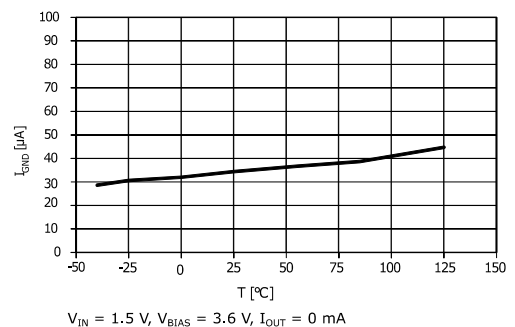
Figure 9: V_{BIAS} line regulation vs. temperature (adjustable)



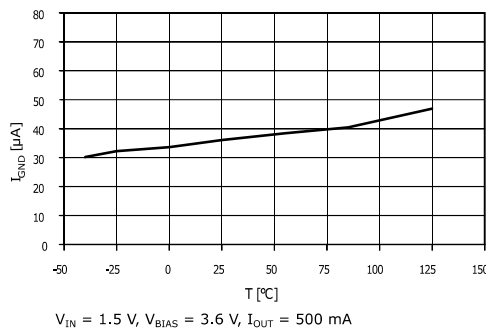
GIPG200620141606RV

Figure 10: Load regulation vs. temperature (adjustable)

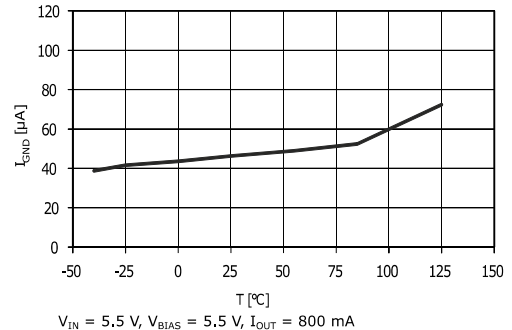
GIPG200620141616RV

Figure 11: Ground current vs. temperature (adjustable, $I_{OUT} = 0 \text{ mA}$)

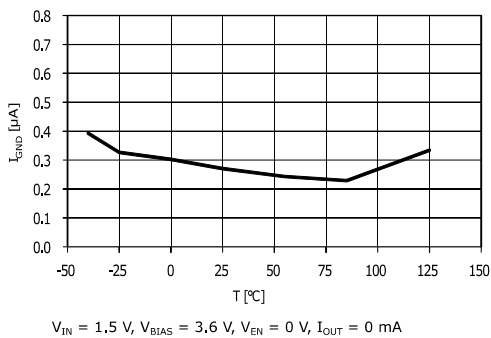
GIPG200620141623RV

Figure 12: Ground current vs. temperature (adjustable, $I_{OUT} = 500 \text{ mA}$)

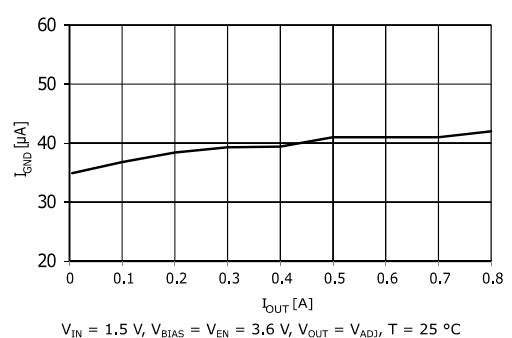
GIPG200620141641RV

Figure 13: Ground current vs. temperature (adjustable, $I_{OUT} = 800 \text{ mA}$)

GIPG200620141649RV

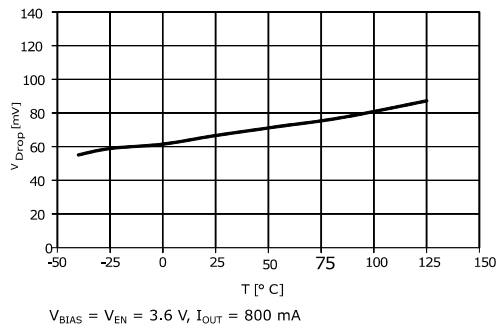
Figure 14: Ground current in off mode vs. temperature (adjustable)

GIPG240620141112RV

Figure 15: Ground current vs. output current (adjustable)

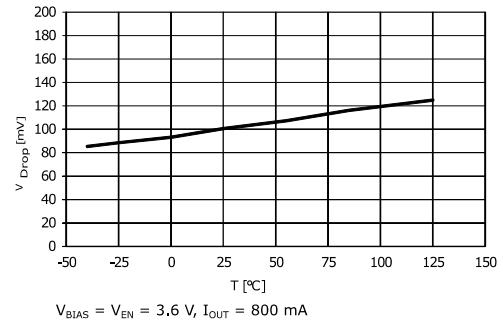
GIPG240620141121RV

Figure 16: Dropout voltage vs. temperature (adjustable)



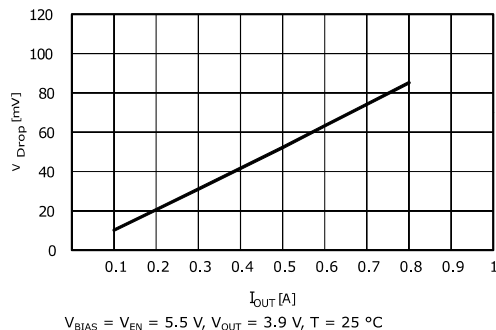
GIPG240620141129RV

Figure 17: Dropout voltage temperature (fixed 3.3 V)



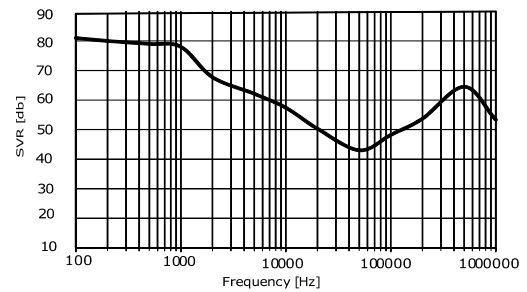
GIPG2406201451141RV

Figure 18: Dropout voltage vs. output current



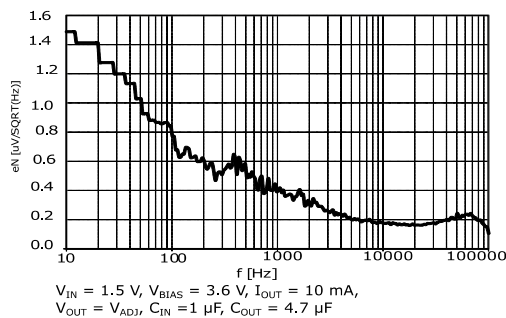
GIPG240620141148RV

Figure 19: Supply voltage rejection vs. frequency



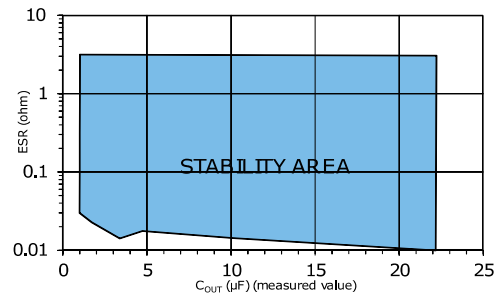
GIPG240620141153RV

Figure 20: Output noise spectral density



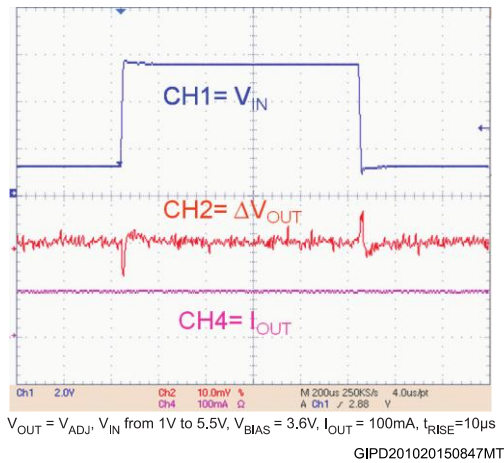
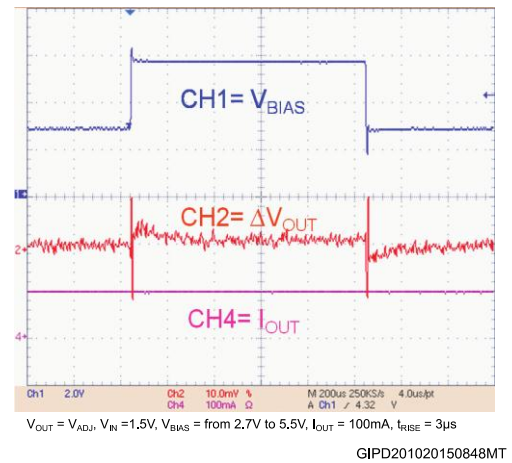
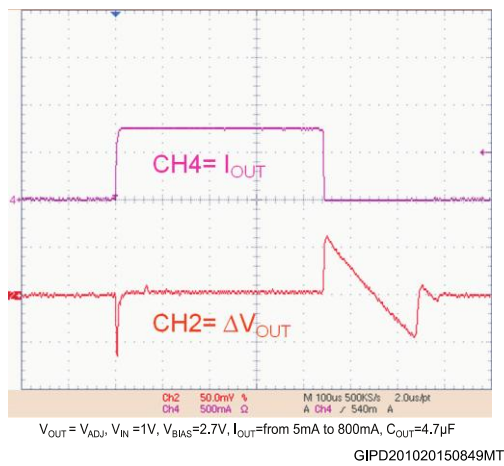
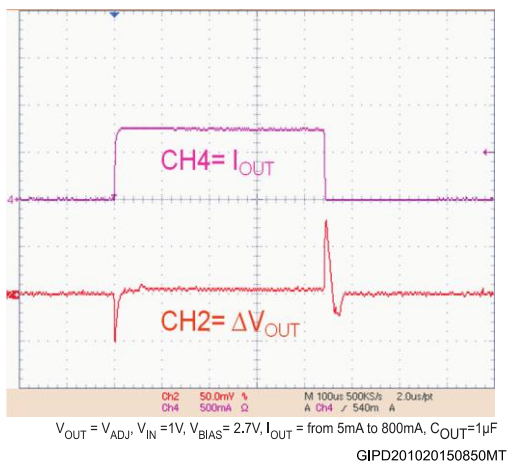
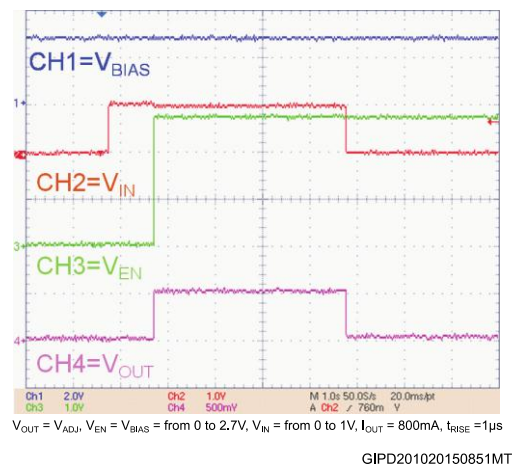
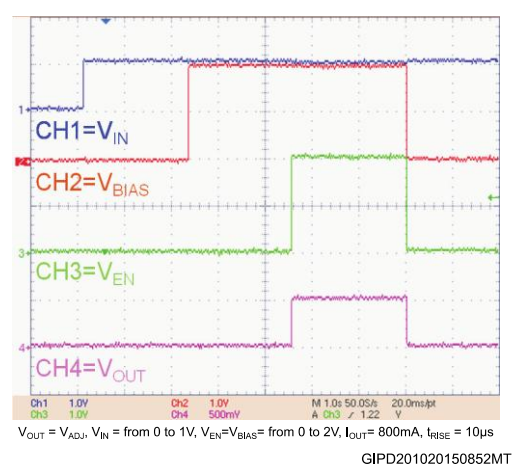
GIPG240620141159RV

Figure 21: Stability area vs. (C_OUT, ESR)



$V_{\text{OUT}} = V_{\text{ADJ}}, V_{\text{BIAS}} = \text{from } 2 \text{ V to } 5.5 \text{ V}, V_{\text{EN}} = \text{High}, V_{\text{IN}} = \text{from } 1 \text{ V to } 5.5 \text{ V}, T = 25 ^{\circ}\text{C}, I_{\text{OUT}} = 1 \text{ mA to } 0.8 \text{ A}, C_{\text{IN}} = C_{\text{BIAS}} = 1 \mu\text{F}$

GIPG240620141205RV

Figure 22: V_{IN} line transientFigure 23: V_{BIAS} line transientFigure 24: Load transient, $C_{OUT} = 4.7 \mu F$ Figure 25: Load transient, $C_{OUT} = 1 \mu F$ Figure 26: Enable transient, V_{BIAS} before V_{IN} Figure 27: Enable transient V_{IN} before V_{BIAS} 

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

8.1 DFN8 (2x3 mm) package information

Figure 28: DFN8 (2x3 mm) package outline

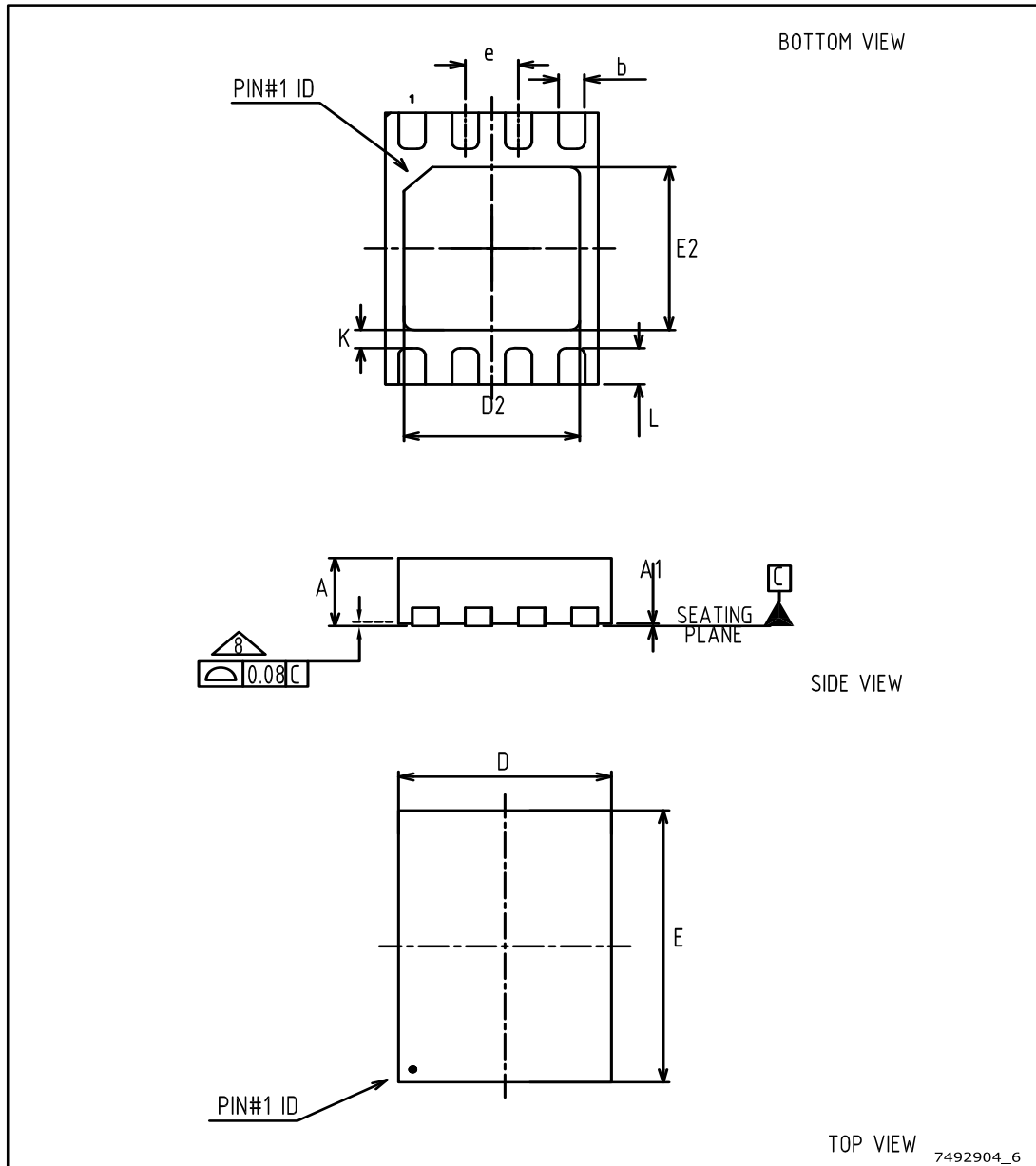
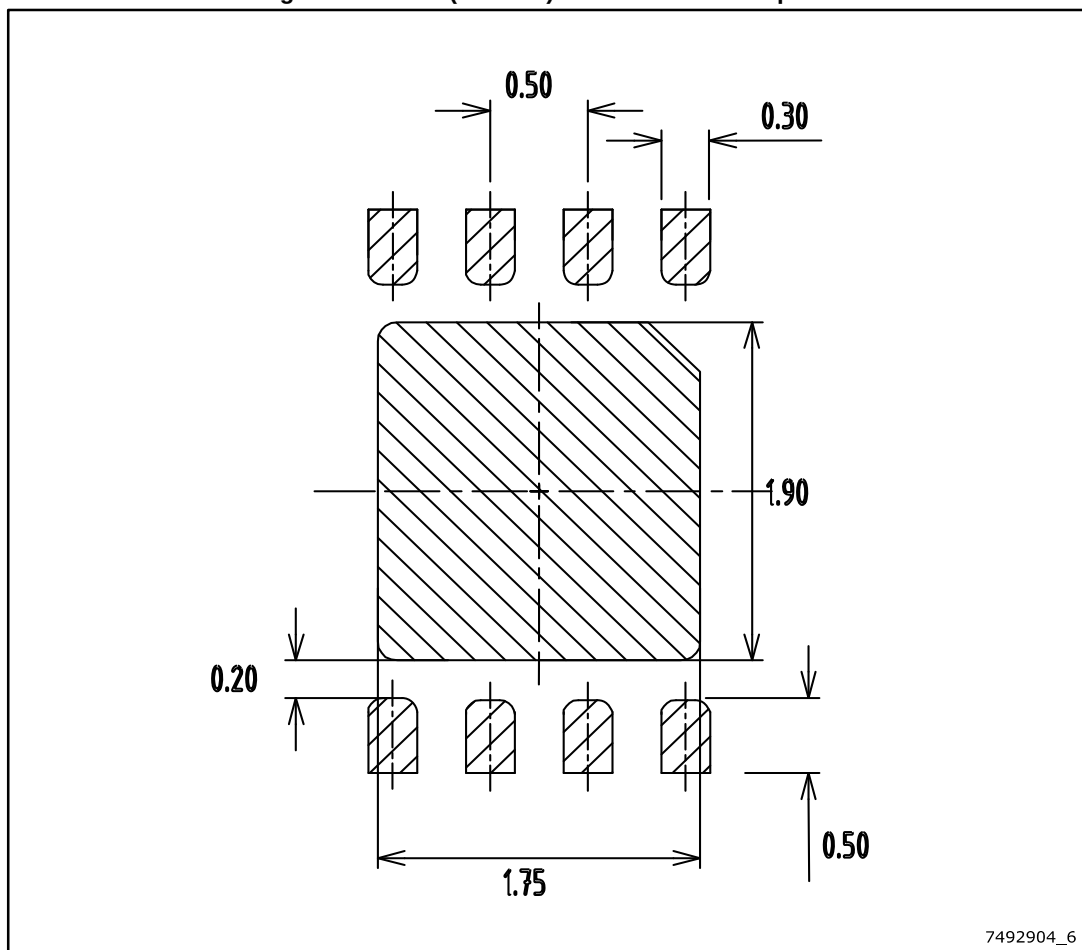


Table 6: DFN8 (2x3 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
c		0.10	
D		2.00	
E		3.00	
D2	1.50	1.65	1.75
E2	1.65	1.80	1.90
e		0.50	
L	0.30	0.40	0.50
K		0.20	

Figure 29: DFN8 (2x3 mm) recommended footprint



8.2 DFN8 (2x3 mm) packing information

Figure 30: DFN8 (2x3 mm) tape outline

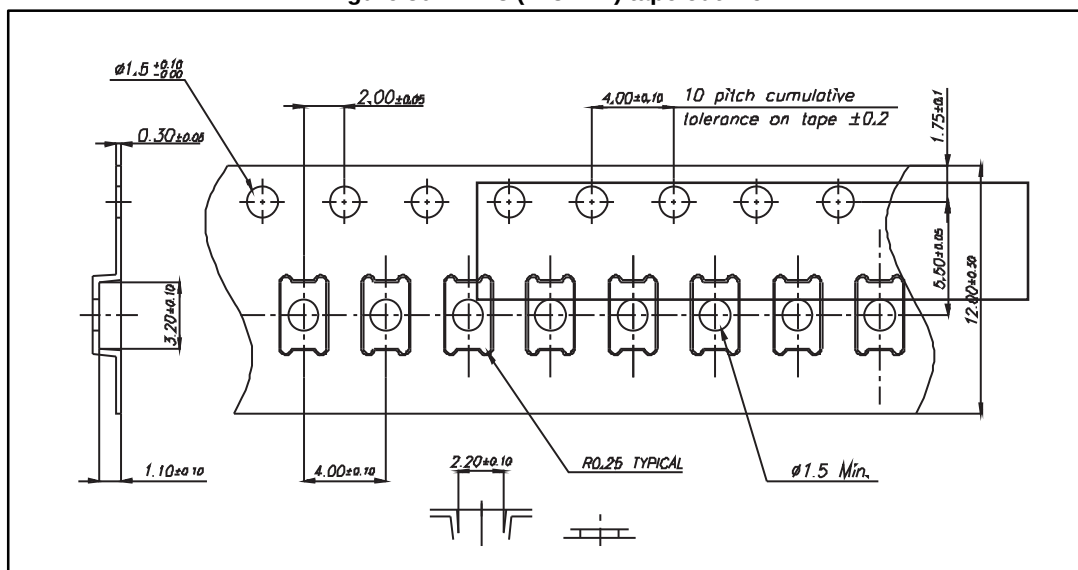


Figure 31: DFN8 (2x3 mm) reel outline

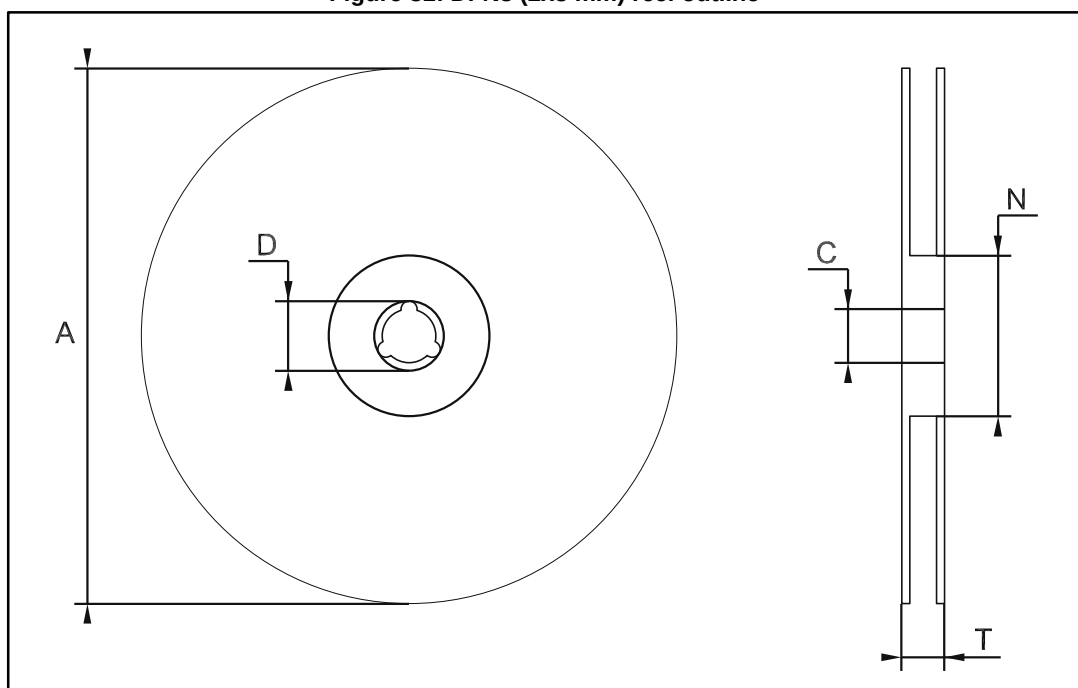


Table 7: DFN8 (2x3 mm) tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			180
C		12.8	13.2
D		20.2	
N		60	
T			14.4

9 Revision history

Table 8: Document revision history

Date	Revision	Changes
23-Oct-2014	1	First release.
16-Nov-2015	2	Updated Table 5: "Electrical characteristics for the ST1L08 (adjustable)" . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved