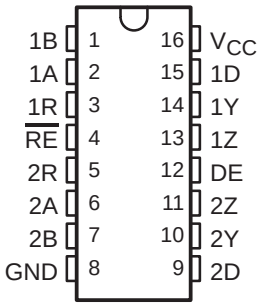
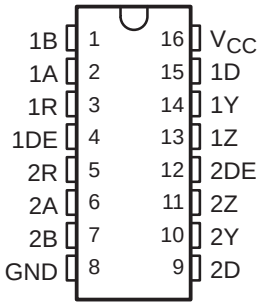
- **Meet or Exceed Standards EIA/TIA-422-B, RS-485, CCITT Recommendation V.11**
- **Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments**
- **Low Supply Current Requirement 50 mA Max**
- **Driver Positive- and Negative-Current Limiting**
- **Driver Common-Mode Output Voltage Range of –7 V to 12 V**
- **Thermal Shutdown Protection**
- **Driver 3-State Outputs Active-High Enable**
- **Receiver Common-Mode Input Voltage Range of –12 V to 12 V**
- **Receiver Input Sensitivity . . . ±200 mV**
- **Receiver Hysteresis . . . 50 mV Typ**
- **Receiver High Input Impedance 12 kΩ Min**
- **Receiver 3-State Outputs Active-Low Enable for SN75ALS1177 Only**
- **Operate From Single 5-V Supply**

SN75ALS1177 . . . N OR NS† PACKAGE
(TOP VIEW)



SN75ALS1178 . . . N OR NS† PACKAGE
(TOP VIEW)



† The NS package is only available in left-end taped and reeled (SN75ALS1177NSLE and SN75ALS1178SNLE).

description

The SN75ALS1177 and SN75ALS1178 dual differential drivers and receivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet standards EIA/TIA-422-B, RS-485, and CCITT Recommendation V.11.

The SN75ALS1177 combines dual 3-state differential line drivers and dual 3-state differential input line receivers, both of which operate from a single 5-V power supply. The drivers and receivers have active-high and active-low enables, respectively, which can be externally connected together to function as direction control. The SN75ALS1178 drivers each have an individual active-high enable. Fail-safe design ensures that when the receiver inputs are open, the receiver outputs are always high.

The SN75ALS1177 and SN75ALS1178 are characterized for operation from 0°C to 70°C.

Function Tables

SN75ALS1177, SN75ALS1178
(each driver)

INPUT D	ENABLE DE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

SN75ALS1177
(each receiver)

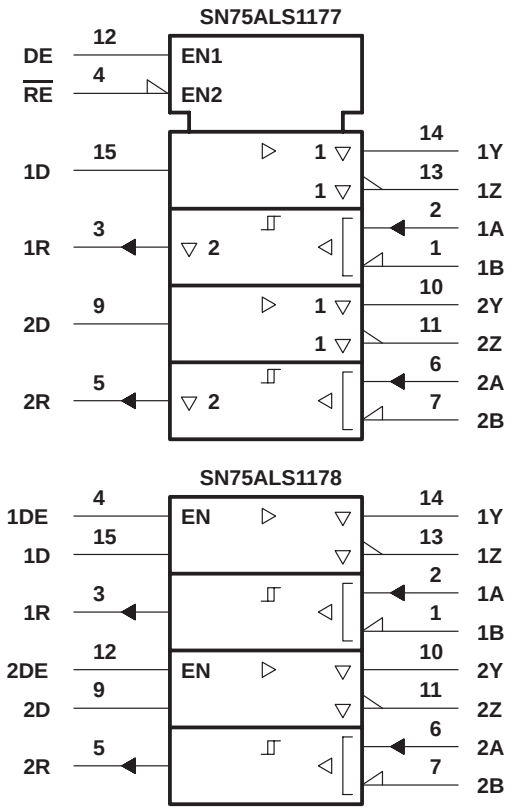
DIFFERENTIAL A – B	ENABLE $\overline{RE}$	OUTPUT Y
$V_{ID} \geq 0.2$ V	L	H
-0.2 V $< V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

SN75ALS1178
(each receiver)

DIFFERENTIAL A – B	OUTPUT Y
$V_{ID} \geq 0.2$ V	H
-0.2 V $< V_{ID} < 0.2$ V	?
$V_{ID} \leq -0.2$ V	L
Open	H

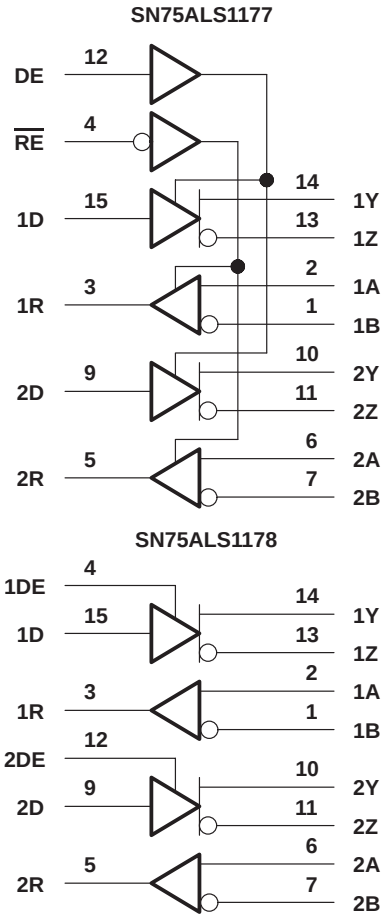
H = high level, L = low level,
? = indeterminate, X = irrelevant,
Z = high impedance (off)

logic symbol†

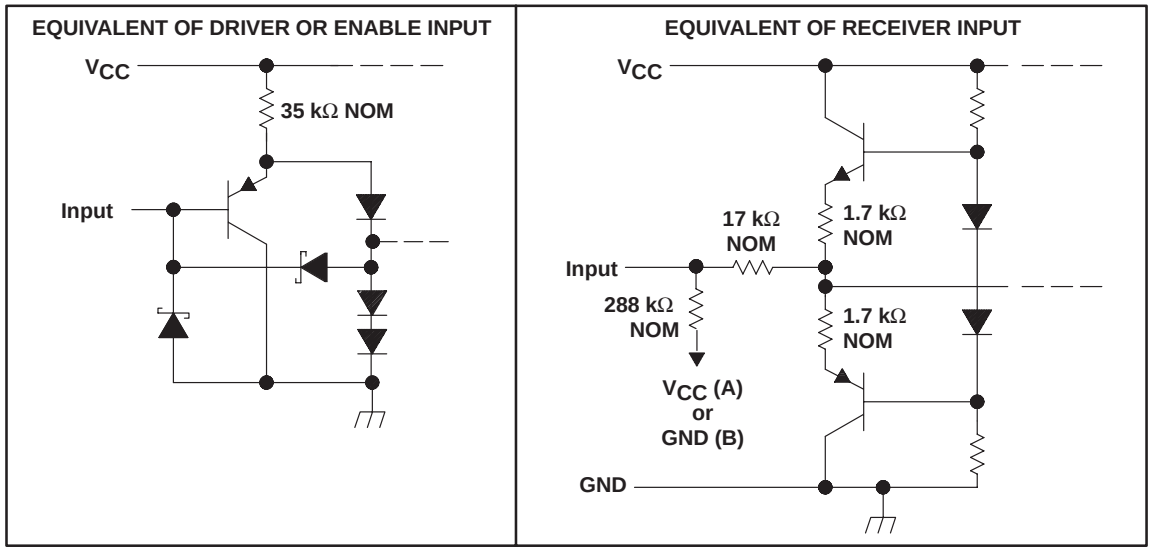


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

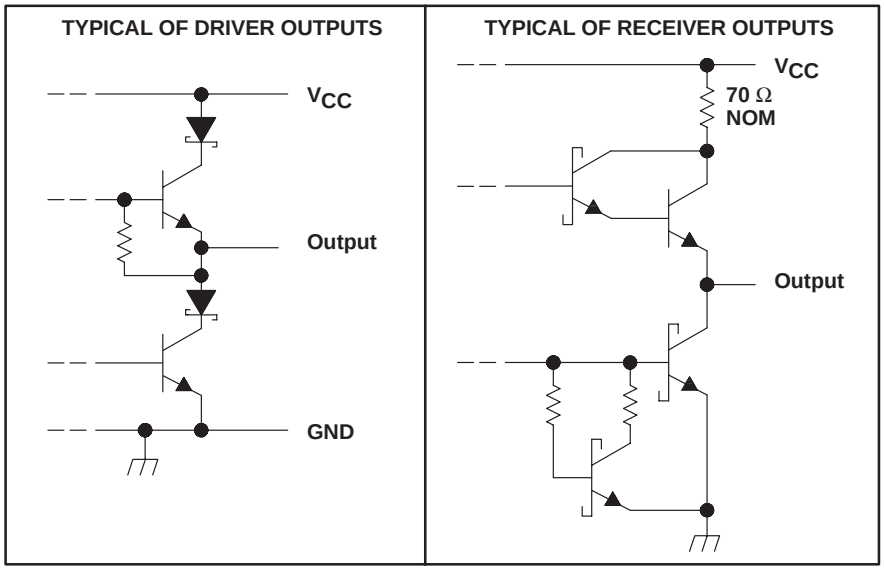
logic diagram (positive logic)



equivalent schematics



schematics of outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I (DE, $\overline{RE}$, and D inputs) . . . . . 7 V
Output voltage range, V_O (Driver) . . . . . –9 V to 14 V
Input voltage range, Receiver . . . . . –14 V to 14 V
Receiver differential-input voltage range (see Note 2) . . . . . –14 V to 14 V
Receiver low-level output current . . . . . 50 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to the network ground terminal.
2. Differential input voltage is measured at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
N	1150 mW	9.2 mW/°C	736 mW
NS	625 mW	4.0 mW/°C	445 mW

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Differential input voltage, V_{ID}	Receiver			±12	V
Common-mode output voltage, V_{OC}	Driver	–7†		12	V
Common-mode input voltage, V_{IC}	Receiver			±12	V
High-level input voltage, V_{IH}	DE, $\overline{RE}$, D	2			V
Low-level input voltage, V_{IL}	DE, $\overline{RE}$, D			0.8	V
High-level output current, I_{OH}	Driver			–60	mA
	Receiver			–400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage level only.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –33 mA			3.3		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 33 mA			1.1		V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See Figure 1	1/2 V_{OD1}			V
				2			
		R_L = 54 Ω		1.5		5	
$\|V_{OD3}\|$	Differential output voltage	See Note 3		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage (see Note 4)	R_L = 54 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage			–1‡		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage (see Note 4)					±0.2	V
$I_{O(OFF)}$	Output current with power off	V_{CC} = 0, V_O = –7 V to 12 V				±100	µA
I_{OZ}	High-impedance-state output current	V_O = –7 V to 12 V				±100	µA
I_{IH}	High-level input current	V_{IH} = 2.7 V				100	µA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				–100	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
		V_O = 0 V				150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		35	50	mA
			Outputs disabled		20	50	

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 3. See EIA Standard RS-485 Figure 3.5, test termination measurement 2.
4. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, high- to low-level output	R_L = 60 Ω, See Figure 3	C_{L1} = C_{L2} = 100 pF,	9	15	22	ns
t_{PHL}	Propagation delay time, low- to high-level output			9	15	22	ns
t_{sk}	Output-to-output skew			0	2	8	ns
t_{PZH}	Output enable time to high level	C_L = 100 pF,	See Figure 4	30	35	50	ns
t_{PZL}	Output enable time to low level	C_L = 100 pF,	See Figure 5	5	15	25	ns
t_{PHZ}	Output disable time from high level	C_L = 15 pF,	See Figure 4	7	15	30	ns
t_{PLZ}	Output disable time from low level	C_L = 15 pF,	See Figure 5	7	15	30	ns

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		V_O = 2.7 V,	I_O = –0.4 mA			0.2	V
$V_{IT–}$	Negative-going input threshold voltage		V_O = 0.5 V,	I_O = 8 mA	–0.2‡			V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)					50		mV
V_{IK}	Enable input clamp voltage	SN75ALS1177	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OH} = –400 μA,	2.7			V
V_{OL}	Low-level output voltage		V_{ID} = 200 mV, See Figure 2	I_{OL} = 8 mA,			0.45	V
I_{OZ}	High-impedance-state output current	SN75ALS1177	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current (see Note 5)		Other input at 0 V	V_I = 12 V			1	mA
				V_I = –7 V			–0.8	
I_{IH}	High-level input current, $\overline{RE}$	SN75ALS1177	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level input current, $\overline{RE}$	SN75ALS1177	V_{IL} = 0.4 V				–100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current		V_O = 0 V,	See Note 6	–15		–85	mA
I_{CC}	Supply current (total package)		No load,	Outputs enabled		35	50	mA

† All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡ The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for common-mode output and threshold voltage levels only.

NOTES: 5. Refer to EIA standards RS-422-A, RS-423-A, and RS-485-A for exact conditions.
6. Not more than one output should be shorted at a time.

switching characteristics at V_{CC} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output		C_L = 15 pF,	See Figure 6	15	25	37	ns
t_{PHL}	Propagation delay time, high- to low-level output				15	25	37	ns
t_{PZH}	Output enable time to high level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PZL}	Output enable time to low level	SN75ALS1177	C_L = 100 pF,	See Figure 7	10	20	30	ns
t_{PHZ}	Output disable time from high level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns
t_{PLZ}	Output disable time from low level	SN75ALS1177	C_L = 15 pF,	See Figure 7	5	12	16	ns

PARAMETER MEASUREMENT INFORMATION

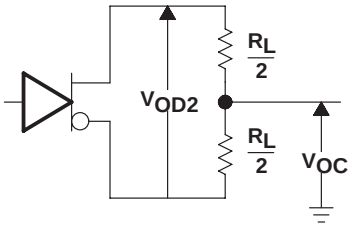


Figure 1. Driver Test Circuit, V_{OD} and V_{OC}

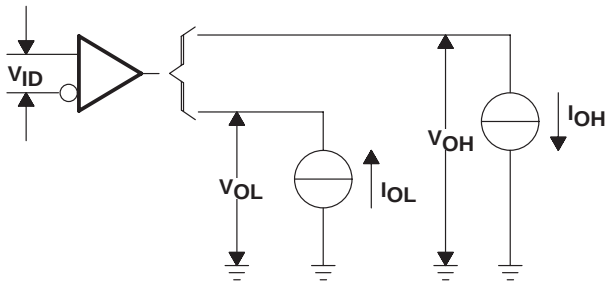
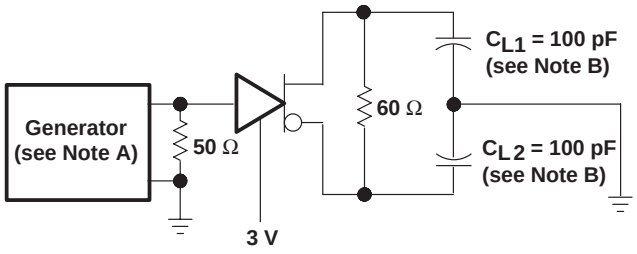
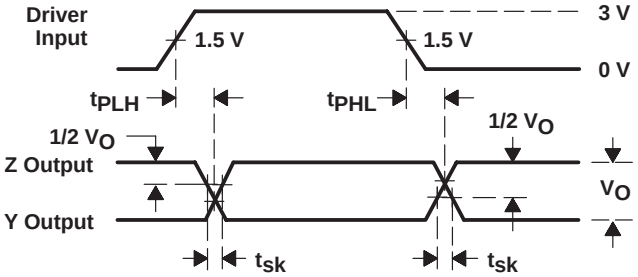


Figure 2. Receiver Test Circuit, V_{OH} and V_{OL}



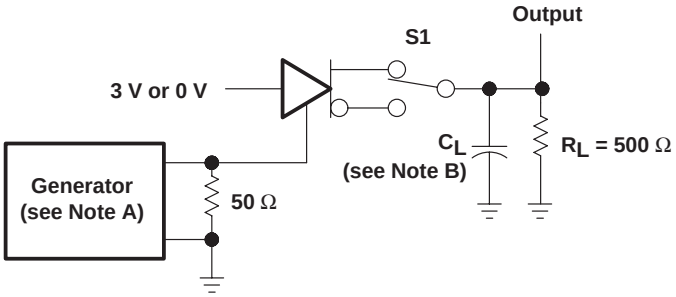
DRIVER TEST CIRCUIT



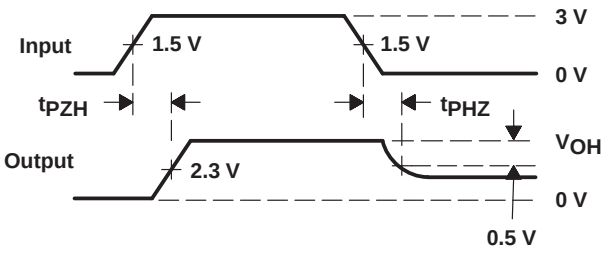
DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 3. Driver Propagation Delay Times



DRIVER TEST CIRCUIT

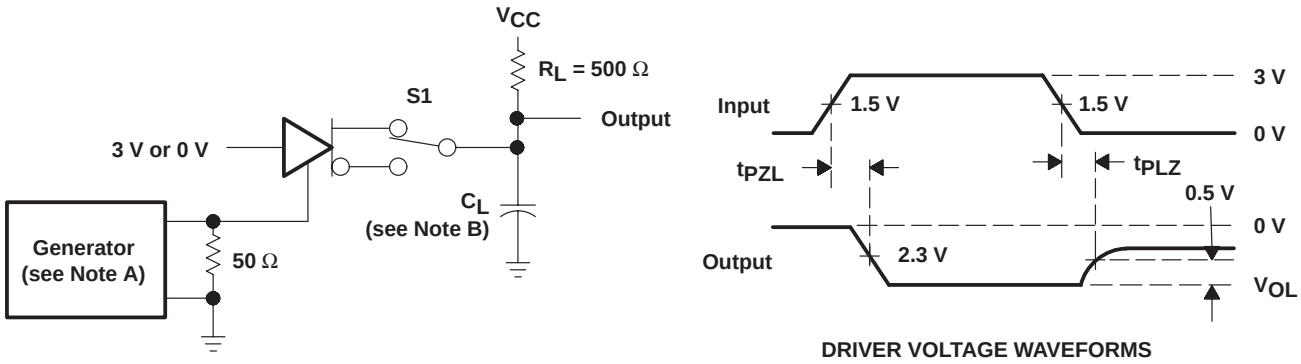


DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 4. Driver Enable and Disable TImes

PARAMETER MEASUREMENT INFORMATION

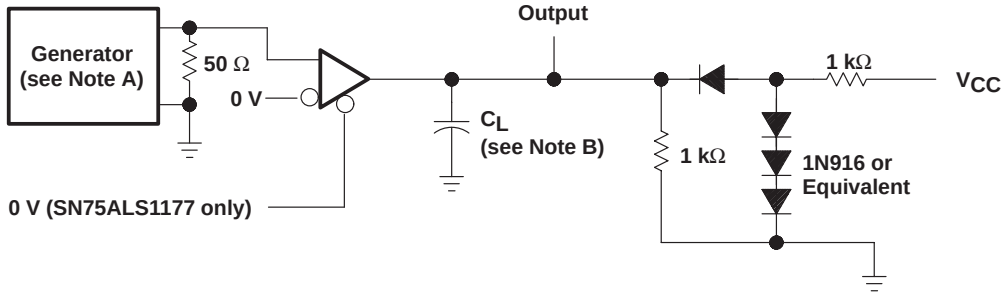


DRIVER TEST CIRCUIT

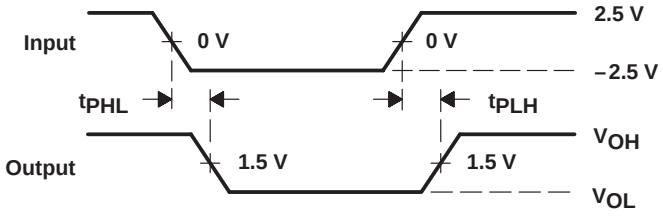
DRIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 5. Driver Enable and Disable Times



RECEIVER TEST CIRCUIT

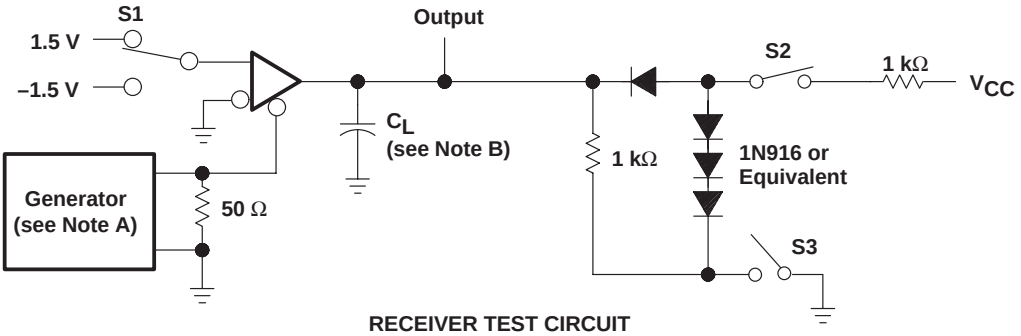


DRIVER VOLTAGE WAVEFORMS

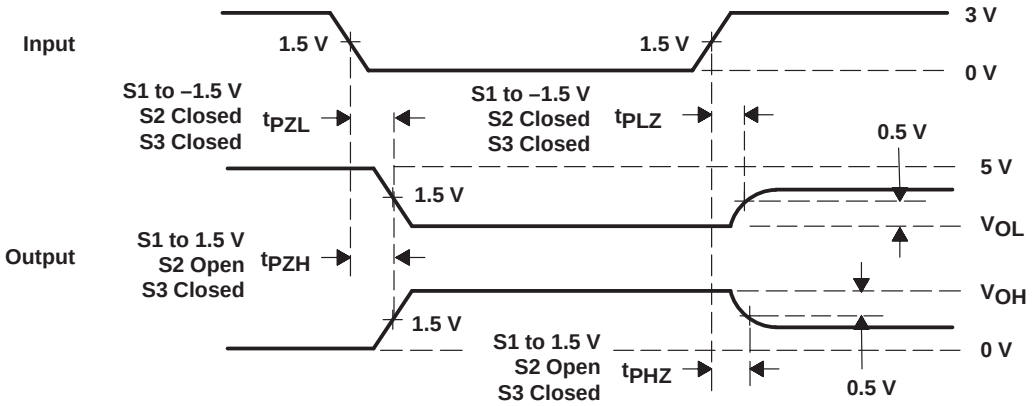
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



RECEIVER TEST CIRCUIT



RECEIVER VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.
B. C_L includes probe and jig capacitance.

Figure 7. Receiver Output Enable and Disable TImes

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