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- Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range up to 24 V
- Low Standby Power Dissipation

#### description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V<sub>CC1</sub> of 5 V and a V<sub>CC2</sub> of up to 24 V.

The SN75372 is characterized for operation from  $0^{\circ}$ C to  $70^{\circ}$ C.



logic symbol<sup>†</sup>



<sup>†</sup> This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

#### schematic (each driver)





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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, V <sub>CC1</sub> (see Note 1)	$\ldots \ldots \ldots -0.5$ V to 25 V
Input voltage, V <sub>I</sub> Peak output current, V <sub>O</sub> (t <sub>w</sub> < 10 ms, duty cycle < 50%) Continuous total power dissipation	500 mA
Operating free-air temperature range, T <sub>A</sub>	

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network GND.

DISSIPATION RATING TABLE									
	PACKAGE	T <sub>A</sub> = 25°C POWER RATING	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	T <sub>A</sub> = 70°C POWER RATING					
	D	725 mW	5.8 mW/°C	464 mW					
	Р	1000 mW	8.0 mW/°C	640 mW					

### recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC1</sub>	4.75	5	5.25	V
Supply voltage, V <sub>CC2</sub>	4.75	20	24	V
High-level input voltage, VIH	2			V
Low-level input voltage, VIL			0.8	V
High-level output current, I <sub>OH</sub>			-10	mA
Low-level output current, IOL			40	mA
Operating free-air temperature, T <sub>A</sub>	0		70	°C



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# electrical characteristics over recommended ranges of $V_{CC1}$ , $V_{CC2}$ , and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP <sup>†</sup>	MAX	UNIT	
VIK	Input clamp voltage		I∣ = −12 mA				-1.5	V	
Vari	High-level output voltage		V <sub>IL</sub> = 0.8 V,	I <sub>OH</sub> = -50 μA	V <sub>CC2</sub> -1.3	V <sub>CC2</sub> -0.8		V	
VOH			V <sub>IL</sub> = 0.8 V,	I <sub>OH</sub> = -10 mA	V <sub>CC2</sub> -2.5	V <sub>CC2</sub> -1.8		v	
			V <sub>IH</sub> = 2 V,	I <sub>OL</sub> = 10 mA		0.15	0.3		
VOL	Low-level output voltage		$V_{CC2} = 15 V \text{ to } 24 V,$ $I_{OL} = 40 \text{ mA}$	V <sub>IH</sub> = 2 V,		0.25	0.5	V	
٧F	Output clamp-diode forward vol	tage	$V_{I} = 0,$	I <sub>F</sub> = 20 mA			1.5	V	
l	Input current at maximum input voltage		VI = 5.5 V				1	mA	
I	Any Any		VI = 2.4 V				40	μA	
lΗ	High-level input current	Any E	V  = 2.4 V				80	μΑ	
۱	Low-level input current	Any A	V <sub>1</sub> = 0.4 V			-1	-1.6	mA	
'IL		Any E	V = 0.4 V			-2	-3.2		
ICC1(H)	Supply current from V <sub>CC1</sub> , both outputs high	ו	V <sub>CC1</sub> = 5.25 V,	V <sub>CC2</sub> = 24 V,		2	4	mA	
ICC2(H)	Supply current from V <sub>CC2</sub> , both outputs high		All inputs at 0 V,	No load			0.5	mA	
ICC1(L)	Supply current from V <sub>CC1</sub> , both outputs low	١	V <sub>CC1</sub> = 5.25 V,			16	24	mA	
ICC2(L)	Supply current from $V_{CC2}$ , both outputs low	1	All inputs at 5 V,			7	13	mA	
ICC2(S)	Supply current from V <sub>CC2</sub> , standby condition		V <sub>CC1</sub> = 0, All inputs at 5 V,	V <sub>CC2</sub> = 24 V, No load			0.5	mA	

<sup>†</sup> All typical values are at  $V_{CC1}$  = 5 V,  $V_{CC2}$  = 20 V, and  $T_A$  = 25°C.

### switching characteristics, V\_{CC1} = 5 V, V\_{CC2} = 20 V, T\_A = 25°C

	PARAMETER		TEST CONDITIONS			TYP	MAX	UNIT
<sup>t</sup> DLH	Delay time, low-to-high-level output	С <sub>L</sub> = 390 рF,	R <sub>D</sub> = 10 Ω,	See Figure 1		20	35	ns
<sup>t</sup> DHL	Delay time, high-to-low-level output					10	20	ns
<sup>t</sup> TLH	Transition time, low-to-high-level output					20	30	ns
<sup>t</sup> THL	Transition time, high-to-low-level output					20	30	ns
<sup>t</sup> PLH	Propagation delay time, low-to-high-level output				10	40	65	ns
<sup>t</sup> PHL	Propagation delay time, high-to-low-level output				10	30	50	ns



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#### PARAMETER MEASUREMENT INFORMATION









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#### **TYPICAL CHARACTERISTICS**



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**RUMENTS** 

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NOTE: For R<sub>D</sub> = 0, operation with C<sub>L</sub> > 2000 pF violates absolute maximum current rating.



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#### THERMAL INFORMATION

#### power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} = P_{S(AV)}$$

where  $P_{DC(AV)}$  is the steady-state power dissipation with the output high or low,  $P_{C(AV)}$  is the power level during charging or discharging of the load capacitance, and  $P_{S(AV)}$  is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load, and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_{H}t_{H} + P_{L}t_{L}}{T}$$
$$P_{C(AV)} \approx C V_{C}^{2} f$$
$$P_{S(AV)} = \frac{P_{LH}t_{LH} + P_{HL}t_{HL}}{T}$$



where the times are as defined in Figure 14.

Figure 12. Output Voltage Waveform

 $P_L$ ,  $P_H$ ,  $P_{LH}$ , and  $P_{HL}$  are the respective instantaneous levels of power dissipation, C is the load capacitance.  $V_C$  is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_{\rm C} = V_{\rm OH} - V_{\rm OL}$$

P<sub>S(AV)</sub> may be ignored for power calculations at low frequencies.

In the following power calculation, both channels are operating under identical conditions:  $V_{OH} = 19.2$  V and  $V_{OL} = 0.15$  V with  $V_{CC1} = 5$  V,  $V_{CC2} = 20$  V,  $V_C = 19.05$  V, C = 1000 pF, and the duty cycle = 60%. At 0.5 MHz,  $P_{S(AV)}$  is negligible and can be ignored. When the output voltage is high,  $I_{CC2}$ is negligible and can be ignored.

On a per-channel basis using data sheet values,

$$\mathsf{P}_{\mathsf{DC}(\mathsf{AV})} = \left[ (5 \ \mathsf{V}) \ \left(\frac{2 \ \mathsf{mA}}{2}\right) + (20 \ \mathsf{V}) \ \left(\frac{0 \ \mathsf{mA}}{2}\right) \right] (0.6) + \left[ (5 \ \mathsf{V}) \ \left(\frac{16 \ \mathsf{mA}}{2}\right) + (20 \ \mathsf{V}) \ \left(\frac{7 \ \mathsf{mA}}{2}\right) \right] (0.4)$$

 $P_{DC(AV)} = 47 \text{ mW per channel}$ 

Power during the charging time of the load capacitance is

 $P_{C(AV)} = (1000 \text{ pF}) (19.05 \text{ V})^2 (0.5 \text{ MHz}) = 182 \text{ mW per channel}$ 

Total power for each driver is

 $P_{T(AV)} = 47 \text{ mW} + 182 \text{ mW} = 229 \text{ mW}$ 

and total package power is

 $P_{T(AV)} = (229) (2) = 458 \text{ mW}.$ 



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#### **APPLICATION INFORMATION**

#### driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pullup resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470- $\Omega$  pullup resistor. The input capacitance (C<sub>iss</sub>) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C<sub>iss</sub> and the pullup resistor is shown in Figure 12(b).



Figure 13. Power MOSFET Drive Using SN75447



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#### **APPLICATION INFORMATION**

A faster, more efficient drive circuit uses an active pullup as well as an active pulldown output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).



Figure 14. Power MOSFET Drive Using SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and  $t_r$  is the desired drive time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3-0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a  $V_{CC}$  of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of  $V_{CC2}$  must be supplied to the MOSFET gate, the SN75374 quad MOSFET driver should be used.



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