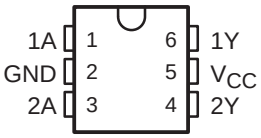
- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **Supports 5-V $V_{CC}$ Operation**
- **Max $t_{pd}$ of 3.4 ns at 3.3 V**
- **Low Power Consumption, 10-μA Max $I_{CC}$**
- **±24-mA Output Drive at 3.3 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Inputs and Open-Drain Outputs Accept Voltages Up To 5.5 V**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

† Contact factory for details. Q100 qualification data available on request.

**DBV OR DCK PACKAGE**
**(TOP VIEW)**




## description/ordering information

This dual inverter buffer/driver is designed for 1.65-V to 5.5-V $V_{CC}$ operation.

The output of the SN74LVC2G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING‡ |
|---|---|---|---|---|
| −40°C to 125°C | SOT (SOT-23) − DBV | Tape and reel | SN74LVC2G06QDBVRQ1 | C06_ |
| | SOT (SC-70) − DCK | Tape and reel | SN74LVC2G06QDCKRQ1 | CT_ |

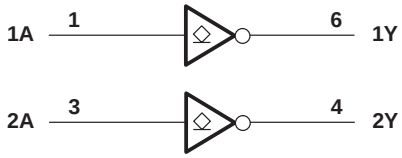
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | H |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$ (see Notes 1 and 2) . . . . . −0.5 V to 6.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) . . . . . −50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DBV package . . . . . 165°C/W
DCK package . . . . . 259°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 5.5 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | 2 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $0.7 \times V_{CC}$ | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | 0.8 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $0.3 \times V_{CC}$ | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | 5.5 | V |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 16 | |
| | | | | 24 | |
| | | $V_{CC}$ = 4.5 V | | 32 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V | | 20 | ns/V |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 10 | |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 5 | |
| $T_A$ | Operating free-air temperature | | −40 | 125 | °C |

NOTE 4: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{OL}$ | | $I_{OL}$ = 100 μA | | 1.65 V to 5.5 V | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | |
| | | $I_{OL}$ = 16 mA | $T_A$ = −40°C to 85°C | 3 V | | | 0.4 | |
| | | | $T_A$ = 125°C | | | | 0.45 | |
| | | $I_{OL}$ = 24 mA | $T_A$ = −40°C to 85°C | 3 V | | | 0.55 | |
| | | | $T_A$ = 125°C | | | | 0.65 | |
| | | $I_{OL}$ = 32 mA | $T_A$ = −40°C to 85°C | 4.5 V | | | 0.55 | |
| | | | $T_A$ = 125°C | | | | 0.65 | |
| $I_I$ | A inputs | $V_I$ = 5.5 V or GND | | 0 to 5.5 V | | | ±5 | μA |
| $I_{off}$ | | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = 5.5 V or GND, | $I_O$ = 0 | 1.65 V to 5.5 V | | | 10 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3 V to 5.5 V | | | 500 | μA |
| $C_i$ | | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 3.5 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.

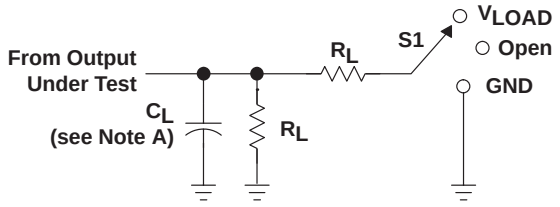
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V ± 0.15 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 5 V ± 0.5 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | Y | 1.8 | 7.2 | 1 | 3.9 | 1 | 3.4 | 1 | 2.9 | ns |

**operating characteristics, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | $V_{CC}$ = 5 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | TYP | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | f = 10 MHz | 2 | 2 | 3 | 4 | pF |

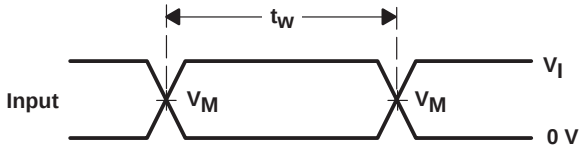
## PARAMETER MEASUREMENT INFORMATION
## (OPEN DRAIN)



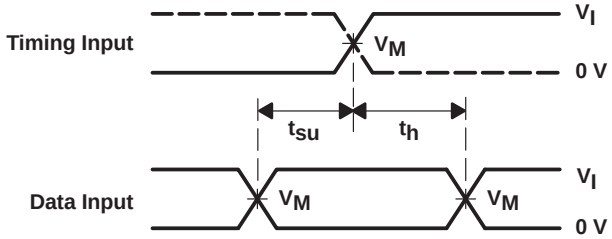

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PZL}$ (see Notes E and F) | $V_{LOAD}$ |
| $t_{PLZ}$ (see Notes E and G) | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | $V_{LOAD}$ |

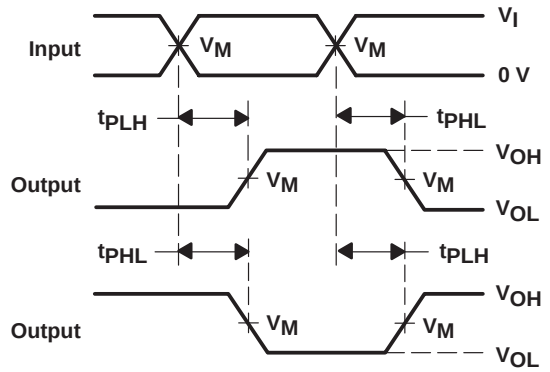
| $V_{CC}$ | INPUT | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤ 2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 3.3 V ± 0.3 V | 3 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 5 V ± 0.5 V | $V_{CC}$ | ≤ 2.5 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 Ω | 0.3 V |



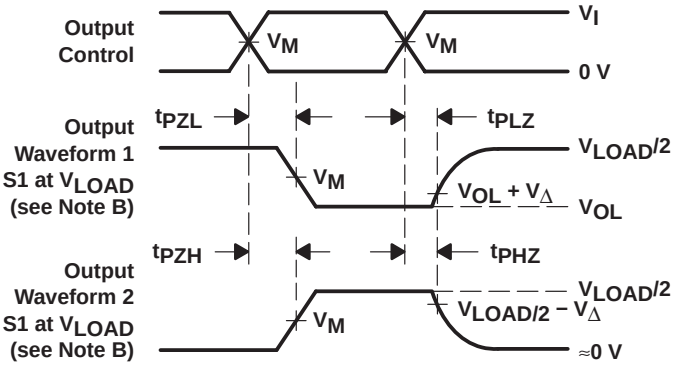

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. Since this device has open-drain outputs, $t_{PLZ}$ and $t_{PZL}$ are the same as $t_{pd}$.
F. $t_{PZL}$ is measured at $V_M$.
G. $t_{PLZ}$ is measured at $V_{OL} + V_\Delta$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

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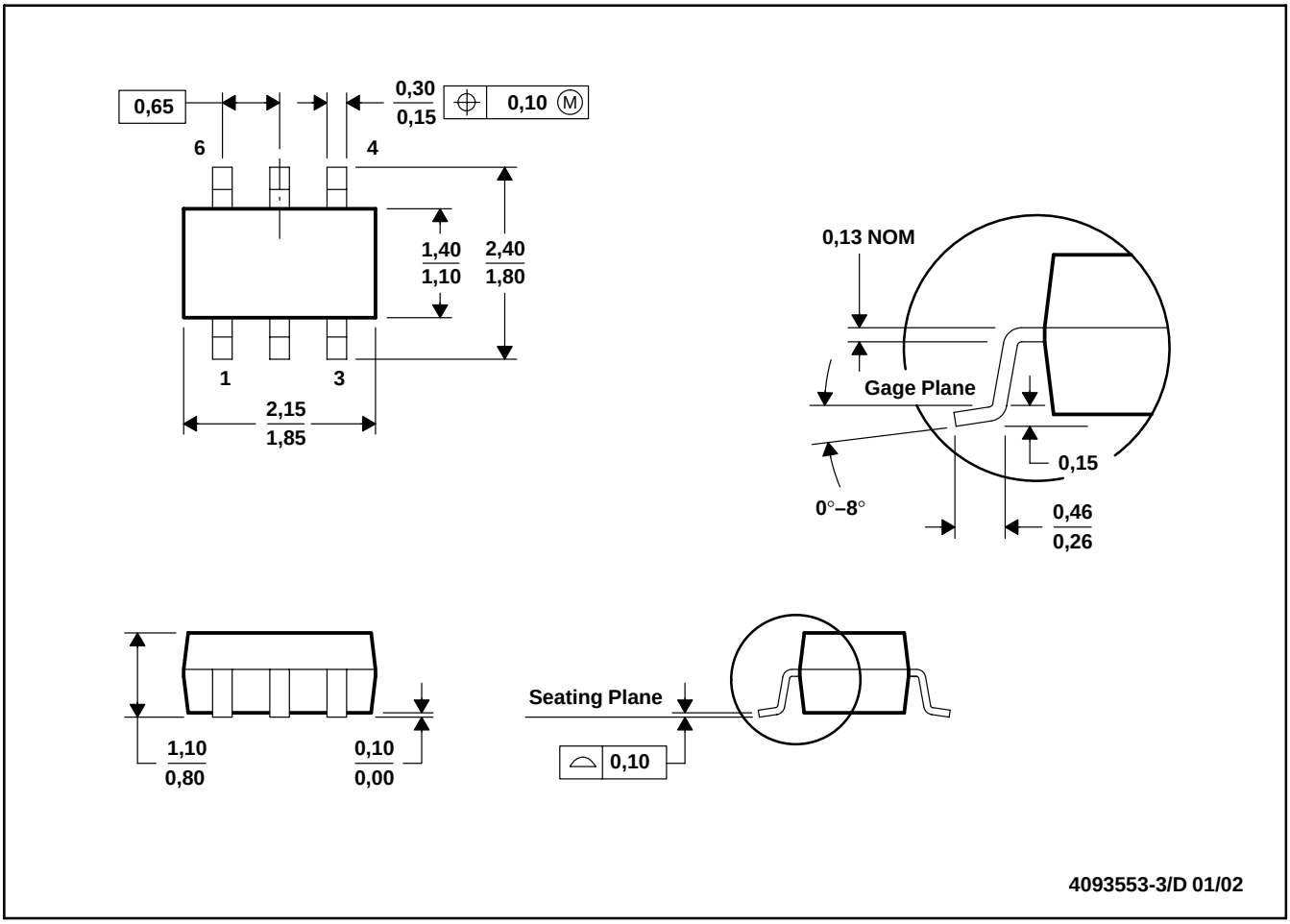
**DCK (R-PDSO-G6)** **PLASTIC SMALL-OUTLINE PACKAGE**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

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