- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Can Be Used as Two 16 Bit Counters or a Single 32 Bit Counter**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 25 ns at 5 V (RCLK to Y)**
- **Typical V_{OLP} (Output Ground Bounce) <0.7 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >4.4 V at V_{CC} = 5 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)

CLKA	1	20	V_{CC}
CLKB	2	19	Y0
$\overline{GAL}$	3	18	Y1
$\overline{GAU}$	4	17	Y2
$\overline{GBL}$	5	16	Y3
$\overline{GBU}$	6	15	Y4
RCLK	7	14	Y5
$\overline{RCOA}$	8	13	Y6
$\overline{CLKBEN}$	9	12	Y7
GND	10	11	$\overline{CCLR}$

description/ordering information

The SN74LV8154 is a dual 16 bit binary counter with 3-state output registers, designed for 2-V to 5.5-V V_{CC} operation.

This 16 bit counter (A or B) feeds a 16 bit storage register and each storage register is further divided into an upper byte and lower byte. The $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ inputs are used to select the byte that needs to be output at Y0–Y7. CLKA is the clock for A counter and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32 bit counter can be realized by connecting CLKA and CLKB together and by connecting $\overline{RCOA}$ to $\overline{CLKBEN}$.

To ensure the high-impedance state during power up or power down, $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PW	Tape and reel	SN74LV8154MPWREP	LV8154ME

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
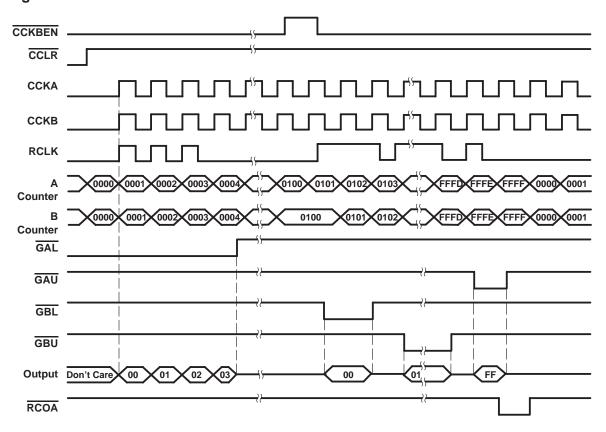
TEXAS INSTRUMENTS

FUNCTION TABLE
(each buffer)

INPUTS				OUTPUT
$\overline{GAL}$	$\overline{GAU}$	$\overline{GBL}$	$\overline{GBU}$	Yn
L	H	H	H	Lower byte in A register
H	L	H	H	Upper byte in A register
H	H	L	H	Lower byte in B register
H	H	H	L	Upper byte in B register
H	H	H	H	Z

Combinations of $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$, other than those shown above, are prohibited. If more than one input is L at the same time, the output data (Y0–Y7) may be invalid.
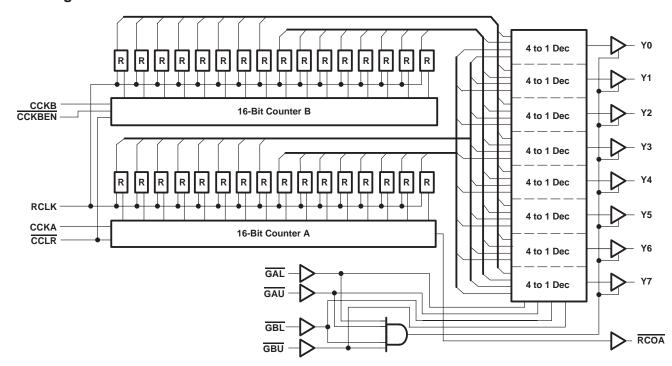
timing diagram

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

block diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} .... −0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
 or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Output voltage range, V_O (see Note 1 and Note 2) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 V) .... −20 mA
Output clamp current, I_{OK} (V_O < 0 V) .... −50 mA
Continuous output current, I_O (V_O = 0 V to V_{CC}) .... ±35 mA
Continuous current through V_{CC} or GND .... ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): .... 83°C/W
Storage temperature range, T_{stg} .... −65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
 functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
 implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	2 V	1.5		V
		3 V to 3.6 V	$V_{CC} \times 0.7$		
		4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	2 V		0.5	V
		3 V to 3.6 V		$V_{CC} \times 0.3$	
		4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	Yn outputs / 2 V		−50	µA
		Yn outputs / 3 V to 3.6 V		−6	mA
		Yn outputs / 4.5 V to 5.5 V		−12	mA
		$\overline{RCOA}$ / 2 V		−50	µA
		$\overline{RCOA}$ / 3 V to 3.6 V		−6	mA
		$\overline{RCOA}$ / 4.5 V to 5.5 V		−12	mA
I_{OL}	Low-level output current	Yn outputs / 2 V		50	µA
		Yn outputs / 3 V to 3.6 V		6	mA
		Yn outputs / 4.5 V to 5.5 V		12	mA
		$\overline{RCOA}$ / 2 V		50	µA
		$\overline{RCOA}$ / 3 V to 3.6 V		6	mA
		$\overline{RCOA}$ / 4.5 V to 5.5 V		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	3 V to 3.6 V		100	ns/V
		4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		−55	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	Yn	$I_{OH} = -50\ \mu A$	2 V	1.9			V
		$I_{OH} = -6\ mA$	3 V	2.48			
		$I_{OH} = -12\ mA$	4.5 V	3.8			
	$\overline{RCOA}$	$I_{OH} = -50\ \mu A$	2 V	1.9			
		$I_{OH} = -6\ mA$	3 V	2.48			
		$I_{OH} = -12\ mA$	4.5 V	3.8			
V_{OL}	Yn	$I_{OL} = 50\ \mu A$	2 V			0.1	V
		$I_{OL} = 6\ mA$	3 V			0.44	
		$I_{OL} = 12\ mA$	4.5 V			0.55	
	$\overline{RCOA}$	$I_{OL} = 50\ \mu A$	2 V			0.1	
		$I_{OL} = 6\ mA$	3 V			0.44	
		$I_{OL} = 12\ mA$	4.5 V			0.55	
I_I		$V_I = 5.5\ V$ or GND	0 V to 5.5 V			±1	μA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V			±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			20	μA
I_{off}		V_I or $V_O = 0$ V to 5.5 V	0 V			5	μA
C_i		$V_I = V_{CC}$ or GND	5 V		3		pF
C_o		$V_O = V_{CC}$ or GND	5 V		5		pF

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3\ V \pm 0.3\ V$ (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, and RCLK high or low	10		ns
		$\overline{CCLR}$ low	22		
t_{su}	Setup time	$\overline{CLKBEN}$ low before CLKB↑	13		ns
		$\overline{CCLR}$ high (inactive) before CLKA↑ or CLKB↑	13		
		CLKA↑ or CLKB↑ before RCLK↑	13		
		RCLK↑ before $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ low	13		
		$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ high (inactive) before RCLK↑	13		
t_h	Hold time	$\overline{CLKBEN}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z[†]	Z-period	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ all high before one of them switches low	200		ns

[†] t_z condition: $C_L = 50$ pF, $R_L = 1\ k\Omega$

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, and RCLK high or low	10		ns
		$\overline{CCLR}$ low	20		
t_{su}	Setup time	$\overline{CLKBEN}$ low before CLKB↑	10		ns
		$\overline{CCLR}$ high (inactive) before CLKA↑ or CLKB↑	10		
		CLKA↑ or CLKB↑ before RCLK↑	10		
		RCLK↑ before $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ low	10		
		$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ high (inactive) before RCLK↑	10		
t_h	Hold time	$\overline{CLKBEN}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z†	Z period	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ all high before one of them switches low	200		ns

† t_z condition: C_L = 50 pF, R_L = 1 kΩ

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
f_{MAX}			C_L = 50 pF		25		MHz
t_{pd}	RCLK	Y		25	1	42	ns
	CLKA	$\overline{RCOA}$		28	1	46	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$	C_L = 50 pF	20	1	35	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y		30	1	50	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y		14	1	24	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
f_{MAX}			C_L = 50 pF		25		MHz
t_{pd}	RCLK	Y		16	1	27	ns
	CLKA	$\overline{RCOA}$		17	1	28	
t_{PLH}	$\overline{CCLR}$	$\overline{RCOA}$	C_L = 50 pF	13	1	21	ns
t_{en}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y		18	1	30	ns
t_{dis}	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, $\overline{GBU}$	Y		9	1	16	ns

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

noise characteristics, V_{CC} = 5 V, C_L = 50 pF

	PARAMETER	T_A = 25°C TYP	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.7	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	−0.75	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	V

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = No load, CCLK = 10 MHz, RCLK = 1 MHz	56	pF

PARAMETER MEASUREMENT INFORMATION

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
  B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
     Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
  D. The outputs are measured one at a time, with one input transition per measurement.
  E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
  F. t_{PZL} and t_{PZH} are the same as t_{en}.
  G. t_{PHL} and t_{PLH} are the same as t_{pd}.
  H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

![Texas Instruments logo]
TEXAS INSTRUMENTS

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
SN74LV8154MPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
V62/06662-01XE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV8154-EP :

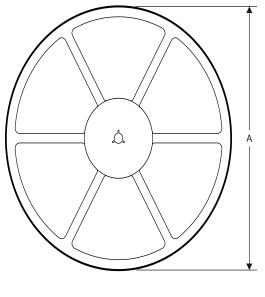● Catalog: SN74LV8154

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product
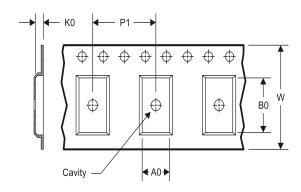
PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8154MPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8154MPWREP	TSSOP	PW	20	2000	367.0	367.0	38.0

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

20   11

Ⓓ 4,50
4,30

6,60
6,20

1   10

6,60
6,40

Ⓒ

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
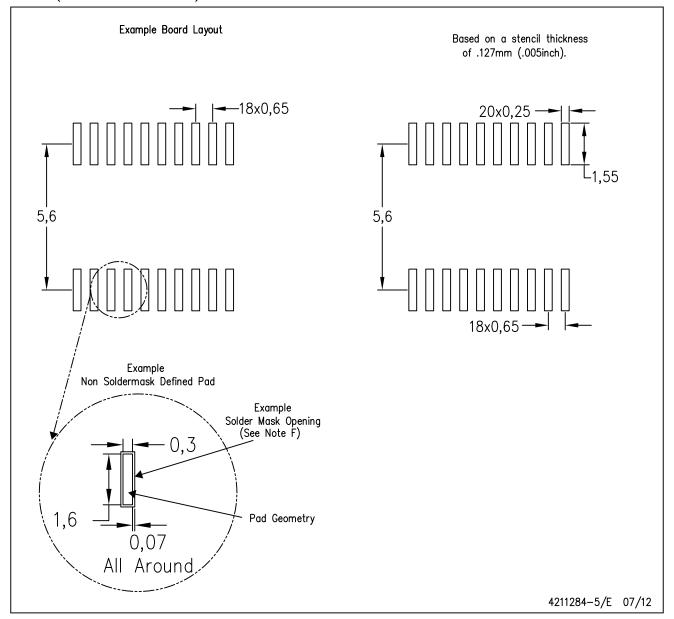0,05

Seating Plane

⌓ 0,10

4040064−5/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        Ⓒ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
            not exceed 0,15 each side.
        Ⓓ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
        E. Falls within JEDEC MO−153

TEXAS INSTRUMENTS
www.ti.com

PW (R−PDSO−G20)   PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness
of .127mm (.005inch).

18x0,65

20x0,25

1,55

5,6

5,6

18x0,65

Example
Non Soldermask Defined Pad

Example
Solder Mask Opening
(See Note F)

0,3

1,6

Pad Geometry

0,07
All Around

4211284−5/E 07/12

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Publication IPC−7351 is recommended for alternate design.
         D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS
INSTRUMENTS
www.ti.com

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		